Reducibility of Sequential Test Generation to Combinational Test Generation for Several Delay Fault Models

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Abstract

This paper presents a new structure, called discontinuous reconvergence structure (DR-structure), of sequential circuits with easy testability for delay faults. We show that the delay fault test generation problem for sequential circuits with DR-structure can be reduced to that for their time-expansion models, which are combinational circuits. Based on the reducibility, we propose a test generation method for delay faults in sequential circuits with DR-structure. This method can be applied to several delay fault models. By some experiments, we show that the proposed method is effective in the hardware overhead, the test generation time and the fault efficiency.

1 Introduction

As the speed of modern VLSI circuits reaches the gigahertz range, delay testing is becoming essential. Until now, several delay fault models have been investigated [8]. The path delay fault model [11] is one of the most general models among them because distributed faults along paths can be tested and the delay size of detectable faults is scalable.

Test generation for sequential circuits under simple fault models such as the single stuck-at fault model is itself generally a hard task. Delay test generation for sequential circuits is a more challenging problem. For such sequential circuits, *design for testability (DFT)* is an important approach to reduce the test generation effort. Given a sequential circuit, a fully enhanced scan technique [3] replaces each flip-flop (FF) by an *enhanced scan FF (ESFF)*. An ESFF can store two bits to apply two consecutive vectors. For a sequential circuit designed by this technique, we can use a combinational delay fault test generation algorithm (*ATPG*) to generate test sequences. Therefore, high fault coverage can be achieved with short test generation time. However, hardware overhead caused by extra memory elements of ESFFs is very high. It can be alleviated by using partial scan techniques [1, 10]. In a partially enhanced scan technique [1], for a sequential circuit, FFs to be replaced with ESFFs are selected such that feedback paths in the circuit are broken if these FFs are removed. For a sequential circuit designed by this partial scan technique, we can consider the circuit to be a feedback free circuit during test generation, and test generation for the feedback free circuit is easier than that for the original circuit. However, there is room for facilitating test generation because it still requires a sequential delay fault ATPG. We have proposed a partially enhanced scan design method [10]. The method is based on *balanced structure* [4]. The class of acyclic sequential circuits properly includes that of balanced sequential circuits. We showed that test sequences for path delay faults in balanced sequential circuits can be generated by applying a combinational delay fault ATPG to their combinationally equivalent circuits. Thus, our prior method can ease delay test generation complexity at the cost of a large number of ESFFs compared with the method [1]. In this paper, we discuss an extended class of sequential circuits for which test sequences can be generated by a combinational delay fault ATPG.

This paper presents a new structure, called *discontinuous reconvergence structure (DR-structure)*, of sequential circuits. The relation among three classes of sequential circuits is as follows: {the class of acyclic sequential circuits} $\supset$ {the class of sequential circuits with DR-structure} $\supset$ {the class of balanced sequential circuits}. DR-structure has a property of easy testability for delay faults: test sequences for delay faults in sequential circuits with DR-structure can be generated by applying a combinational delay fault ATPG to their equivalent combinational circuits. For acyclic sequential circuits, notation of time-frames [9] and notation of *time-expansion models* [6] have been proposed as ways to denote equivalent combinational circuits. In this paper, we employ time-expansion models as notation of equivalent combinational circuits, and show the reducibility of test generation for delay faults in a sequential circuit with DR-structure to that for the corresponding delay faults in its time-expansion model. Based on the reducibility, we propose a delay test generation method for sequential circuits with DR-structure. By experiments, we confirm the following: test generation time can be reduced and fault efficiency can be enhanced by using our method instead of an ordinary method using a sequential delay fault ATPG. In order to apply the proposed method to general sequential circuits, we use a partially enhanced scan technique. Theoretically, DR-structure can be extracted from the circuits with low hardware overhead compared with balanced structure. In this paper, we also confirm it experimentally.

2. Preliminaries

In general, a sequential circuit consists of combinational logic blocks (CLBs) connected with each other directly or

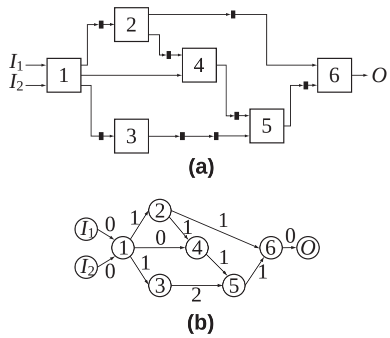

Figure 1. (a) Sequential circuit: S; (b) Topology graph of S: G.

through FFs. A CLB in the circuit is a region of connected combinational logic. The circuit can be modeled by a weighted directed graph defined as follows.

Definition 1 The *topology graph* for a sequential circuit S is a weighted directed graph $G = (V, A, w)$, where

- V is the set of vertices representing primary inputs, primary outputs and CLBs in S,
- $A \subset V \times V$ is the set of arcs representing FFs and wires in S, and
- $w : A \mapsto \{0\} \cup N$, where N is the set of natural numbers, defines the weights of the arcs, and $w(u,v)$ $(u, v \in V)$ denotes the number of FFs on a connection $(u,v) \in A$. □

Example 1 Examples of a sequential circuit and its topology graph are shown in Figure 1. In Figure 1(a), $1, 2, \ldots, 6$ are CLBs, and black blocks are FFs. □

In this paper, we assume that FFs have no hold capability, and those are of D-type. This assumption does not impose restriction on circuit representation because any FF with hold capability or the other types of FFs can be modeled by a D-type FF and some logic gates.

2.1. Target fault models

In this paper, we consider three delay fault models: the path delay fault model, segment delay fault model and transition fault model. However, in the remaining paper, we focus on the segment delay model because it can represent both the path delay fault model and the transition fault model.

In a circuit, a segment is defined as an ordered set of gates $(g_1, g_2, \ldots, g_L)$, where L is the length of the segment, and gate g_i is an input to gate g_{i+1} $(1 \leq i \leq L-1)$. The length of the segment, L, can be anywhere from 1 to L_{max}, where L_{max} represents the number of gates in the longest path in the circuit. A segment has a delay fault if propagation time of rising or falling transition through the segment exceeds a specified limit. Such a delay fault on a segment is said to be a *segment delay fault (SDF)* [5]. It is assumed that a segment delay fault is large enough to cause delay faults on all paths that include the segment. In test generation for the segment delay fault model, the fault list consists of all segments whose length is L and all paths whose length is less than L. When $L = 1$, the segment delay fault model reduces to the transition fault model. When $L = L_{\text{max}}$, it is equivalent to the path delay fault model [5].

Next, we define the testability of an SDF in both sequential circuits and combinational circuits.

Definition 2 Let S and s be a sequential circuit and a segment in S, respectively. Let f and S_f be the SDF on s and the faulty circuit of S with f, respectively. Let C be the combinational circuit composed of all the CLBs on s, and let t be a specified clock period of S. In a *slow-fast-slow testing* [8], f is *testable* if there exists an input sequence T for S and S_f such that the following conditions hold.

1. By applying an input vector pair (v_1, v_2) to C, the desired transition is launched at the starting point of s, and the transition is propagated to the ending point of s along s. Then, at time t, the value induced by v_2 at the ending point in S_f is different from that in S.
2. By applying T to S_f, (v_1, v_2) is justified to C, and the fault effect of f at the ending point is propagated to a primary output.

Such an input sequence T is regarded as a *test sequence* for f. □

In this paper, we assume a slow-fast-slow testing strategy in test application because a sequential circuit can be considered delay fault-free in both the fault initialization and the fault effect propagation phases.

Definition 3 Let C and s be a combinational circuit and a segment in C, respectively. Let f and C_f be the SDF on s and the faulty circuit of C with f, respectively. Let t be a specified limit time. The fault f is *testable* if there exists an input vector pair (v_1, v_2) for C and C_f such that the following conditions hold.

1. By applying (v_1, v_2) to C and C_f, the desired transition at the starting point of s is launched, and the transition is propagated to the ending point of s along s. Then, at time t, the value induced by v_2 at the ending point in C_f is different from that in C.
2. The fault effect of f at the ending point is propagated to a primary output by applying (v_1, v_2) to C_f.

Such an input vector pair (v_1, v_2) is regarded as an *two-pattern test* for f. □

2.2. Transformations

In the test generation method proposed in Section 4, test sequences for delay faults in sequential circuits with DR-structure are generated by applying a combinational ATPG to their equivalent combinational circuits. In this paper, we employ *time-expansion models* [6] as notation of equivalent combinational circuits. A time-expansion model for an acyclic sequential circuit is defined based on the following *time-expansion graph* [6].

Definition 4 Let S be an acyclic sequential circuit, and let $G = (V, A, w)$ be the topology graph of S. Let $E = (V_E, A_E, t, l)$ be a directed graph, where V_E is the set of vertices, A_E is the set of arcs, t is a mapping from V_E to the set of integers, and l is a mapping from V_E to V. If E satisfies the following four conditions, E is said to be a *time-expansion graph (TEG)* of G.

C1 (CLB preservation) The mapping l is surjective, i.e., $\forall v \in V$, $\exists u \in V_E$ s.t. $v = l(u)$.

C2 (Input preservation) Let u be a vertex in E. For any direct predecessor of $l(u)$ in G, $v \in pre(l(u))$, there exists a vertex u' in E such that $u' \in pre(u)$ and $l(u') = v$, where $pre(x)$ is the set of direct predecessors of a ver-

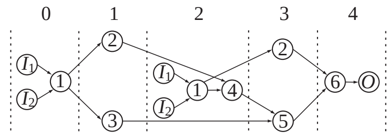

Figure 2. Time-expansion graph of G: E.

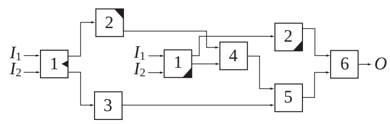

Figure 3. Time-expansion model of S based on E: $C_E(S)$.

tex x.

C3 (Time consistency) For any arc $(u,v) \in A_E$, there exists an arc $(l(u),l(v)) \in A$ such that $t(v) - t(u) = w(l(u),l(v))$.

C4 (Time uniqueness) For any vertices $u,v \in V_E$, if $t(u) = t(v)$ and $l(u) = l(v)$, then the vertices u and v are identical, i.e., $u = v$.

□

Example 2 Figure 2 shows the TEG of G (Figure 1(b)). In Figure 2, the character denoted in a vertex is that of the corresponding vertex in G, and the number located at the top of each column denotes the value of the label of vertices in the column. The graph E satisfies all the conditions in Definition 4. □

Note that a TEG of an acyclic sequential circuit is unique if the circuit is a single-output one [6]. This property does not hold if C4 of Definition 4 is absent.

Definition 5 Let S be an acyclic sequential circuit, and let $G = (V,A,w)$ be the topology graph of S. Let $E = (V_E,A_E,t,l)$ be a TEG of G. The combinational circuit $C_E(S)$ obtained by the following procedure is said to be the *time-expansion model (TEM)* of S based on E [6].

1. For each vertex $u \in V_E$, let $l(u) \in V$ be the CLB corresponding to u.
2. For each arc $(u,v) \in A_E$, connect the output of u to the input of v with a wire in the same way as $(l(u),l(v)) \in A$. Note that the connection corresponding to (u,v) has no FF even if the connection corresponding to $(l(u),l(v))$ has some FFs (i.e., $w(l(u),l(v)) \neq 0$).
3. In each CLB, lines and logic gates that are reachable to neither other CLBs nor primary outputs are removed.

□

Example 3 Figure 3 shows the TEM of S (Figure 1(a)) based on E (Figure 2). In Figure 3, a highlighted part in a CLB represents a portion of the lines and gates removed by Step 3 in Definition 5. □

Next, we define the following transformation that represents the relation between segment delay faults in an acyclic sequential circuit and segment delay faults in its TEM.

Definition 6 Let S be an acyclic sequential circuit, and let $G = (V,A,w)$ be the topology graph of S. Let $E = (V_E,A_E,t,l)$ be a TEG of G, and let $C_E(S)$ be the TEM of S based on E. Let f be the SDF on a segment s in S, and let C be the combinational circuit composed of all the CLBs on s in S. Let B be the set of the combinational circuits corresponding to C in $C_E(S)$, and let B' the subset of B whose the input (resp. output) corresponding to the starting (resp. ending) point of s in $C_E(S)$ does not removed. A transformation such that $B' = \mu(C)$ is said to be the *sub-circuit transformation*[1]. Let s' in each $b' \in B'$ be the segment corresponding to s, and let F_E be the set of SDFs composed of all the s'. A transformation such that $F_E = \sigma(f)$ is said to be the *fault transformation*[2]. □

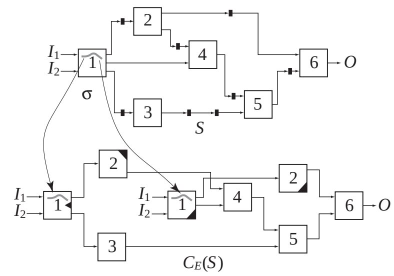

Figure 4. Fault transformation σ.

Example 4 Figure 4 illustrates the fault transformation. In general, an SDF in S corresponds to one or more SDFs in $C_E(S)$. Notice that, from Definition 4, there exists at least one SDF in $C_E(S)$ corresponding to an SDF in S even though lines or logic gates in $C_E(S)$ are removed by Step 3 in Definition 5. □

Finally, we define the following transformation that represents the relation between input sequences in an acyclic sequential circuit and input vector pairs in its TEM.

Definition 7 Let S be an acyclic sequential circuit, and let $G = (V,A,w)$ be the topology graph of S. Let $E = (V_E,A_E,t,l)$ be a TEG of G, and let $C_E(S)$ be the TEM of S based on E. Let $t_{\min}$ be the minimum value of labels assigned to vertices in E, and let d be the sequential depth of S. Let $I_u = (v_1,v_2)$ be an input vector pair to each primary input $u \in V_E$ in $C_E(S)$. A procedure transforming I_u into the input pattern to the primary input $l(u) \in V$ of S at time k $(= 0,1,\ldots,d+1)$ is said to be the *sequence transformation* τ. That is, for each u,

$$I_{l(u)}(k) = \begin{cases} v_1 & \text{if } k = t(u) - t_{\min} \\ v_2 & \text{if } k = t(u) - t_{\min} + 1 \\ \mathit{don't\ care} & \text{otherwise.} \end{cases}$$

Such an input sequence with the length $d+2$ is regarded as a *two-pattern sequence*. □

3. Discontinuous reconvergence structure

Our test generation method proposed in Section 4 generates test sequences for delay faults in sequential circuits with *discontinuous reconvergence structure*. We define the structure as follows.

Definition 8 Let $G = (V,A,w)$ be the topology graph of an acyclic sequential circuit S, and let $P(u,v)$ be the set of paths from u to v $(u,v \in V)$. Let $n(p)$ $(p \in P(u,v))$ be the number of FFs on a path p. The circuit S is said to be *discontinuous reconvergence structure (DR-structure)* if it satisfies the following condition.

$$|n(p_i) - n(p_j)| \neq 1 \quad (\forall u,v \in V, \forall p_i,p_j \in P(u,v)) \quad □$$

If structure of a sequential circuit is DR-structure, it is guaranteed that conflict of patterns does not occur in the

[1] Transforming $b' \in B'$ into C is denoted as μ^{-1}.

[2] Transforming $f_e \in F_E$ into f is denoted as σ^{-1}.

sequence transformation. In general, an acyclic sequential circuit does not satisfy this property.

Example 5 An acyclic sequential circuit S (Figure 1(a)) satisfies Definition 8. Therefore, S is a sequential circuit with DR-structure. □

Notice that, from Definition 8, the class of sequential circuits with DR-structure properly includes that of balanced sequential circuits [4, 10].

4. Test generation

In this section, we propose a delay test generation method for sequential circuits with DR-structure, and discuss the correctness of the method.

4.1. Test generation method

Given a sequential circuit S with DR-structure, our test generation method proceeds as follows.

For each output cone S_c of S,

1. Make an SDF list F of S_c.
2. Construct the topology graph G of S_c.
3. Create the TEG E of G.
4. Construct the TEM $C_E(S_c)$ of S_c based on E.
   For each SDF $f \in F$,
   (a) For $C_E(S_c)$, obtain the set of SDFs corresponding to f, and generate a two-pattern test t_e for an SDF f_e in the set by using a combinational ATPG[3].
   (b) Transform t_e into a test sequence T for f in S_c by using the sequence transformation.
   (c) Transform T into a test sequence T' for f in S.

As mentioned previously, a TEG of a acyclic sequential circuit is unique if the circuit is a single-output one. Therefore, in Step 3, E is also unique. In this paper, since we use a slow-fast-slow testing strategy in test application, a sequential circuit can be considered delay fault-free except in applying a fast clock. This implies that it is sufficient to generate a two-pattern test for at least one SDF in Step 4(a). In Step 4(c), T is always transformed into T' by applying T to the primary inputs of S corresponding to the primary inputs of S_c. Note that, for the other primary inputs of S, *don't care* values are assigned, i.e., each *don't care* value of T' is placed by 0 or 1.

4.2. Proof of correctness

In the following discussion, all the proofs of lemmas are omitted due to limitations of space. However, Lemma 1, 2 and 3 can be easily proved from Definition 4 and 8, Definition 2 and 4, and Definition 4 and Lemma 1, respectively.

Lemma 1 Let S be a single-output acyclic sequential circuit, and let $G=(V,A,w)$ be the topology graph of S. Let $E=(V_E,A_E,t,l)$ be the TEG of G. If S is a sequential circuit with DR-structure, S satisfies the following condition.

$$|t(u)-t(v)| \neq 1 \quad (\forall u,v \in V_E \text{ s.t. } l(u)=l(v)) \qquad \square$$

Lemma 1 guarantees that a two-pattern test t_e is transformed into a test sequence $\tau(t_e)=T$ without conflict of patterns in Step 4 (b) of our test generation method. Notice that, from Lemma 1, if structure of a sequential circuit is not DR-structure but acyclic structure, conflict of patterns must occur in the sequence transformation. Hence, test generation for such a sequential circuit must be performed by using a sequential delay fault ATPG.

Lemma 2 Let S^{DR} be a sequential circuit with DR-structure, and let f be any SDF in S^{DR}. If f is testable, there exists a test sequence formed as a two-pattern sequence. □

Lemma 3 Let S^{DR} be a single-output sequential circuit with DR-structure, and let $G=(V,A,w)$ be the topology graph of S^{DR}. Let $E=(V_E,A_E,t,l)$ be the TEG of G, and let $C_E(S^{DR})$ be the TEM of S based on E. Let $t_{\min}$ be the minimum value of labels assigned to vertices in E, and let d be the sequential depth of S^{DR}. Let $I_C=(v_1,v_2)$ be an arbitrary input vector pair to S^{DR}, and let $\tau(I_C)$ be the two-pattern sequence. Then, the value O_u observed from a primary output $u \in V_E$ by applying v_2 to $C_E(S^{DR})$ is equal to the value $O_{l(u)}(t(u)-t_{\min}+1)$ observed from the primary output $l(u) \in V$ at time $t(u)-t_{\min}+1$ by applying $\tau(I_C)$ to S^{DR}. □

From Lemma 1–3, we can have the following theorem.

Theorem 1 Let S^{DR} be a single-output sequential circuit with DR-structure, and let $G=(V,A,w)$ be the topology graph of S^{DR}. Let $E=(V_E,A_E,t,l)$ be the TEG of G, and let $C_E(S^{DR})$ be the TEM of S^{DR} based on E. Let F be the set of all SDFs in S^{DR}. Then,

1. an SDF $f \in F$ is testable if and only if at least one SDF $f_e \in \sigma(f)$ is testable, and
2. a two-pattern test for the SDF $f_e \in \sigma(f)$ can be transformed into a test sequence for the SDF $f=\sigma^{-1}(f_e)$.

(Proof) Let S^{DR}_f be the faulty circuit with f on a segment s of S^{DR}, and let $C_{E_{f_e}}(S^{DR})$ be the faulty circuit with f_e of $C_E(S^{DR})$. Let C be the combinational circuit composed of all the CLBs on s, and let $t_{\min}$ be the minimum value of labels assigned to vertices in E. Let d be the sequential depth of S^{DR}, and let τ^{-1} be the inverse transformation of τ.

First, we show that if f is testable, at least one f_e is also testable. From Lemma 2, there exists a two-pattern sequence T_f if f is testable. From Definition 2, if f is testable, T_f must justify input patterns v_1 and v_2 to C at time i and $i+1$, respectively. Let C' be the combinational circuit composed of CLBs such that $t(c)=i+t_{\min}$, where c is a CLB in $\mu(C)$. From Definition 4 and Lemma 3, if we apply $\tau^{-1}(T_f)$ to $C_{E_{fe}}(S^{DR})$, (v_1,v_2) is justified to C'. From Definition 4, since the logic function of the combinational circuit on s with f and that on the corresponding segment s_e with f_e are identical, the value appeared from the ending point of s_e by applying the 2nd vector of $\tau^{-1}(T_f)$ to $C_{E_{fe}}(S^{DR})$ is equal to the value appeared from the ending point of s at time $i+1$ by applying T_f to S^{DR}_f. From the above discussion and Lemma 3, in a slow-fast-slow testing, the value observed from a primary output $u \in V_E$ by applying the 2nd vector of $\tau^{-1}(T_f)$ to $C_{E_{fe}}(S^{DR})$ is equal to the value observed from the primary output $l(u) \in V$ at time $t(u)-t_{\min}+1$ by applying T_f to S^{DR}_f. $C_{E_{fe}}(S^{DR})$ and the TEM $C_E(S^{DR}_f)$ of S^{DR}_f based on E are isomorphic because f_e is an SDF on s_e corresponding to s. Therefore, for the 2nd vector of $\tau^{-1}(T_f)$, the output response of $C_E(S^{DR}_f)$

[3]If all the SDFs corresponding to f are identified as redundant faults by a combinational ATPG, f is also redundant.

is different from that of $C_E(S^{DR})$. Hence, if f is testable, at least one $f_e \in \sigma(f)$ is also testable.

Next, we show that if f_e is testable, $f = \sigma^{-1}(f_e)$ is also testable. If f_e is testable, there exists a two-pattern test t_{f_e}. Let s' and $C_{s'}$ be the segment with f_e and the combinational circuit composed of all the CLBs on s', respectively. Let $t_{s'}$ be the label of CLBs in $C_{s'}$, and let (v'_1, v'_2) be a vector pair to the input of $C_{s'}$. From Definition 4 and Lemma 3, we can justify (v'_1, v'_2) to the input of $\mu^{-1}(C_{s'})$ in S_f^{DR} by applying $\tau(t_{f_e})$ to S_f^{DR}. From Definition 4, since the logic function of the combinational circuit on s' and that on the corresponding segment s'_e are identical, the value appeared from the ending point of s' by applying the 2nd vector of t_{f_e} to $C_{E_{f_e}}(S^{DR})$ is equal to the value appeared from the ending point of s'_e by applying $\tau(t_{f_e})$ to S_f^{DR} at time $t_{s'} - t_{\min} + 1$. From the above discussion and Lemma 3, the value observed from a primary output $u' \in V_E$ by applying the 2nd vector of t_{f_e} to $C_{E_{f_e}}(S^{DR})$ is equal to the value observed from the primary output $l(u') \in V$ at time $t(u') - t_{\min} + 1$ by applying $\tau(t_{f_e})$ to S_f^{DR} in a slow-fast-slow testing. By the same reason as previously, $C_{E_{f_e}}(S^{DR})$ and the TEM $C_E(S_f^{DR})$ of S_f^{DR} based on E are isomorphic. Therefore, for $\tau(t_{f_e})$, the output response of S^{DR} and that of S_f^{DR} are different. Hence, if f_e is testable, $f = \sigma^{-1}(f_e)$ is also testable.

Finally, from Lemma 1, any two-pattern test for f_e can be always transformed into a test sequence for $f = \sigma^{-1}(f_e)$ by using the sequence transformation τ. Thus, the theorem is proved. □

From this theorem and the contraposition of condition 1 in the theorem, we can see that our test generation method can not only generate test sequences for all the testable SDFs in sequential circuits with DR-structure, but also identify all the redundant SDFs in the circuits. Note that Theorem 1 still holds for both the path delay fault model and the transition fault model because the segment delay fault model can represent the both models.

5. Evaluation of our test generation method

5.1. Characteristics of this work and prior works

From Definition 8, we can see that the relation among three classes is as follows: {the class of acyclic sequential circuits} ⊃ {the class of sequential circuits with DR-structure} ⊃ {the class of balanced sequential circuits}. In general, a sequential circuit is classified as none of these circuit structures. Therefore, if we generate test sequences for delay faults in such a sequential circuit by using the method [1], [10] or our method, we need to extract respective circuit structures by using DFT techniques, e.g., partially enhanced scan techniques. In the following discussion, we suppose that partially enhanced scan techniques are used to extract respective circuit structures.

Here, we discuss test generation complexity for each class of sequential circuits and hardware overhead (the number of ESFFs) required for extracting each structure.

Acyclic structure: The hardware overhead for making a general sequential circuit acyclic is lowest among three structures. However, given an acyclic sequential circuit, the test generation is more complex than the others because a sequential delay fault ATPG is required for generating test sequences.

Table 1. Circuit characteristics.

Circuit name	#PIs	#POs	#FFs	#gates
C1	16	24	80	5,528
C2	24	32	112	6,151
C3	128	96	288	20,239

Table 2. Percentages of enhanced scan FFs.

Circuit name	Acyclic structure		DR-structure		Balanced structure	
	#ESFFs	Scan (%)	#ESFFs	Scan (%)	#ESFFs	Scan (%)
C1	24	30.0	32	40.0	48	60.0
C2	24	21.4	32	28.6	48	42.9
C3	128	44.4	160	55.6	192	66.7

Balanced structure: In the test generation method [10], given a balanced sequential circuit, test sequences for delay faults in the circuit are generated by applying a combinational delay fault ATPG to its combinationally equivalent circuit. The combinationally equivalent circuit is obtained by just replacing each FF with a wire, and the sizes of the original circuit and the transformed circuit are equal except for FFs. Therefore, the test generation is much easier than the ordinary test generation using a sequential delay fault ATPG. However, the hardware overhead is highest among three structures.

DR-structure: The hardware overhead is lower than that of balanced structure. Furthermore, we can also generate test sequences for delay faults in a sequential circuit with DR-structure by applying a combinational delay fault ATPG to its time-expansion model. Therefore, the test generation can be much easier than the ordinary test generation using a sequential delay fault ATPG.

In the next subsection, we evaluate the effectiveness of our test generation method.

5.2. Experimental results

Here, we evaluate the effectiveness of the proposed method in hardware overhead required for extracting DR-structure, test generation time and fault efficiency. The following experiment was performed on a Sun Blade 1000 workstation, and we used a combinational/sequential delay test generation tool TetraMAX ATPG (Synopsys) on the workstation. We considered a fault model in test generation as the transition fault model. The difference between test generation for the transition fault model and that for the other fault models (path delay fault model and segment delay fault model) is only the number of mandatory assignments in propagating a desired transition along a faulty site. Therefore, test generation result for the transition fault model would be similar to that for the other fault models.

First, we compare hardware overheads required for extracting acyclic structure, DR-structure and balanced structure from a sequential circuit. We used three circuits shown in Table 1. In Table 1, Columns “#PIs”, “#POs” and “#FFs” denote the number of primary inputs, primary outputs and FFs, respectively. Column “#gates” denotes the area of a circuit estimated by Design Compiler (Synopsys). Table 2 shows hardware overheads required for extracting respective structures. Columns “#ESFFs” and “Scan (%)” in each column of circuit structure denote the number of ESFFs

Table 3. Test generation result.

Circuit name	Acyclic structure (Sequential ATPG)		DR-structure (Combinational ATPG)		Balanced structure (Combinational ATPG)	
	TGT (s)	FE (%)	TGT (s)	FE (%)	TGT (s)	FE (%)
C1	3,797	99.55	51	99.98	14	99.98
C2	16,740	91.18	941	98.81	729	99.37
C3	54,750	98.20	1,814	99.98	1,553	99.95

and the percentage of ESFFs in each structure, respectively. Note that we obtained each sequential circuit with acyclic structure, S^A, by an exact algorithm [2], and each sequential circuit with DR-structure, S^{DR}, and each sequential circuit with balanced structure, S^B, were extracted by applying a greedy algorithm to S^A. Here, let us explain the greedy algorithm for S^{DR} briefly. The greedy algorithm traverses S^A from the primary inputs to the primary outputs in a depth-first fashion. In traversing S^A, if paths of S^A do not satisfy the condition of Definition 8, an FF on the paths is replaced by an ESFF in order for the paths to satisfy the condition. Thus, we obtained S^{DR} from S^A. S^B was obtained in a similar way. In Table 2, "Scan" of S^{DR} was larger than that of S^A. However, "Scan" of S^{DR} was the value of about -15.1% on average compared to that of S^B. From this result, DR-structure can be obtained from a sequential circuit by paying low hardware overhead compared to balanced structure.

Next, we evaluate test generation time and fault efficiency for S^A, S^{DR} and S^B. In Table 3, column "Acyclic structure" denotes the test generation result using a sequential ATPG for S^A, and column "DR-structure" denotes the result using a combinational ATPG for the time-expansion model of S^{DR}. Column "Balanced structure" denotes the result using a combinational ATPG for the combinationally equivalent circuit of S^B. Columns "TGT (s)" and "FE(%)" in each column of circuit structure denote test generation time and fault efficiency under the non-robust criterion for transition faults, respectively. Our method achieved high fault efficiency with very short test generation time (about 41 times faster on average) compared to the conventional method using a sequential ATPG. Moreover, we obtained the almost same fault efficiency as "Balanced structure" with slightly long test generation time compared to the method [10]. Thus, our method can significantly improve test generation time and fault efficiency by paying large hardware overhead compared to acyclic structure.

From the above results, we can see that our method is effective in hardware overhead, test generation time and fault efficiency.

6. Conclusions

This paper presented a new structure, called discontinuous reconvergence structure (DR-structure), of sequential circuits with easy testability for delay faults. We proposed a delay test generation method for sequential circuits with the structure. In our method, instead of a sequential delay fault ATPG, a combinational delay fault ATPG is used to generate test sequences for delay faults. We theoretically proved the correctness of the proposed method. Our method can handle several delay fault models which can be detected by two-pattern tests, e.g., the path delay fault model, segment delay fault model and transition fault model. We confirmed that our test generation method can reduce test generation time and can enhance fault efficiency compared to the ordinary test generation method using a sequential delay fault ATPG. To apply our method to general sequential circuits, we used a partially enhanced scan technique. Theoretically, the class of sequential circuits with DR-structure properly includes that of balanced sequential circuits. Therefore, it is conceivable that DR-structure is extracted from a sequential circuit with low hardware overhead compared with balanced structure (our previous work [10]). We also confirmed it experimentally.

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