A Fast and Accurate Per-Cell Dynamic IR-drop Estimation Method for At-Speed Scan Test Pattern Validation

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Abstract

In return for increased operating frequency and reduced supply voltage in nano-scale designs, their vulnerability to IR-drop-induced yield loss grew increasingly apparent. Therefore, it is necessary to consider delay increase effect due to IR-drop during at-speed scan testing. However, it consumes significant amounts of time for precise IR-drop analysis. This paper addresses this issue with a novel per-cell dynamic IR-drop estimation method. Instead of performing time-consuming IR-drop analysis for each pattern one by one, the proposed method uses global cycle average power profile for each pattern and dynamic IR-drop profiles for a few representative patterns, thus total computation time is effectively reduced. Experimental results on benchmark circuits demonstrate that the proposed method achieves both high accuracy and high time-efficiency.

1. Introduction

Ever-shrinking process technology has made it possible to produce a VLSI design with high clock frequency and/or low supply voltage. At the same time, at-speed scan testing, where test response is captured at the system clock speed to detect delay faults, has become mandatory to ensure the product quality and reliability since timing-related defects are dominant in deep-submicron (DSM) devices [1].

However, at-speed testing is facing a serious challenge of test-induced yield loss due to excessive IR-drop on power and ground distribution network. Power consumption in at-speed scan testing is usually much higher than that of functional operation because of high switching activity derived from highly compacted test pattern set for simultaneous massive fault detection. In addition, low-power design techniques, such as clock gating is usually disabled during test. This also leads to a wide gap of switching activity between functional and test operation. Excessive switching activity causes large switching current flow through power and ground network, and spawns IR-drop which reduces switching speed on each cell instance. As a result, timing failure may occur only during at-speed scan testing and thus yield loss is incurred.

Fig. 1 illustrates IR-drop issues in at-speed scan testing based on widely adopted *launch-on-capture* (LOC) clocking scheme [2]. In shift mode for loading test vectors and unloading circuit response with clock pulses S_1 to S_L, excessive IR-drop on clock paths may cause severe clock skew resulting in shift operation failure due to hold time violation. On the other hand, in capture mode for launching a transition at the first clock pulse C_1 and capturing corresponding response at the second clock pulse C_2 with functional clock speed, excessive IR-drop on sensitized functional paths may cause capture malfunction due to setup time violation.

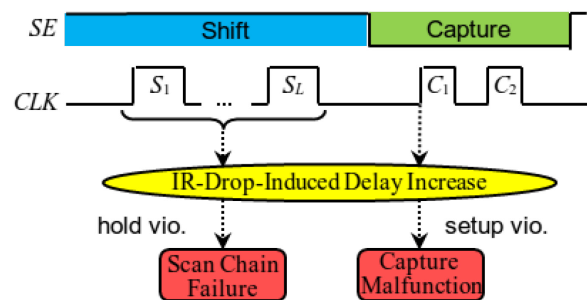

Fig. 1 IR-drop issues in LOC at-speed scan testing.

Since test pattern is one of major factors affecting IR-drop, a variety of low-power test pattern generation/modification techniques [3 – 7] has been proposed. However, in most of the techniques the generated test patterns are only evaluated by reduction effect of switching activity, power, or IR-drop while not referring to delay increase on sensitized paths which is the real cause of timing failures. Although reducing the power consumption itself is important, from the viewpoint of avoiding IR-drop-induced timing failures, it is also necessary to validate whether or not the increased delay exceeds the design timing margin. Generally, IR-drop is non-uniformly distributed over the circuit layout depending on the cell location where transitions occur. At the same time, the effect of IR-drop-induced delay increase at a cell depends on the amount of IR-drop at the cell. Therefore, to accurately evaluate IR-drop-induced delay increase for a pattern, precise amount of IR-drop, instead of indirect evaluation metrics, for individual cell instance needs to be known.

1.1 Related Work

Previous pattern evaluation metrics can be classified into two categories: ***path-independent metrics*** and ***path-dependent metrics*** as described below. Path-independent

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metrics basically try to estimate power consumption in a whole circuit or in each of locally partitioned regions. *Toggle count* (TC) and *weighted switching activity* (WSA) are common metrics because of their computational simplicity. In [9], *switching cycle average power* (SCAP) is defined as the average power consumed during the time frame of the entire switching activity and it is reported to have a good correlation with IR-drop and can be used to identify patterns suspected to cause high IR-drop. Techniques in [10] and [11] consider power consumption for local regions since locally high power consumption tends to affect IR-drop at particular region. The technique in [10] partitions a circuit layout into multiple regions and considers even power distribution among regions during test compaction to avoid some regions having high power consumption and hence being affected by IR-drop. WSA for each region is then calculated for evaluation. In the technique [11], a circuit layout is divided into multiple regions and a test pattern is evaluated based on not only global metrics such as *global toggle constraint* (GTC) which limits toggle count in a whole circuit throughout the test cycle and *global instantaneous toggle constraints* (GITC) which limits toggle count in a whole circuit at any time instant, but also a local metric of *regional instantaneous toggle constraint* (RITC) which limits toggle count in each region at any time instant. However, although these metrics have correlation with IR-drop and IR-drop-induced delay increase, therefore help identify patterns with high IR-drop, the methods do not accurately estimate actual path delays increased due to IR-drop. To estimate actual path delays, it is necessary to associate the evaluated power with the information of sensitized paths.

On the other hand, path-dependent metrics focus on the relation between cells on a path as victims and cells of its proximity as aggressors since the cells in proximities of the path have high impact on IR-drop-induced delay increase. A path under consideration is either a long sensitized path [8], [12] or a clock path [13]. In [8], *critical capture transition* (CCT) which adds the *critical weight* as an additional weight to WSA, which reflects the impact of a transition at an aggressor on victims. To more accurately reflect the transition impact on the aggressors, *transition-time-relation* (TTR) based metric in which earlier transitions than the transition at on-path node are considered for impact calculation, has been proposed in [12]. These methods help identify paths which may cause IR-drop-induced timing failures for a given test pattern. However, WSA-based power evaluation is inaccurate since IR-drop varies among cells even if their WSAs are the same.

A way to accurately evaluate path delays is dynamic timing analysis using voltage-aware static timing analysis technique [14]. Indeed, commercial timing analysis tools employ such kind of functions. The analysis is performed through gate level logic simulation, dynamic power/IR-drop analysis, and timing analysis with back-annotated voltage.

Similarly, in [15], the proposed method is evaluated by IR-drop-induced delay increase. The evaluation process includes dynamic IR-drop analysis for each cell, back-annotation of supply voltages for each cell on critical paths, and SPICE simulation for the paths. However, in any case, dynamic IR-drop analysis needs to be performed to obtain voltage profiles for all test patterns one by one for test pattern validation. Obviously, this is computationally too expensive and practically impossible.

1.2 Contribution and Paper Organization

A novel per-cell dynamic IR-drop estimation method is proposed in this paper to overcome the drawbacks of the previous metrics discussed above. The proposed method derives an IR-drop estimation function for each cell instance in a circuit based on cycle average power profiles and dynamic IR-drop profiles for a few representative patterns in a test set. This results in saving computation time because of minimized effort for performing dynamic IR-drop analysis, as is well known to consume large amounts of time. As a result, pattern-dependent per-cell IR-drop for any pattern can be quickly obtained by using estimation functions associated with each cell. Moreover, accurate estimation can also be achieved since the estimation functions are derived based on precise IR-drop analysis.

Consequently, test patterns are evaluated in terms of timing by performing timing analysis with annotated effective voltage (i.e. supply voltage minus IR-drop) for each cell which is estimated by the proposed method. Therefore, the proposed method helps find test patterns which may cause IR-drop-induced timing failures during scan testing.

It should be noted that, although we focus on delay increase on sensitized paths at launch cycle in this paper, the proposed method is also applicable for clock skew analysis at shift cycle since IR-drop is estimated for all cells including clock buffers.

The remainder of this paper is organized as follows: Section 2 shows the motivation of this work based on preliminary experiments, Section 3 describes the detail of the proposed method. Section 4 shows experimental results, and Section 5 concludes the paper.

2. Preliminary Experiment

To investigate the effect of delay increase due to IR-drop, we conducted several experiments on ITC’99 b14 benchmark circuit [16] with 5,419 cells layout. The layout was designed using Synopsys SAED90nm EDK Digital Standard Cell Library with 1.2V power supply voltage [17]. To see as much IR-drop variation as possible, power distribution network was designed with two pads placed on upper right and lower left corners, a power ring, and no power straps. After the layout design, the circuit had 245 scan flip-flops and 9,742 gates in 2-input NAND gate equivalent. The clock period was set 3ns. As for a test

pattern set, path delay fault (PDF) ATPG was conducted to obtain the information of sensitized paths. 953 patterns detecting 4,443 PDFs were generated. Dynamic timing analysis was performed for these patterns with the flow shown in Fig. 2. First, logic simulation is performed for each pattern using a circuit delay profile in *standard delay format* (SDF), and the switching information is stored in *value change dump* (VCD) format. Then, per-pattern power consumption is computed by power analysis using netlist, parasitics, and VCDs. After that, IR-drop analysis is performed to obtain per-cell effective voltage profiles. Finally, timing analysis with annotated effective voltages reports the timing information for sensitized paths of each pattern. Note that, we used average IR-drop over launch clock cycle for voltage annotation in timing analysis since the linear correlation between path delay and the difference of supply voltage and average IR-drop per cycle (VDD - DVD_{avg}) has been proven in [19]. Hereinafter, "average IR-drop over single clock cycle" is merely referred to as "IR-drop".

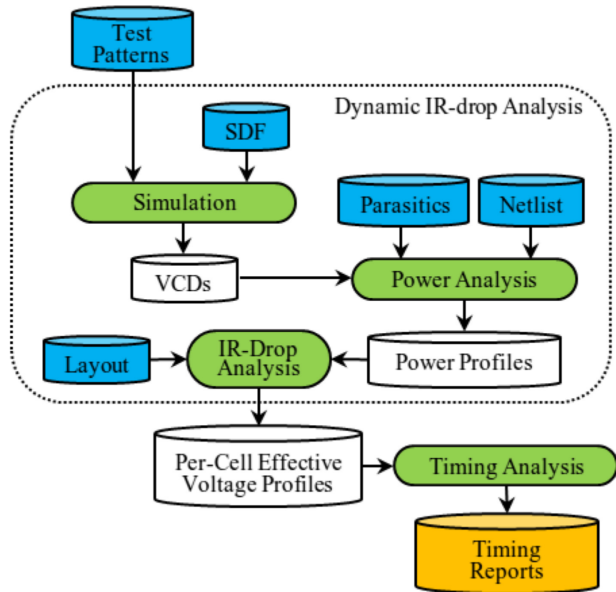

Fig. 2 Flow of the dynamic timing analysis.

Fig. 3 shows the IR-drop map for one of the patterns in which four paths were sensitized. The location of the paths and their delay increase rate are also shown.

IR-drop distributes within the range of 4mV (blue region) to 64mV (red region). Here, some blanks seen in the map indicate the locations where no cells are placed. It can be seen that, the delay increase on two paths running through high IR-drop area are higher than the others, i.e. delay increase effect depends on the amount of IR-drop at on-path cells. This clearly points out the necessity to know per-cell IR-drop for accurate timing evaluation. The breakdown of the total execution time was: logic simulation 1.6%, power analysis 18.7%, dynamic IR-drop analysis 68.8%, and voltage-annotated timing analysis 10.9%. Obviously the bottleneck is dynamic IR-drop analysis and its percentage is expected to increase explosively in larger circuits. Therefore, it is impractical to apply such time-consuming analysis for validating many test patterns.

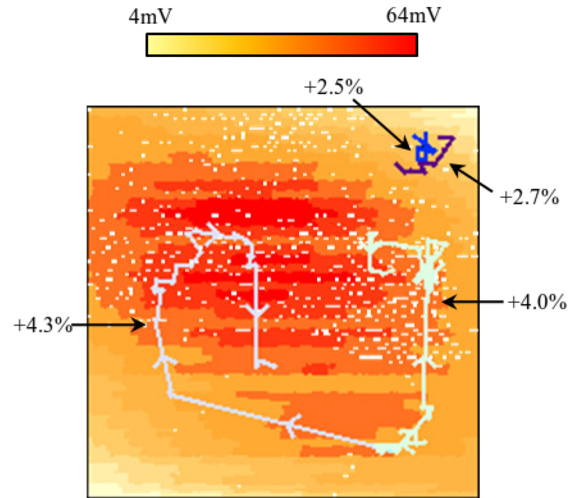

Fig. 3 Effect of path delay increase due to IR-drop.

To trade-off between accuracy and efficiency, we focused attention on cycle average power for a whole circuit which has better correlation with IR-drop and can be calculated in relatively less time. The correlation coefficients between cycle average power and IR-drop are calculated for each cell and summarized in Table 1.

Table 1 Correlation coefficient distribution.

Correlation Coefficient	#Cells
0.82 – 0.84	1
0.84 – 0.86	8
0.86 – 0.88	14
0.88 – 0.90	79
0.90 – 0.92	65
0.92 – 0.94	209
0.94 – 0.96	267
0.96 – 0.98	1814
0.98 – 1.00	2953

The correlation coefficients are distributed within 0.837 to 0.996 and the average is 0.975. Fig. 4 shows the relation between cycle average power and IR-drop for some cells with relatively high correlation coefficients. Clearly, IR-drop for these cells is almost linearly related with cycle average power even each cell has different slope.

The relation for the cell with the lowest correlation (0.837) is also plotted in Fig. 5 to investigate the IR-drop variation under the same cycle average power.

As shown in Fig. 5, the maximum IR-drop variation under the same cycle average power is approximately 10mV, which is 0.8% of the ideal power supply voltage 1.2V. It is reported that, in 90nm technology, 1% voltage variation causes approximately 4% change in gate delay [18], thus

the delay variation of this cell can be approximately 3.2%. However, Table 1 shows that only a small fraction of the cells has relatively low correlation. Since path delay consists of multiple gates/interconnects delay, the impact of delay variation on such minority cells can be negligibly small in terms of the total delay on long paths. Based on the above observation, IR-drop for a pattern can be estimated based on its cycle average power.

Our experiments seem to be inconsistent with several IR-drop analyses that consider power consumption in some restricted local regions [8, 10-13]. Naturally, local power consumption may have the better correlation with local IR-drop than global power consumption, however, the above experimental results suggest the potential to estimate IR-drop from global power. Therefore, the proposed method uses one global metric, ***cycle average power***. In the proposed method, we estimate IR-drop values of all the cells and then use the estimated voltages to evaluate path delays. That is, the estimated IR-drop values enable per-cell delay analysis for each pattern, and obtain more accurate path delay evaluation.

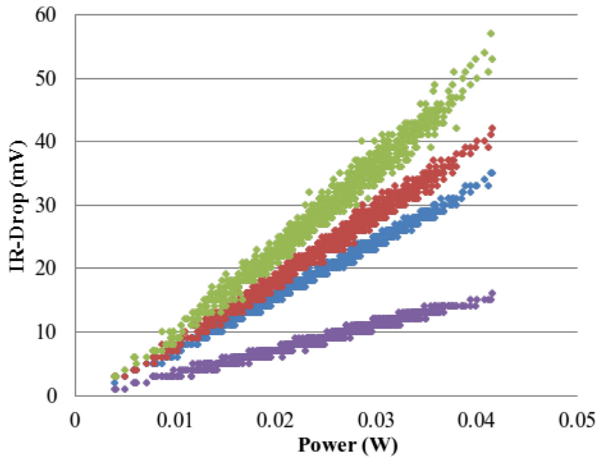

Fig. 4 Power vs. IR-drop on the cells with high correlation.

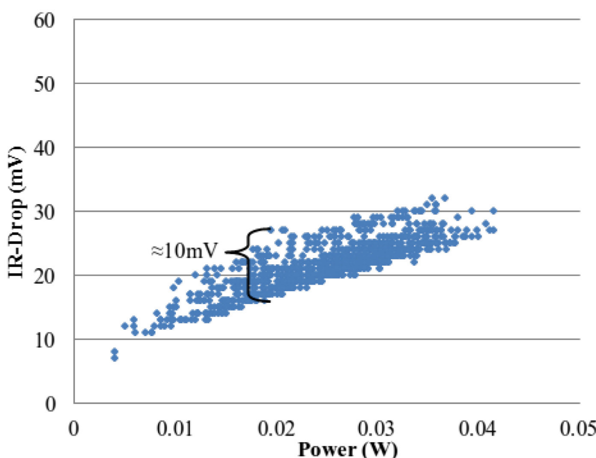

Fig. 5 Power vs. IR-drop on the cell with min. correlation.

3. Proposed Per-Cell IR-drop Estimation Method

This section describes the proposed per-cell IR-drop estimation method for achieving both high accuracy and high efficiency so as to quickly identify test patterns falling within a test set which may cause test-induced timing failure.

Fig. 6 depicts the general flow of the proposed method. The flow consists of three major steps: (Step 1) ***target pattern selection***, (Step 2) ***IR-drop estimation function derivation***, and (Step 3) ***per-cell effective voltage estimation***. After the power analysis for given test pattern set, each step of the proposed method is performed. In Step 1, a few representative patterns are selected as the inputs of the following dynamic IR-drop analysis. Next, dynamic IR-drop analysis shown in Fig. 2 (surrounded by dotted frame) is performed for selected target patterns. In Step 2, IR-drop estimation function for each cell is then derived using linear least squares fitting based on cycle average power and corresponding IR-drop value. After that, in Step 3, per-cell effective voltage profile for every pattern is obtained from cycle average power by using the estimation functions of cycle average power. Finally, voltage-annotated timing analysis is performed to obtain timing reports. The detail of each step is described in the following subsections.

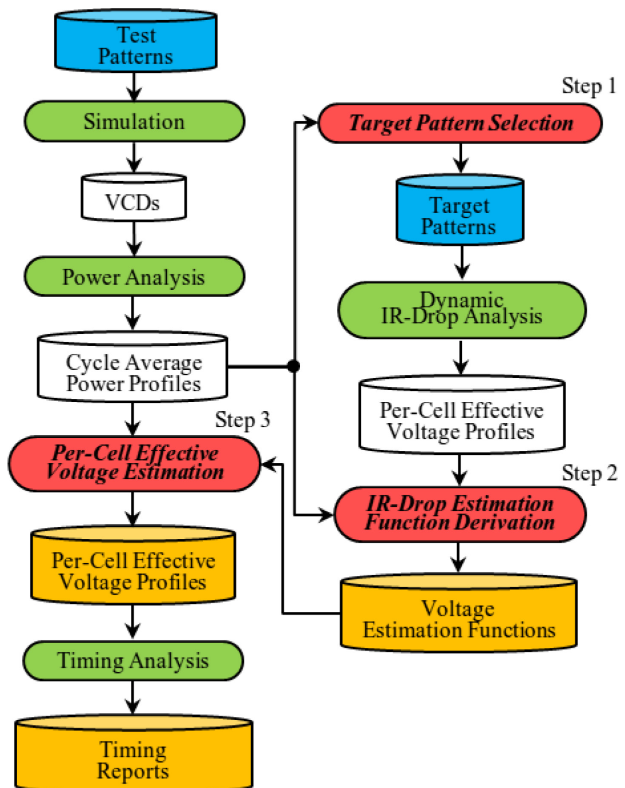

Fig. 6 General flow of the proposed method.

3.1 Target Pattern Selection

In this step, the target patterns, whose individual cycle average power profile is used for the following steps, are selected. Therefore, appropriate patterns should be selected since the way of the selection has a huge effect on the fitting accuracy.

In addition, the number of target patterns is an important factor for fitting. It also affects the total computation time since the number of dynamic IR-drop analysis executions is equal to the number of target patterns. In the experiments, we set 3, 4 and 5 as the numbers of target patterns.

The proposed method selects a given number of target patterns with a strategy to balance their cycle average power. A pseudo-code for target pattern selection is shown in Fig. 7.

```
Algorithm: Target_Pattern_Selection {
  INPUT: T = test pattern list ;
             n = number of targets ;
  OUTPUT:  T' = target pattern list ;

  sort T in descending order of cycle average power ;
  s = floor((|T| - 1) / (n – 1)) ;
  for ( i = 0 to n - 1 ) {
     append T[i * s] to T'  ;
  }
  return T' ;
}
```

Fig. 7 Target pattern selection.

For example, in the case where a list of 300 patterns, $T = \{t_0, t_1, \ldots, t_{299}\}$ (sorted in descending order of cycle average power) and the number of target patterns, $n = 3$ are given, the target pattern list will be obtained as $T' = \{t_0, t_{149}, t_{298}\}$.

The time complexity of the target pattern selection is $O(m\log m)$ for sorting a list of m test pattern plus $O(n)$ for picking up n target patterns.

This way, patterns are selected in a balanced manner, thus, accurate estimation functions are expected to be derived at the next step.

3.2 IR-drop Estimation Function Derivation

After the target pattern selection, precise dynamic IR-drop analysis is performed for the selected target patterns to obtain per-cell effective voltage profiles. Consequently multiple pairs of cycle average power and IR-drop voltage are obtained for each cell. Using the obtained pairs, the proposed method derives IR-drop estimation functions based on linear least squares fitting as described below:

Definition* 1**: Let n be the number of target patterns. Given n power-IR-drop pairs $\{(p_1, v_1), (p_2, v_2), \ldots, (p_n, v_n)\}$ where p_i and v_i are the cycle average power and IR-drop for i-th target pattern respectively, assume that an ***IR-drop estimation function for a cell with n power-IR-drop pairs is $v = b + ap$, the slope a and the intercept b are calculated as:

$$a = \frac{n\sum_{i=1}^{n} p_i v_i - \sum_{i=1}^{n} p_i \sum_{i=1}^{n} v_i}{n\sum_{i=1}^{n} p_i^2 - (\sum_{i=1}^{n} p_i)^2}$$

$$b = \frac{\sum_{i=1}^{n} p_i^2 \sum_{i=1}^{n} v_i - \sum_{i=1}^{n} p_i v_i \sum_{i=1}^{n} p_i}{n\sum_{i=1}^{n} p_i^2 - (\sum_{i=1}^{n} p_i)^2}$$

The time complexity of this step is $O(mn)$ where m is the number of cells in a circuit, and n is the number of target patterns selected in the previous step.

As a result, once the IR-drop estimation functions are derived, per-cell effective voltage for any other test pattern can be quickly estimated from its cycle average power since all cells have their individual IR-drop estimation function.

4. Experimental Results

The proposed method was implemented in Perl programming language for evaluation. In addition to the circuit b14 used in preliminary experiments in Section 2, b17, b18, and b19 of ITC'99 were also used. For these circuits, the structures of the power distribution networks are the same as b14 except that several power straps were added uniformly to avoid too much IR-drop. Clock speeds were set 3ns for b17, and 5ns for b18 and b19. To evaluate both IR-drop and delay, PDF ATPG was performed for each circuit. Per-cell effective voltage profiles for all patterns were collected by both proposed estimation method and dynamic IR-drop analysis for comparison. The number of target patterns in Step 1 of the proposed method was set 3, 4, and 5, respectively for case analysis.

Firstly, the time efficiency was evaluated in terms of CPU time as summarized in Table 2. For the proposed method, the time in computing Step 1 to 3 and in IR-drop analysis are shown in separated columns. As can be seen from Table 2, the proposed method ("Total") ran hundreds of times faster than dynamic IR-drop analysis for all patterns ("All"). The speedup ratios were almost equal to the total number of test patterns divided by the number of target patterns, since the runtimes in computing Step 1 to 3 were negligibly small. Thus, the larger the number of test patterns in a test set, the more effective the proposed method is.

In terms of accuracy, the results were evaluated based on two perspectives, IR-drop and delay as shown in the following subsections.

Table 2 CPU time for IR-drop estimation/analysis.

Circuit	#Cells (#Gates)	#Pat.	#Target Pat.	CPU Time (s) Proposed Step 1-3	IR-Drop Analysis	Total	All	Speedup Ratio
b14	5419 (10k)	953	3	0.1	20.7	20.8	6304.5	303
			4	0.1	30.1	30.2		209
			5	0.1	35.7	35.8		176
b17	16007 (32k)	983	3	0.3	60.9	61.2	20134.3	329
			4	0.4	75.6	76.0		265
			5	0.5	90.6	91.1		221
b18	48491 (89k)	1100	3	0.9	178.7	179.6	63444.9	353
			4	1.1	216.6	217.7		291
			5	1.3	293.9	295.2		215
b19	90422 (168k)	1213	3	1.6	298.9	300.5	118078.0	393
			4	2.1	381.2	383.3		308
			5	2.5	499.0	501.5		235

4.1 Evaluation on IR-drop

For each pattern, we computed the correlation coefficient and the absolute errors of all cells between estimated IR-drop and analyzed IR-drop. The results are summarized in Table 3.

Table 3 IR-drop estimation results.

Circuit	IR-drop (mV) Max.	Min.	Avg.	# Target Pat.	Correlation Coefficient Max.	Min.	Avg.	Abs. Err. (mV) Max.	Min.	Avg.
b14	77	1	30.2	3	0.9958	0.5295	0.8896	19	0	2.1
				4	0.9947	0.6483	0.9240	19	0	1.8
				5	0.9943	0.6640	0.9240	18	0	1.8
b17	59	1	20.3	3	0.9996	0.8620	0.9715	14	0	1.6
				4	0.9995	0.9015	0.9733	13	0	1.5
				5	0.9991	0.8723	0.9781	12	0	1.4
b18	134	1	37.1	3	0.9999	0.9334	0.9896	27	0	3.4
				4	0.9995	0.9358	0.9912	27	0	3.0
				5	0.9996	0.9318	0.9891	28	0	3.4
b19	347	3	157.6	3	0.9999	0.9612	0.9922	78	0	8.9
				4	0.9993	0.9668	0.9950	67	0	8.1
				5	0.9997	0.9683	0.9942	80	0	8.4

Averagely high correlation coefficients were obtained for every case. Average absolute errors were maintained within approximately 10% of analyzed average IR-drop. In addition, the correlation coefficient tends to increase as the increasing size of circuit. Indeed in b19, over 80% of all test patterns had the correlation coefficient greater than 0.99 for all cases as can be seen from Fig. 8. Moreover, the correlation further improved with increasing the number of target patterns, especially from 3 to 4.

Fig. 9 shows per-cell IR-drop maps for the patterns with (a) the maximum, (b) the median, and (c) the minimum correlation in the case of 3 target patterns in b19. For these patterns, IR-drop occurred within the range of 4mV to 308mV. As the correlation decreases, IR-drop also decreases. Especially the pattern with the minimum correlation causes notably low IR-drop compared to the other patterns.

To further investigate the relation between correlation and IR-drop, a scatter graph is plotted in Fig. 10. It can be seen that the patterns with relatively low correlation tends to cause low IR-drop. Therefore, even though there are a few patterns which have relatively low correlation, the effect on IR-drop aware timing analysis may be negligible since the delay increase in such low IR-drop pattern occurs on a small scale.

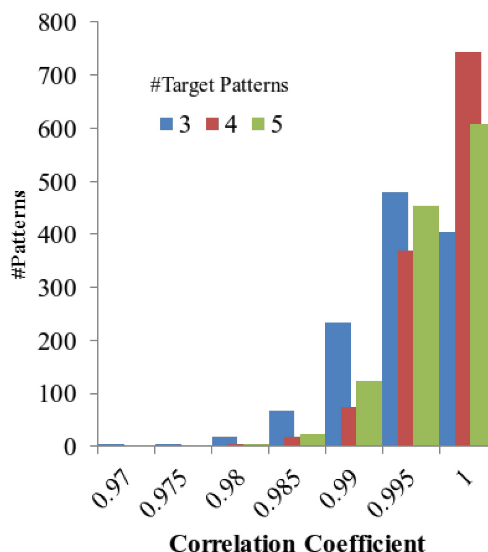

Fig. 8 Correlation coefficient distributions.

4.2 Evaluation on Delay

Next, the voltage-aware timing analysis was conducted for path delay evaluation. PDFs detected by each pattern were given as the paths under analysis. Per-cell effective voltage profiles obtained from the proposed method and dynamic IR-drop analysis were respectively used for annotation. For each path, the error rate to the delay obtained by analyzed IR-drop annotation was computed. The results are summarized in Table 4.

Table 4 Delay estimation results.

Circuit	# Paths	Delay w/ Analyzed IR-drop (ps) Max.	Min.	Avg.	# Target Pat.	Correl. Coeff.	Error Rate (%) Max.	Min.	Avg.
b14	4443	3075	616	2045.2	3	1.0000	0.8	0.0	0.2
					4	1.0000	0.8	0.0	0.1
					5	1.0000	0.7	0.0	0.1
b17	11832	2922	502	2019.0	3	1.0000	0.8	0.0	0.1
					4	1.0000	0.7	0.0	0.1
					5	1.0000	0.6	0.0	0.1
b18	18480	4975	592	2135.2	3	1.0000	1.4	0.0	0.1
					4	1.0000	1.6	0.0	0.1
					5	1.0000	1.3	0.0	0.1
b19	34858	5832	576	2191.0	3	0.9998	8.9	0.0	0.7
					4	0.9999	8.4	0.0	0.7
					5	0.9998	8.9	0.0	0.7

In terms of delay, better correlations than that of IR-drop can be seen as most of the cases have the correlation coefficients 1.0000. Indeed, the error rates were

maintained 8.9% at maximum and 0.7% on average. This indicates that the proposed method accurately estimated IR-drop especially at on-path cells.

Fig. 11 shows the relation of path delays of b19 between that obtained by analyzed IR-drop (x-axis) and that obtained by estimated IR-drop (y-axis). Regression line, regression function, correlation coefficient (R), and determination coefficient (R^2) are also shown in the graphs. For all cases, the proposed method achieved the slope of regression function and the determination coefficient nearly equal to 1, i.e., the path delays of each other are almost identical.

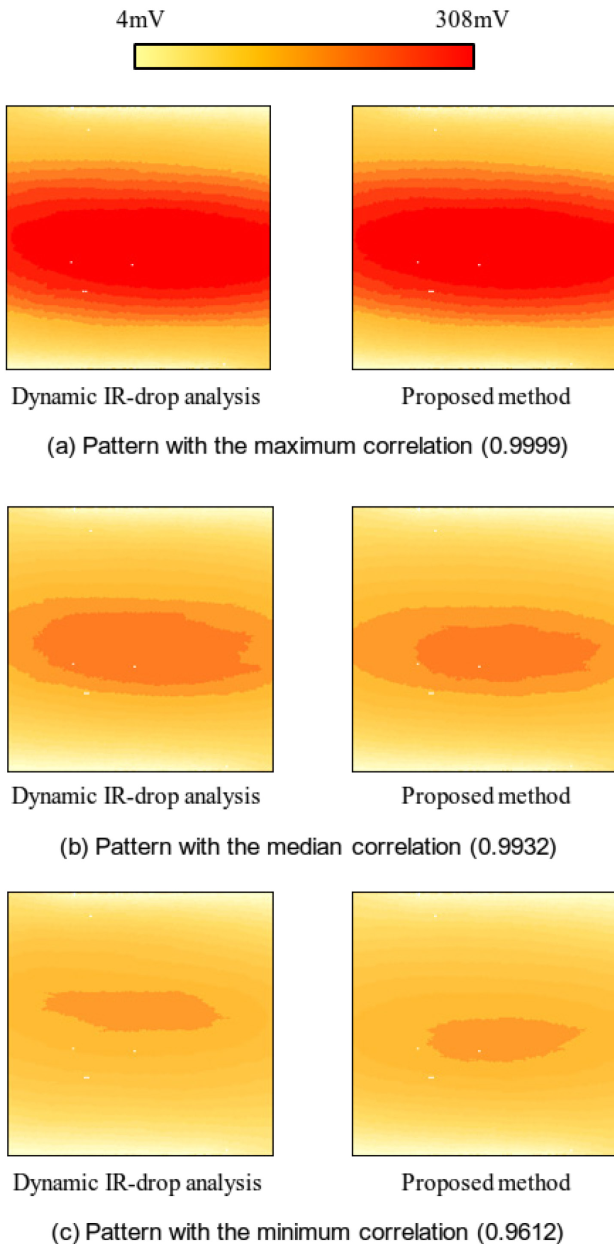

Fig. 9 IR-drop maps of characteristic patterns.

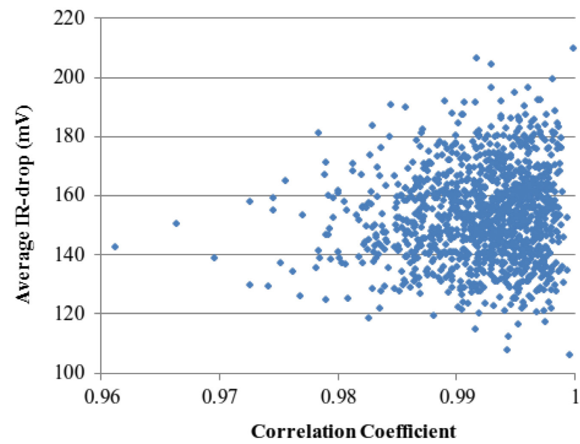

Fig. 10 Correlation vs. average IR-drop.

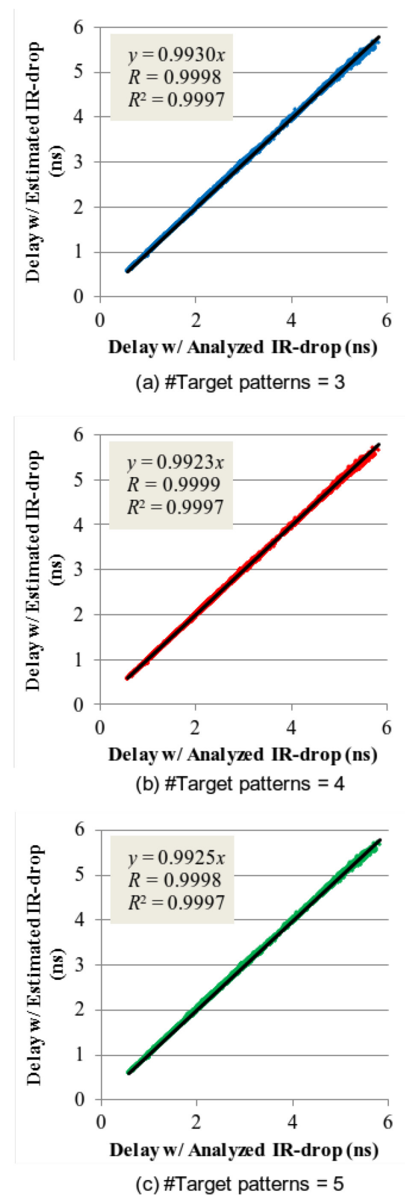

Fig. 11 Delay relations.

5. Conclusions

This paper presented a novel per-cell dynamic IR-drop estimation method for at-speed test pattern validation. The proposed method basically uses a global metric, cycle average power for estimation. For a few selected target patterns, dynamic IR-drop analysis is performed to associate global cycle power with obtained per-cell IR-drop. Then, IR-drop estimation functions are derived for each cell. As a result, the proposed method makes it possible to estimate per-cell IR-drop for other patterns using its cycle average power. In other words, local IR-drop can be estimated by global cycle average power. Experimental results have demonstrated both high accuracy and high efficiency of the proposed method. Future work includes: (1) evaluation with larger design; and (2) evaluation for shift clock skew.

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