Defect and Elemental Analysis of Oxide TFT toward an All-solution processed Device

(全溶液処理プロセスを目指した酸化物薄膜トランジスタの欠陥と元素分析)

March 2018

Chaiyanan KULCHAISIT

Graduate School of Materials Science

Nara Institute of Science and Technology

Regards to you

Abstract

The Internet of Things (IoT) has been the current trend in various applications and play an important role continuously to the future. Forthcoming information device has been introduced such as flat panel display technology, smartphone, or smart wall/ window. However, the demand for each product is rapidly getting higher in recent years. One of the most important parameters is the thin-film transistor (TFT), which acts as a switch driving current in the circuit or controlling in each pixel on the display. TFTs using amorphous oxide-semiconductor (AOS) have been emerging as a next-generation display because AOS TFTs exhibit high electron mobility even if those TFTs were fabricated at room-temperature.

Chapter 1 introduced amorphous metal oxide semiconductors such as amorphous Indium Gallium Zinc Oxide (*a*-IGZO) and amorphous Indium Zinc Oxide (*a*-IZO) semiconductor which have been used as an active channel layer in TFT, due to their high mobility (μ), good uniformity, reasonable reliability, and low power consumption. Unfortunately, costly vacuum-based techniques are required, which is a drawback in mass production. Solution-processed methods have been recently developed to replace those costly processes. However, it is extremely challenging to improve the performance of solution processed TFTs to be comparable with the traditional vacuum-based TFTs.

This study focuses on the method to improve the performance of oxide TFTs through a hybrid material called “Siloxane” utilized as a passivation layer or gate insulator (GI). Each chapter will show the improvement of electrical characteristics and study of the defect analysis mainly by Secondary ion mass spectrometry (SIMS) and X-ray photoelectron spectroscopy (XPS) to develop a high-quality device suitable for the industrial application towards the all-solution process.

In chapter 2, I examined the influence of siloxane-based passivation on the reliability of *a*-IGZO TFTs. I also examined the effect of the amount of OH bonds contained in the siloxane precursor on the reliability of *a*-IGZO TFTs. Siloxane with different chemical bonding such as high OH-bond and less OH-bond were employed. I proposed that the amount of OH-bonds in the siloxane chemical structure affects the reliability of *a*-IGZO TFTs. TFT transfer characteristic is measured by drain current (I_{ds}) - gate voltage (V_{gs}) to observe the switching behavior and to calculate the electrical characteristics. TFT reliability is characterized by a positive bias stress (PBS), the reliability was evaluated by determining the amount of threshold voltage shift (ΔV_{th}). After subjecting to PBS, the transfer curve shifted positively in parallel, and the amount of ΔV_{th} during the PBS was ΔV_{th} = 6.1 V from the initial state to 10000 sec. The film samples are investigated to study the mechanism to understand the reliability control by XPS and SIMS.

The TFTs passivated with a siloxane having less and high OH-bond were characterized after PBS (V_{gs} = 20 V, and 10000 sec). The TFTs with a siloxane having high OH-bond shows a hump effect in the I_{ds}- V_{gs} curve. The transfer characteristics of the TFTs with a siloxane having less OH-bond yielded better transfer characteristics without the hump and excellent reliability of ΔV_{th} = 1.4 V even after the PBS test.

In chapter 3, I focus on *a*-IGZO TFT top gate structure by using siloxane as a GI. This study shows a comparison of the TFT characteristics of bottom gate contact with SiO_2 GI and top gate *a*-IGZO TFT with siloxane GI. The top gate TFT showed good transfer characteristics with higher field-effect mobility (μ_{FE}) of 38.09 cm^2/Vs, lower threshold voltage (V_{th}) of 3.21 V, and lower subthreshold swing (*S.S.*) of 0.16 V/decade., Moreover, the TFT with siloxane GI also showed a smaller hysteresis loop than that of

the SiO_2 GI. The analysis results proved that hydrogen from siloxane layer diffused into *a*-IGZO layer and siloxane protected the surface of *a*-IGZO from ambient effects which improved the characteristics. The formation of additional O-H bonds in the *a*-IGZO layer from siloxane layer generated free electrons which increased the μ_{FE}. Furthermore, I confirmed that the siloxane's surface quality is suitable for GI application leading to only a slightly higher leakage current of ~10^{-9} A compared to SiO_2 GI, which has a leakage current of ~10^{-10} A.

In chapter 4, I fabricated a self-aligned TFTs through an all-solution process method by using *a*-IZO with an atomic ratio of In:Zn = 77:23 as both a semiconductor and electrode material. Here, I will show how UV treatment can be used to increase the amount of oxygen vacancies in *a*-IZO and transform it into an electrode. The 50-nm-thick *a*-IZO layer is deposited by spin coating on the substrate. GI used is a siloxane with a thickness of around 100 nm. To make source/drain and gate electrodes I deposit *a*-IZO layer again on top and then utilize the UV treatment to irradiate specific areas of the *a*-IZO film reducing the resistivity of the affected area from 7.0×10^{-2} Ω-cm to 6.73×10^{-4} Ω-cm after UV-induced transformation. This study also showed the first switching characteristics without any metal electrode fabricated by an all-solution process, in which the μ_{FE}, V_{th}, *S.S.*, and on/off ratio were 8.02 cm^2/Vs, 3.70 V, 0.32 V/decade, and 10^7, respectively.

This research establishes the benefits of solution processed siloxane as a good passivation layer and gate insulator in improving oxide TFT electrical characteristics. Hydrogen, oxygen, and hydroxide from siloxane support the oxide channel to improve the TFT performance. According to these results, the novel structure of an all-solution processed TFT will play a major role in the next generation devices.

Contents

Chapter 1
Introduction

1.1 Background

The Internet of Things (IoT) is becoming increasingly commonplace nowadays. IoT consists of a gigantic network of internet-connected things and devices. Presently, people are spending a few minutes to access information across the world, interact with machines through the screen system, receive worldwide information by using a personal computer or easily communicate with each other via a social network. This generational trend started when the machines have been providing direct communication with people.

The first radio voice transmission took place in 1900 and then the development of computers began in the 1950s [1], which are necessary components for developing IoT. The name IoT has not been around for very long and the concept became more clearly imagined in 1994 when the world's first smartphone from IBM was developed which included telephone touchscreen features, email capability, and other functionalities [2].

In 2007, human living behavior was changed after the first iPhone was released by Apple Inc. [3]. The most interesting thing is the buttonless or touchscreen system with expanded and wider display that made the mobile phone more beneficial with a variety of application such as playing games, watching movies, or browsing the internet. With these applications, it is undeniable that the iPhone is a standard prototype for the smartphone in the 2000s. Recently, the smartphone market is getting more competitive together with the challenge of device development by breaking through several material limitations. Figure 1.1 shows the trend of the smartphone evolution from the past until

now, starting with curved to rollable display. All trends lead to incorporating the flexibility of the whole device, which can be wearable, comfortable, and unbreakable.

Flat-panel display (FPD) is one of the most important components which plays a major role in this technology: not only is the demand in the smartphone market increasing but also the demand for automotive touch panel monitors as shown in Figure 1.2. FPDs are finding widespread use in many new products, such as smartphones, automotive displays, tablets, portable games, laptop personal computers (PCs). Organic light emitting diode (OLED) and active matrix OLED (AMOLED) display become trending nowadays as in Figure 1.3 and 1.4, respectively, due to their higher resolution, less noise, and brighter light while using less energy than existing LCD/LED technologies. These devices are expected to be slim, lightweight, rugged, and portable. Having all these attributes will enable a wide variety of commercial applications in the future.

A display is composed of a grid or matrix of picture elements called pixels. Thousands or millions of these pixels together create an image on the display. Thin-film transistors (TFTs) act as switches to individually turn each pixel on to pass light or off to darken the display. The TFTs are the active elements, arranged in a matrix, on the display. In many types of research, researchers fabricate TFTs because an advantage of TFTs is that a wide array of substrates can be used. For instance, the flexible display was developed by fabrication of TFTs on plastic substrates to respond to a high demand for flexible display in the future as shown in Figure 1.5.

Figure 1.1 Display evolution trend until now [4].

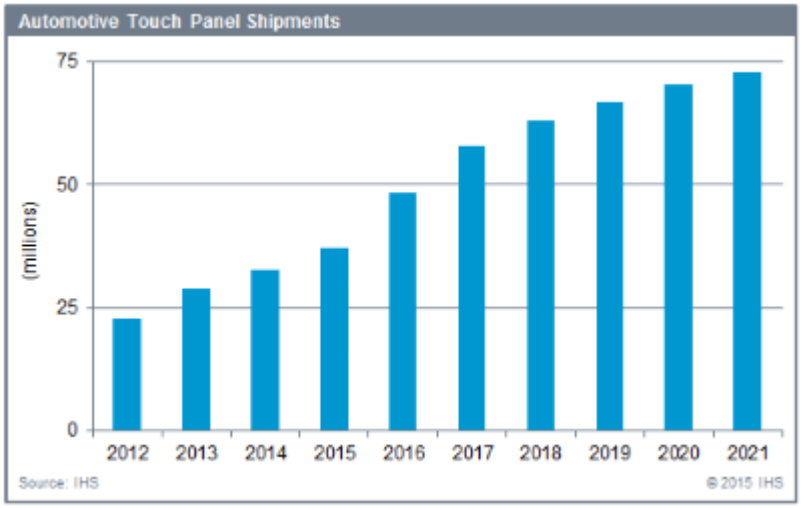

Figure 1.2 Automotive touch panel forecast by IHS [5].

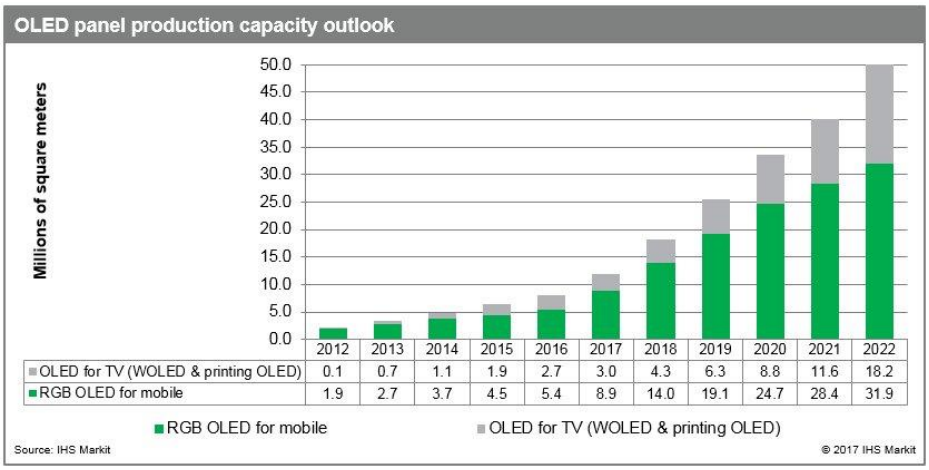

Figure 1.3 OLED panel production forecast by IHS [6].

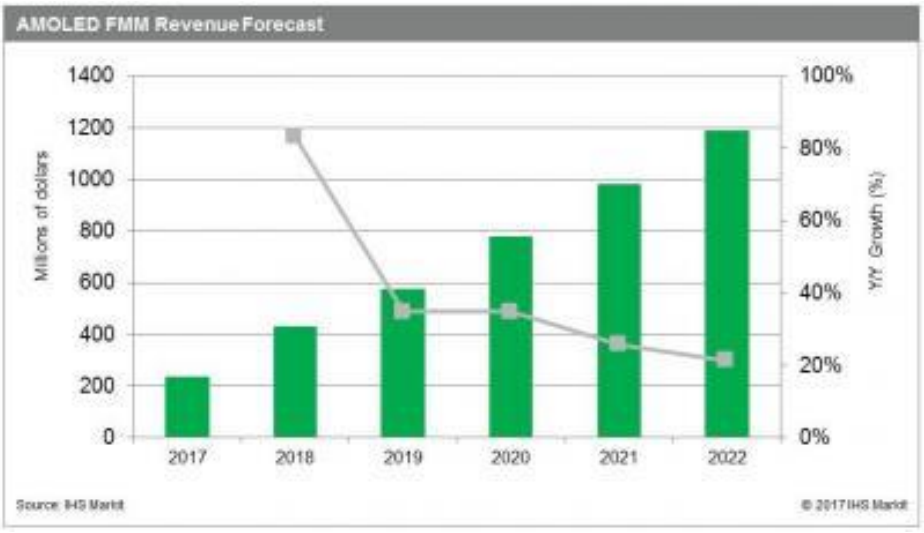

Figure 1.4 AMOLED forecast by IHS Market [7].

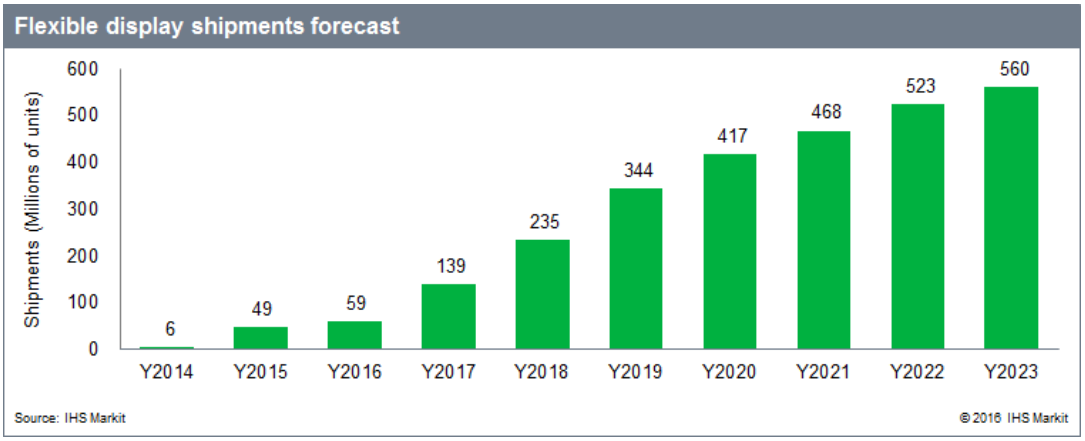

Figure 1.5 flexible display shipment forecast by IHS [8].

1.2 Thin-film Transistor (TFT)

1.2.1 TFT technology and performance

Thin-film transistors (TFTs) are indispensable in future extensive network technology as they can be used to develop advanced electronic devices applications such as liquid-crystal display (LCD) technology, displays attachable to windows and walls as shown in Figure 1.6, that may have advantages such as flexibility, lightweight, impact

resistance and low cost [9]. TFT is a special kind of field-effect transistor which consists of a semiconductor, gate insulator, electrode, and substrate as the main structure called metal-insulator semiconductor field-effect transistor (MISFET) [10].

At this moment, the thin layer can be mainly formed by two kinds of processes. The most common process is vacuum process such as physical vapor deposition and plasma-enhanced chemical vapor deposition. An emerging method that is used instead of the traditional process is solution process such as spin-coating, sol-gel, and 3D printing technology [11]. After a sputtered material was formed on the substrate, a pattern can be created by a lithography technique and etching [12].

For the operation of TFTs, TFTs have three metal-electrode terminals: the source, gate, and drain. Usually, the source is at zero potential, and the required voltage is applied to the drain. The semiconductor region between the source and drain is called the channel and the resistance of the channel changes when a voltage is applied to the gate. The current which flows between the source and drain is controlled by the gate voltage and the TFTs act as switches in a circuit. Various materials have been examined as a channel layer, amorphous oxide materials are promising for next-generation display because they can provide high electrical mobility (>8 cm^2/Vs), lower process fabrication temperature (room temperature), and higher scalability (2200×2500 mm) compared with a commercial silicon [13]. For more detail, the oxide semiconductor will be described in section 1.4.

Figure 1.6 The example of future display project of self-driving car by Mercedes (left) and transparent display by Panasonic (right) [14,15].

A TFT is a class of field-effect transistor (FET) comprising three important terminals (gate, source, and drain) and including semiconductor, a gate insulator, and conductive electrode. The semiconductor placed between the source and the drain electrodes to form the channel layer or the current flow between drain and source. Next is the gate insulator that is located between the gate electrode and the semiconductor, usually using a high dielectric constant (k) material as a gate insulator to increase the TFT transconductance and avoid the dielectric breakdown. The general idea for this device is to control the current between drain and source (I_{ds}) by varying the potential between gate and source (V_{gs}), which induces free charge accumulation at the gate insulator/semiconductor interface [16].

TFT structure can be specified by four possible ways by stacking order of the gate electrode, channel layer, and source/drain electrodes. As illustrated in Figure 1.7, these four structures are (i) staggered bottom-gate, (ii) staggered top-gate, (iii) coplanar bottom-gate, and (iv) coplanar top-gate [17]. This designation depends on the gate electrode location as well as the relative position of the source/drain and gate terminals. For more simplicity, if the gate electrode is on top of the channel layer, the device structure is a top-gate type. In contrast, if the gate electrode is below the channel layer, the device structure is a bottom-gate type. When the source/drain electrodes and the gate

electrode are on the opposite side of the channel, the device has a staggered structure. Furthermore, if both the source/drain electrodes are on the same layer with the channel, the device has a coplanar structure.

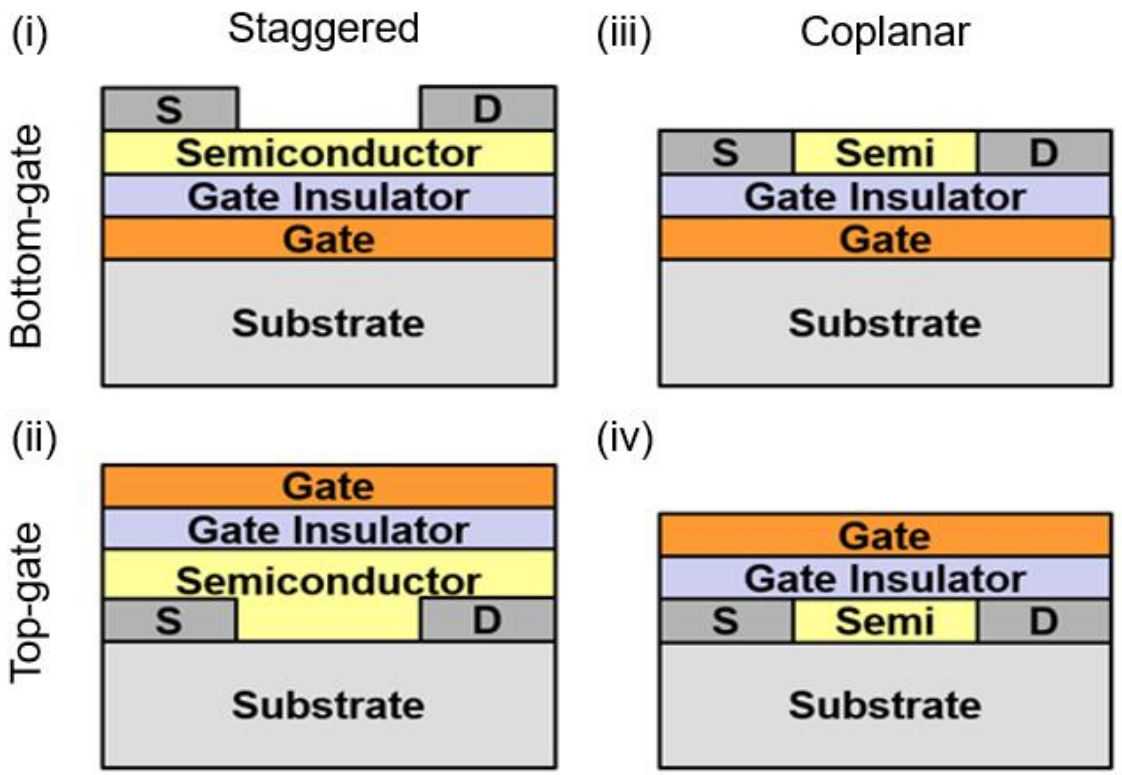

Figure 1.7 Illustration of the different types of TFT structure.

The selection of a structure depends on the suitable parameters such as the material type, fabrication methods, deposition technique, post-processing treatment, or a number of steps of the UV-lithography masks involved. For example, if the semiconductor is very sensitive to the ambient environment, a top-gate structure is a favorable choice because the semiconductor layer is protected by the top layers such as gate insulator layer and provides self-passivation. However, since the gate insulator film is deposited after the semiconductor layer, the fabrication conditions for the gate insulator,

such as the processing temperature or plasma condition, become a concern because they can alter semiconductor properties. Another example in which either a staggered bottom-gate or a coplanar top-gate structure would be preferred if the semiconductor layer is very fragile. In such a situation, source/drain electrode formation should not involve the use of an etchant. Instead, a liftoff patterning procedure is preferred [18].

For the TFT operation, the type can be designated by enhancement or depletion mode depending if the threshold voltage (V_{th}) is positive or negative. Enhancement mode is typically preferred because a gate voltage is not necessary to turn off the device or to achieve its off-state [19]. The depletion mode devices are still useful for circuit fabrication such as loads for nMOS logic circuitry. When $V_{gs}>V_{th}$, a significant density of electrons is accumulated at the gate insulator/semiconductor interface and a large I_{ds} starts flowing, depending on the drain-to-source potential (V_{ds}).

A typical characterization of TFTs involves source to drain (I_{ds}) versus voltage from gate to source (V_{gs}) measurements where transfer curves are obtained as shown in Figure 1.8. The transfer curve offers a quantitative analysis and the following electrical characteristics can be determined: (i) Field-effect mobility (μ_{FE}) is one of the most used methods to determine in TFTs, which is obtained after the transconductance (g_m) at low V_{ds}. (ii) Saturation mobility (μ_{sat}) is also commonly determined in TFTs and it describes a situation with the effective length. As for μ_{sat}, it is obtained from g_m but at high V_{ds}. (iii) The threshold voltage (V_{th}) corresponds to the V_{gs} for which a significant charge is accumulated close to the gate insulator/semiconductor interface. A possible methodology to determine this parameter is using a linear extrapolation of the I_{ds}-V_{gs} at low V_{ds}. (iv) Subthreshold swing (SS) is the parameter that indicates the V_{gs} required to increase I_{ds} by one decade, as seen in the subthreshold region, which is defined in V/decade. (v) On/off

ratio (I_{on}/I_{off}) is the ratio of the maximum to minimum I_{ds}. The on and off current have prescribed values wherein a higher on-current offers better driving capability, while a lower "off" current results in low leakage current and reduced idle power consumption. All these parameters are extremely relevant to evaluate the TFTs performance and understanding these can enable TFT integration into more complex systems.

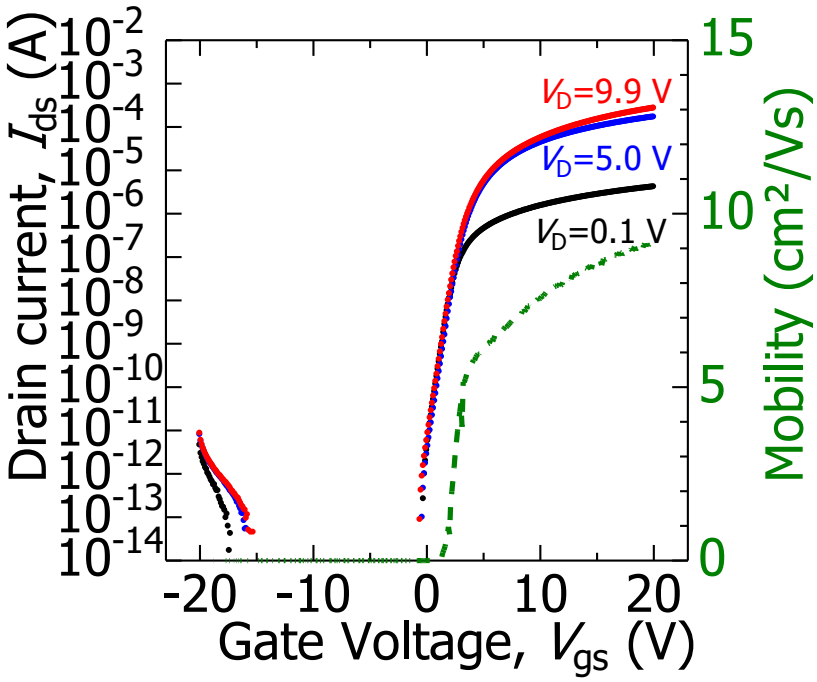

Figure 1.8 Transfer curve of an n-type TFT.

1.3 Trend and issues of future TFTs

Even though the lack of ability compared to the principal TFT technology which is *a*-Si:H, oxide TFTs are starting to assume a dominant role in the display industry, through a lot of announcements of commercially available products integrating this technology: from large area 4k OLED TVs to smartphones. Moreover, a lot of progress will certainly be performed in the future on oxide TFTs that will enable an ever more

applicable existence in different markets, ranging from fully transparent displays to disposable products.

The current research trends in this area are summarized by following: research of new approaches in order to optimize processes, improve TFT performance, and reduce the high cost during the fabrication process. Beside this, there is a consistent research for alternative and sustainable oxide semiconductors and gate insulators, both in terms of creating novel materials such as hybrid inorganic/organic are also included, and innovative structures, where nanostructures as multi-channel nanowires and nanoparticles are deserving increased attention for ultimate performance levels [20].

Another interesting topic is the transfer of fabrication process from vacuum process to simpler solution process, such as spin coating, sol-gel, or printing technology. Even if the initial works on solution processed oxide TFTs were based on high temperature processes and yielded low performance [21,22], currently, there are quite interesting reports on these devices processed at temperatures as low as 200°C suitable for the flexible plastic substrate, giving similar characteristics to their vacuum processed counterparts [34–36].

In terms of p-type oxide TFTs, which are required for CMOS architectures using oxide technology, materials as tin and copper oxide have been produced at room temperature and annealed at temperatures as low as 200 °C. However, the device performance is far subpar compared with that achieved with n-type oxide TFTs [23,24]. With these research techniques, oxide materials can be processed at very low temperatures given the great environmental concern these days. Flexible substrates and low power circuits have also been considered. Nowadays, researchers are developing new

ideas such as introducing paper in electronics, realizing a recycle electronics concept. [25,26].

1.4 Oxide semiconductor TFTs

1.4.1 Oxide material properties and its applications as a channel layer of TFTs

In principle, the semiconductor materials that are used as TFT channel layers are hydrogenated amorphous silicon (*a*-Si:H) and polycrystalline silicon semiconductors. However, compared to *a*-Si:H TFTs, Amorphous oxide semiconductor (AOS) TFTs provide much higher mobility. In contrast, compared to polycrystalline silicon TFTs, AOS shows much lower off current, more suitable fabrication in large-area electronics applications because of the absence of grain boundaries that provide good uniformity, ultra-smooth surface and it can be made by low temperature process.

AOS materials are one of semiconductor channel materials candidate used to make a TFT. Other semiconductor materials can also be used as TFT channel layers such as organic semiconductors. However, organic TFTs still have many issues such as poor mobility, poor reliability, and non-uniformity. Among all AOS materials that have been studied, most are n-type semiconductor [27]. The p-type AOS material has also been reported in [28] but the film contains nanocrystalline-embedded amorphous phases.

AOS are ionic materials composed of multi-cation-component metal oxides [29]. Cations employed are selected from the periodic table columns 11 to 15 and rows 4 to 6. Such cations possess an outer shell electronic configuration of $(n-1)d^{10}ns^{0}$, where $n \geq 4$. Out of all the 15 metal elements in this group, only a few metal oxide combinations have been found to be useful for TFT applications. Some metals form oxides with poor

conductivity. Due to these cations providing a demerit in each element, some elements have high toxicity such as As, Cd, Hg, Pb or some element are expensive such as Ga, Ge, In, Au. The most common AOS currently under investigation include indium gallium zinc oxide (IGZO) [30], zinc-tin-oxide (ZTO) [31], and indium zinc oxide (IZO), since they can generate high mobility and large on/off current ratio[32]. At the moment, IGZO TFTs are mainly moving towards commercialization with high mobility, low sub-threshold swing, and better bias stress stability compared to other oxide materials.

The AOS material development concept originated from Hosono and coworkers, in the topic of " Novel oxide amorphous semiconductors: transparent conducting amorphous oxides" and "Working hypothesis to explore novel wide bandgap electrically conducting amorphous oxides and examples" in 1996 [33,34] for creating transparent conductive oxides. To achieve both high transparency and conductivity, Hosono and his coworkers, summarized their research following (i) a large overlap between relevant orbitals is required. (ii) Use multiple cations to depress film crystallization and keep the material amorphous. (iii) Multi-component oxides are preferable to single oxides with respect to the formation of an amorphous state.

In ionic oxides, the conduction band minimum (CBM) is formed primarily by the metal cation's vacant ns-orbital. Since a ns orbital is isotropic and has large ionic radii, the electron clouds of atoms are jointed together like a chain as in Figure 1.9 [35]. Due to the direct overlap between neighboring metal ns-orbitals, a continuous path will be formed, which improves carrier transport and mobility. For comparison, in a conventional covalent semiconductor such as silicon, the conduction band minimum, and valence band maximum are made of highly directional sp^3 hybridized orbitals that form anti-bonding and bonding states, respectively. For covalent amorphous semiconductors, structural

distortion significantly degrades bond overlap. Therefore, the electron mobility is reduced severely. For example, the mobility of *a*-IGZO TFT is in the range of 10-40 cm^2/V-s, while the mobility of *a*-Si:H TFT is only around 1 cm^2/V-s or less.

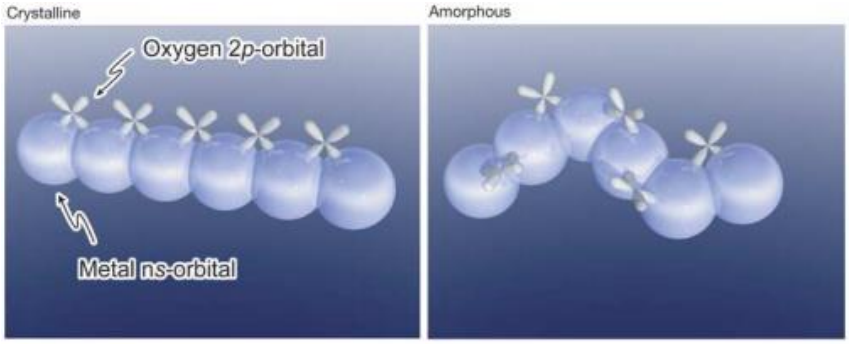

Figure 1.9 Schematic orbital drawing for the carrier transport path of crystalline and amorphous oxide semiconductors [35].

1.4.2 Degradation of TFTs on the backchannel

Figure 1.10 shows the major degradation behavior of the oxide semiconductor which focuses on the ambient effect or adsorption and desorption of the water and oxygen molecules on the backchannel surface [36]. Ambient impurities can easily adsorb on the backchannel and act as an electron donor by increasing electrons in the backchannel surface makes higher carrier concentration which affects the threshold voltage shifts to the negative side. In contrast, oxygen from the ambient will react with electrons inside the channel layer forming an oxygen ion, which induces a lower carrier concentration and makes the threshold voltage shifts to the positive side. This phenomenon leads to the poor reliability of oxide TFTs, especially those with a bottom gate structure [37,38].

Other degradation behavior is related to the vacuum process deposition, which damages the backchannel during deposition of succeeding layers. This effect generates

interface trap which worsens the electrical characteristics or induces the channel layer to become highly conductive [39].

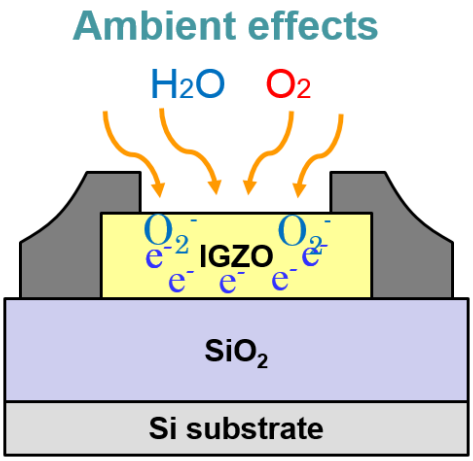

Figure 1.10 Illustration of adsorption and desorption of the water and oxygen molecules in the backchannel of bottom gate *a*-IGZO TFTs.

1.4.3 Gate insulators and their issues

Gate insulators are an important parameter in the TFT design structure, which usually require smooth surface roughness to avoid electron scattering from the channel, high capacitance to increase the electrical transconductance, and high thickness to avoid breakdown voltage and current leakage. The most common gate insulator is silicon dioxide, which has a capacitance of 3.45×10^{-8} F/cm^2 with 100-nm-thickness, on the silicon substrate since fabricating the silicon dioxide is very simple while adhering to gate insulator requirements.

Unfortunately, the limitation of silicon dioxide makes TFT electrical performance not reach as high as expected. It is very difficult to match an alternative gate insulator material with an oxide TFT due to a combination of physical adjustments. Because of the capacitance and thickness constraints are almost directly opposed to each other. An important parameter to support that requirement, which would allow higher

capacitance with the same thickness is to use high dielectric constant (high-k) materials. High-k materials are used as a gate insulator, which can generate high electrical characteristics such as very high mobility, low operation voltage, and increased current density.

However, there are physical limitations with high-k materials such as interface quality which limits the ability to maintain high dielectric constants at high frequencies. Although high-k materials have high-permittivity, most results of high-k gate insulators shown non-ideal insulating behavior due to their complicated transistor fabrication process integration and presence of various charged defects such as fixed charges, interface/bulk traps, accumulated charges and mobile ions [40]. These effects have been studied by observing the TFT stability test such as bias stress test, hysteresis loop, and/or a degradation in the transfer curve due to charge scattering [41].

Solution-processed high-k gate insulators were introduced to be an alternative for all-solution processed flexible electronics applications, but it seems like charge defect issues have become more seriously problematic [42]. The main issues of solution gate insulator are the degradation, which caused by the trapping of electric charge due to weak bonds such as hydrogen in the insulator film. In the case where a large amount of hydrogen is contained in the gate insulator, deterioration of threshold voltage and sub-swing threshold shift due to hydrogen diffusing into oxide semiconductor to form a shallow trap state [43].

As mentioned above, in order to improve the electrical performance of the oxide TFT, it is required to select the gate insulator having a smooth surface, small trap level, high dielectric constant, and able to apply with solution process devices.

1.4.4 Solution process fabrication routes

Solution process fabrication is recently booming in both inorganic and organic TFT research and development. This alternative method is used instead of the traditional vacuum-based process to increase scalability with cost-effective manufacturing [43]. In history, the first motivation for solution process is a manufacturing cost reduction due to an increase in throughput as measured in area per unit time [44]. Krebs et al, also estimated the comparison process cost, materials cost, and step cost between traditional and solution manufacturing [45].

The starter routes is a formation of a chemical structure to create a solution precursor or a nanoparticle, which form as an electronic material after heat treatment [43]. The solution or particle is able to be deposited on the substrate by a variety of deposition techniques such as spin-coating, blade-coating, dip-coating, sol-gel, spray pyrolysis, electrochemical, ink-jet printing, and screen printing.

Solution processes usually include two baking step, which is (i) pre-baking above 100ºC for a decomposition or hydrolysis and (ii) post-baking in a higher temperature for alloying or dihydroxylation cured a thin-film on the substrate [43]. However, the electrical characteristics of solution processed TFT tend to depend on synthetic conditions. Ultimately, the TFT performance of solution processed TFTs is poorer compared with vacuum-based processed TFT. It is a big challenge in this thesis to improve the solution processed TFT performance together with lower process complexity in the TFT fabrication process.

1.5 Objectives

This thesis is composed of 5 chapters which are explained in the following sections. Three main objectives will be discussed in each section. The main goal is to understand the elemental effect, which can improve the TFT performance applying for all-solution processed flexible devices application. In the previous study [46], I found that the defects inside the semiconductor can be suppressed by siloxane passivation layer. Moreover, siloxane passivation is a solution processable inorganic-organic hybrid material, which combined many desirable properties such as high thermal resistant, high transparent, and easy to fabricate by spin-coating. However, high amount of hydroxide on the *a*-IGZO surface can instigate hump phenomenon that decreases the reliability of the TFTs.

Beginning with chapter 2, to evaluate the reliability of TFT devices both chemical and physical influences should be considered, because multiple variables, that can affect the properties of the channel layer, can increase the performance of the oxide TFT. the study of the impact of –OH content in siloxane passivation materials, which affects the reliability of *a*-IGZO TFTs is discussed. The reliability issue will be solved by finding suitable passivation used to improve the reliability and also enhancing the electrical characteristics of *a*-IGZO TFTs that can be fabricated by solution process for next generation of flexible electronics.

Inorganic-organic hybrid passivation based on siloxane-bond will be compared with the amount of the hydroxide-bond in the chemical structure inside the siloxane passivation, which are high OH-bond, less OH-bond and oxide TFT without passivation as a reference. This study will have a high impact for solution processed TFTs, in which I suggest that siloxane not only a great barrier protecting the semiconductor surface from

external ambient but also elements inside siloxane such as hydrogen, oxygen, and hydroxide have significant roles to play in improving the performance of the channel layer which is lacking in solution processed TFTs. Bias stress results of siloxane passivation, which are high OH-bond and less OH-bond are compared with unpassivated TFT. Together with the Secondary Ion Mass Spectrometry (SIMS), X-ray Photoelectron Spectroscopy (XPS), the reliability tests, the stability improvement mechanisms are examined and the role of H, O, and OH in improving the stability and properties of *a*-IGZO are discussed in the mechanism section.

Chapter 3 will be discussing the methods to improve the performance of top gate *a*-IGZO TFTs using a solution processed gate insulator. As mentioned in the previous section about the trend of using high-k materials for gate insulator to lower operating voltages and increase current density; although high-k gate insulator seems to be the best candidate for making as a gate insulator, various limitations still need to be improved. The new challenge begins with the development of a suitable material for gate insulator. In the previous chapter, I proposed that the amount of H and OH from siloxane layer affects the electrical characteristic of bottom gate oxide TFTs. As measured by a metal-insulator-metal (MIM) method, siloxane shows comparable capacitance and gate dielectric value with the traditional *a*-Si:H GI suitable for making a solution processed GI on oxide TFTs.

In this chapter, I try to prove that this material can improve the TFT characteristics and reliability as both passivation layer and gate insulator roles, which can be used in printable, flexible, and transparent devices in the future. Understanding an effect of hydrogen and hydroxide, which affects the TFT electrical characteristics is also

important for many semiconductor research field to find a suitable technique for improving the device performances.

The evaluation of TFT performance will be discussed by examining the value of electrical characteristics that are mobility (μ), the threshold voltage (V_{th}), subthreshold swing (*SS*), on/off ratio, and hysteresis (V_H). The improvement of the TFT performance will be confirmed by SIM, XPS, Scanning Transmission Electron Microscopy (STEM), and Atomic Force Microscopy (AFM) analysis to observe the defect and elemental effect.

The benefit of solution processed hybrid inorganic-organic siloxane materials suitable for both passivation and gate insulator leads us to begin the new challenge to fabricate and develop high performance all-solution processed TFTs which is discussed in chapter 4 to make an all-solution process TFT without any additional source/drain metal deposition electrodes by UV treatment.

This chapter, transparent conducting oxide (TCO) films will be introduced and the *a*-IZO material is selected as a candidate to transform semiconductor-to-conductor in a selected area by increasing the number of oxygen vacancies inside the *a*-IZO bulk. The self-aligned TFTs are fabricated through an all-solution process method by using *a*-IZO with an atomic ratio of In:Zn = 77:23 as a semiconductor and electrode material.

Here, I will show how UV treatment can be used to increase the number of oxygen vacancies in *a*-IZO and transform it into an electrode. All layers will be deposited by only spin-coating process together with using UV lithography for patterning. for simplicity, I still used a thermally oxidized SiO_2 on Si as a substrate, which has no effect on those deposited layers on top. Elemental composition, structure, and defects were observed by performing cross-sectional imaging by the STEM (elemental and structural analysis) with Energy-dispersive X-ray (EDX) Spectroscopy. The electrical properties

are evaluated by analyzing the TFT transfer characteristics. To confirm the transformation of *a*-IZO from semiconductor to conductor, the resistivity is calculated by the value of the sheet resistance measured by a 4-point-probe. Furthermore, the mechanism will be elucidated by performing SIMS for diffusion study, and XPS for chemical structural observations and comparing the oxygen vacancy concentrations between IZO before and after UV treatment. This study will gain a large impact on the solution processed devices to reduces the process complexity, process cost, together with electrical characteristics improvement.

Chapter 5 is the overall conclusion of this thesis and further suggestions for expanding developments are also discussed in this chapter. The results and analysis in this thesis will provide benefits especially for the state-of-the-art research on solution processed TFTs by developing highly reliable, printed, transparent, and flexible oxide semiconductor devices.

References

[1] K. D. Foote, A Brief History of the Internet of Things dataversity, (2016).

[2] D. AAmoth, First smartphone Turns 20, TIME, (2014).

[3] D. Grabham, History of the iPhone 2007-2017, T3 Smarter Living, (2017).

[4] LG Display, www. lgdisplay.com.

[5] IHS, Automotive Touch Panel Shipments, (2015).

[6] IHS, OLED panel production capacity outlook, (2017).

[7] IHS Markit, AMOLED FMM Revenue Forecast, (2017).

[8] IHS Markit, Flexible display shipments forecast, (2016).

[9] K. Nomura, et al., Appl. Phys. Lett. **99**,053505 (2011).

[10] S. J. Lim, et al., Appl. Phys. Lett. **91**, 183517 (2007).

[11] S. W. Hsieh, et al., Appl. Phys. Lett. **74**, 2638 (1993).

[12] E. Lausecker, et al., Appl. Phys. Lett. **96**, 263501 (2010).

[13] K. Nomura, et al., Appl. Phys. Lett. Vol. **45**, No. 5B, pp. 4303-4308 (2006).

[14] CES Conference, Self-Driving car, (2015).

[15] CES Conference, Transparent Display, (2016).

[16] A.C. Tickle, Wiley, (1969).

[17] S. Wolf and R. N. Tauber, Lattice Press, (2000).

[18] J.-H. Lee, S.-T. Wu, and D.N. Liu, Wiley, p. 280 (2008).

[19] R.L. Hoffman, B.J. Norris, J.F. Wager, Appl. Phys. Lett. **82**(5), 733 (2003).

[20] C. Opoku, K. F. Hoettges, M. P. Hughes, V. Stolojan, S. R. P. Silva, and M. Shkunov, Nanotechnology, **24**(40), 405203 (2013).

[21] Y. Wang, S. W. Liu, X. W. Sun, J. L. Zhao, G. K. L. Goh, Q. V. Vu, and H. Y. Yu, J. Sol-Gel Sci. Technol. **55**(3), 322-327 (2010).

[22] K. Song, D. Kim, X. S. Li, T. Jun, Y. Jeong, J. Moon, J. Mater. Chem. **19**(46), 8881-8886 (2009).

[23] K. K. Banger, Y. Yamashita, K. Mori, R. L. Peterson, T. Leedham, J. Rickard, and H. Strringhaus, Nat. Mater. **10**(1), 45-50 (2011).

[24] Y.-H. Yang, S. Yang, C.-Y. Kao, and K.-S. Chou, IEEE Electron Device Lett. **31**(4), 329-331 (2010).

[25] R. F. P. Martins, A. Ahnood, N. Correia, L. M. N. P. Pereira, R. Barros, P. M. C. B. Barquinha, R. Costa, I. M. M. Ferreira, A. Nathan, Adv. Funct. Mater. **23**(17), 2153-2161 (2013).

[26] R. Martins, A. Nathan, R. Barros, L. Pereira, P. Barquinha, N. Correia, R. Costa, A. Ahnood, I. Ferreira, E. Fortunato, Adv. Mater. **23**(39), 4491-4496 (2011).

[27] T. Kamiya and H. Hosono, NPG Asia Mater. **2**(1), 15-22 (2010).

[28] T. Kamiya, et al., Adv. Func. Mater. **15**, pp. 968-974 (2005).

[29] H. Hosono, Journal of Non-Crystalline Solids, **352**, pp. 851-858 (2006).

[30] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, Nature, **432**, 488-492 (2004).

[31] H. Chiang, J. Wager, R. Hoffman, J. Jeong, and D. A. Keszler, Appl. Phys. Lett. **86**, 013503-013503-3 (2005).

[32] N. Dehuff, E. Kettenring, D. Hong, H. Chiang, J. Wager, R. Hoffman, et al., J. Appl. Phys. **97**, 064505-064505-5 (2005).

[33] H. Hosono, M. Yasukawa, and H. Kawazoe, J. Non-Crystalline Solids, **203**, 334-344 (1996).

[34] H. Hosono, N. Kikuchi, N. Ueda, and H. Kawazoe, J. Non-Crystalline Solids, **198**, 165-169 (1996).

[35] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, Nature, **432**(7016), 488-492 (2004).

[36] D. Kang, H. Lim, C. Kim, I. Song, J. Park, Y. Park and J. Chung, Appl. Phys. Lett., **90**, 192101 (2007).

[37] K.-H. Lee, J. S. Jung, K. S. Son, J. S. Park, T. S. Kim, R. Choi, J. K. Jeong, J.-Y. Kwon, B. Koo, and S. Lee, Appl. Phys. Lett., **95**, 232106 (2009).

[38] J. K. Jeong, H. W. Yang, Jong Han Jeong, Yeon-Gon Mo, and Hye Dong Kim, Appl. Phys. Lett. **93**, 123508, (2008).

[39] T.-C. Chen, T.-C. Chang, T.-Y. Hsieh, C.-T. Tsai, S.-C. Chen, C.-S. Lin, M.-C. Hung, C.-H. Tu, J.-J. Chang, and P.-L. Chen, Appl. Phys. Lett. **97**, 192103 (2010).

[40] S. Y. Lee, S. Chang, and J.-S. Lee, Thin Solid Films, **518**, 3030-3032 (2010).

[41] A. I. Kingon, J.-P. Maria, and S. K. Streiffer, Nature, **406**, (2000).

[42] H. Kim, Y.-J. Kwack, E.-J. Yun, and W.-S. Choi, Sci. Rep. **6**:33576 (2016).

[43] W. Xu, H. Wang, L. Ye, and J. Xu, J. Mater. Chem. C. **27**, (2014).

[44] D. B. Mitzi, Solution Processing of Inorganic Materials, Wiley, (2008).

[45] F. C. Krebs, M. Jørgensen, K. Norrman, O. Hageman, J. Alstrup, T. D. Nielsen, J. Fyenbo, K. Larsen, and J. Kristensen, Solar Energy Materials & Solar Cell, **93**, 422-441 (2009).

[46] C. Kulchaisit, Master thesis, Nara Institute of Science and Technology (2015).

Chapter 2
Analysis of the oxide TFTs using solution processed siloxane passivation

2.1 Introduction

Oxide TFTs have critical instability issues against light illumination, temperature, bias stress, and ambient gases which cause unstable electrical characteristics. Among these instability issues, oxide TFTs are vulnerable to threshold voltage (V_{th}) shifts caused by O_2 and H_2O acting as donor-like states and acceptor-like states, shifting the V_{th} of oxide TFTs to a positive and negative direction. For these reasons, protection in the form of a passivation layer is necessary for the oxide TFTs to prevent adsorption of ambient O_2 and H_2O [1].

A passivation material is deposited on an AOS layer to provide electrical stability to enable prevention of the transistor surface from electrical and chemical conditions in the environment; to reduce reverse-current leakage, to increase breakdown voltage and to raise the power dissipation rate. The common passivation materials used in *a*-IGZO is inorganic and organic passivation materials. This work will discuss the fabrication process and a comparison between both passivation materials [1-4].

In this study, an inorganic-organic hybrid passivation material called siloxane is introduced with the goal of replacing inorganic or organic materials. This is because the siloxane itself can combine both the merits of inorganic and organic due to its designable chemical structure. Different types of siloxane categorized by its photo-sensitive function type and material properties are also introduced, which affect the *a*-IGZO electrical

characteristics. The ideal siloxane type that is suitable for *a*-IGZO in this research is then chosen, together with an explanation of the fabrication process of the siloxane passivation with the *a*-IGZO TFTs in each condition.

The electrical characteristics and reliability of the TFTs after passivation in each condition are measured. The mechanism of the main defect in this study, which is the trap defects due to ambient and hump effect, are also explained in the last section. Controlling the amount of OH-bond in the siloxane material affects the electrical characteristics and reliability of the device. Thus, elemental characterization and analysis are important to understand the effect of the passivation layers on the *a*-IGZO TFTs.

2.2 Passivation material type

The passivation layer growth on the surface of a semiconductor to provide electrical stability by isolating the transistor surface from electrical and chemical conditions in the environment; this reduces reverse-current leakage, increases breakdown voltage and raises power dissipation rating. Many kinds of passivation material exhibited improved bias stability due to effective protection from external molecules. Research has shown that inorganic and organic material passivation layers to prevent O_2 and H_2O adsorption [1-18].

2.2.1 Inorganic passivation layers

Inorganic materials such as SiO_x [2, 5-6], SiN_x [2,7], Al_2O_3 [8,9] Y_2O_3 [10], and TiO_x [11] are well-known passivation layers which act as a barrier that protects the oxide semiconductor. Extensive research has shown that oxide TFTs can be improved by adding these materials, which act as good protectors from external ambient effects. This can be

observed from results derived from bias stress tests such as positive bias stress (PBS) and negative bias stress (NBS) together with other effect condition such as under light illumination and high temperature.

However, high vacuum, high temperature, and more complex fabrication processes are needed in vacuum-based processes – such as physical vapor deposition (PVD), plasma-enhanced chemical vapor deposition (PECVD), and atomic layer deposition (ALD). Moreover, plasma damage during the fabrication process increases traps or defects on the oxide semiconductor surface [12]. This side effect decreases the electrical characteristics of the device such as threshold voltage and electrical uniformity. To solve this problem, researchers have shown that by adding the etching stop layer (ESL), the plasma damage effect is significantly reduced, but more complicated processes are needed.

2.2.2 Organic passivation layers

Inorganic materials are used as the conventional passivation layers of oxide TFT. However, high-temperature process requirements are incompatible with flexible display devices because fabrication on a polymer substrate requires a low fabrication temperature (<200˚C). Also, their low flexibility results in a limitation of flexible display devices due to brittle properties. Furthermore, plasma-based vacuum processes cause performance degradation of the TFTs, are typically complicated processes, and incur a high unit cost of production.

Current trends entail a low cost and simplified process wherein an organic passivation has become one of the candidates to replace the conventional inorganic passivation layer for their properties of low dielectric constant. There have been studies

on organic passivation materials such as polydimethylsiloxane (PDMS) [19], poly(methyl methacrylate) (PMMA) [20], photoacryl and CYTOP [12], to overcome the above-mentioned limitations of inorganic passivation layers. These materials can be fabricated at low temperatures (under 200˚C) at atmospheric conditions, thus eliminating the need for expensive vacuum equipment, through solution process methods such as spin coating, sol-gel methods, and printed process [14-18].

By using these methods, organic passivation has a major advantage compared to vacuum-based inorganic passivation because of the potential for largely scalable fabrication that uses a less complex method. The solution process method such as printing is also an additive process which involves less waste and has a location-selective deposition. However, barrier performance against ambient gas is lower than inorganic passivation layers because of high permeability against gases caused by the intrinsic material properties [19,20].

2.3 Siloxane hybrid materials

According to the problems mentioned earlier for both inorganic and organic passivation, to overcome the disadvantages of conventional inorganic and organic materials, a siloxane hybrid material can be used for making passivation layer [21]. Table 1.1 shows a comparison of polymer materials for passivation. Siloxane is the most promising material for the future device because of its excellent heat resistance and transparency, which is suitable for high-temperature fabrication process of transparent TFT.

Table 1.1 Comparison of passivation materials [21].

Materials	Siloxane	Polyimide	Acrylic resin
Dielectric constant	3-3.8	3.5	3.5-3.8
Refractive index	1.5-1.6	1.5-1.6	1.5-1.6
Transmittance	>99%	<90%	98%
Heat resistance	~350ºC	~350ºC	~250ºC

2.3.1 Types of siloxane and their chemical structure

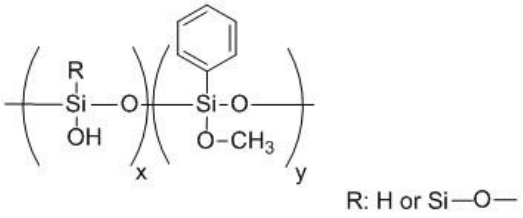

Figure 2.1 Chemical structure of siloxane material.

Organic-inorganic hybrids based on a Si-O backbone, siloxane combines many desirable properties of conventional organic and inorganic components by adjusting the radical bonding in the chemical structure, such as good thermal stability, rigidity, transparency to UV and visible light, and photo-stability. As shown in Figure 2.1 – the chemical structure of siloxane that is used in this work – the Si-O backbone has an inorganic bond with the methyl, phenyl, and other designable organic constituent groups. These designable functional groups make siloxane a versatile material. The attached constituent groups can be tailored to fit a variety of characteristics such as photosensitive and non-photosensitive functionality.

One of the merits of photosensitive type siloxane film is that it can be removed by a solution after UV exposure without needing an additional method such as dry etching or sputtering deposition for inorganic passivation layer. Nonetheless, non-photo-sensitive

siloxane still has good demand for device industries because of the manufacturing process to make attractive future printed applications and devices.

In my previous study [22], I fabricated both photosensitive and non-photo-sensitive siloxane to compare the electrical characteristics and reliability of *a*-IGZO TFTs. I subjected the TFTs to bias stress test to understand the effect of the passivation on the reliability of *a*-IGZO TFT. Positive bias stress (PBS, V_{GS} = 20 V) was applied to both photo-sensitive and non-photo-sensitive siloxane passivated TFTs.

A comparison of the electrical characteristics of the device after PBS showed that photo-sensitive siloxane had less ΔV_{th} than other conditions with just only the hump effect decreasing the reliability (section 2.5 explains the hump effect). On the other hand, a non-photo-sensitive siloxane with more molecular weight showed a large negative shift of ΔV_{th}. Thus, holes are trapped in the shallow state, making the *a*-IGZO TFTs unstable. Hence, hydrogen on the *a*-IGZO surface can instigate hump effect to occur on I_{DS}-V_{GS} curves, because of charge accumulation present around the source and drain before channel formation.

In this study, I demonstrate the reliability improvement of siloxane passivated *a*-IGZO TFT by optimizing the number of hydroxyl or OH-bond inside the chemical structure of siloxane to reduce the extra charge, which causes the hump effect.

2.3.2 Material properties

Siloxane materials are organic-inorganic hybrid materials that combine the inorganic characteristics presented by the siloxane bond (Si-O-Si), which constitutes the main chain, and the organic characteristics presented by the organic functional group that constitutes the side chain such as methyl, phenyl, and vinyl.

Siloxane has a feature where the design flexibility is very high since the siloxane bond of the inorganic structure shows excellent transparency (~99%), heat resistance (<350˚C), hardness, and electrical resistance.

The organic functional group gives such functions as compatibility or dispersion stability, adjustment of fraction and permittivity, and reactivity (epoxy, acryl, etc.). More specifically, the organic functional group conquers the disadvantages of organic materials, including brittleness, flexibility, formability, and reactivity, and the siloxane-bond supplements the disadvantages of organic materials, including heat resistance, weather resistance, dimensional stability (thermal expansion), and flame resistance.

Furthermore, it is known that siloxane shows a random structure, ladder structure, cage structure, and shows different characteristics not only by changing the types of organic functional bases, but also the control of such structures, the degree of polymerization, or the molecule end group [s].

2.3.4 Fabrication process and characterization of *a*-IGZO TFT with siloxane passivation

Figure 2.2 illustrates the fabrication process of *a*-IGZO TFTs with the siloxane passivation layer. Gate electrode and gate insulator material are made of highly conductive n-type Si substrate with a thermally oxidized SiO_2 layer of 100 nm. These substrates were cleaned by concentrated sulfuric acid (H_2SO_4) at 80°C for 10 minutes then mixed with hydrogen peroxide (H_2O_2) for 10 minutes. The cleaned substrates were inserted to the sputtering chamber and vacuumed at 10^{-6} – 10^{-7} Torr and deposition of the 70-nm-thick *a*-IGZO layer, which was mainly studied in this work, as the channel material by RF magnetron sputtering method at room temperature (RT) was carried out.

Argon and oxygen were introduced at 4.5×10^{-3} Torr before sputtering. 13.56 MHz RF at a power of 100 W was applied at RT and then argon plasma was generated. The generated plasma sputters the *a*-IGZO target whose stoichiometric ratio is 2:2:1:7. To obtain a stable deposition rate, pre-sputtering was performed for 5 minutes. Finally, the *a*-IGZO was deposited at a rate of 10 nm/minute.

The *a*-IGZO films used in this study were evaluated in the as-deposited condition. The channel material was patterned using UV photolithography and wet etching by HCl solution for 7-14 minutes. In this study, photolithography was utilized in order to pattern the channel material to reduce the off-current. Contact type mask aligner (SUSS MicroTec) was used in this process.

First of all, a positive photoresist was evenly formed on the sample by spin-coating with a rate of 3000 rpm. The sample was then baked on the hot plate at 100^{o}C to harden the photoresist: this process is called pre-bake. Through the metal mask, the sample received intensive UV light. The exposure duration was set to 10 seconds. The desired pattern was formed when the sample was dipped in the developer: AZ 300 MIF developer (2.38 %, AZ Electronic Materials plc) etches cured resist for 90 seconds at RT.

In order to stabilize the designed photoresist pattern, the sample was finally heated at 120^{o}C what is so-called post-bake. The photolithographic patterned sample was needed to be etched to pattern the *a*-IGZO layer. To etch the *a*-IGZO layer, 0.02 M HCl was used. Because the area which was covered with photoresist is inert to the solvent, only bare *a*-IGZO would be etched. The etching process was performed at RT with a rate of 5.0 nm/minutes. After 14 minutes etching, the photoresist was removed by acetone to obtain the surface of the *a*-IGZO. The source and drain electrodes were a stack of 80-nm-thick molybdenum and 20-nm-thick platinum deposited by a RF magnetron sputtering

method and patterned using a lift-off technique. The *a*-IGZO channel layer patterned with photo-resist on SiO_2/ Si substrate was inserted into the sputtering chamber and vacuumed at 10^{-6} – 10^{-7} Torr. Argon was introduced at 4.5×10^{-3} Torr before sputtering. RF with 13.56 MHz at a power of 100 W was applied at RT and then argon plasma was generated.

The depositions of metal were fabricated with a deposition rate of 10 nm/min for 80-nm-thick molybdenum and 20-nm-thick platinum. To form the source and drain pattern, metal layer which deposited on a designed area of photoresist was etched away by acetone called lift-off process. Cleaning by methanol and deionized water was performed to finish the process. All fabricated TFTs were subjected to post-annealing at 300°C for 120 minutes in the ratio of N_2/O_2 (4/1) ambient atmosphere. The fabricated TFTs had a bottom gate top contact structure and the channel width (W) and length (L) were 90 and 10 μm, respectively.

We fabricated siloxane with less OH-bond with the different synthetic condition from siloxane with high OH-bond. This material will be polymerized by condensation between Si-OH branches. We accelerated the condensation reaction, depending on the type and amount of catalyst, by changing the catalyst between Si-OH bonds. Furthermore, increasing the condensation reaction will give less residual –OH bond by losing higher density water molecules as a by-product of the solution.

For the siloxane with less OH-bond, we changed the catalytic species which allows for more condensation reaction and, thus, there will be less –OH group. Here, the residual –OH bond is more than 85 % in the high OH-bond solution and 10% in the less OH-bond solution. Spin-coating served a siloxane polymer layer on TFTs, at a rate of 1500 rpm for 15 seconds. Prebaking was then performed at a temperature of 110°C for 1 minute. The contact holes for non-photo-sensitive siloxane passivation were fabricated

by reactive ion etching (RIE) process with a gas ratio of CF_4/ Ar =30/ 45 sccm for 60 seconds. To remove the volatile and finish the cross-linking reaction of the siloxane, baking was performed under an N_2 atmosphere at 230°C for 20 minutes and 300°C for 20 minutes, respectively. A post-annealing treatment at 300°C for 120 minutes in oxygen ambient atmosphere finished making TFTs with passivation layer as shown in figure 2.3.

Current (I) - Voltage (V) characteristics such as transfer characteristics measurements were performed with Agilent HP4156C semiconductor parameter analyzer. The switching of fabricated devices was traced by applying voltage to gate from -20 V to 20 V whose step was 100 mV, and applying voltage to drain from 0.1 V to 9.9 V whose step was 4.9 V. In order to check the stability, the TFTs with/without passivation were characterized after positive bias stress (PBS) with the condition of gate voltage V_{GS} = 20 V for 10000 seconds and negative bias stress (NBS) with the condition of gate voltage V_{GS} = -20 V for 10000 seconds. For understanding the mechanism, both *a*-InGaZnO TFTs with and without passivation were analyzed by XPS and SIMS [21].

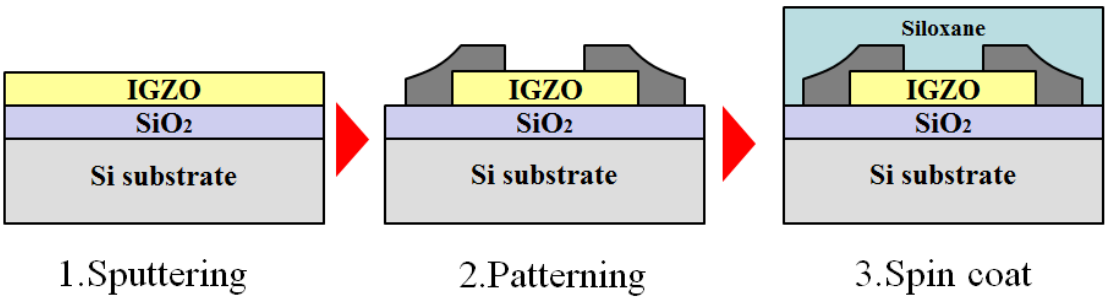

Figure 2.2 Fabrication process of *a*-IGZO TFTs with passivation layer.

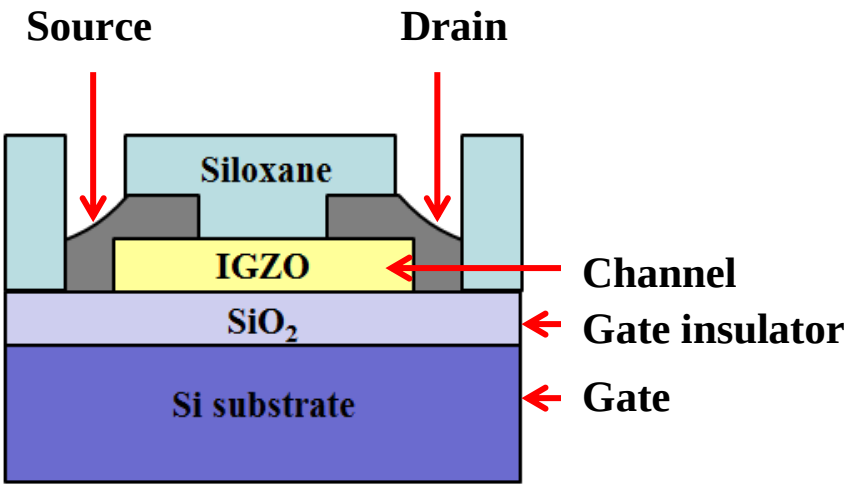

Figure 2.3 Structure and operation principle of the TFT.

2.4 Improvement of electrical characteristics and stability test of bottom gate oxide TFT

The principal TFT electrical characteristics operation is usually observed from the transfer characteristics, which plots the current from source to drain (I_{ds}) versus voltage from gate to source (V_{gs}) across different voltages from drain to source (V_{ds}). With I_{ds}- V_{gs} transfer curve, we can measure the carrier mobility in the channel (μ), the pseudo-constant or threshold voltage (V_{th}), subthreshold swing (SS), and on/off current ratio, which is major parameters used to evaluate the quality of the TFT. The field-effect mobility (μ_{FE}) is a general term including μ_{sat}, while it is also used as a specific definition. The μ_{FE} is calculated from transfer characteristics in the linear I_{ds}- V_{gs} region and V_{ds} must be as small as possible, in this case, we used V_{ds} at 0.1 V and used equation (2.1).

$$I_{ds} = \frac{W}{L}\mu C_i V_{ds}\left(V_{gs} - V_{th}\right) \tag{2.1}$$

Where W is the width, L is the length of the oxide channel, C_i is the capacitance of the gate insulator, and V_{th} is obtained from the plotting of I_{ds}- V_{gs} or defined as the V_{gs} at 1 nA. In the linear region (at low V_{ds}), μ can be obtained by directly measuring the transconductance (g_m), which is a function of V_{gs} and is the ratio of the change in I_{ds} to the change in V_{gs}. Thus, the μ is obtained by the maximum value using the following equation:

$$\mu = g_m \frac{L}{WC_iV_{ds}} \tag{2.2}$$

The TFT characteristics are also evaluated from the output characteristics, which plots I_{ds} versus V_{ds} at different V_{gs}. Basically, output characteristics of oxide TFTs will show a clear separate region of linear and saturation region. For the *SS* value, which reflects the value of V_{gs} required to obtain a 10 times larger I_{ds} in the subthreshold region. It is defined as $SS = dV_{gs}/dlog_{10}I_{ds}$. Ideally, the value of *SS* should be as small as possible or the subthreshold region of the transfer characteristics should be as steep as possible to enable quicker turn-on operation of the TFT.

I fabricated *a*-IGZO TFTs without passivation as a reference to serving as a standard for the fabricated TFTs. The post-annealing treatment at 300°C for 120 min in ambient atmosphere showed good transfer characteristics for the TFTs, which has a channel width and a length of 90 and 10 μm, respectively. Figure 2.4 showed the initial transfer characteristics of three types of TFTs: TFT without passivation, TFT with a siloxane having less OH-bond which showed the effective switching behavior, and TFT with a siloxane having high OH-bond which exhibited a defect phenomenon called hump effect. The hump effect often affects the transfer characteristics of the TFTs and is present

in the subthreshold region of the device. It is related to the accumulated charge in the active layer on the two lateral sides of the channel, resulting in a crowding of the electric field lines and local reduction in the V_{th}. All conditions were measured and the resulting TFT characteristics were good [23]; the mobility was more than 9 $cm^2 \cdot V^{-1} \cdot s^{-1}$, sub-threshold swing (*SS*) was less than 200 mV/decade, and the on-off current ratio (I_{on}/I_{off}) was larger than 10^6.

The most important parameter to evaluate the quality of the passivation is to measure the reliability. The bias stress testing is an important tool to analyze the reliability of *a*-IGZO TFTs [24]. Stress can be applied by applying a constant voltage on the V_{gs}, V_{ds}, or both over a long period of time. In general, when bias stress is applied to TFTs, the device will exhibit degraded behavior in the transfer characteristics as a change in μ, a shift in V_{th}, and hump effect. The reliability was evaluated by determining the amount of threshold voltage shift (ΔV_{th}). In this thesis, all tested TFTs had a channel *W/L* of 90 µm and 10 µm, respectively. All stress conditions were performed for 10^4 s with no applied voltage across the source and drain electrodes (V_{ds} = 0 V). Bias stress tests were carried out with a semiconductor parameter analyzer (Agilent, 4156C) under dark condition, room temperature, and air ambient atmosphere.

Figure 2.5 (a) shows the transfer characteristics of the unpassivated *a*-IGZO TFT during PBS test. After subjecting to PBS, the transfer curve of unpassivated *a*-IGZO TFT shifted positively in parallel, and the amount of ΔV_{th} shift during the PBS was ΔV_{th} = 6.1 V from an initial state to 10^4 seconds. The TFTs with siloxane that has a high amount of OH-bonds were characterized by PBS (V_{gs} = 20 V, and 10^4 seconds), as shown in Figure 2.6 (a), the ΔV_{th} shift reduced to nearly 0 V but the large hump effect occurred on I_{ds}-V_{gs} curve leading to instability.

The transfer characteristics of the TFTs with a siloxane having less OH-bond are shown in Figure 2.7 (a). These TFTs exhibited good transfer characteristic without the hump and excellent reliability with a ΔV_{th} = 1.4 V even after the PBS. Comparison of the two passivated samples shows that the TFTs with a siloxane having less OH-bond not only have a lesser ΔV_{th} but also lesser degradation in *SS*. Without including the hump phenomenon, it can be observed that there is a very small ΔV_{th} shift after each bias stress for both passivated TFTs which confirmed that a protection film reduces the degradation due to trap defect or adsorption and desorption of the water and oxygen molecules on the surface of the *a*-IGZO semiconductor [21].

In contrast, even if the ΔV_{th} of *a*-IGZO TFTs is hardly affected by NBS because *a*-IGZO TFTs is n-type, the hump effect in the subthreshold region occurs after NBS. This hump effect during NBS is larger than in PBS test, especially in the TFTs with a siloxane having high OH-bond.

To confirm the hypothesis, TFT with siloxane passivation without OH-bond was fabricated as a reference. The chemical structure of this siloxane was adjusted by adding methyl radical instead of -OH radical to avoid the hump phenomenon. As shown in figure 2.8, the TFT shows better reliability compared with unpassivated TFT without hump phenomenon. Notice that methyl-group-based functional groups inside siloxane chemical structure can easily shrink during the fabrication that causes the non-uniform thickness and enables oxygen from the ambient to pass through the passivated layer resulting in a shifting of ΔV_{th}.

These results show TFTs with a siloxane having less OH-bond have excellent barrier properties to prevent adsorption of oxygen and water, which demonstrate an

improved stability of *a*-IGZO TFTs. It is also important to point out that the amount of OH-bond directly affects the electrical characteristics of the passivated *a*-IGZO TFTs.

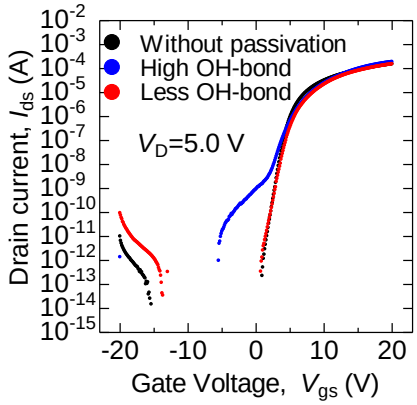

Figure 2.4 Initial transfer characteristics of three types of TFTs: TFT without passivation (black), with siloxane having high OH-bond (blue) and with siloxane having less OH-bond (red) passivation. (V_{ds}=5.0 V)

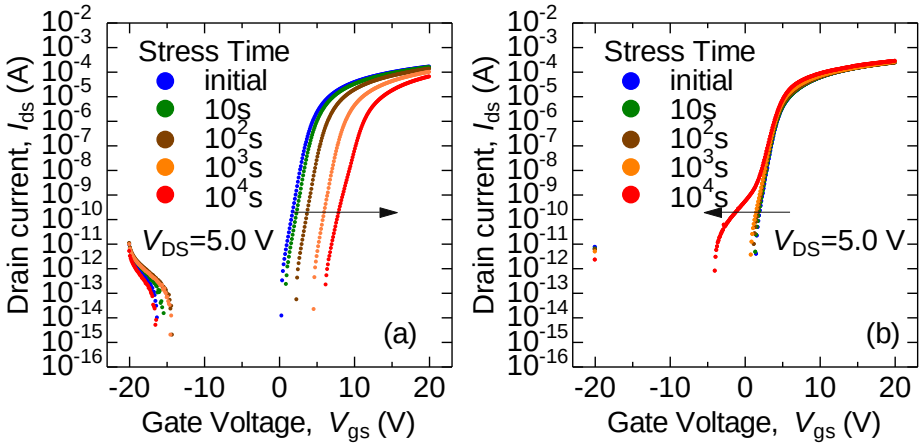

Figure 2.5 Transfer characteristics under PBS (V_{gs} = 20 V) (a) and NBS (V_{gs} = -20 V) (b) for unpassivated *a*-IGZO TFT.

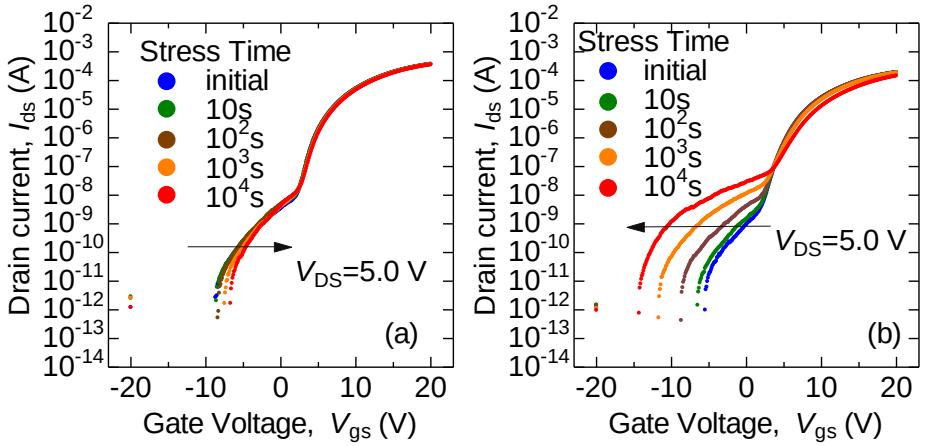

Figure 2.6 Transfer characteristics under PBS (V_{gs} = 20 V) (a) and NBS (V_{gs} = -20 V) (b) of *a*-IGZO TFT with siloxane passivation having high OH-bond.

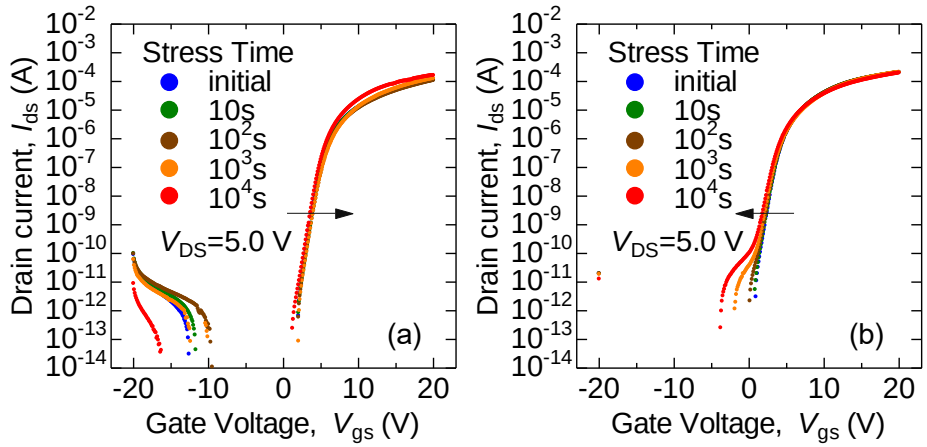

Figure 2.7 Transfer characteristics under PBS (V_{gs} = 20 V) (a) and NBS (V_{gs} = -20 V) (b) of *a*-IGZO TFT with siloxane passivation having less OH-bond.

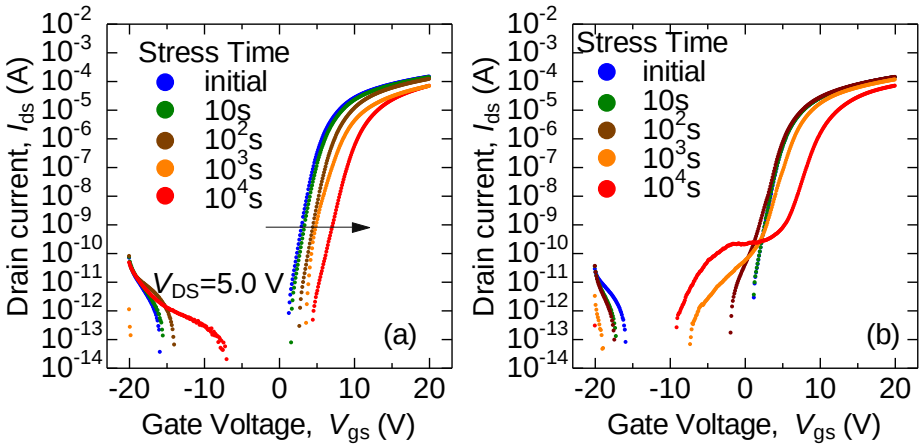

Figure 2.8 Transfer characteristics under PBS (V_{gs} = 20 V) (a) and NBS (V_{gs} = -20 V) (b) of *a*-IGZO TFT with siloxane passivation without OH-bond.

2.5 Reduction of hump effect

The improvement of the reliability during PBS is because siloxane acts as a good barrier of *a*-IGZO TFTs to protect the *a*-IGZO surface from the adsorption and desorption of water and oxygen molecules. After passivation, oxygen cannot pass through the passivated layer which makes ΔV_{th} smaller as shown in Figure 2.6 (a) and Figure 2.7 (a).

The large hump effect of TFTs with a siloxane having high OH-bond indicates that this hump phenomenon occurs through the accumulation of positive charge that comes from oxygen vacancies or hydrogen interstitials [25]. This phenomenon is observed in the passivated TFTs which have high OH bond which showed the largest hump in the transfer characteristics. Meanwhile, the suitable amount of OH bond represented by the passivated TFTs which have less OH bond shows extremely sharp subthreshold region without a significant hump.

To confirm the mechanism of the hump phenomenon, the change in chemical bonding states of oxygen (O1s) in the *a*-IGZO layer was studied using XPS. The siloxane passivation layer on *a*-IGZO was removed by RIE process prior to measuring the surface

of *a*-IGZO. As shown in Figure 2.9, the interface analysis of O1s XPS profiles revealed the emergence of a 3rd peak in the passivated sample at ~ 532 eV (blue curve in Figure 2.9) which is attributed to a peak related to hydroxide that was shown only in the passivated TFTs [21].

This result confirmed that hydroxide from the siloxane with less OH-bond produced less bonding transformation at *a*-IGZO surface compare with the siloxane with high OH-bond. Both passivated and unpassivated samples show the deconvolution of two peaks at ~ 531 (red curve in Figure 2.9)) and ~ 530 eV (green curve in Figure 2.9) which is attributed to oxygen deficiency region which roughly corresponds to V_O amount, and oxygen bonding with metal, respectively [21].

The amounts of hydroxide can be estimated by the area ratio of the peaks (the peak area related to hydroxide region divided by all area). The area ratio of the hydroxide region (~532 eV) of the TFTs with the siloxane having high OH-bond exhibited the highest value of 27% than that of the passivated TFTs with siloxane with less OH-bond, which have only 4%. Moreover, the data of V_O amount represented by oxygen deficiency region peak (~ 531 eV) also confirmed that the peak of V_O area ratio decreased from 48% to 34% for both passivated samples compared to unpassivated TFT. This result suggests that there is a reduction in V_O after the passivation. The increase of the hydroxide bond and reduction of the V_O are reflected in the ΔV_{th} reduction for both passivated TFTs.

These results prove that the hump phenomenon occurs when the *a*-IGZO has residual hydroxyl-group on the surface. Siloxane with less OH-bond showed good TFT switching behavior without hump effect in the initial state of the transfer curve. The hump from the initial state, which occurs only for the high OH-bond condition as shown in figure 2.6, is due to a high number of hydroxyl groups from the siloxane passivation layer.

Figure 2.10 shows the intensity comparison of OH-bonds in *a*-IGZO bulk (around 70 nm-thick) by SIMS (ULVAC-PHI ADEPT-1010) with Cs+ ion source (1keV and 50 nA). The results support the effect of hydroxyl (-OH) group which enables the improvement of the reliability and electrical characteristics of the device. The intensity of 16O + 1H shows the amount of OH-bond between without passivation, high OH-bond, and less OH-bond. Both passivated samples had higher OH in the *a*-IGZO especially near the *a*-IGZO/passivation interface compared to the unpassivated samples and siloxane with high OH-bond samples show the highest intensity. These results confirmed that OH from siloxane diffuses into the *a*-IGZO bulk layer and affects the characteristic of *a*-IGZO TFTs.

Figure 2.11 shows both passivated samples had much higher H in the *a*-IGZO layer from the *a*-IGZO/passivation interface compared to the unpassivated samples. The hydrogen diffused into the *a*-IGZO layer from the passivation layer during the post-bake process. Both passivated samples show almost similar 1.2 H intensity, this result is related to the ΔV_{th} reduction projected on the transfer curve.

The hydrogen behavior can be explained by both XPS and SIMS results. Hydrogen as an electron donor can either suppress the V_O side or form OH by bonding with O which can act as an electron acceptor in the *a*-IGZO bulk. This can be observed in the reduction of the oxygen deficiency region peak (~ 531 eV) and an increase in the hydroxide peak (~ 532 eV).

The hump effect in the subthreshold region also can be explained by the roles of hydrogen [26-27]. Hydrogen dissociates from weak OH-bond and drifts towards the drain-channel interface. The larger hump depends on the amount of OH-bond on the surface of the *a*-IGZO layer. The higher amount of hydrogen ions from hydroxide

bonding position can form an accumulation of positive charge [25], forming a set of smaller transistors which turns on faster than the main transistor. Therefore, parasitic transistors are considered to be one of the causes of the hump [28]. These results confirmed by the comparison between 16 O + H and 1.2 H intensity of both passivated samples, high OH-bond passivated sample shows the higher intensity of 16 O + 1 H but not have any change in the result of 1.2 H intensity.

This can be explained by the illustration in Figure 2.12 during the post-annealing with 300°C, H from both passivation materials diffuse to *a*-IGZO layer and suppress the V_O. The extra H is re-bonded with O to form extra OH in the *a*-IGZO layer, especially in the surface area. The higher amount of OH according to the result of a siloxane with the high OH-bond condition, which is possible to stack as a residual hydroxyl-group at the interface of the semiconductor and source/drain electrode makes shallow traps that cause of a hump phenomenon in the sub-threshold region.

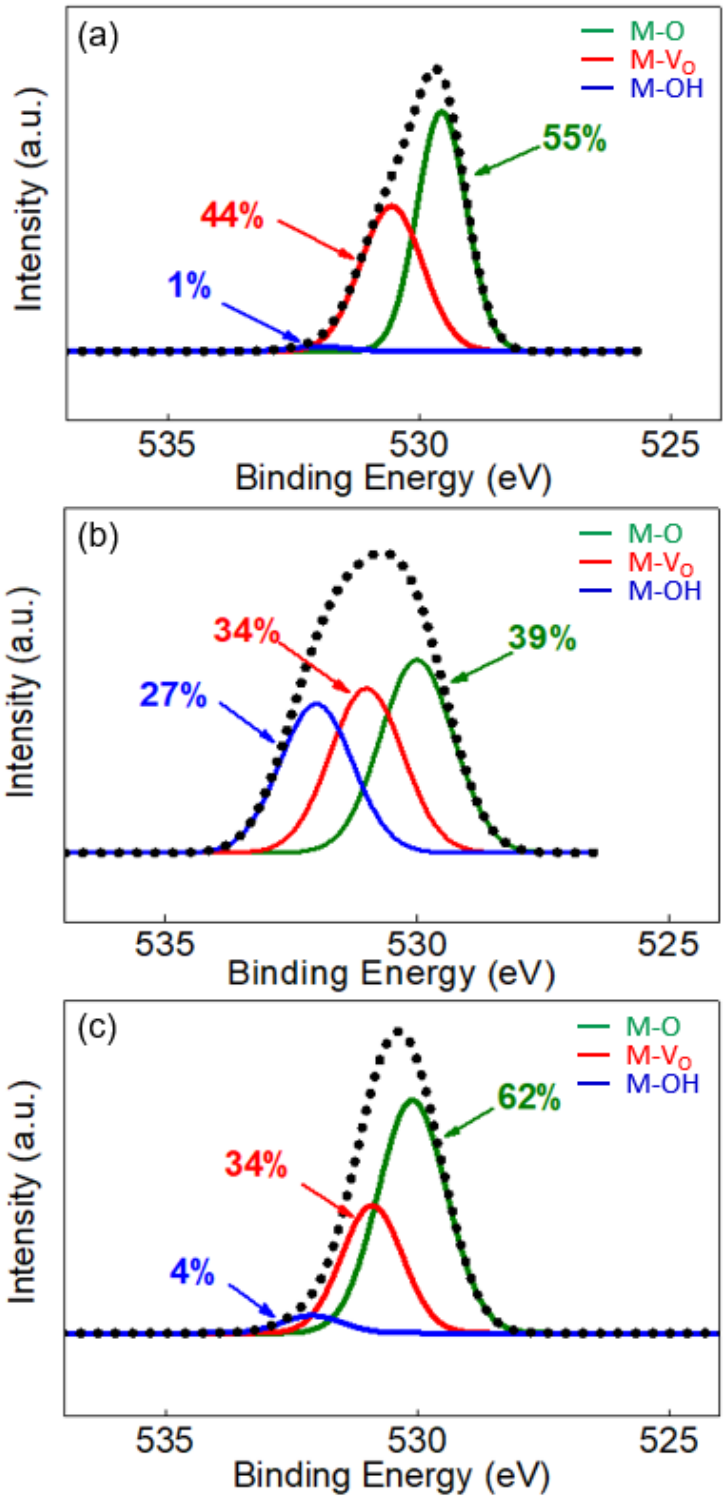

Figure 2.9 O1s XPS spectra in the *a*-InGaZnO layer (a) unpassivated, (b) siloxane with high OH-bond, (c) siloxane with less OH-bond.

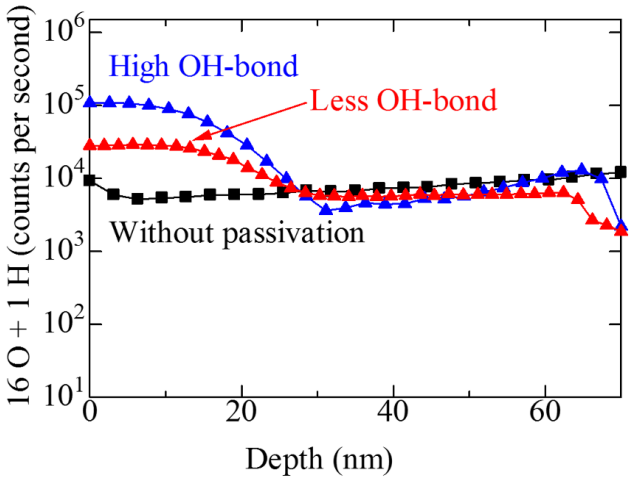

Figure 2.10 Hydroxide depth profile in the 70-nm-thick a-InGaZnO layer of unpassivated and passivated TFTs. The 0 nm depth is the side nearest the passivation layer or surface of *a*-InGaZnO.

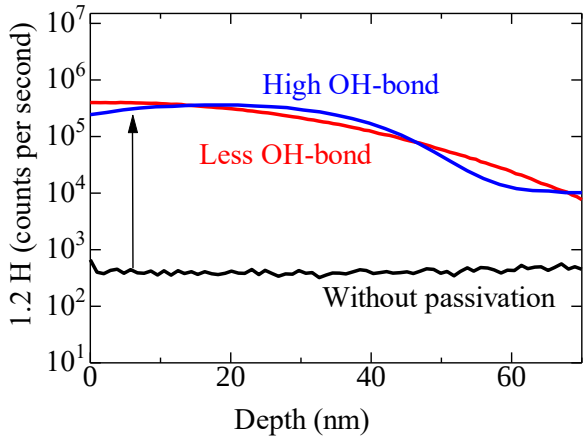

Figure 2.11 Hydrogen depth profile in the 70-nm-thick a-InGaZnO layer of unpassivated and passivated TFTs. The 0 nm depth is the side nearest the passivation layer or surface of *a*-InGaZnO.

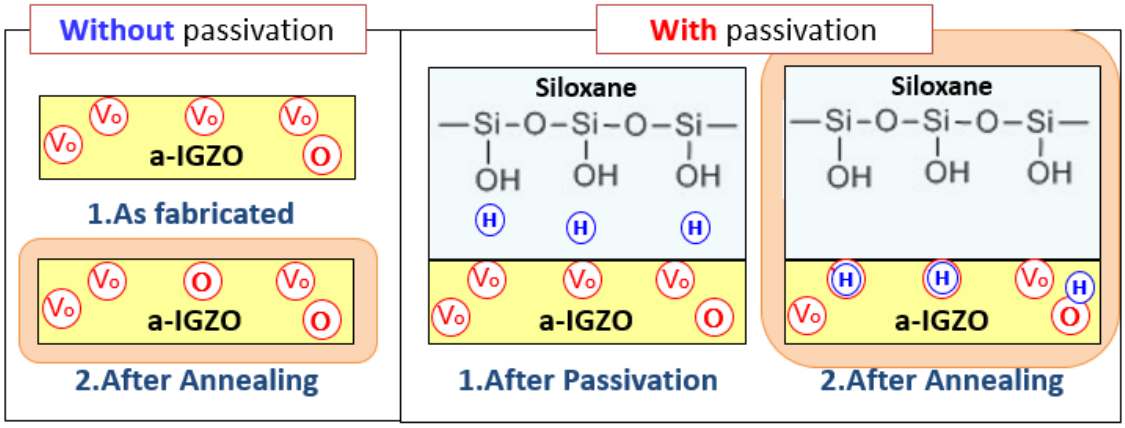

Figure 2.12 Mechanism of hydrogen from siloxane layer showing the diffusion into the *a*-IGZO layer after post annealing and showing how H can occupy the V_O to form H_O and how H can form bonds with O to form OH.

2.6 Summary

The reduction of the hump and improvement of the reliability of siloxane-passivated *a*-IGZO TFT are discussed. The comparison of inorganic and organic passivation materials are introduced with their merits and demerits. In the previous study [22], I showed siloxane passivation materials with unique photosensitivity, which are photo-sensitive and non-photo sensitive, enhances the electrical properties of oxide TFTs but hump effect increased by hydroxide content in siloxane material.

In section 2.3, I examined the influence of siloxane-based passivation on the reliability of *a*-IGZO TFTs and also developed a novel material, which is suitable for passivation of *a*-IGZO TFTs. Non-photosensitive siloxane with different chemical bonding such as methyl-group-based siloxane (without OH-bond) as a reference, less OH-bond (10% OH-bond content) and high OH-bond (more than 85% OH-bond content) was employed.

I proposed that the amount of OH-bond in siloxane structure affects the reliability of *a*-IGZO TFTs. TFT reliability characterized by a PBS and NBS test. *a*-IGZO

TFT was measured by I_{ds} - V_{gs} characteristics, transfer curves of TFT without passivation, passivation by siloxane without OH-bond, with less OH-bond, and with high OH-bond was evaluated.

From the results in section 2.4, unpassivated *a*-IGZO TFTs characteristics are unstable due to ambient effects which degrade the reliability of the device. Both siloxane passivated *a*-IGZO TFTs show a clear improvement in device reliability (less ΔV_{th}) tested by PBS. Meanwhile, *a*-IGZO TFTs are hardly affected by NBS because *a*-IGZO TFTs are n-type. The μ was more than 9 $cm^2 \cdot V^{-1} \cdot s^{-1}$, *SS* was less than 200 mV/decade, and I_{on}/I_{off} was larger than 10^6 for all conditions. However, hump effect showed on the TFT passivated by siloxane with high OH-bond. Conversely, TFT passivation by siloxane with less OH-bond significantly improve the reliability without any hump.

Section 2.5 shows that the key to controlling the reliability of oxide TFTs is by controlling –OH content on the surface of *a*-IGZO for future electronics applications. Improvement of the reliability during PBS is because siloxane acts as a good barrier of *a*-IGZO TFTs to protect the *a*-IGZO surface from the adsorption and desorption of water and oxygen molecules. Analysis of O1s XPS profiles shows that after passivation, both passivated *a*-IGZO TFT has lower V_O compared to unpassivated *a*-IGZO TFT. The O1s XPS profiles also confirmed that OH increase on the surface of *a*-IGZO layer especially on the result of a siloxane with high OH-bond.

SIMS analysis confirmed that increasing the H and OH concentration is at the interface of siloxane and *a*-IGZO layer. These results proved that hump occurs when the *a*-IGZO have residual hydroxyl-group on the surface. The increase of the OH bond and reduction of the V_O are reflected in the ΔV_{th} reduction for both passivated TFTs. OH-bonds act as 2 major roles which are as an electron donor or form hump effect. Thus,

higher amounts of OH can form larger hump reflected in the subthreshold region. I have shown that *a*-IGZO TFT with siloxane with less OH-bond are excellent passivation material, which showed good TFT switching behavior without any hump occurring in the transfer curve.

In conclusion, the effect of OH-bond for clarifying the mechanism of the hump phenomenon and reliability improvement in *a*-IGZO TFTs by using siloxane passivation was studied. The *a*-IGZO TFTs with siloxane passivation as bottom gate structure were fabricated and characterized in detail. Moreover, reliability of *a*-IGZO TFTs was changed after the passivation. Passivated TFT showed a good sign to increase reliability by preventing the ambient effect.

OH-bond in the passivation layer is a key factor to reduce the hump phenomenon and improve the reliability of *a*-IGZO TFTs. Siloxane with less OH-bond has excellent reliability with ΔV_{th} after PBS without hump phenomenon. Meanwhile, a siloxane with high OH-bond showed higher hump phenomenon for both PBS and NBS results. The effect of hump phenomenon occurs by OH-bond inside siloxane was confirmed by supporting data of siloxane without OH-bond. Although, the TFT reliability wasn't improved due to the shrinkage of the passivation material they have no hump shown in this condition. With the result, we conclude that siloxane with less OH-bond is a promising passivation material for next-generation display

References

[1] D. H. Cho, S. H. Yang, J.-H. Shin, C. W. Byun, M. K. Ryu, J. I. Lee, C. S. Hwang, and H. Y. Chu, J. Korean Phys. Soc. **54**, 531 (2009).

[2] J. Li, F. Zhou, H.-P. Lin, W.-Q. Zhu, J.-H. Zhang, X.-Y. Jiang, Z.-L. Zhang, Vacuum, **86,** 1840 (2012).

[3] K. B. Chung, B. D. Ahn, J. Park, and J.-S. Park, J. Korean Phys. Soc. **59**, 3376 (2011).

[4] W. Jevasuwan, T. Maeda, N. Miyata, M. Oda, T. Irisawa, T. Tezuka, and T. Yasuda, Appl. Phys. Express **7**, 011201 (2013).

[5] J. K. Jeong, H. W. Yang, J. H. Jeong, Y.-G. Mo, and H. D. Kim, Appl. Phys. Lett., **93**, 123508 (2008).

[6] A. Sato, K. Abe, R. Hayashi, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano and H. Hosono, Appl. Phys. Lett. **94,** 133502 (2009).

[7] D. H. Kang, I. Kang, S. H. Ryu, Y. S. Ahn, J. Jang, J. of Display Technol., **9**, (2013) 699.

[8] J. Kolodzey, E. A. Chowdhury, G. Qui, J. Olowolafe, C. P. Swann, K. M. Unruh, J. Suehle, R. G. Wilson, and J. M. Zavada, Appl. Phys. Lett. **71**, 3802 (1997).

[9] C. H. Ahn, K. Senthil, H. K. Cho, S. Y. Lee, Nature Sci. Rep., **3**, (2013) 2737.

[10] C. X. Li and P. T. Lai, Appl. Phys. Lett. **95**, 022910 (2009).

[11] H.-S. Seo, J.-U. Bae, D.-H. Kim, Y. Park, C.-D. Kim, I. B. Kang, I.-J. Chung, J.-H. Choi, and J.-M. Myoung, Electrochem. Solid State Lett. **12,** H348 (2009)

[12] S.-H. Choi , J.-H. Jang, Kim, J.-Joo, M.-K. Han, IEEE Elect. Dev. Lett. **33**, 381 (2012).

[13] J. K. Jeong, H. W. Yang, J. H. Jeong, Y.-G. Mo, and H. D. Kim, Appl. Phys. Lett., **93**, 123508 (2008).

[14] S. J. Kim, G. H. Kim, D. L. Kim, D. N. Kim, and H. J. Kim, Phys. Stat. Solidi A. **207**, No. 7, 1668-1671 (2010).

[15] C. D. Sheraw, D. J. Gundlach, and T. N. Jockson, Mat. Res. Soc. Symp. Proc., vol. **558**, article 403 (2000).

[16] T. Kawase, H. Sirringhaus, R. H. Friend, and T. Shimoda, Adv. Mater., vol. **13**, no. 21, pp. 1601–1605 (2001).

[17] H. Klauk, M. Halik, U. Zschieschang, G. Schmid, W. Radlik, and W. Weber, J. Appl. Phys., vol. **92**, no. 9, p. 5259 (2002).

[18] J. A. Rogers, Z. Bao, A. Makhija, and P. Braun, Adv. Mater., vol. **11**, no. 9, pp. 741–745 (1999).

[19] X. Xu, L. Feng, S. He, Y. Jin, and X. Guo, IEEE Electron Device Lett., **33**, 1420−1422 (2012).

[20] K. H. Kim, Y. H. Kim, H. J. Kim, J. I. Han, and S. K. Park, IEEE Electron Device Lett., **32**, 524−526 (2011).

[21] J. P. Bermundo, Y. Ishikawa, H. Yamazaki, T. Nonaka, and Y. Uraoka, ECS J. Solid State Sci. Technol. **3**, Q16, (2014).

[22] C. Kulchaisit, Master thesis, Nara Institute of Science and Technology (2015).

[23] T. Kamiya, K. Nomura, and H. Hosono, Sci. Technol. Adv. Mater. **11**, 044305, (2010).

[24] A. Suresh and J. F. Muth, Appl. Phys. Lett., **92**, 033502 (2008).

[25] M. Mativenga, M. Seok, and J. Jang, Appl. Phys. Lett. **99**, 122107 (2011).

[26] B. D. Ahn, J. S. Park, and K. B. Chung, Appl. Phys. Lett. **105**, 163505 (2014).

[27] Y. Hanyu, K. Domen, K. Nomura, H. Hiramatsu, H. Kumomi, H. Hosono, and T. Kamiya, Appl. Phys. Express **103**, 202114 (2013).

[28] S. H. Choi and M. K. Han, Appl. Phys. Lett. 100, 043503 (2012).

Chapter 3

Top gate TFTs by using solution processed siloxane as a gate insulator

3.1 Introduction

Aside from the channel layer, the gate insulator (GI) or gate dielectric, which is one of the critical factors controlling the performance of the TFT device has also been considered. Thermally grown SiO_2 was used as the traditional GI for decades because of its simplicity and suitability with Si substrates [1-3]. However, the use of SiO_2 as a GI has reached the technical limit as the trend to fabricate future flexible TFTs became more active.

Recently, many researchers are trying to find alternative GI materials or enhance the quality of GI to break through those technical limits [4-9]. Therefore, suitable fabrication process matching with those material properties are needed. Similar to the passivation process, the chemical composition, mobile ions, and properties of the GI materials will affect the electrical characteristics of the oxide TFTs. There are two main fabrication methods, which are vacuum process and solution process. In section 3.2, I compared a variety of GI materials, explained their merits and demerits together with introducing a method to fabricate these materials.

Siloxane with less OH-bond material from chapter 2 is selected in this study as a GI due to its reliability enhancement, having no hump effect, and the possibility to be fabricated by simple solution process. In addition, the OH-bond from siloxane is

promising to improve the performance of *a*-IGZO TFTs by choosing a suitable chemical structure for the siloxane.

Capacitance measurement is a popular technique to analyze the GI properties [4]. Although many traditional GI materials already have well-reported properties analyzed by capacitance measurement method and set as their standard value, the GI properties of siloxane materials are still unknown due to the adjustability of the chemical structure in each type. This study will show the capacitance of siloxane under low frequency (1 kHz) and high frequency (1 MHz).

The interface trap density (D_{it}) is one of the main determinants of transistor performance and there is a noticeable interrelationship between the electrical performances and D_{it} [4]. Therefore, the influence of the interface trap density (D_{it}) existing at the channel/dielectric layer interface on the electrical characteristics and stabilities of *a*-IGZO TFT is clearly established. Section 3.3 will show how to estimate D_{it} from capacitance value. This helps in diagnosing fabrication processes and optimizing these parameters effectively in order to obtain the enhanced performance of TFT devices.

The electrical characteristics and stability of bottom gate TFT as a reference and top gate TFT with siloxane GI are measured. The mechanism to improve TFT performance is studied. The key factor is that the hydrogen and hydroxide in the siloxane's chemical structure suppress the defect inside the *a*-IGZO and generate additional free electron which enables top gate TFTs with siloxane GI to have improved electrical characteristics and stable hysteresis compared with the bottom gate TFT.

3.2 Siloxane as a gate insulator

3.2.1 Comparison of gate insulator materials

Focusing on film quality, the GI fabricated by vacuum process is the traditional fabrication method, which is fabricated under high vacuum. Commonly, a vacuum process is separated into two main methods, which are PVD such as direct current (DC) sputter and radio frequency (RF) sputter and CVD such as PECVD. The keys to improving TFT characteristics are controlling the contamination, thickness, surface quality of the GI due to the electrons localized at the subgap traps and holes are transported into traps in the channel/ GI interface or the GI itself [5]. This supports the merit of depositing GI by a vacuum process, which has a high film quality, controllable thickness, and minimal contamination. In general, films fabricated with vacuum process tend to exhibit better characteristics according to the key factors introduced above.

However, vacuum process also has many problems to be resolved such as plasma damage, complicated fabrication, and high cost, which are explained in chapter 2. High-k oxide materials such as Ta_2O_5 [6], $SrTiO_3$ [7], Al_2O_3 [8], HfO_2 [9], and ZrO_2 [9] have been employed as the GI in top gate structure by a vacuum process because these materials can possibly drive TFTs at low gate voltages and have enhanced mobility.

However, plasma damage from GI fabrication by vacuum process makes V_{th} shift negatively, have large hysteresis (V_H), poor threshold voltage control, high leakage current, and worse stability [6-9]. An additional barrier layer such as etching stop layer between GI to stabilize the TFT characteristics is another way to solve these problems [10] but it uses more complicated processes and has a high cost.

Fujii *et al.*'s research about using Ionic liquids or ion gels as a GI to induce an electric double layer (EDL) is also motivating because these ionic liquids GI have a very high capacitance (10^{-6}) which enables TFT operation at an extremely low voltage less than 3V and low *SS* value under 100 mV/dec. However, the liquid phase is difficult to control because of chemical degradation, the necessity to control its shape by using an extra cover pattern, and thickness in the TFT, which makes it not suitable for industrial application [11].

In order to make a future display that addresses more requirements such as scalability, total cost-efficiency, and high electrical performance, an alternative method to deposit films is the solution process. As opposed to the vacuum process, solution process have benefits such as the possibility to operate with a shorter time, the possibility of fabricating a wide-area device, and very simple fabrication process. Several GI fabricated by solution process are being investigated to reduce production cost and improve TFT performance [12]. Nevertheless, performance reduction due to high leakage current, high standby power consumption, and stability are still problems for TFTs with solution-processed GI [13-17].

The most common use of the solution process techniques is organic GIs, such as polyimide [14], polyvinylphenol [15,16], and polymethylmethacrylate [17]. Although this organic polymer GIs fabricated by lower process temperatures, there is a tradeoff such that there is a decrease in the TFT electrical properties and stability.

Organic-inorganic hybrid material such as siloxane which is usually used as an adhesion promoter and binder in the anti-corrosive coating was recently introduced for applications in next-generation flexible and transparent TFTs due to its high transparency, flexibility, ease of fabrication, and low cost [18-21].

Siloxane was introduced as a passivation layer as a robust TFT barrier and protective layer [18] and to improve the performance of *a*-IGZO TFT[22]. As in chapter 2, I previously proved that by controlling the chemical bonding of the siloxane this material can improve the TFT characteristics and reliability as a passivation layer.

3.2.2 Fabrication process of *a*-IGZO TFT with siloxane gate insulator

I fabricated bottom and top gate structures within a single TFT to enable a comparison between bottom gate TFT using SiO_2 as a GI and top gate structure using siloxane as a GI as shown in Figure 3.1 (a). At first, the bottom gate electrode and gate insulator material are made of highly conductive n-type Si substrate with a thermally oxidized SiO_2 layer of 100 nm. These substrates were cleaned with concentrated sulfuric acid at 80°C for 10 minutes then mixed with hydrogen peroxide (H_2O_2) for 10 minutes.

The 70-nm-thick *a*-IGZO layer was deposited on this substrate as the channel material by RF magnetron sputtering method under vacuumed at 10^{-6} – 10^{-7} Torr at room temperature. Argon and oxygen were introduced at 4.5×10^{-3} Torr before sputtering. RF with 13.56 MHz at a power of 100 W was applied at RT and then argon plasma was generated. The generated plasma sputters the IGZO target whose stoichiometric ratio is 2:2:1:7. The channel material was patterned using UV photolithography and wet etching by 0.02 mol/L HCl solution for 7-14 minutes.

Depositions of metal electrodes were performed to fabricate 80-nm-thick molybdenum and 20-nm-thick platinum, layers. I used a lift-off technique to pattern the source and drain electrodes. A rotation speed of 3000 rpm was used for spin-coating 250-nm-thick siloxane layer on the TFTs. Siloxane was cured in air at 230°C for 20 minutes

and 300°C for 20 minutes. Contact holes for the siloxane layer were fabricated by reactive ion etching (RIE) process with a gas ratio of CF_4/ Ar =30/ 45 sccm for 60 seconds. The passivated TFTs are deposited once again to make a gate pattern by UV photolithography. For the final step, the passivated *a*-IGZO channel layer patterned with patterned photo-resist was inserted into the sputtering chamber and vacuumed at 10^{-6} – 10^{-7} Torr. Argon was introduced at 4.5×10^{-3} Torr before sputtering. RF with 13.56 MHz at a power of 100 W was applied at RT and then argon plasma was generated. The depositions of metal were fabricated with a deposition rate of 10 nm/min for 150-nm-thick molybdenum. To form the gate pattern, a metal layer which deposited on a designed area of photoresist was etched away by a lift-off process to finish the technique. A post-oxygen annealing treatment served only the siloxane deposited TFTs at 300°C for 120 minutes in the ratio of N_2/O_2 (0/5) ambient to finish the fabrication of *a*-IGZO TFTs with siloxane layer (Figure 3.1 (a)).

Analysis of I-V characteristics by measuring transfer characteristics was performed with Agilent HP4156C semiconductor parameter analyzer. The switching of fabricated devices was traced by applying a voltage to the gate from -20 V to 20 V whose step was 100 mV, and applying a voltage to the drain from 0.1 V to 9.9 V whose step was 4.9 V. The reverse step also measured right after the forward step are finished.

To fabricate siloxane film as a metal-insulator-metal (MIM) structure device, Si was prepared as a substrate. After conducting SPM cleaning, Mo and Pt were deposited using radiofrequency (RF) magnetron sputtering. Mo with a thickness of 80 nm was deposited as the gate electrode, and Pt with a thickness of 20 nm was deposited as a cover layer on top of Mo. After the deposition, siloxane solution was spin-coated and then prebaked using the same process as siloxane passivated on TFT fabrication condition (see

the previous chapter). Then, siloxane was cured in air at 230°C for 20 minutes and 300°C for 20 minutes. Molybdenum (80 nm) was used as an electrode and platinum (20 nm) was used as a protective layer to prevent oxidation of molybdenum. Patterning of top electrode regions was done by covering the metal mask on a substrate during the metal sputtering process. Three different patterns with diameters of 100 μm, 300 μm, and 500 μm were deposited.

The capacitance (C) – voltage (V) was measured to calculate the dielectric constant of siloxane. Characteristics of each condition were measured using a prober, and the analysis of fabricated device was done using a semiconductor parameter analyzer (B1500A). The cross-section of the fabricated metal-insulator-metal (MIM) is shown in Figure 3.1(b).

To measure the chemical bonding state on the surface of *a*-IGZO with siloxane layer, siloxane/ *a*-IGZO/ SiO_2/ Si film was fabricated. The siloxane/ *a*-IGZO film layer was analyzed by SIMS and XPS to understand the degradation mechanism. Surface quality and roughness were analyzed by atomic force microscopy (AFM). Additionally, Mo film is coated on the sample for cross structure analysis by Scanning Transmission Electron Microscope (STEM).

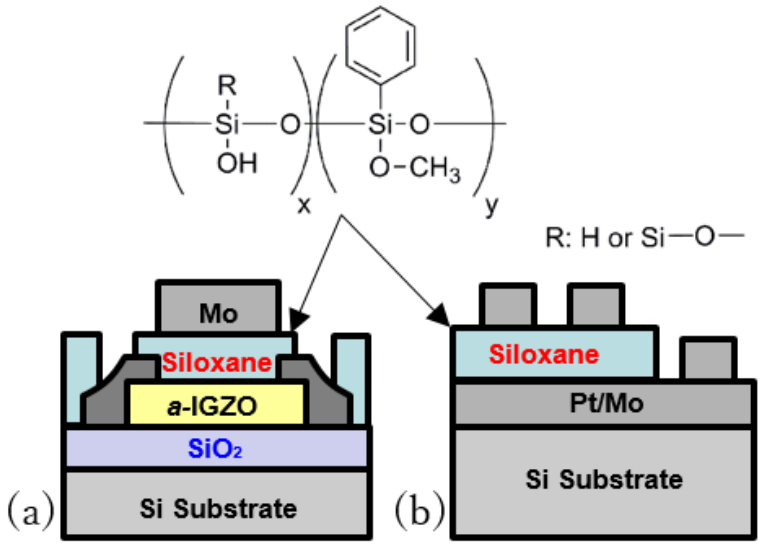

Fig. 3.1 (a) Schematic of *a*-IGZO TFT device using siloxane as a passivation or GI dependent on whether the bottom or top gate is activated, and (b) MIM structure of the Mo/siloxane/Mo film with siloxane chemical structure.

3.3 Improvement of electrical characteristics of top gate oxide TFT

3.3.1 Comparison between traditional bottom gate TFT using SiO_2 as a gate insulator and top gate TFT using siloxane as a gate insulator

I fabricated bottom and top gate *a*-IGZO TFTs with siloxane layer as a passivation or GI depending on which gate is used. The bottom gate *a*-IGZO TFTs using siloxane as a passivation obtained excellent electrical characteristics after post-annealing treatment at 300°C for 120 min in an oxygen atmosphere, which has a channel width and a length of 90 and 10 μm, respectively. The mobility is obtained from the equation:

$$\mu = g_m \frac{L}{WC_i V_{ds}} \quad (3.1)$$

where g_m is the measured transconductance, C_i is the gate insulator capacitance per unit area, and V_{ds} is the drain voltage. The μ was 9.52 $cm^2 \cdot V^{-1} \cdot s^{-1}$, *SS* was 200 mV/decade, and I_{on}/I_{off} was ~10^7. Right after patterning the top gate Mo electrode, the transfer characteristics (Figure 3.1 (a)) of the top gate TFTs are measured.

The TFTs with siloxane GI (Figure 3.2) showed a very high mobility (μ) = 38.09 $cm^2 \cdot V^{-1} \cdot s^{-1}$. Other electrical characteristics also measured as threshold voltage (V_{th}) = 3.21 V, sub-threshold swing (*SS*) = 0.16 V/dec, leakage current (I_{gs}) = 5.0×10^{-10} A, and the on-off current ratio (I_{on}/I_{off}) was about 10^6. From the results, I found that siloxane GI with top gate TFT improved the stability after observing the hysteresis loop. To confirm this hypothesis, the stability of bottom gate TFT using SiO_2 within the same TFT was measured as a reference. The comparison results of both structures are shown in Figure 3.3 at V_D = 5.0 V. The SiO_2 GI TFT shows a hysteresis shift (V_H) of 2.36 V while the siloxane GI TFT shows negligible V_H that is 0.01 V. The summary of the electrical characteristics for comparison of both TFT is shown in Table 3.1.

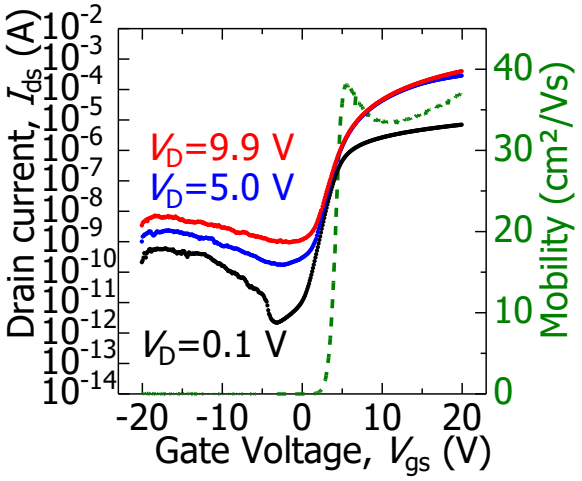

Figure 3.2 The transfer characteristics of top gate *a*-IGZO TFTs using siloxane as a GI for V_D from 0.1 V to 9.9 V and the mobility curve.

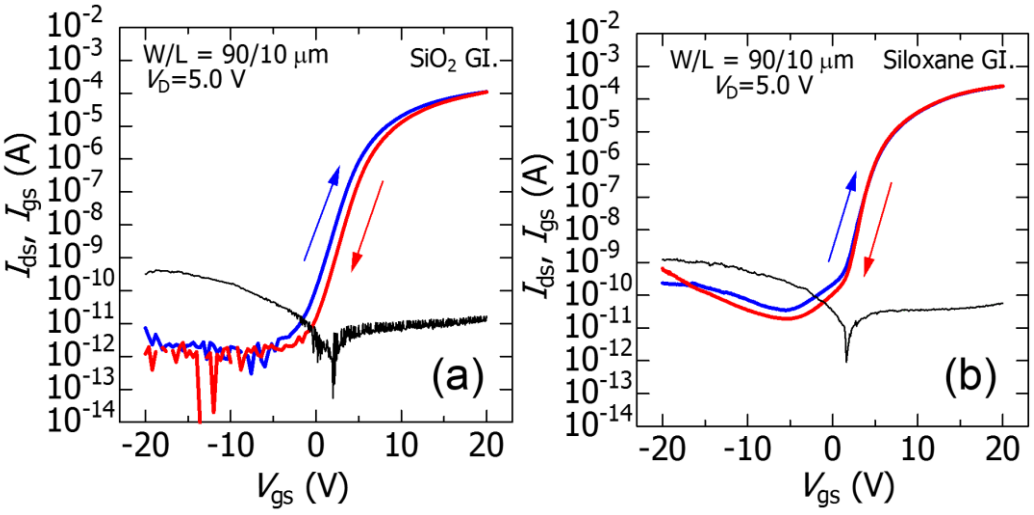

Figure 3.3 Comparison of hysteresis curves and leakage current between *a*-IGZO TFTs with (a) a bottom gate structure using SiO_2 as GI, and (b) a top gate structure using siloxane as GI.

Table 3.1 Comparison of the electrical characteristics between bottom gate and top gate TFT using SiO_2 and siloxane as a GI, respectively.

	SiO_2	*Siloxane*
μ (cm^2/Vs)	9.52	38.09
V_{th} (V)	3.91	3.21
***SS* (V/dec)**	0.20	0.16
On/off ratio	~10^7	~10^6
V_H (V)	2.36	0.01
I_{gs} (A)	0.1×10^{-10}	5.0×10^{-10}

3.3.2 Interface stage density estimation using the C-V technique

The C-V technique has been used in the assessment of oxide TFTs mainly to estimate the interface state density (D_{it}) by evaluating the frequency dependence. C-V technique is useful for *a*-IGZO because it is known that the electrical characteristics are changed by thermal annealing and that the carrier mobility depends on the carrier density. This was first demonstrated by Kimura et al. [23], who used this method to investigate and assess polycrystalline silicon TFTs [4].

To evaluate the quality of the siloxane GI films, the capacitance of siloxane measured by capacitance-voltage (C-V) measurements on the MIM structure as shown in Figure 3.4 shows the plots of capacitance per unit area (C_i) of the MIM structures against frequency (f) and voltage (V) values of siloxane at low frequency (1 kHz) and high frequency (1 MHz). The C-V curves show a variation in the capacitance values upon sweeping from -1V to +1V. The decreasing capacitance as frequency increases is due to the slow polarization effect or ionic impurities [24]. The dielectric constant (κ) is calculated using the equation given below

$$Ci = \varepsilon_0 \kappa / d \tag{3.2}$$

Where ε_0 is permittivity of vacuum and d is the dielectric thickness, respectively. Using this formula, κ is estimated to be 3.78 using capacitance values at 1 kHz, which is commensurate with both solution processed SiO_2 and conventional SiO_2 which has a range of 3.0-3.9 at the same frequency [25,26]. In order to check the improvement of the

electrical characteristic of all conditions as explained by termination of defects at the *a*-IGZO/GI interface, the interface state density (D_{it}) is calculated as shown below

$$D_{it} = C_i \frac{SSlog(e)}{kT} - \frac{1}{q} \tag{3.3}$$

Where, k is Boltzmann's constant, T is the absolute temperature, and q is the magnitude of electronic charge. The D_{it} is an important value to determine the suitable combination of the GI and the channel layer. A higher D_{it} means that there are higher amount of traps or defects at the interface leading to the poor TFT performance. The values of D_{it} from SiO_2 GI TFT and TFT with siloxane GI are 7.17×10^{11} and 2.23×10^{11} $cm^{-2}eV^{-1}$, respectively. These results support that a lower D_{it} can improve μ, V_{th}, and reduce the hysteresis loop [27]. The summary of the film properties of SiO_2 and siloxane are shown in Table 3.2.

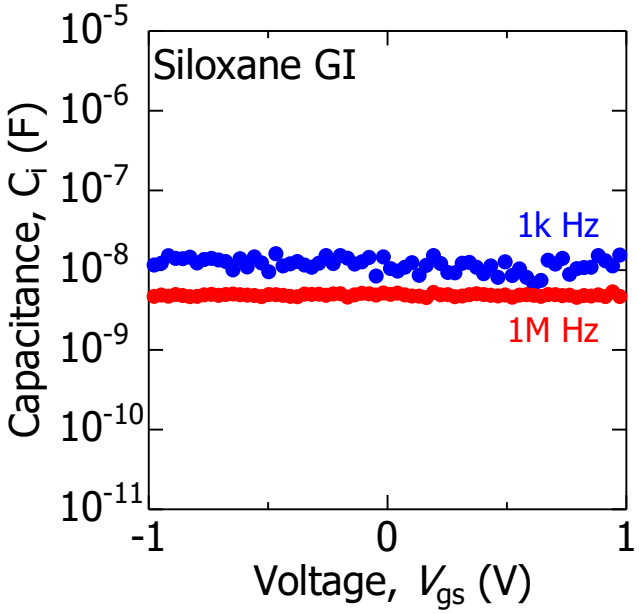

Figure 3.4 Capacitance-voltage measurement of O_2 annealed siloxane at 1 kHz and 1 MHz.

Table 3.2 Comparison of the properties between SiO_2 and siloxane film.

	GI Material	
	SiO_2	*Siloxane*
κ	3.90	3.78
C_i **(F/cm^2)**	3.45×10^{-8}	1.34×10^{-8}
D_{it} **(cm^{-2}eV^{-1})**	7.17×10^{11}	2.23×10^{11}

3.4 Key factor to improve the performance of top gate oxide TFTs

From the results, top gate *a*-IGZO TFT using siloxane as a GI improves the electrical characteristics and stability. Not only because siloxane acts as a good barrier of *a*-IGZO TFTs to protect the *a*-IGZO surface from the adsorption and desorption of water and oxygen molecules, but also the chemical reaction and film quality itself supports the channel layer.

The I_{gs} for solution processed GI generally increase due to the physical defect such as physical holes or pores, which generate hot spots of the applied electric field during electrical measurement [25-26]. The STEM (Hitachi HD-2700) image (Figure 3.5) proves that siloxane has a minimal defect in either the bulk area or the interfaces which supports the result of comparable I_{gs} with sol-gel processed SiO_2 GI technique (<10nA/cm^2) [26]. Figure 3.5 also shows the thickness of siloxane layer, which can be controlled by the rotation speed. Although, increasing the GI thickness results in a lower I_{gs}; a thicker GI, however, tends to decrease the capacitance as explained in Equation 3.2 [12]. Figure 3.6 also showed an ultra-smooth surface measured by a Shimadzu SPM-9600

atomic force microscopy (AFM) that shows a root-mean-square (RMS) surface roughness (R_{rms}) of 0.62 nm – comparable with vacuum processed SiO_2 film [28]. It is well known that mobility improves by improving the interface between the channel layer and GI because the carrier transport scattering caused by interface roughness is suppressed [28-30].

In terms of the chemical reaction, the O1s intensity from XPS with monochromatic Al Kα (Shimadzu KRATOS AXIS-165) profiles (Figure 3.7) shows the comparison of the area ratio percentages of the deconvoluted sub-peaks. The chart shows 3 peaks at 530, 531, 532 eV which is attributed to metal oxide (M-O) bonding, oxygen deficiency region (M-V_o), and hydroxide (M-OH), respectively [18]. The deconvolution suggests that hydrogen from siloxane diffused into the surface area of *a*-IGZO and reacted with lattice oxide created a hydroxide dangling bond as represented in binding energy around 532 eV together with the generation of more free electron from the chemical reaction. This diffusion occurs during the annealing process due to the incorporation of hydrogen that diffused from the siloxane layer into the *a*-IGZO layer, which also able to suppresses the oxygen vacancies as shown in the decreasing of the binding energy around 531 eV. Furthermore, the increase in M-O bonding implies that there are more carrier pathways in the *a*-IGZO, which improved the mobility. Besides the effect of the siloxane layer, oxygen from post-oxygen annealing also suppress the generation of oxygen vacancies and enhances the device performance.

To confirm the mechanism of the improvement of the electrical characteristic, Figure 3.8 shows the comparison of the intensity of 1.2H (hydrogen) and 16O + 1H (hydroxide) in *a*-IGZO bulk (70 nm-thick) by SIMS (ULVAC-PHI ADEPT-1010) with Cs+ ion source (1 keV and 50 nA). Both intensities of 1.2H and 16O + 1H in the IGZO

region near siloxane shows higher intensity than the region near SiO_2. These results confirmed that both H and OH from siloxane diffuses into the IGZO bulk layer and affects the characteristic of *a*-IGZO TFTs.

Supported by XPS results, this shows that hydrogen from siloxane layer diffused into the *a*-IGZO layer and siloxane protected the surface of *a*-IGZO from ambient effects, which improved electrical characteristics. Furthermore, the O-H bonds from siloxane layer reacted with *a*-IGZO surface and generated free electrons. Free electrons from the hydrogen and hydroxide reaction in the siloxane layer suppress the formation of electron traps on the *a*-IGZO surface as shown in the reduction of D_{it} value improving TFT mobility, stability, and lower voltage operation [31-33]. Moreover, an extra hydrogen from siloxane remains on the *a*-IGZO surface which enhances mobility as shown in the result.

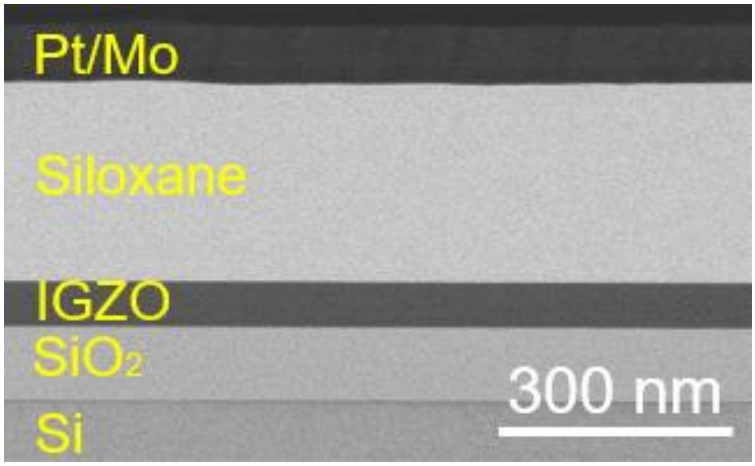

Figure 3.5 STEM cross-sectional image of siloxane/IGZO/SiO_2/Si film.

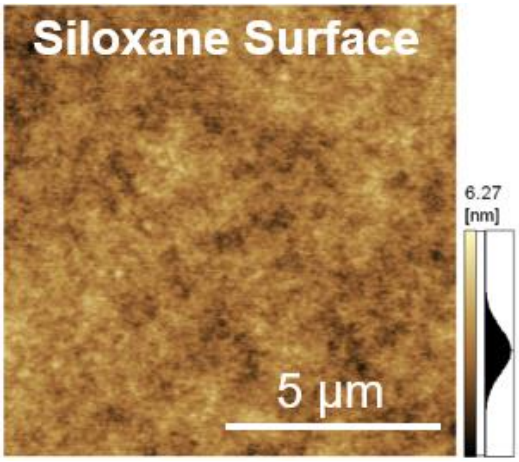

Figure 3.6 Surface roughness of siloxane observed by AFM.

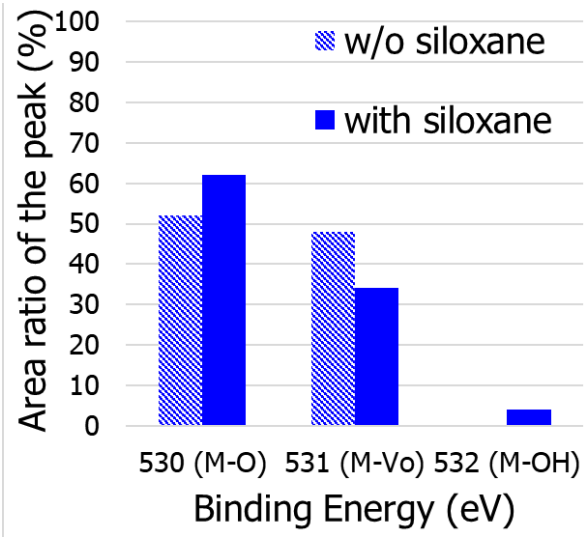

Figure 3.7 The comparison chart of O1s core level XPS spectra of the *a*-IGZO surface.

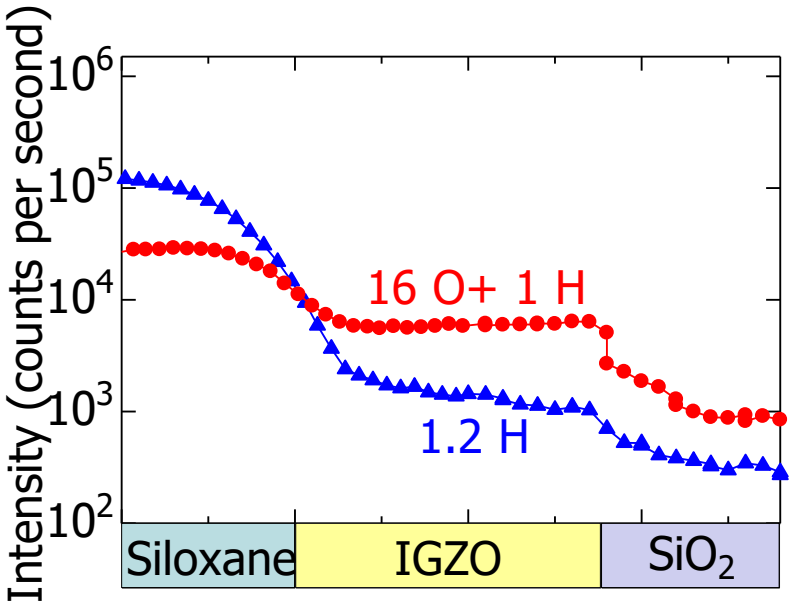

Figure 3.8 Hydrogen (1.2 H) and hydroxide (16 O+ 1 H) SIMS depth profile in the siloxane/*a*-IGZO/SiO_2 layer after oxygen annealing.

3.5 Summary

I succeeded in fabricating high-performance TFT using siloxane for both passivation and GI in the same TFT dependent on whether the bottom or top gate structure is activated. In this study, I demonstrated that siloxane is not only an excellent barrier film but also an alternative candidate for solution processed dielectric material for lower process cost and improved TFT performance. I demonstrated that the excellent film-forming properties of oxide semiconductor enabled a higher dielectric constant compared with SiO_2.

The effect of the hydrogen and hydroxide bonding from siloxane was investigated and I found that these diffuse into the *a*-IGZO layer and improve the electrical characteristics. By using siloxane as a GI, the best TFT which used a top gate configuration with siloxane GI had a mobility (μ) = 38.09 $cm^2 \cdot V^{-1} \cdot s^{-1}$, threshold voltage

(V_{th}) = 3.21 V, sub-threshold swing (*SS*) = 0.16 V/dec, and hysteresis (V_H) = 0.01 V. In addition, with such a high mobility (38.09 $cm^2 \cdot V^{-1} \cdot s^{-1}$), this GI candidate will fulfill the criteria for future display with good characteristics such as high resolution and high frame rate. This phenomenon can be explained by the increasing intensity of both 1.2H and 16O+ 1H around the surface (close to siloxane side) observed by SIMS analysis. The O1s intensity from XPS also confirmed that the M-V_o peak or the oxygen vacancies on the surface of *a*-IGZO bulk are reduced after siloxane deposition on *a*-IGZO.

The effect of the interface state density (D_{it}) on the electrical properties and stability has been calculated and the results showed that siloxane as GI have extra hydrogen, oxygen, and hydroxide supporting the channel to reduce D_{it} which also increases μ, reduces V_{th}, *SS*, V_H, and comparable I_{gs} from the I_d-V_g curve. These results posit that using siloxane is an excellent candidate together with oxide semiconductors in fabricating high performance transparent and flexible devices by solution-based processes in the near future.

References

[1] S. W. Hsieh, C. Y. Chang, and S. C. Hsu, J. Appl. Phys. **74**, 2638 (1993).

[2] E. Chong, Y. S. Chun, and S. Y. Lee, Appl. Phys. Lett. **97**, 102102 (2010).

[3] K. Nomura, T. Kamiya, and H. Hosono, Appl. Phys. Lett. **99**, 053505 (2011).

[4] M. Kimura, R. Nozawa, S. Inoue, T. Shimoda, B. O.-K. Lui, S. W.-B. Tam, and P. Migliorato, Jpn. J. Appl. Phys. **40**, pp. 5227-5236 (2001).

[5] K.-H. Lee, J. S. Jung, K. S. Son, J. S. Park, T. S. Kim, R. Choi, J. K. Jeong, J.-Y. Kwon, B. Koo, and S. Lee, Appl. Lett. **95**, 232106 (2009).

[6] P. K. Roy and I. C. Kizilyalli, Appl. Phys. Lett. **72**, 2835 (1998).

[7] R. A. McKee, F. J. Walker, and M. F. Chisholm, Phys. Rev. Lett. **81**, 3014 (1998).

[8] J. Kolodzey, E. A. Chowdhury, G. Qui, J. Olowolafe, C. P. Swann, K. M. Unruh, J. Suehle, R. G. Wilson, and J. M. Zavada, Appl. Phys. Lett. **71**, 3802 (1997).

[9] S. Y. Lee, S. Chang, and J. S. Lee, Thin Solid Films **518**, 3030-3032 (2010).

[10] X. Li, E. Xin, L. Chen, J. Shi, and J. Zhang, AIP Adv. **3**, 032137 (2013).

[11] M. N. Fujii, Y. Ishikawa, K. Miwa, H. Okada, Y. Uraoka, and S. Ono, Sci. Rep. **5**, 18168 (2015).

[12] H. Kim, Y. J. Kwack, E. J. Yun, and W. S. Choi, Sci. Rep. **6**, 33576 (2016).

[13] S. J. Kim, G. H. Kim, D. L. Kim, D. N. Kim, and H. J. Kim, Phys. Stat. Solidi A. **207**, No. 7, 1668-1671 (2010).

[14] C. D. Sheraw, D. J. Gundlach, and T. N. Jockson, Mat. Res. Soc. Symp. Proc., vol. **558**, article 403 (2000).

[15] T. Kawase, H. Sirringhaus, R. H. Friend, and T. Shimoda, Adv. Mater., vol. **13**, no. 21, pp. 1601–1605 (2001).

[16] H. Klauk, M. Halik, U. Zschieschang, G. Schmid, W. Radlik, and W. Weber, J. Appl. Phys., vol. **92**, no. 9, p. 5259 (2002).

[17] J. A. Rogers, Z. Bao, A. Makhija, and P. Braun, Adv. Mater., vol. **11**, no. 9, pp. 741–745 (1999).

[18] J. P. Bermundo, Y. Ishikawa, H. Yamazaki, T. Nonaka, M. N. Fujii, and Y. Uraoka, Appl. Phys. Lett. **107**, 033504 (2015).

[19] A. Tewari, S. Gandla, A. R. Pininti, K. Karuppasamy, S. Böhm, A. R. Bhattacharyya, C. R. McNeill, and D. Gupta, Appl. Phys. Lett. **107**, 103302 (2015).

[20] T. S. Chang, T. C. Chang, P. T. Liu, S. W. Tsao, F. S. Yeh, Thin Solid Film **516**, 374-377 (2007).

[21] S. A. Wheelock, J. N. Bremmer, D. S. Schwab, L. Moore, K. Kozel, G. Bujouves, J. Lommel, and D. Rast, SEMICON China (2003).

[22] K. Chaiyanan, Y. Ishikawa, M. N. Fujii, H. Yamazaki, J. P. Bermundo, S. Ishikawa, T. Miyasako, H. Katsui, K. Tanaka, K. Hamada, M. Horita, and Y. Uaoka, J. Disp. Technol. **12**, no. 3 (2016).

[23] M. Kimura, T. Nakanishi, K. Nomura, T. Kamiya, and H. Hosono, Appl. Phys. Lett. **92**, 133512 (2008).

[24] J. Veres, S. Ogier, and G. Lloyd, Chem. Mater. **16**, 4543 (2004).

[25] M. Esro, O. Kolosov, P. J. Jones, W. I. Milne, and G. Adamopoulos, Appl. Mater. Interfaces, **9**, 529-536 (2017).

[26] F. Jaehnike, D. V. Pham, R. Anselmann, C. Bock, and U. Kunze, Appl. Mater. Interfaces, **7**, 14011-14017 (2015).

[27] Y. G. Chang, D. H. Kim, G. Ko, K. Lee, J. H. Kim, and S. Im, IEEE Electron Device Lett. 32, no. 3 (2011).

[28] M. R. Amirzada, A. Tatzel, V. Viereck, and H. Hillmer, Appl. Nanosci. **6**:215-222 (2016).

[29] T, Yamanaka, S. J. Fang, H. C. Lin, J. P. Snyder, and C. R. Helms, IEEE Electron Device Lett. **17**, no. 4, 178-180 (1996).

[30] R. Kuroda, T. Suwa, A. Teramoto, R. Hasebe, S. Sugawa, and T. Ohmi, IEEE Trans. Electron Devices., **56**, 291-298 (2009).

[31] M.F.Lin, X. Gao, N. Mitoma, T. Kizu, W. O. Yang, S. Aikawa, T. Nabatame, and K. Tsukagoshi, AIP Adv. **5**, 017116 (2015).

[32] T. Kamiya, K. Nomura, and H. Hosono, J. Display Technol. **5**, 273 (2009).

[33] M. Benwadih, J. A. Chroboczek, G. Ghibaudo, R. Coppard, and D. Vuillaume, J. Appl. Phys. 115, 214501 (2014).

Chapter 4
UV-induced electrode/channel of all- solution processed self-aligned oxide TFTs

4.1 Introduction

Large area, flexible electronic devices fabricated via a low-temperature solution process has potential to unlock new direction in electronic studies. Usage of solution processed TFTs to build electronic devices for low-cost devices fabricated by spin coating, sol-gel, or 3D printing techniques on a large area, flexible substrates is a key challenge in this emerging field [1-3]. The idea of TFTs with solution-processed semiconductors is quite new as compared to traditional vacuum processed TFTs. However, the inferior quality of solution processed transistor devices needs to be solved especially their low yield, strict fabrication parameters, and high contamination.

Flexible all-solution processed TFTs are expected to be one of the most promising next-generation display technologies, as described in Chapter 1. However, when the application of *a*-IGZO to all-solution processed TFTs is considered, there are many issues to resolve. In this chapter, fabrication processes for all-solution processed TFTs are discussed from the viewpoint of developing novel fabrication methods. Regarding the TFT structure, it is difficult and very challenging to fabricate a whole device with the all-solution process since it is crucial that the bulk of the semiconductor, gate insulator, and electrode to not have any accumulated parasitic charge or induced traps. Also, the interface of the gate insulator/semiconductor is required to be ultra-smooth with fewer defects, holes, or pores which are directly related to issues such as

poor electrical characteristics, high leakage current, and non-uniformity. For the semiconductor layer, material candidates which are possible to fabricate by solution process: inorganic, organics, or nanomaterials now have comparable performance with *a*-Si:H, with mobility around 1 $cm^2V^{-1}s^{-1}$ [4-6]. In this chapter, solution *a*-IZO is selected since this material is promising to generate high mobility and it is possible to transform from a semiconductor into a conductor, which enables the possibility to make an electrode-semiconductor in a single layer to reduce the parasitic charge that occurs in the contact between semiconductor and electrode, which will be discussed in section 4.4.

For gate insulators, high-k, ion-gel, and polarizable ionic materials show comparable electrical characteristics such as good mobility and low operation voltage [7,8]. However, thickness and flatness need to be controlled to avoid fixed charges, interface traps, bulk traps and mobile ions [9]. As in chapter 3, solution inorganic-organic hybrid material based on siloxane will be used in this chapter, because this material shows a good combination with an oxide semiconductor, by suppressing oxygen vacancies and increasing conductive path to enhance high mobility and improved stability. The last part is dedicated in discussing the electrodes: conductive metal oxide, printed metal, and carbon materials have been used by several researchers toreplace vacuum processed materials, but these materials still need high annealing temperature and have high material cost [10-12]. In section 4.4, the principle of transparent metal oxide will be introduced and lead the way to make an oxide material transform to the conductive material by UV treatment.

As mentioned on the issues above, the new design of the novel all-solution processed self-aligned TFT structure will be introduced mainly to improve the solution processed TFT performance together with reducing the complex fabrication process. The

new all-solution processed TFT fabrication process and its electrical characteristics are introduced in section 4.5. The effect of UV-induced self-aligned structure is also explained in section 4.6.

The key factors are separated into two parts based on the *a*-IZO area with and without the UV affected zone. The first part discusses how the solution *a*-IZO semiconductor without UV effect is improved by the hydrogen and hydroxide from the siloxane's chemical structure which suppresses the defect inside the *a*-IZO and generates an additional free electron. The second part is about the *a*-IZO within the UV affected area, which was successfully transformed into conductive electrodes which were confirmed by a change of resistivity before and after UV treatment due to an increase of oxygen vacancies as observed by XPS analysis.

4.2 Solution process and the selection of the channel material

A thin film may be deposited from precursors in vapor, liquid, or even solid phases, or a combination of several phases, depending on the nature of the precursors and the desired functionality and specification of the resulting thin solid film. Physical and chemical vapor deposition methods, such as sputtering and epitaxy, are some examples of vapor phase deposition methods. These processes require well-controlled atmosphere and are usually performed in a vacuum, using expensive equipment and energy-intensive processes. Therefore, it is not surprising that the resulting thin films made by vapor phase methods are high-quality films with fewer defects. On the other hand, the liquid-phase methods for deposition of thin films from solution or colloidal mixtures, such as spin coat, sol-gel, and printing methods, are cheaper but less controllable and repeatable, which may affect the quality of the thin films. It can be observed that some thin films may be

deposited by several methods, whereas some others are only compatible using a particular deposition route. For example, highly crystalline thin film semiconductors need to be deposited via the vapor phase methods, such as epitaxy. Organic thin films are usually deposited with a low-temperature solution. Whereas some other materials, inorganic thin film semiconductors such as *a*-IZO, may be deposited from both the vapor and liquid phases. The vapor phase film deposition methods are well studied and established. Therefore, the focus of this paper is more on the potential for flexible, large-scale, low-cost fabrication of thin film devices that can be processed in solution using wet chemistry and deposited using proper printing or coating techniques [13].

In this thesis, selecting a solution oxide material that can possibly undergo a semiconductor-to-conductor transformation to act as both a channel and electrode within a layer is proposed. Using previous studies of the role of each element for *a*-IGZO material, increasing the In ratio was correlated with decreasing of the electrical resistivity because a high In ratio leads to an increase of the amount of oxygen vacancies and Zn interstitials which are the origin of electrons. An increase of In atoms in IZO induced a negative shift and increasing on-current (I_{on}) and off-current (I_{off}) of transfer curve due to having more electrons. Therefore, as In ratio was increased in IGZO TFTs, field-effect mobility (μ_{FET}) was increased [13]. For the Ga effect in *a*-IGZO TFTs, Kim et al. [14] explained that if the Ga/Zn ratio increased, the electron concentration decreases and the electrical resistivity inversely increases. This is because Ga composition acted as a suppressor in *a*-IGZO thin films. Ga ions have stronger chemical bonds with oxygen than that of the In and Zn ions due to larger formation energy of oxygen vacancy [14]. The incorporation of Ga content in the *a*-IGZO played the role of effective control of carrier generation which is related to oxygen vacancies. In *a*-IGZO, higher electrical

conductivity came from In and Zn. To reduce the effect of carrier suppressors, I selected *a*-IZO instead of *a*-IGZO to increase the possibility to substantially increase the oxygen vacancies to the treatment-selected area and keep a good quality of *a*-IZO semiconductor as a channel layer in the covered area.

There are varieties of treatment techniques to increase the amount of oxygen vacancies such as by inducing the plasma effect directly to the target sample such as plasma treatment, excimer laser annealing (ELA), or even reactive ion etching (RIE) [15]. However, these treatment methods require high energy and complex methods. For simpler, faster operation, and low cost, ultraviolet rays that are usually used together with ozone treatment – commonly used to clean the sample surface are selected instead of the complex treatment methods stated above. With the UV light with wavelengths of 184.9 nm and 253.7 nm, it is possible to increase the number of oxygen vacancies inside the oxide semiconductor, which are discussed in the next section.

4.3 UV and UV-ozone treatment

In general, UV/O_3 treatment is used for material surface cleaning application such as glass plates, chrome masks, metals, and semiconductors for coating of a photoresist and improving the adhesive force. The uses of UV/O_3 treatment can be (i) surface treatment prior to coating, plating, or vaporization, (ii) clean oxidation of metal and semiconductor surfaces, (iii) modification of polymer surfaces, (iv) peeling and etching of photoresist thin films.

The principle of UV/O_3 treatment can be explained by the organic compounds, which are converted into volatile substances such as water, carbon dioxide, nitrogen by decomposition by ultraviolet rays and by strong oxidation during the formation and decomposition of O_3, and are removed from the contaminated surface. The major

wavelengths of the ultraviolet rays radiated from a well-known low-pressure mercury vapor lamp are 180 nm and 254 nm. When atmospheric oxygen O_2 is irradiated with ultraviolet rays with a wavelength of 180 nm, the oxygen absorbs the ultraviolet rays to form O_3 by the following reaction:

Ultraviolet rays with a wavelength of 180 nm

$$O_2 \rightarrow O + O$$

$$O + O_2 \rightarrow O_3$$

Ozone O_3 irradiated with ultraviolet rays with a wavelength of 254 nm absorbs the ultraviolet light to decompose O_3. During the process of formation or decomposition of O_3, atomic oxygen O having a strong oxidizing ability is generated. Then, contaminant organic compounds are irradiated with ultraviolet rays and absorb the ultraviolet rays to cause photolysis and generate the substances, which are ions, free radicals, excited molecules, and neutral molecules.

Focusing on the UV light energy source, The UV treatment which adapted from the UV/O_3 treatment create an impact application to transform the semiconductor to the conductor. The energy (E) of an electromagnetic wave has a relationship with the wavelength λ as expressed by the following equation below:

$$E = hc/\lambda \qquad (4.1)$$

Where h is Planck's constant = 6.626 x 10^{-34} J·sec, c is the velocity of light = 2.998 x 10^{10} cm·sec^{-1}, and λ is the wavelength (cm). According to equation 4.1, the energy (E) of ultraviolet rays with a wavelength of 180 nm is 6.7 eV. In the same calculation, the E of ultraviolet rays with a wavelength of 254 nm is 4.9 eV.

Table 4.1 shows the bond energies of In – O and Zn – O, these inorganic compounds can be decomposed by irradiating them with energy stronger than the bond

energy. According to this chemical-bond energy, light energy with a wavelength of both 180 nm and 254 nm from UV treatment is high enough to make *a*-IZO generate more oxygen vacancies from the weak bond.

In this study, UV/O_3 is used for surface treatment to improve hydrophilic properties to a substrate in the fabrication process. Meanwhile, applying only UV light with the same energy level tend to reduce the resistivity of the oxide material by cutting the oxygen bond without external oxygen suppression from the oxygen radicals generated by the ozone. Notice that enhancing the conductivity of oxide semiconductor, it is important to removing O_3 in the method to increase a probability of the oxygen vacancy formation.

Table 4.1 chemical-bond energy in eV [16]

Bonds	**Chemical-bond energy**
In – O	~1.7 eV
Zn – O	~1.5 eV

4.4 Transparent metal oxide electrode

Transparent conductive electrodes (TCEs) are widely used in organic light-emitting diodes (OLEDs), liquid crystal displays (LCDs), and organic solar cells. Many candidates have been developed for use as transparent electrodes, including carbon nanotubes (CNTs) [17], conducting polymers [18], and graphene [19]. However, these alternative materials cannot fulfill all requirements such as high transparency, high electrical conductivity, uniform conductance, and high adhesion to substrates. Recently, the common material to be used as a transparent electrode is a transparent metal oxide electrode material.

The transparent metal oxide electrode or transparent conducting oxide (TCO) films have been prepared by several combinations of the sputtering method have been reported as a technique for coating TCOs, which has merits such as electrical conductivity, high transparency, and environmental stability. The TCO materials which are commonly used are InZnO (IZO), InSnO (ITO), InGeO, InZnSnO, and InTaO [20-26]. However, most transparent electrodes are produced by vacuum deposition process, which is not suitable for continuous processing, which is the fabrication strategy being pursued to develop next-generation flexible electronics.

As alternative processes, TCO material has been fabricated by a solution process such as IZO, ITO, and ZnO [27,28]. Among various deposition methods, solution processed TCO has become a subject of interest due to their ease of fabrication, scalability, and the potential to lower device-manufacturing making steps and costs. However, the demerit of solution processed TFT using TCO electrode is low electrical performance and their non-uniformity [27,28]. To reduce parasitic resistance and contact resistance between electrode and semiconductor interface, a single layer of semiconductor-conductor fabrication to improve the all-solution processed TFT electrical performance is a challenge in this thesis.

4.5 Analysis of novel all-solution processed self-aligned oxide TFTs

4.5.1 Fabrication process

To fabricate self-aligned top gate structure that was used in this study, I begin with Figure 4.1 which illustrates the fabrication process of all-solution processed *a*-IZO

TFTs with siloxane as a GI. The SiO_2/Si substrates were cleaned with concentrated sulfuric acid at 80°C for 10 minutes then mixed with hydrogen peroxide (H_2O_2) for 10 minutes. UV/O_3 was performed to enhance the hydrophilic properties on the surface of the SiO_2/Si substrate with a wavelength of 180 nm and 254 nm at 115˚C in 10 min,

The cleaned substrates were placed on the spin coater, and rotation speed was set at the rate of 300 rpm in 3 second and 3000 rpm in 30 second, respectively. The deposition of the 50-nm-thick *a*-IZO layer was prepared by IZO solution precursor with an In:Zn ratio of 77:23. The deposition rate is 10 nm/cycle of spin coating. The prebake and post bake processes are performed in every deposited layer at 150˚C in 5 min and 300˚C in 5 min in air. The first prebake is for the decomposition of the organic radical, while the post bake is applied for hydrolysis to form the metal-oxide bond. After looping the spin coating 5 times (aiming for 50-nm-thick), the *a*-IZO was put on the hot plate and post bake as performed for dehydroxylation and alloying at 300˚C in 60 min as seen in Figure 4.2.

a-IZO films used in this study were evaluated in the as-deposited condition. Identical to chapter 2 and 3, the channel material was patterned using UV photolithography and wet etching by 0.02 M HCl solution for 2-4 minutes. To fabricate a siloxane GI on top, spin-coating served a siloxane polymer layer on TFTs, at a rate of 1500 rpm for 15 seconds. Prebaking was then performed at a temperature of 110°C for 1 minute. To remove the volatile constituents and finish the cross-linking reaction of the siloxane, baking was performed at 230°C for 20 minutes and 300°C for 20 minutes in the air, respectively.

Right after deposition of the siloxane GI, the TFT samples were placed inside UV/O_3 treatment to enhance the hydrophilic properties on the surface of siloxane layer at

115˚C in 5 min before deposit the top gate *a*-IZO on the top with the same condition of solution *a*-IZO spin-coat deposition as mention before. To perform patterning of source/drain electrode, the TFT sample was patterned using UV photolithography and wet etching by 0.02 M HCl solution for 2-4 minutes to remove non-resist-covered *a*-IZO area.

The non-resist-covered siloxane area can be removed by RIE process with the gas ratio of CF_4/ Ar =30/ 45 sccm for 30 seconds. The resist was then removed with acetone, methanol, and pure water to finish the processes for as-fabricated samples. To make *a*-IZO source, drain, and gate electrodes, the TFT sample was treated by UV treatment under wavelength of 180 nm and 254 nm at 115˚C in 15 min with UV lamp power of 15 mW/cm^2 which finishes all the processes. The top-view structure is shown in Figure 4.3 observed by optical microscope.

I_{ds}-V_{gs} characteristics measurement were performed with an Agilent HP4156C semiconductor parameter analyzer. The switching of fabricated devices was traced by apply voltage to gate from -20 V to 20 V whose step was 100 mV, and apply voltage to drain from 0.1 V to 9.9 V whose step was 4.9 V. The sheet resistance was performed by 4-point-probe method using 1×1 cm^2 *a*-IZO film before and after UV treatment at 115˚C in 15 minute.

Elemental composition, structure, and defects were observed by performing cross-sectional imaging by the STEM and observe the elemental and structural analysis by EDX Spectroscopy. To confirmed that this TFT is fabricated without any metal electrodes, the TFT cross-sectional structure was observed by the STEM and elemental mapping observation by EDX as shown in Figure 4.4 and 4.5. Note that the TFT was coated with W and C for sample preparation during cutting by Focused Ion Beam (FIB).

The electrical properties were evaluated by analyzing the TFT transfer characteristics. To confirm the transformation of *a*-IZO from semiconductor to conductor, the resistivity is calculated from the value of the sheet resistance. Furthermore, the mechanism will be elucidated by performing SIMS for diffusion study and XPS for chemical structural observations and comparing the oxygen vacancy concentrations between *a*-IZO before and after UV treatment.

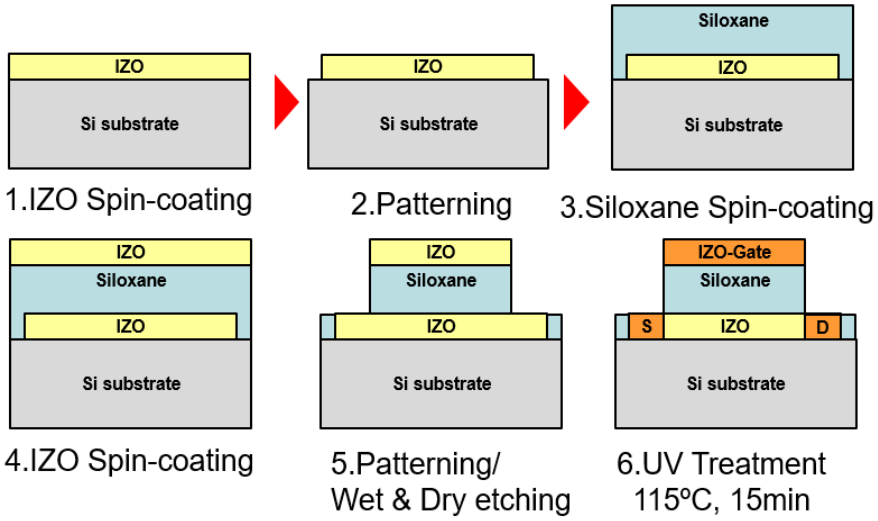

Figure 4.1 Illustration of process flow of the all-solution process self-aligned *a*-IZO TFT device without any metal electrodes.

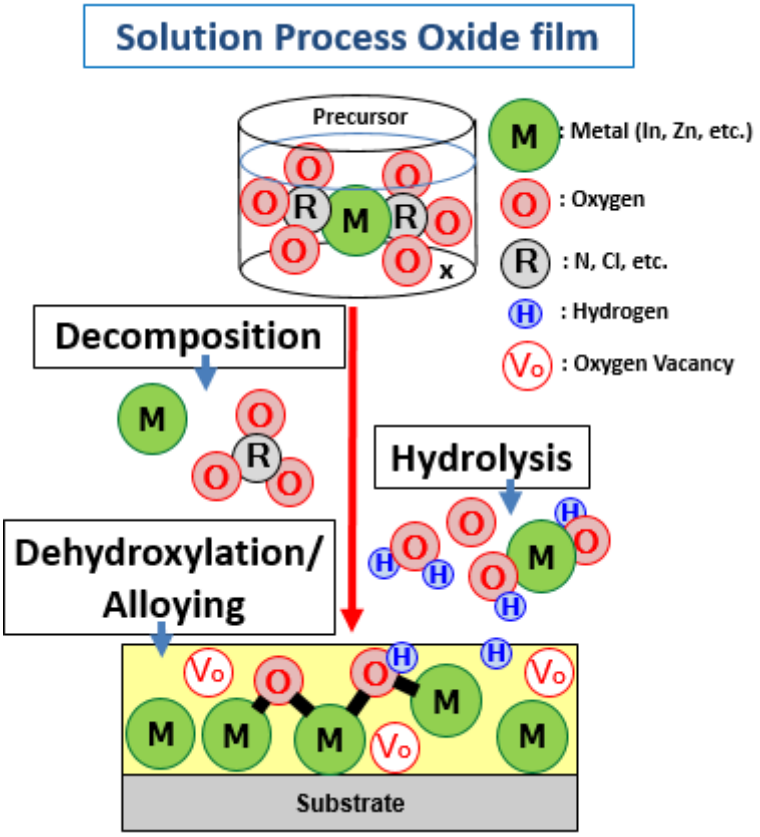

Figure 4.2 Illustration of three steps of solution processed oxide film deposition following decomposition, hydrolysis, and dihydroxylation/alloying.

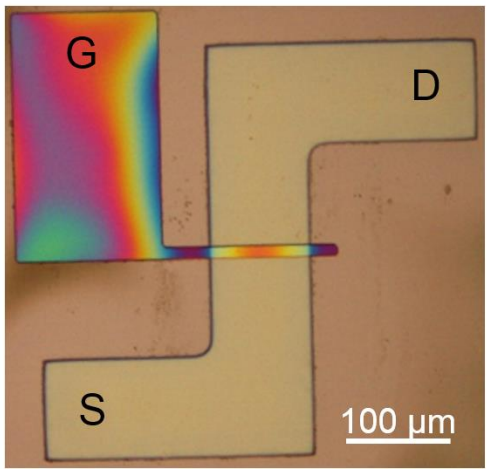

Figure 4.3 Top view of the all-solution processed *a*-IZO TFT including source (S), drain (D), gate (G), and channel layer under the gate observed by optical microscope.

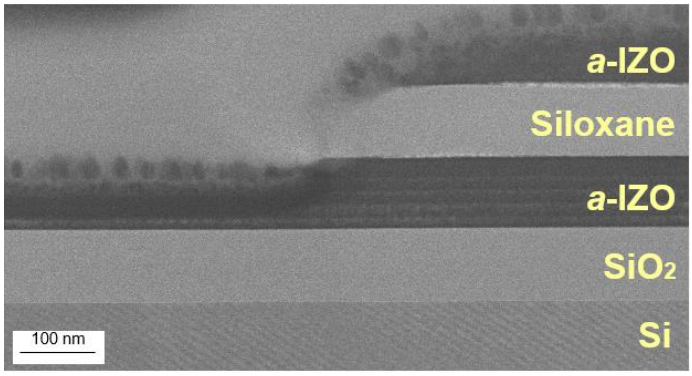

Figure 4.4 Cross section of the all-solution processed *a*-IZO TFT observed by STEM.

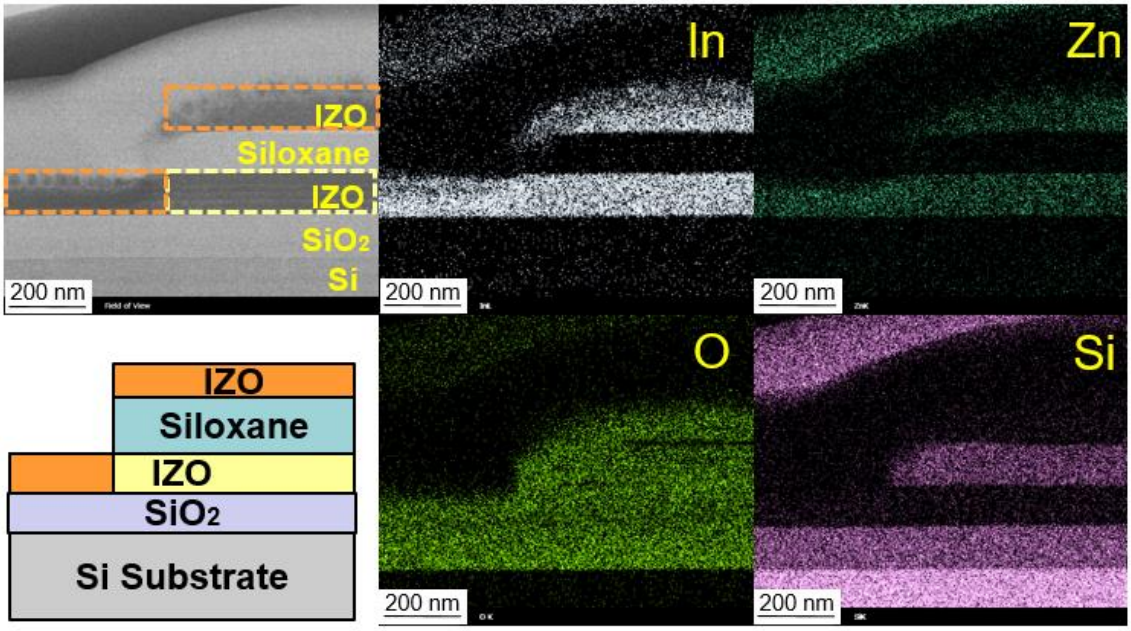

Figure 4.5 Elemental mapping of the all-solution processed *a*-IZO TFT observed by EDX, proved that this TFT was fabricated without any metal electrodes. Note that TFT was coated by W and C during cutting by FIB.

4.5.2 Electrical characteristics

The effects of UV-induced transformation of semiconductor-to-conductor on the electrical characteristics of self-aligned *a*-IZO TFTs were measured by I_{ds}-V_{gs} characteristics. The as-fabricated or before UV treated TFTs and after UV treated TFTs had a *W/L* of 90/20 μm. Figure 4.6 shows a comparison of the transfer characteristics of self-aligned *a*-IZO TFT before UV as Figure 4.6 (a) and after treated by UV at 115˚C in 15 min as Figure 4.6 (b). As expected, the transfer characteristics show that as-fabricated TFT show poor characteristics – with no switching behavior and low current because of the source, drain, and gate *a*-IZO were still not activated. Meanwhile, TFTs treated by UV at 115˚C in 15 min show effective switching behavior. The TFT characteristics with UV at 115˚C in 15 min was measured.

In this chapter, I used a 100-nm-thick siloxane as a GI. Following equation 3.1, the resulting TFT was excellent: the μ was 8.02 $cm^2 \cdot V^{-1} \cdot s^{-1}$, V_{th} was 3.70 V, *SS* was 320 mV/decade, and I_{on}/I_{off} was ~10^7. This result shows that UV treatment at very low temperatures and short treatment time are enough to activate the conductive behavior of *a*-IZO to act as electrodes. Moreover, siloxane GI also supported the *a*-IZO semiconductor area to show a very high performance TFT compared with other solution processed TFT [3,29] or even comparable with vacuum processed *a*-IZO TFT which has a μ range from around 5-30 $cm^2 \cdot V^{-1} \cdot s^{-1}$, *SS* around 300-800 mV/decade, and I_{on}/I_{off} less than 10^8 [30-32].

More studies about the degradation of all-solution processed *a*-IZO TFTs was performed by 10-time continuous measurement as shown in Figure 4.7. The results clearly show that the TFT dramatically degrades with both on and off current after the same TFT is consecutively re-measured 10 times, but the TFT switching behavior still

remains after 10th measurement. I suggested that the oxygen vacancies inside the activated *a*-IZO electrodes are mobile. However, these results show a great move in term of TFT operated without any metal electrodes and generate extremely high performance of initial electrical characteristics.

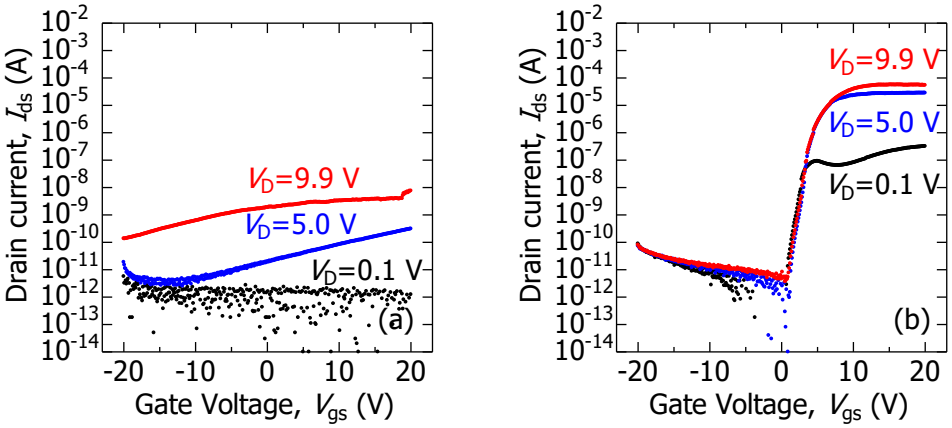

Figure 4.6 Comparison of transfer characteristics of self-aligned *a*-IZO TFT (a) before UV, (b) after UV treated TFT, TFTs had a *W/L* = 90/20 µm.

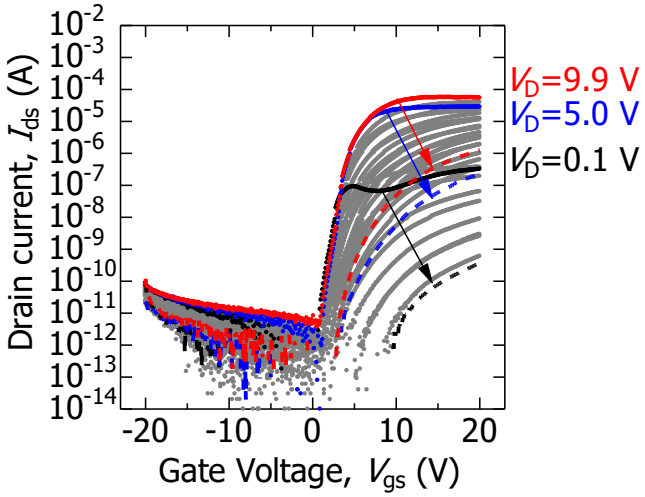

Figure 4.7 The 10 times transfer characteristics measurement of self-aligned *a*-IZO after UV treatment, TFTs had a *W/L* = 90/20 µm.

4.6 Analysis of the UV-induced TFTs

In the previous section, no degradation is observed in the saturation region of the initial transfer characteristics, suggesting good contact region between the *a*-IZO semiconductor and activated *a*-IZO electrodes. Suggesting that the UV treatment can penetrate through the bulk of the affected *a*-IZO, which is confirmed by the calculation of the penetration depth by Lambert's law of absorption equation as given below,

$$\frac{1}{\alpha} = \lambda/4\pi k \quad (4.1)$$

Where k is IZO's extinction coefficient and λ is UV wavelength = 254 nm. After calculation, the penetration depth of UV through *a*-IZO bulk is estimated to be 75.53 nm, which confirms that the UV light can affect through the *a*-IZO bulk layer except the channel area protected by 100-nm-thick siloxane GI, which has a maximum absorption coefficient of 6×10^{-4} μm^{-1} under 1700 nm-wavelength [33].

The *a*-IZO film samples were fabricated to measure the sheet resistance to facilitate comparison of *a*-IZO without UV treatment and *a*-IZO with UV treatment. The sheet resistance values were measured by 4-point-probe measurement (KEITHLEY2401). The 4-point-probe contains four thin collinearly placed tungsten wires probes which are made to contact the sample under test. The current will flow between the outer probes, and the voltage is measured between the two inner probes and assume that the interprobe spacings are equal. After measuring 10 times, the results are shows the average value as follow; *a*-IZO without UV treatment and *a*-IZO with the UV treatment show sheet resistance of 14553.34 Ω/square and 134.68 Ω/square, respectively. This result shows that *a*-IZO after UV treatment has a drastically reduced resistance compared with before UV treatment.

The resistivity of *a*-IZO with and without UV treatment was calculated by the value of sheet resistance measured by 4-point-probe multiplied by the *a*-IZO film thickness. The results of calculation of *a*-IZO without UV treatment and *a*-IZO with UV treatment show the resistivity of 0.07 Ω-cm and 6.73×10^{-4} Ω-cm, respectively. These results show that after UV, resistivity decreased from before UV by almost 2 order of magnitude, makes *a*-IZO become a conductive comparable even with commercial ITO electrodes [34] as shown in Table 4.2. These results proved that the UV-induced on oxide TFT is a promising method to make a TCO material, which is simple, low cost, low temperature, and fast operation process.

Table 4.2 TCO materials resistivity comparison

TCO	**Techniques**	**Resistivity**
ITO	Commercial	~1.90×10^{-4} [33]
ITO	PLD	8.45×10^{-5} [33]
ITO	Spray pyrolysis	~1.29×10^{-4} [33]
IZO	Without UV treatment	7.25×10^{-2}
IZO	With UV treatment	6.73×10^{-4}

The whole mechanism to clearly explain the enhanced TFT performance is not yet well understood and is still being developed since this structured design is a state-of-the-art technique. For more understanding of the mechanism, there are a variety of techniques that were previously used to enhance the conductivity of oxide semiconductor such as Kang *et al*, enhance the conductivity of IZO thin films by self-combustion technique by inducing exothermic heat from a combustion, which leads to enhancement of the IZO electrical conductivity [35] and D.-S. Liu *et al*, showed the temperature

dependence of oxygen ambient annealed IZO film, in which the resistivity of IZO film is increased after increasing the temperature [36]. However, these techniques transform the oxide material to become an electrode for the whole layer and are unable to make a selective region conductive. H. Liu *et al* also reported that electrical conduction in TCOs is achieved by introducing native defects such as oxygen vacancies or doping higher-valence elements to increase the carrier concentration around 10^{20} cm^{-3} [33].

According to the literature review above, the transformation of semiconductor-to-conductor in this research is strongly dependent on the amount of oxygen vacancies (V_O) since the nature of these created states is ionized oxygen vacancy (V_O^{2+}). These additional V_O^{2+} states act as deep hole trapping centers and increase the carrier concentration by giving free carriers in *a*-IZO which increases the conductivity [37].

For more understanding of the mechanism, the *a*-IZO film samples without UV treatment and with UV treatment are analyzed by SIMS and XPS. SIMS analysis was performed to understand the composition change of each element through the bulk of IZO as shown in Figure 4.8. They have to significantly change the atomic counts of 18O, 1.2H, and 16O+1H which represent the amount of oxygen, hydrogen, and hydroxide, respectively. To support this data, the comparison of O1s XPS spectra of *a*-IZO before UV treatment and *a*-IZO after UV treatment are shown in Figure 4.9. From the result, there is a slight change of the M-V_O peak of each sample means they have some change of the bonding inside of the *a*-IZO sample after UV treatment.

The O1s XPS spectra of *a*-IZO without UV treatment in Figure 4.10 (a) and *a*-IZO with UV treatment in Figure 4.10 (b) on the surface of the *a*-IZO layer. The spectra show the comparison of the area ratio percentages of the deconvoluted sub-peaks with the total FWHM in the range of 1.4-1.6 eV for each component. The peak shows 4 peaks

at 530, 531, 532, 533 eV which is attributed to metal oxide (M-O) bonding, oxygen deficiency region (M-V_o), hydroxide (M-OH), and chemisorbed water molecules (H_2O), respectively [38,39].

The deconvolution shows a solid increase of M-V_O peak by 5% and M-O also decreases by 7%, suggesting that they have some effect during fabrication process which supports the idea that the oxide layer generates more oxygen vacancies when subjected to processes such as RIE method that induces plasma damage during operation. As reported by Chien *et al*, a resist-related phenomenon during plasma charging must be taken into a consideration [40]. The RIE etching on that *a*-IZO area that has to resist overlayer may exhibit extra defects, although the detailed charging mechanism needs further investigation. The result in Figure 4.6 (a) also supports this statement by the small switching behavior occurring on the TFT transfer curve before UV treatment. After the RIE method, the metal oxide bond was cut by the UV light which increases the number of oxygen vacancies making *a*-IZO after UV treatment to demonstrate a more conductive behavior as shown in Figure 4.7 (b).

In the *a*-IZO semiconductor region, as same as explained in chapter 3, the increase in M-O bonding implies that there are more carrier pathways in the *a*-IZO from siloxane GI, which improved the mobility. Besides the effect from the siloxane layer, the higher densification after post-baking at 300°C in 1 hour also suppress the generation of oxygen vacancies inside the channel layer and enhances the device performance.

The hypothesis of the mechanism of UV-induced transformation is primarily due to the increase of oxygen vacancies on the *a*-IZO surface as shown in Figure 4.11. There are no significant changes in the number of each element such as oxygen, hydrogen, and hydroxide as observed by SIMS analysis. After RIE process in combination with UV

treatment, the M-O ratio will be decreased and the M-V_O ratio will be increased, which suggests that the generation of more oxygen vacancies made *a*-IZO to have higher conductivity. This mechanism needs further investigation for a clearer understanding and is described as a future work as discussed in chapter 5.

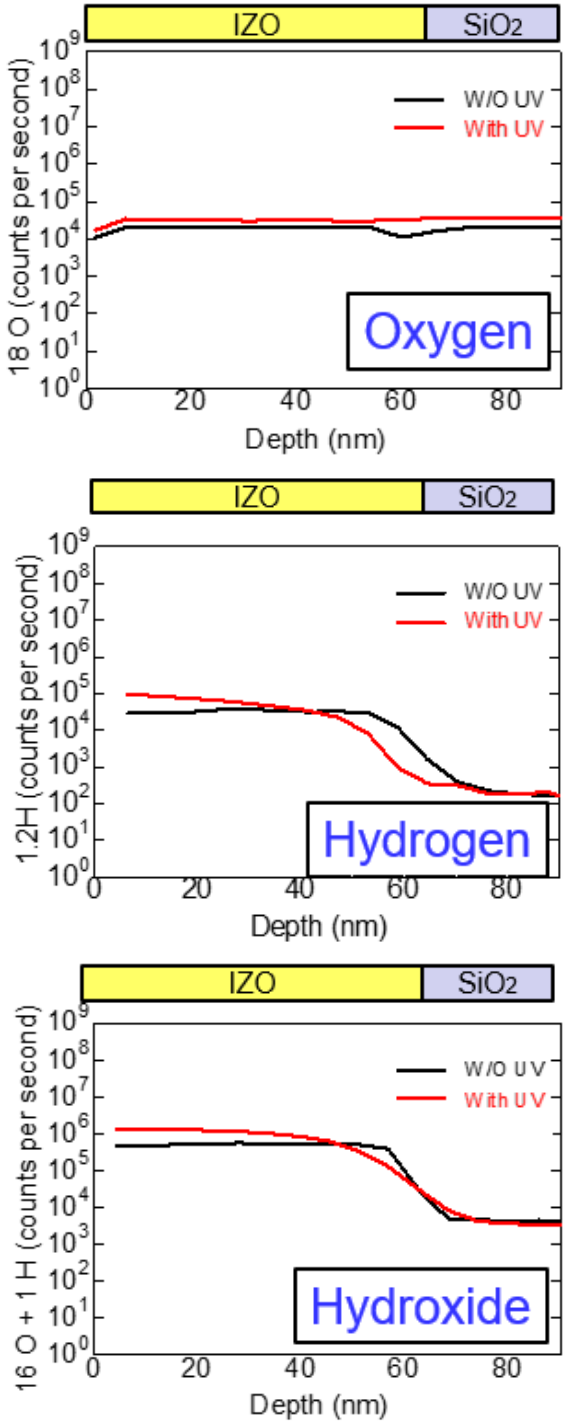

Figure 4.8 The 10 times transfer characteristics measurement of self-aligned *a*-IZO after UV treatment, TFTs had a *W/L* = 90/20 µm.

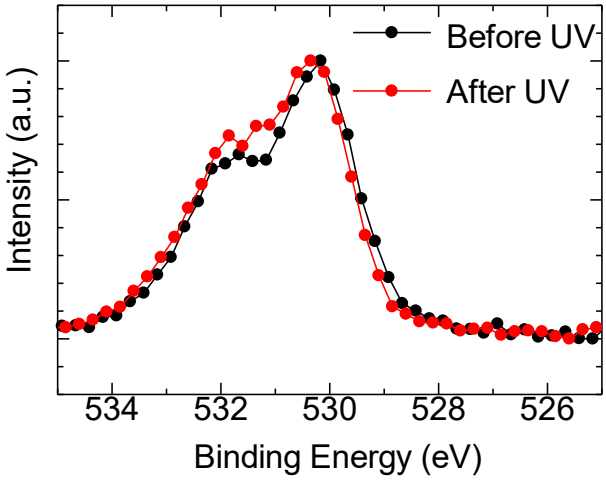

Figure 4.9 Comparison of O1s XPS spectra in the *a*-IZO layer before UV treatment (black line) and after UV treatment (red line).

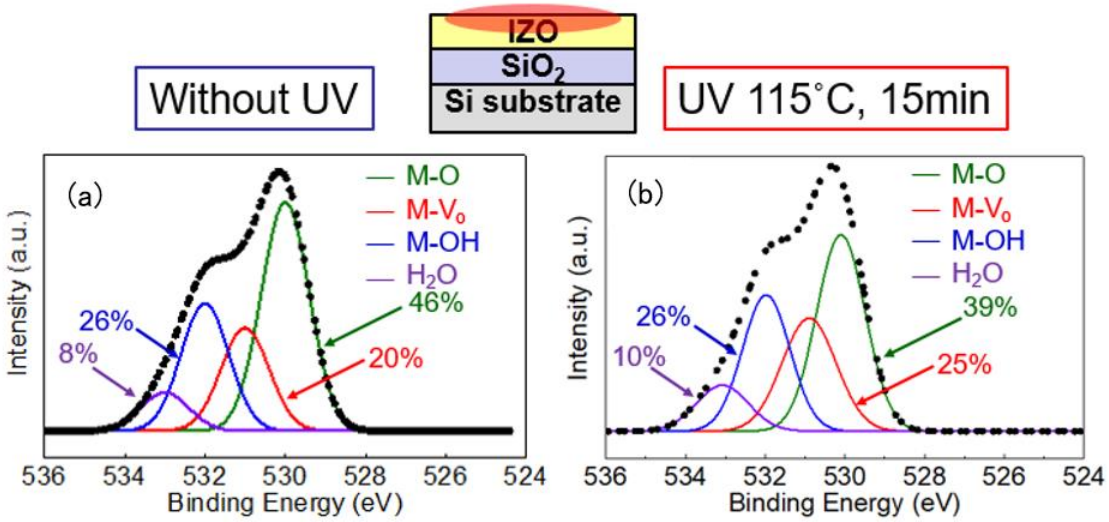

Figure 4.10 O1s XPS spectra on the *a*-IZO surface of (a) without UV and (b) with UV treatment.

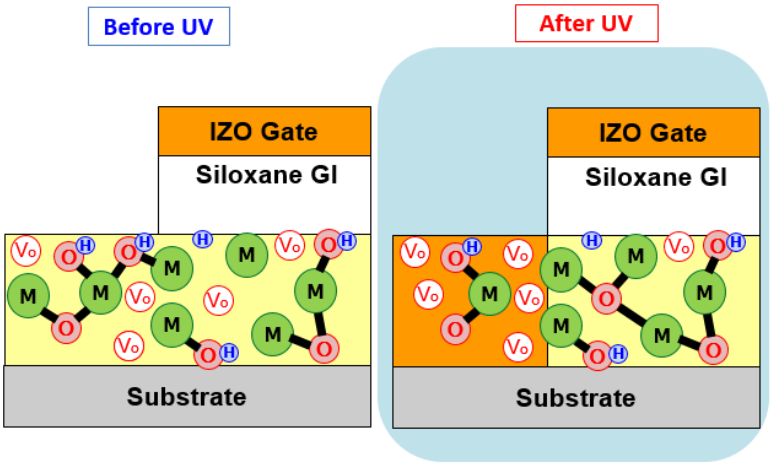

Figure 4.11 Illustration of the mechanism of the oxygen vacancies generation on *a*-IZO surface before and after UV treatment.

4.7 Summary

Developing all-solution processed oxide TFT for flexible and wide area display is rapidly receiving interest and has become an important research topic in the industry of display development. In section 4.2, many traditional vacuum processes were introduced to compare with solution process fabrication. Many research groups have shown different methods to point out the problem of lowering the complexity of the fabrication process, lower the process temperature, and lower the production cost. The solution process results of many research groups show interesting progress in making solution processed TFT instead of vacuum processed TFT. I used *a*-IZO TFT instead of *a*-IGZO TFT due to the higher conductive behavior without Ga suppressor, which will benefit the transformation of the semiconductor-to-conductor layer and also possible to fabricate by solution method as many researchers have succeeded.

The UV and UV/O_3 treatment was introduced in section 4.3 and shows the common application of UV/O_3 in cleaning up the surface of the target sample. By observing the mechanism of the UV/O_3 treatment; we can activate a TCO material by

using the UV ray under the wavelength of 180 nm and 254 nm to increase the number of oxygen vacancies inside the oxide semiconductor as explained in section 4.4.

The fabrication method of all-solution processed *a*-IZO TFT without any metal electrodes are given in section 4.5, which shows a very simple fabrication process with just only spin-coating and patterning to finish up the processes. Moreover, the all-solution processed *a*-IZO TFT without any metal electrodes shows extremely high electrical characteristics after UV treatment at 115˚C in just 15 minutes – comparable with vacuum processed *a*-IZO TFT. In addition, this is the first time that the TFT characteristics demonstrate switching behavior even without any metal electrode. However, suppressing the degradation of the solution processed material is still needed to improve.

The effect of UV-induced transformation on self-aligned structure *a*-IZO TFT was confirmed, with the entire depth of the *a*-IZO bulk layer shown to be affected by UV light under wavelength of 184.9 nm and 253.7 nm as shown by the calculation of the UV penetration depth through the *a*-IZO layer. After calculating the resistivity of before UV and after UV treated *a*-IZO samples of 0.07 Ω-cm and 6.73 x 10^{-4} Ω-cm, respectively. This 2 order of magnitude of reduction of the resistivity after treatment by UV light is a good sign for this treatment method because the UV treatment method is very simple, fast operation, and has low process cost.

Section 4.6 The *a*-IZO film before UV and after UV treatment is also confirmed by SIMS and XPS analysis that the amount of element inside *a*-IZO films such as oxygen, hydrogen, and hydroxide will not change after being treated by UV. But the chemical bonding inside as observed by O1s XPS spectra significantly changes, however, the differences of M-V_O are not high as expected. The metal oxide bond at 530 eV-binding energy was reduced only by 7% after treatment and oxygen vacancies at 531 eV-binding

energy were increased only by 5%. Suggesting that resist-related phenomenon during plasma charging by RIE etching affects the changing of the number of oxygen vacancies or make Oxygen dangling bond become easier to remove after irradiating by UV light, which makes *a*-IZO transform into a conductor.

This chapter guided that the UV-induced transformation of oxide semiconductors is a promising method to make TCO materials, which is a simple, cost-effective, low temperature and fast operation process. Particularly, the novel all-solution processed *a*-IZO TFT design improved the TFT performance while simultaneously reducing cost and reducing the fabrication steps. This simple UV method will drive solution processed TFT research to move to the next step.

References

[1] D. B. Mitzi, Solution Processing of Inorganic Materials, Wiley, (2008).

[2] Y. G. Sun and J. A. Rogers, Adv. Mater. 19, 1897-1916 (2007).

[3] M.-G. Kim, M. G. Kanatzidis, A. Facchetti, and T. J. Marks, Nat. Mater. **10**, (2011).

[4] H. Yan, et al., Nature, **457**, 679-686 (2009).

[5] R. C. G. Naber, et al., Nat. Mater. **4**, 243-248 (2005).

[6] T. Sakanoue and H. Sirringhaus, Nat. Mater. **9**, 736-740 (2010).

[7] R. P. Ortiz, A. Facchetti, and T. Marks, Chem. Rev. **110**, 205-239 (2010).

[8] M. N. Fujii, Y. Ishikawa, K. Miwa, H. Okada, Y. Uraoka, and S. Ono, Sci. Rep. **5**, 18168 (2015).

[9] S. Y. Lee, S. Chang, and J.-S. Lee, Thin Solid Films, **518**, 3030-3032 (2010).

[10] M. J. Alam and D. C. Cameron, Thin Solid Films, **420**, 76-82 (2002).

[11] Y. L. Wu, Y. N. Li, and B. S. A. Ong, J. Am. Chem. Soc. **129**, 1862-1863 (2002).

[12] S. Bae, et al., Nat. Nanotech. **5**, 574-578 (2010).

[13] G. H. Kim, B. D. Ahn, H. S. Shin, W. H. Jeong, H. J. Kim, and H. J. Kim, Appl. Phys. Lett. **94**, 233501 (2009).

[14] G. H. Kim, W. H. Jeong, and H. J. Kim, Phys. Status Solidi A **207**, 1677 (2010).

[15] J. P. S. Bermundo, Y. Ishikawa, M. N. Fujii, H. Ikenoue, and Y. Uraoka, Appl. Phys. Lett. **110**, 133503 (2017).

[16] S. Kim and L. Donald, Chemistry LibreTexts, Bond Energy, (2017).

[17] Q. Cao , S. H. Hur , Z. T. Zhu , Y. Sun , C. Wamg , M. A. Meitl , M. Shim , and J. A. Rogers , Adv. Mater. **18**, 304, (2006).

[18] M. Vosgueritchian , D. J. Lipomi , and Z. Bao , Adv. Funct. Mater. **22**, 421 (2012).

[19] S. Pang , Y. Hernadez , X. Feng , and K. Müllen , Adv. Mater. **23**, 2779 (2011).

[20] D.-Y. Cho, K.-B. Chung, S.-I. Na, H.-K. Kim, J. Phys. D: Appl. Phys. **46**, 295305 (2013).

[21] H.-M. Lee, S.-B. Kang, K.-B. Chung, and H.-K. Kim, Appl. Phys. Lett. **102**, 021914 (2013).

[22] K.-W. Seo, J.-H. Lee, H.-J. Kim, S.-I. Na, and H.-K. Kim, Appl. Phys. Lett. **105** 031911, (2014).

[23] C.-Y. Park, C.-Y. You, K.-R. Jeon, and S.-C. Shin, Appl. Phys. Lett. **100**, 222409 (2012).

[24] H. Lee, H. Lee, J.-H. Park, H.-K. Kim, B.H. Kong, and H.K. Cho, Jpn. J. Appl. Phys. **50**, 055805 (2011).

[25] Y.-S. Park, H.-K. Park, S.-W. Cho, J.-A. Jeong, K.-H. Choi, H.-K. Kim, J.-Y. Lee, J.-H. Lee, H.-D. Bae, Y.-H. Tak, and W.-J. Cho, Solid-State Lett. **11**, J85–J88 (2008).

[26] Y.-Y. Choi, S.J. Kang, and H.-K. Kim, Curr. Appl. Phys. **12**, S104–S107 (2012).

[27] S. Edinger, N. Bansai, M. Bauch, R. A. Wibowo, G. Újvári, R. Hamid, and G. Trimmel, J. Mater. Sci, **52**:8591-8602 (2017).

[28] S. Bouden, A. Dahi, F. Hauquier, H. Randriamahazaka, and J. Ghilane, Sci. Rep. **6**:36708 (2016).

[29] S. Yoon, S. J. Kim, Y. J. Tak, and H. J. Kim, Sci. Rep. **7**:43216 (2017).

[30] N. L. Dehuff, E. S. Kettenring, D. Hong, H. Q. Chiang, J. F. Wager, R. L. Hoffman, C. H. Park, and D. A. Keszler, J. Appl. Phys., **97**, 064505 (2005).

[31] B. Yaglioglu, H. Y. Yeom, R. Beresford, and D. C. Paine, Appl. Phys. Lett., **89**, 062103 (2006).

[32] J. I. Song, J. S. Park, H. Kim, Y. W. Heo, J. H. Lee, J. J. Kim, G. M. Kim, and B. D. Choi, Appl. Phys. Lett., **90**, 022106 (2007).

[33] S. Hegde, Optical Attenuation in Siloxane Polymer Waveguides (2010).

[34] H. Liu et al., Superlattices and Microstructures **48**, 458-484 (2010).

[35] Y.H. Kang, K.S. Jang, C. Lee, and S.Y. Cho, ACS Appl. Mater. Interfaces, **8**(8):5216-23 (2016).

[36] D.-S. Liu, C.-H. Lin, C.-S. Sheu, and C.-T. Lee, Thin Solid Films **516**(10):3196-3203 (2008).

[37] H. Oh, S. Yoon, M. K. Ryu, C. Hwang, S. Yang, and S. K. Park, Appl. Phys. Lett., **97** 183502 (2010).

[38] J. P. Bermundo, Y. Ishikawa, H. Yamazaki, T. Nonaka, M. N. Fujii, and Y. Uraoka, Appl. Phys. Lett. **107**, 033504 (2015).

[39] A. Celebioglu, S. Vempati, C. O. –Akgun, N. Biyikli, and T. Uyar, RSC Adv. **106**, (2014).

[40] C.-H. Chien, C.-Y. Chang, H.-C. Lin, T.-F. Chang, S.-G. Chiou, L.-P. Chen, and T.-Y. Huang, IEEE Electron Device Letters, Vol. **18**, No. 2 33 (1997).

Chapter 5
Conclusions

5.1 Conclusions

All-solution processed fabrication of TFTs is a promising fabrication method because the high demand of flat panel displays will dramatically increase every year coupled with the need to reduce the process cost while keeping the high performance of devices. In order to manufacture high-performance all-solution processed oxide TFTs aiming to develop flexible and wide area electronic devices, investigation of each part of TFT structure is an important factor, as described in Chapter 1. In this study, the influence of the fabrication process to TFT performance was evaluated by various techniques mainly the comparison between vacuum technique and solution technique.

The key point to enhance the performance of solution process is the element control such as hydrogen, oxygen, and/or hydroxide on the surface and interface of the TFT such as gate insulator/semiconductor or electrodes/semiconductor. The main issue of the oxide channel materials is the degradation resulting in poor reliability versus ambient effects. The TFT performance can be supported with a suitable gate insulator beside thermally oxidized SiO_2, which has limited application in future devices.

This thesis mainly described the effects of the defect and the elemental analysis of oxygen, hydrogen, and hydroxide on the electronic properties of oxide TFT. In addition, the fabrication of all-solution processed oxide TFT applications with a high performance aiming for future flexible devices was also considered. The results obtained in this study are important from both a scientific academic and an engineering industry viewpoint.

Selection of a passivation material suitable for oxide semiconductor such as *a*-IGZO was successful. The hybrid inorganic-organic material based on siloxane-bond are introduced in chapter 2. To protect the back channel, which is sensitive to the ambient effect that contributes to degradation. The control of hydroxyl-bond inside siloxane's chemical structure is discussed and it is found that siloxane with less OH-bond shows the best result when acting as a passivation layer which results to having good transfer characteristic without a hump and excellent reliability for ΔV_{th} = 1.4 V even after PBS. Moreover, the mobility was more than 9 $cm^2 \cdot V^{-1} \cdot s^{-1}$, sub-threshold swing (*SS*) was less than 200 mV/decade, and the on-off current ratio (I_{on}/I_{off}) was larger than 10^6. The main issue of passivation is that hump effect often occurs in the I_{ds}-V_{gs} transfer characteristics which makes it a problem for many researchers to find a suitable passivation for their TFT.

This thesis concluded the key factor to reduce the hump effect on the sub-swing threshold area. The hump effect occurs by an accumulate of charges such as oxygen vacancy, hydrogen interstitials near the interface of electrode/semiconductor area which formed a parasitic charge – which turn on switching faster than the channel layer formation. A proper amount of hydroxide from the siloxane passivation layer can suppress the oxygen vacancies inside the *a*-IGZO layer after annealing, resulting in no hump effect.

In chapter 3, the analysis of the electronic properties of siloxane material was performed using the *C*–*V* method. Siloxane shows good electrical properties suitable to perform as a GI. The bottom gate TFT using SiO_2 as a GI and top gate TFT using siloxane as a GI within the same TFT were compared. From comparisons of the electrical characteristics, it was found that *a*-IGZO TFT using siloxane as a GI had a very high

mobility of 38.09 $cm^2 \cdot V^{-1} \cdot s^{-1}$, V_{th} = 3.21 V, *SS* = 0.16 V/dec, $I_{gs} = 5.0 \times 10^{-10}$ A, I_{on}/I_{off} was about 10^6, and without a shift of hysteresis, which gives better results compared with a traditional SiO_2 GI. The key factor to improve those electrical characteristics and stability is also a hydroxide from the siloxane layer that diffuses to the *a*-IGZO layer lowering the oxygen vacancy, increasing the carrier path, and lowering the trap density. This siloxane GI will be a good candidate for the solution processed TFT research field.

In chapter 4, I combined the knowledge of study in previous chapters together with utilizing the UV treatment to fabricate an all-solution processed oxide TFT. Especially the TFT of this work will not include any metal electrodes. By selected *a*-IZO semiconductor to make a semiconductor/conductor within the same layer to reduces the fabrication step and the contact resistance in the interface of electrodes/semiconductor problem.

The fabrication of this TFT is very simple, fewer process steps, and fast by using just only spin-coating and patterning by UV-lithography finalize by UV treatment with low temperature at 115°C within 15 minutes. The electrical characteristic results proved that this TFT can be operated with extremely high μ of 8.02 $cm^2 \cdot V^{-1} \cdot s^{-1}$, V_{th} was 3.70 V, *SS* was 320 mV/decade, and I_{on}/I_{off} was ~10^7, which are comparable with vacuum processed *a*-IZO TFT. The key to making this TFT turn on switching without any metal electrodes is to increase the oxygen vacancy in the selected area to act as a source, drain, and gate electrode. In fact, it is possible to use other treatment instead of UV treatment such as plasma treatment or ELA, but more complicated fabrication and costly process are required in this method.

Successfully operating all-solution processed oxide TFT without any metal electrodes demonstrates the high quality and high performance suitable for future flexible

and wide area device application with low cost but still enhancing the electrical characteristics.

5.2 Suggestions for future work

The most important result obtained in this study comes from the understanding of defect and element control in the important area of the TFT. The hydroxyl groups from the external source of the channel layer such as from passivation or GI are effective to improve the quality of semiconductor layer, resulting in the improvement of the electrical characteristics. However, there are still challenges and problems that need to be improved. The following are suggested as future work.

1. Reliability improvement of all-solution processed oxide TFTs

This thesis shows the first step of all-solution processed TFTs which truly reduces the cost while still enhancing the TFT performance. However, the main issue about the degradation of this TFT still needs to be solved. Optimization of the all-solution processed TFT's parameter is an important factor such as adjusting the properties of oxide semiconductor from the initial precursor, adjusting the chemical structure of the GI materials, or optimizing the suitable temperature and time for a UV treatment that will make a better film quality. In another way, finding an alternative method to increase the oxygen vacancy inside the oxide electrodes area such as ELA method. However, the reliability should be investigated using stress measurements under various atmospheres and temperatures.

2. Study of the oxygen vacancy movement

The presence of oxygen vacancy is a critical issue for all oxide semiconductor materials. To control the TFT degradation or improve the conductivity of the oxide semiconductor, the movement of the oxygen vacancy also needs to be understood, which has not been clarified yet. A simulation technique such as Atlas or COMSOL could be useful in this study. With this study, more understanding of a degradation mechanism of the oxide TFT will be demonstrated.

3. Development of low temperature all-solution processed TFTs

Fabrication of a high-performance all-solution processed oxide TFTs was successful in this thesis. However, the maximum temperature is still too high (300 °C), which is not suitable for most plastic or flexible substrates. Investigation of low-temperature TFT is needed in this case. The development should start from the initial precursor of both channel and gate insulator material especially the possibility to crosslink or alloy under low temperature. The other way is using UV/O_3 treatment with the optimized condition to rearrange the formation of the chemical structure that can help to form a solid film easier under low temperature.

This study will step forward the fabrication of oxide TFTs with a flexible substrate that revealed the possibility of the true high-performance flexible oxide TFT fabricated by an all-solution process. However, the TFT needs to be tested by the bending test to confirm the flexibility and performance of TFT under the bending condition, since this was a preliminary study from the perspective of flexible electronics. Further study is required to obtain better electrical characteristics for TFTs fabricated using an all-solution process.

List of publications

A. Academic journals

1. Chaiyanan Kulchaisit, Yasuaki Ishikawa, Mami N. Fujii, Haruka Yamazaki, Juan Paolo Soria Bermundo, Satoru Ishikawa, Takaaki Miyasako, Hiromitsu Katsui, Kei Tanaka, Ken-ichi Hamada, Masahiro Horita, and Yukiharu Uraoka, "Reliability Improvement of Amorphous InGaZnO Thin-Film Transistors by Less Hydroxyl-Groups Siloxane Passivation", Journal of Display Technology, Vol. 12, No. 3 (2016).

Presented Works

A. Presentations at domestic conference

[1] **Analysis of Degradation Mechanism on Bottom Gate Amorphous InGaZnO Thin-Film Transistors with Siloxane Passivation Layer**, **Chaiyanan Kulchaisit**, Yasuaki Ishikawa, Yoshihiro Ueoka, Juan Paolo Bermundo, Masahiro Horita, and Yukiharu Uraoka, The 2014 Japan Society of Applied Physics, Aoyama Gakuin University, Kanagawa, Japan, 2014/ 03 [Oral].

[2] **Analysis of Oxygen vacancies in the Interface of amorphous InGaZnO / Siloxane passivation film by X-ray photoelectron spectroscopy**, **Chaiyanan Kulchaisit**, Haruka Yamazaki, Juan Paolo Bermundo, Mami Fujii, Masahiro Horita, Yasuaki Ishikawa, and Yukiharu Uraoka, The 2015 Japan Society of Applied Physics, Shonan campus, Tokai University, Kanagawa, Japan, 2015/ 03 [Oral].

[3] **Defect Analysis of Siloxane Gate Insulator and its Interface in *a*-IGZO Thin-Film Transistor**, **Chaiyanan Kulchaisit**, Juan Paolo Bermundo, Mami Fujii, Yasuaki Ishikawa, and Yukiharu Uraoka, The 2016 Japan Society of Applied Physics, Pacifico, Yokohama, Japan, 2017/ 03 [Oral].

B. Presentations at international conference

[4] **Reliability of Bottom Gate Amorphous InGaZnO Thin-Film Transistors with Siloxane Passivation Layer**, **Chaiyanan Kulchaisit**, Mami Fujii, Yoshihiro Ueoka, Juan Paolo Bermundo, Masahiro Horita, Yasuaki Ishikawa, and Yukiharu Uraoka, The 2014 International Meeting for Future of Electron Devices, Ryokoku University Avanti Kyoto Hall, Kyoto, Japan, 2014/ 06 [Oral], [Best paper award].

[5] **Improvement of the Reliability of Bottom Gate Amorphous InGaZnO Thin-Film Transistors with Siloxane Layer**, **Chaiyanan Kulchaisit**, Mami Fujii, Haruka Yamazaki, Juan Paolo Bermundo, Masahiro Horita, Yasuaki Ishikawa, and Yukiharu Uraoka, The 11th International Thin-Film Transistor Conference, Rennes, France, 2015/ 26 [Poster].

[6] **Reliability Improvement of Amorphous InGaZnO Thin-Film Transistors by Less Hydroxyl-Groups Siloxane Passivation**, **Chaiyanan Kulchaisit**, Yasuaki Ishikawa, Mami N. Fujii, Haruka Yamazaki, Juan Paolo Bermundo, Satoru Ishikawa, Takaaki Miyasako, Hiromitsu Katsui, Kei Tanaka, Ken-ichi Hamada, Yukiharu Uraoka, The 22nd International Display Workshops, Otsu, Japan, 2015/ 09 [Poster], [Outstanding Poster Paper Award].

[7] **High Performance Siloxane Hybrid Polymer Gate Insulator for Amorphous InGaZnO Thin-Film Transistors**, **Chaiyanan Kulchaisit**, Yasuaki Ishikawa, Mami N. Fujii, Haruka Yamazaki, Juan Paolo Bermundo, Yukiharu Uraoka, The 16th International Meeting on Information Display, ICC Jeju, Jeju Island, Korea, 2016/ 08 [Oral].

[8] **Performance Improvement of top gate a-InGaZnO TFTs with Siloxane Gate Insulator by UV-Ozone and Thermal treatment**, **Chaiyanan Kulchaisit**, Juan Paolo Bermundo, Mami N. Fujii, Yasuaki Ishikawa, Yukiharu Uraoka, International Conference on Flexible and Printed Electronics, Yamagata University, Yonezawa City, Yamagata, Japan, 2016/ 09 [Poster].

[9] **Effect of UV/Ozone Treatment on Self-Aligned InZnO Thin-Film Transistors towards an All-Solution Process**, **Chaiyanan Kulchaisit**, Juan Paolo Bermundo, Mami N. Fujii, Yasuaki Ishikawa, Yukiharu Uraoka, Materials Research Society Fall Meeting and Exhibit, Hynes Convention Center, Boston, MA, USA, 2017/ 10 [Poster].

Supplements

Acknowledgements

After studying for five years at NAIST: writing this thank note is my impression throughout this final dissertation. It has been a long period of great learning for me, not only in the study life but also in my personal life. Writing this dissertation has had a big impact on me. I would like to reflect on the people who have supported and helped me all over this period.

Foremost, I would like to express my sincere gratitude to my principle supervisor Prof. Yukiharu Uraoka for his kind encouragement, motivation, continuous guidance, great advice, and continuous support of my Ph.D study and related research. I am very indebted to him that gives an opportunity to me for study in this institute.

I would like to thank my supervisor members, Assoc. Prof. Fumihiko Matsui and Prof. Shun Hirota, for their supervision, insightful comments, critical advice, suggestions, and encouragement.

I wish to thankful Associate Prof. Yasuaki Ishikawa for the guidance, immense knowledge, great vision, valuable advice, brilliant comments, and suggestions. And I also owe a deep sense of gratitude to Assistant Prof. Mami N. Fujii and Assistant Prof. Juan Paolo Soria Bermundo for their timely suggestions with kindness, helpful discussions, and valuable advice. Their advice helped me in all the time of research and writing of this dissertation.

I also indebted to Assistant Prof. Masahiro Horita, Assistant Prof. Mutsunori Uenuma, Ms. Ryoko Miyanaga, Mr. Hirotoshi Kawahira, and Mr. Akio Watanabe for their advice and technical help.

I would like to express my deepest appreciation to our collaborators: Mr. Satoru Ishikawa, and members from JSR Corporation, and Mr. Shinichi Maeda, and members from Nissan Chemical. I also would like to express my appreciation of Mr. Noritaka Koike, Mr. Kazuhiro Miyake and Mr. Yasuo Okajima for technical help, Ms. Yukiko Morita, and all international affair staffs for wonderful help and support of my study and daily life.

I would like to thank my TFT group members, Ms. Kaori Kise, Mr. Michael Paul, Ms. Hiromi Okada, Mr. Kenta Komori, Ms. Dianne Corsino, Mr. Yoshitaka Watanabe, and Ms. Aimi S. Safaruddin for being a great teammate, helpful discussions, and grateful help. I also would like to thank all of my Information device science laboratory members for helpful discussions, supports, friendship and help me to improve my Japanese skill.

Last but not the least, words cannot express how grateful I am to my family, Ms. Midori Emori and all of my friends for supporting me spiritually throughout writing this thesis and encourage me throughout my life in general.

March, 2018

Chaiyanan KULCHAISIT