High Performance TFT Technologies for the AM-OLED Display Manufacturing

December 2016

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Abstract

An active-matrix organic light-emitting diode (AM-OLED) display has superior features such as high contrast ratio, high response speed, thin shape and light weight; however, it also has some issues to be solved. The improvements of the luminous efficiency and the life-time are the issues for the organic electroluminescence device, and the improvements of the stability, the mobility, and the manufacturing cost are the issues for the thin-film transistor (TFT) device.

In this study, a micro-crystalline silicon TFT and an oxide TFT are extracted to realize low cost, substrate-size-scalable manufacturing like the a-Si (amorphous-Silicon) TFT and highly stable, high mobility device like LTPS (Low Temperature Poly Silicon) TFT. In the case of micro-crystalline silicon TFT, the process flow of the a-Si TFT manufacturing was followed to achieve low cost manufacturing. And the new indirect laser annealing technique using Mo-capped silicon precursor and a stable continuous wave (CW) laser are adopted to realize small grained uniform crystallization and uniform and stable TFT characteristics. In the case of oxide TFT, the low cost manufacturing is also achieved by using the scalable and efficient production tools which are commonly used in the a-Si TFT manufacturing. And the adopted AlOx passivating film prevents from the water and hydrogen diffusion, which degrades the TFT characteristics, and realizes stable TFT characteristics. In addition, a newly proposed self-aligned top-gate TFT structure with low parasitic capacitance achieved the high resolution, high frame rate AM-OLED display driving.

These TFTs have mobilities of 3.1 cm^2/Vs and 9.8~30.9 cm^2/Vs for micro-crystalline silicon TFT and oxide TFTs, respectively. And the long lifetime over 10 years were estimated for AM-OLED display by the results of bias temperature stress tests. Using these TFTs, the AM-OLED display prototypes were fabricated and demonstrated the utility. A flexible panel and a transparent panel were also fabricated and demonstrated in order to utilize the low temperature nature of the oxide TFT manufacturing process and the transparent feature of the oxide semiconductor materials.

Both TFTs can be chosen for the AM-OLED display manufacturing according to the manufacturing environment or the required specifications of the panel. I hope that this thesis contributes to the diffusion of the AM-OLED display into the market.

Contents

Chapter 1 General introduction

1-1. AM-OLED display

The information display has been widely used for the electric devices since the spread of the cathode ray tube (CRT). In the early 1990's, the trend of the information display has dramatically changed from the cathode ray tube (CRT) to the flat panel display (FPD). Several display modes were proposed for FPD, and the active matrix-liquid crystal display (AM-LCD) led the change owing to its image quality and its simple manufacturing method. In 2000, an LCD has become a majority in the information display; however, all of its specification is not satisfied and several other technologies have also been developed.

As the image quality, there are several major factors to be required by the customers.

1. Uniformity (Mura, cross talk, sticking)
2. Stability
3. Size & resolution
4. Color reproduction (color gamut, gray scale)
5. Brightness (peak luminance)
6. Contrast ratio (black)
7. Response time
8. Viewing angle

In addition, there are several important factors for the customers besides of image quality.

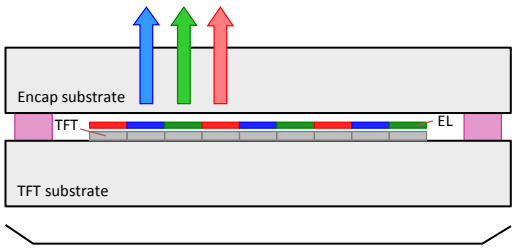
9. Power consumption
10. Cost (material cost, productivity, yield rate)

The image quality of the LCD became fine for these several years; however, its color reproduction, contrast, viewing angle, and response time still have room to be improved.

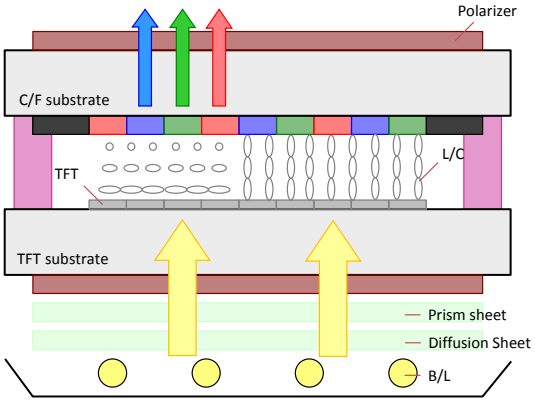
In 1987, C. W. Tang reported the organic light-emitting diode (OLED) device with high luminous efficiency (1.5 lm/W), and brightness (>1000 cd/m^2) [1]. After this report, many researchers studied the OLED device for a display [2, 3, 4, 5]. An OLED device has high color gamut, high contrast ratio, wide viewing angle, and quick response. These characteristics are suitable for the information display, and also are the

negative points of LCD. Therefore, an OLED display comes to be expected as an information display.

Fig. 1 shows the structures of an OLED display and a LCD. A LCD consists of a liquid crystal cell with a thin-film transistor (TFT) substrate, a color filter (CF) substrate, some optical films including two polarizers, and a backlight module. A liquid crystal cell just acts as an optical switch, therefore, a backlight module as a light source and some optical films to realize uniform luminance are necessary. On the other hand, an OLED is the self-emitting device, and can achieve a very simple structure. This simple structure contributes to the light weight devices or the flexible devices by changing the glass substrates to the flexible substrates.



(a) OLED display



(b) LCD

Fig. 1 Cross-sectional structures of (a) OLED display and (b) LCD.

The development of OLED display was extensively from 1990 's, and the small size AM-OLED displays started to be commercialized from the beginning of 2000's (Fig. 2 (a), (b)) [6, 7]. The medium-large size AM-OLED displays including the use for televisions also started to be commercialized form the 2nd half of 2000's (Fig. 2 (c), (d)) [8, 9].

(a) Kodak/Digital Camera: “LS-633” [2.16 inch 521x218 pixels] [6].

(b) SONY/PDA: “VZ-90” [3.8 inch qVGA] [7].

(c) SONY/TV: “XEL-1” [11” qHD] [8].

(d) LG Electronics/TV: “55EM970” [55 inch FHD] [9].

Fig. 2　Commercialized AM-OLED displays.

In recent years, the image quality of the OLED display has been improved dramatically, and has come to be preferred by the whole customers compared with that of a LCD. And then, the interest of customers has moved to the power consumption and the cost. The power consumption has been reduced gradually year by year by the improvement of the OLED materials or the device structure. For the cost improvement, the low cost materials, the low cost manufacturing processes / equipment, or the low cost simple device structures have been studied. Especially, the low cost TFT device which takes the place of LTPS TFT has been expected.

1-2. TFT device

To drive the active matrix OLED (AM-OLED) display, thin film transistor (TFT) is used as a switching device. In the case of AM-LCD, amorphous silicon (a-Si) is widely used as a channel material of the TFT because of its high productivity. However, for the AM-OLED display, a-Si TFT has disadvantage in the field effect mobility and the stability, and is hard to be used. Because the OLED is a current-driven device, high current flow is required for the TFT to realize high luminance. In case of the a-Si TFT, high bias is applied to the TFT to realize high current flow, and the threshold voltage of the TFT easily shifts due to the bias temperature stress, which is continuously applied during the driving period. Therefore, other TFTs with higher mobility and more stable channel materials have been proposed (Table 1) [10]. A low temperature poly Si (LTPS) including a solid phase crystalized Si (SPC-Si) is a good candidate especially in stability; however, its low productivity owing to its long manufacturing steps is a serious issue. The manufacturing of LTPS TFT requires a lot of manufacturing apparatus and a lot of materials, so the initial investment and the manufacturing cost are much higher than other TFTs. Moreover, the manufacturing of LTPS TFT requires special apparatus such as excimer laser annealing (ELA), ion doping, and high temperature annealing apparatuses in the Si crystallization, ion doping, and activation processes. These apparatuses have demerits in not only expensive, but also having restrictions in the size of the glass substrates which can be used.

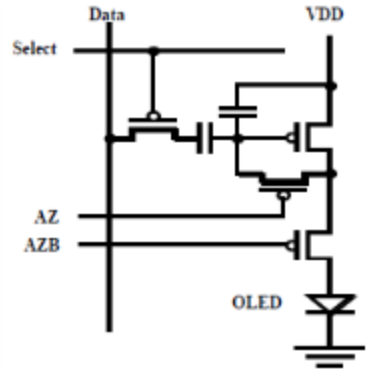
Table 1 TFT candidates for AM-OLED display [10].

Channel material	a-Si	μc-Si	SPC-Si	LTPS	Oxide
Field effect mobility [cm^2/Vs]	0.5	2~5	~50	~150	10~50
Stability	Low	Med.~High	Med.	High	Low→High
Uniformity	Good	Good	Fair	Fair	Good
Productivity	High	Med	Low	Low	High
Plate size	Gen.10 (3.1×2.8m)	Gen.10	Gen.6 (1.8×1.5m)	Gen.6	Gen.10
Mask number (for TFT only)	5	6	7 ~ 10	7 ~ 10	4 ~ 5

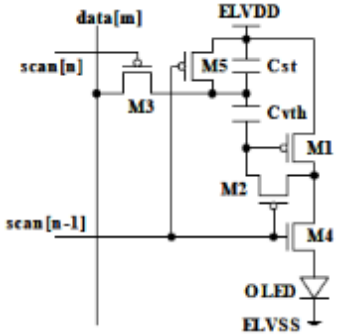
In this thesis, I propose a micro-crystalline silicon (μc-Si) TFT and an oxide TFT as the driving device for the AM-OLED display. When applying to the production, both TFTs have some advantages. In the following chapters, the development results of the both TFTs are reported.

1-3. Compensation circuit

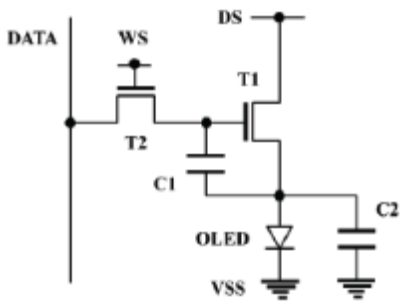
To drive the AM-OLED display, several thin film transistors are required for the pixel circuit. Dawson's team reported a voltage programed compensation pixel circuit in 1998-1999 [11, 12, 13]. This circuit is composed of four transistors and two capacitors (4Tr2C), and compensates the threshold voltage variation in a panel (Fig. 3 (a)). After this report, many compensation circuits were reported to compensate the threshold voltage variation of TFTs [14, 15, 16]. Fig. 3 (b) [15] and (c) [16] shows the examples of compensation circuits. And, Table 2 shows the comparison of the component number and the compensation target of those compensation circuits.



(a) 4Tr2C circuit [11, 12, 13]



(b) 5Tr2C circuit [15]



(c) 2Tr2C circuit [16]

Fig. 3 Schematics of the compensation circuits.

Table 2　Compensation circuits and the number of components.

Number (/sub pixel)	(a) 4Tr2C	(b) 5Tr2C	(c) 2Tr2C
Transistor	4	5	2
Capacitor	2	2	2
Horizontal line	3	3	2
Vertical line	1	1	1
Compensation target	Vth	Vth	Vth and Mobility

All of the compensation circuit is more complicated than the pixel circuit of the LCD. To realize the high resolution display with high manufacturing yield, a simpler circuit is preferable. This submitted 2Tr2C compensation circuit would be the most preferable due to its simple composition from the manufacturing point of view.

Fig. 4 shows the timing diagram and the operation diagrams of the 2Tr2C compensation circuit [16]. Here, DS controls the light emitting period. WS is the gate pulse of T2 (write scan transistor) for controlling the write and cancel operations. DATA is the signal pulse of the WS transistor and takes two data voltages; Vofs or Vsig. Vofs is a constant reference voltage for compensating variations in Vth of T1 (drive transistor). Vsig is the signal voltage that is correlated with the luminescence of each pixel. According to this operation, the gate bias Vg (Drv. Tr Gate) and the source bias Vs (Drv. Tr Source) of T1 are controlled to compensate the Vth and mobility variation of T1, and the emitting current (I_{OLED}) flows to the OLED device.

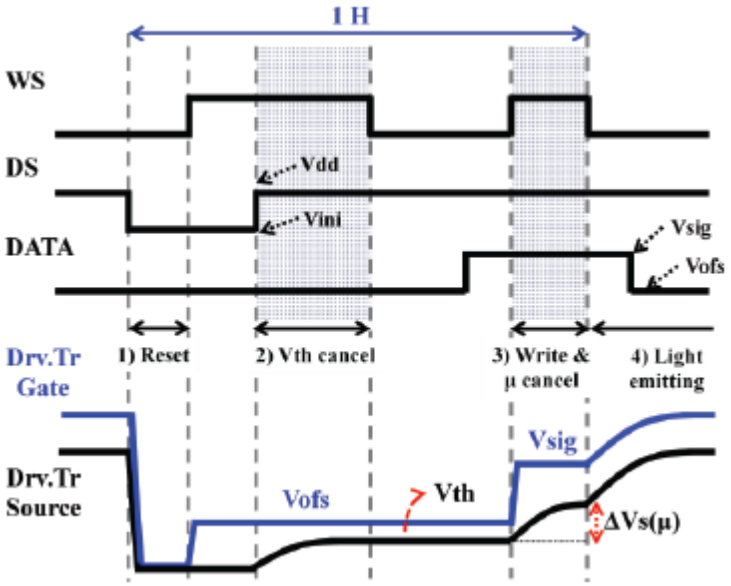
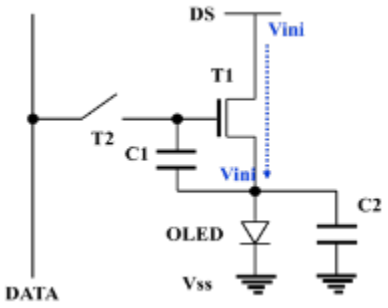


Fig. 4　Timing diagram of the 2Tr2C compensation circuit [16].

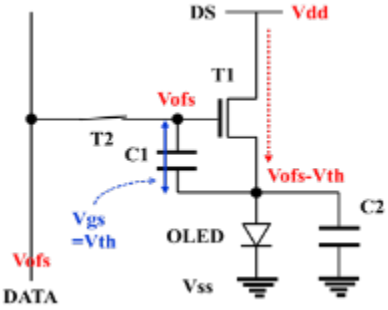
Fig. 5 shows the operation diagrams of the 2Tr2C compensation circuit [16]. Here, a driving operation is illustrated by following four operations.

1) Reset operation: The DS line converts a positive supply voltage (Vdd) to the initial voltage (Vini). Vini can be set to a low voltage in order to completely turn off the OLED device.
2) Vth compensation operation: When T2 is turned on, Vofs is applied to the gate node of T1 from the DATA line. Then, the DS line changes to Vdd from Vini, and T1 is turned on in the saturation region. Since the driving current flows to the OLED device, the source node of T1 gradually increases and the driving current decreases. Finally, the source node reaches Vofs−Vth, and T1 is then turned off. Consequently, the Vth of T1 is stored in C1 after WS is turned off.
3) Write and mobility compensation operation: The DATA line changes to Vsig from Vofs. When T2 is turned on again, Vsig is applied to the gate voltage of T1 from the DATA line and T1 is turned on again. The source voltage increases when WS is high. As a result, the source node increases by $\Delta Vs(\mu)$. Since Vth compensation has previously been accomplished, $\Delta Vs(\mu)$ approximately depends on the mobility of T1, and the mobility variations of T1 can be controlled.
4) Light emitting operation: When T2 is turned off, the gate-source voltage (Vgs) of T1 is stored in C1. The value of Vgs is given by $Vsig-Vofs+Vth-\Delta Vs(\mu)$. The emitting current (Ioled) flows to the OLED device. The gate and source voltages of T1 both increase with maintaining the Vgs of T1. Finally, the source voltage reaches the emission voltage (Voled).

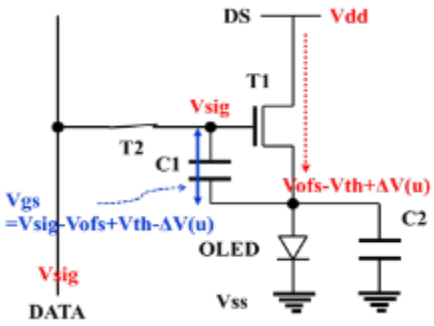
As a result, this pixel driving method automatically compensates the threshold voltage and the mobility through the 3rd and 4th of the four operations.



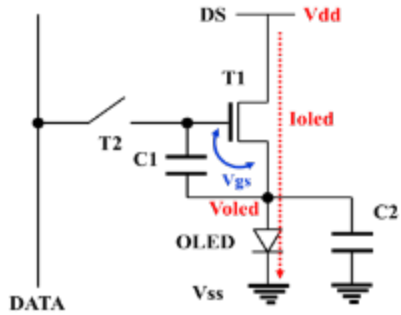
(1) Reset



(2) V_{th} compensation



(3) Write and mobility compensation



(4) Light emitting

Fig. 5 Operation diagrams of the 2Tr2C compensation circuit [16].

According to the above operations compensating both threshold voltage and mobility, I_{OLED} is given by the following equation.

$$I_{OLED} = \frac{1}{2} k\mu(\mathrm{Vgs} - \mathrm{Vth})^2 = \frac{1}{2} \mathrm{k}\mu(\mathrm{Vsig} - \mathrm{Vofs} - \Delta\mathrm{Vs}(\mu) - \mathrm{Vth})^2$$
$$= \frac{1}{2} \mathrm{k}\mu(\mathrm{Vsig} - \mathrm{Vofs} - \Delta\mathrm{Vs}(\mu))^2 \quad (1)$$
$$\left(\mathrm{k} = \frac{\mathrm{W}}{\mathrm{L}} \mathrm{Cox}\right)$$

(μ : field effect mobility, ΔVs(μ): bias shift according to the mobility, W: channel width of the TFT, L: channel length of the TFT, Cox: capacitance of the gate insulator)

This equation implies that the variations of both Vth and the mobility of T1 are canceled out. Consequently, the 2Tr2C pixel circuit enables a highly uniform pixel-to-pixel luminance to be realized despite its tiny size.

This operation is to link the gate potential Vg of the drive transistor with the source potential Vs according to the charge up operation by T2 into the storage capacitor C1, so is called a boot strap operation. The ability of the bootstrap operation is called a bootstrap gain (Gb), and is expressed by the following equation [17].

$$\mathrm{Gb} = \mathrm{Cs}/(\mathrm{Cs} + \mathrm{Cw} + \mathrm{Cp}) \quad (2)$$

Here, Cs is the capacitance of the storage capacitor C1, Cw is the capacitor between gate and source nodes of the write scan transistor, and Cp is the parasitic capacitor between gate node of the drive transistor and the other structurally nearby nodes. The bootstrap gain Gb closer to one means a higher gain Gb. That is, the gain Gb closer to one means that the ability for correcting the drive current of the drive transistor and the emitting current of the OLED device I_{OLED}.

To realize higher Gb, it looks easy to prepare large Cs; however, larger area in a pixel and much electron charge for the operation are required. It is contradictory to the high resolution or the low power consumption displays. Therefore, the reduction and the uniformalization of the parasitic capacitances (Cw and Cp) are effective to realize effective compensation driving.

1-4. EL device

Fig. 6 shows the electroluminescence (EL) device structure which C. W. Tang reported [1]. The EL materials are formed between the anode and the cathode, and the luminescent light is observed through the transparent anode. After their report, a lot of EL device structure and materials were reported, and the luminance, efficiency, and reliability have been so much improved; however the basic EL device structure does not change.

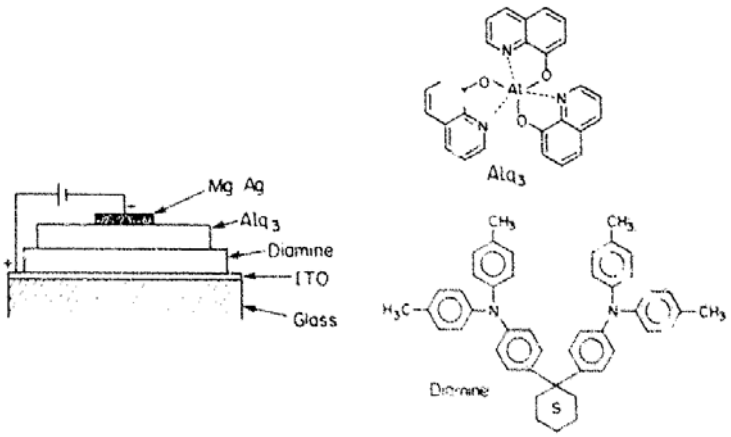
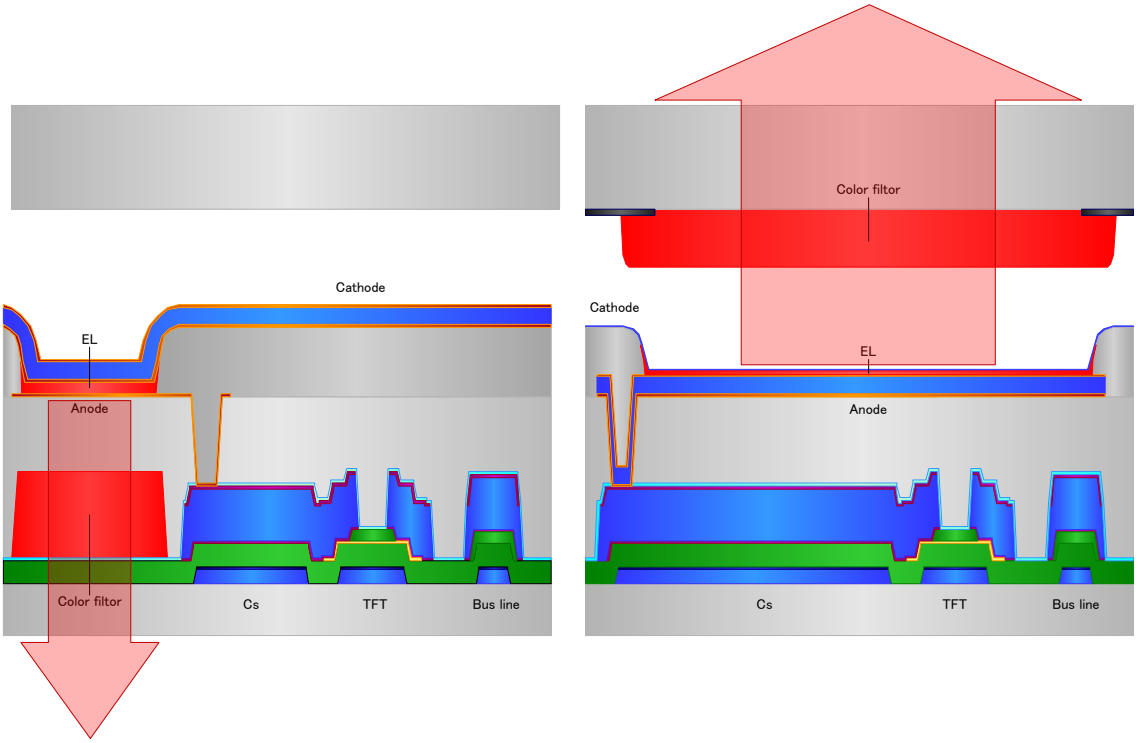


Fig. 6 EL device structure of the first report [1].

For the TFT array of the AM-OLED display, the emitting direction of the EL device is important. Fig. 7 shows two kinds of device structures with different emitting direction. A bottom emission device (Fig. 7 (a)) looks easy to fabricate because all of the devices are covered by the cathode metal which acts as a passivation; however, the EL device is formed besides TFT array, and therefore the emitting area needs to be small. On the contrary, a top emission device (Fig. 7 (b)) has a difficulty in encapping the device; however, the EL device can be formed on the TFT array, and therefore the emitting area can be large and also the storage capacitances can be designed freely. The advantages of the top emission device are as follows, for example.

- wide emission area
    - high luminescence
    - long life due to low operating bias
- free TFT array design
    - high boot strap gain by enlarging Cs size
    - high manufacturing yield by enlarging the space between lines and devices
    - long life due to low operating bias by enlarging channel width
    - uniform image due to uniform TFT current by enlarging channel length



(1) Bottom emission type (2) Top emission type

Fig. 7 Cross-sectional OLED device structures.
(The red arrow means the light emitting direction.)

As a matter of course, the top emission structure is preferable for the AM-OLED display.

1-5. Display trend

(a) Display modes

Thanks to the invention by K. F. Brown in 1897, a cathode ray tube (CRT) had been widely used as an information display, and contributed to the human life and the growth of the industry for several decades. After the invention of liquid crystal display (LCD) by G. H. Heilmeier in 1964, many researchers started the development of flat panel display (FPD). In 1990, the mass-production of color LCD was started and the developments of many types of FPDs were accelerated in the world. Table 3 shows the features of the developed FPDs. As the early TN (Twisted Nematic) mode LCD had serious issues in viewing angle and response time, other LCD mode such as VA (Vertical Alignment) , IPS (In-Plane Switching), or OCB (Optically Compensated Bend) modes were developed. Furthermore, other display modes were also developed to realize better image quality or expand the range of FPD applications. The field emission display (FED) and surface-conduction electron-emitter display (SED) were good candidates to realize quick response; however, those mass-production were not successful due to those production difficulty. The plasma display panel (PDP) was ever used as TV positively from late 1990's to early 2000's; however, it went out of production due to the difficulties in the power consumption, the panel resolution or the manufacturing cost.

Table 3 Features of FPDs.

Dsiplay mode / Characteristics	LCD			FED	SED	PDP	EPD	OLED
	TN	VA, IPS	OCB				MC	
Resolution	Excellent	Excellent	Excellent	Good	Good	Poor	Excellent	Good
Color reproduction	Fair	Fair	Fair	Good	Good	Good	Poor	Excellent
Brightness	Good	Good	Good	Good	Good	Good	Poor	Good
Contrast	Poor	Poor	Poor	Good	Good	Good	Poor	Excellent
Response	Poor	Poor	Fair	Excellent	Excellent	Good	Poor	Good
Viewing angle	Poor	Fair	Fair	Good	Good	Good	Good	Good
Power consumption	Good	Good	Good	Fair	Fair	Poor	Excellent	Fair

* TN: Twisted nematic LC
VA: Vertical align. LC
IPS: In-plane switching
OCB: Optically compensated bend
MC: Micro capsule (eINK)

(b) LCD vs. OLED display

At this moment, the use of LCD is dominant in the information display; however, the OLED display is expected to be replaced with the LCD due to its superior features such as high color reproduction, high contrast, or quick response features. Furthermore, its thin device structure without back-light systems is expected for the

thin, light weight and flexible display. The new production technologies for the thin, light weight, or flexible displays are also required.

1-6. Requirements for TFT device to drive AM-OLED display

In order to design, drive, and maintain the function of the active matrix flat panel display (AM-FPD), there are several requirements for the properties of the TFT device. Here I pick up several important factors, which are required for the AM-OLED manufacturing, and discuss the causes why high performances are required and the level to be required.

(a) Reliability

The performances of the TFT often degrade by various stresses. In general, the degradation due to the bias temperature stress (BTS), the hot carrier injection (HCI), the time dependent dielectric breakdown (TDDB), and the stress migration (SM) are well known. Especially, the positive bias temperature stress (PBTS) and the negative bias temperature stress (NBTS) instabilities are the most remarkable issues for the TFT. For example, a threshold voltage (Vth) of the TFT shifts due to the generated interface traps by the applied bias. In the case of the oxide TFT, the humidity temperature stress (THS) instability and the negative bias and illumination stress (NBIS) instability are also remarkable issues, because the electrical property of the metal oxide often changes by the humidity and the short wavelength light illumination.

When designing the display, certain degradation is assumed to be; however, there is a merit to become lower power consumption or longer life time if the lower bias setting can be achieved by the low-degradation device. Therefore, the highly reliable TFT is expected.

(b) Uniformity

The uniformity of the TFT performance is important even in the case of using compensation circuit. The non-uniformity can be classified into the wide range non-uniformity and the short range non-uniformity. The wide range non-uniformity is mainly caused by the plasma or thermal non-uniformity of the manufacturing apparatuses, and the adjustment of facilities and the adjustment of the process conditions are important. On the other hand, the short range non-uniformity is caused by the especial reasons. Especially, when the characteristics of the TFTs suddenly change on a line, that line can be assumed as a Mura.

In the case of LTPS TFT, the TFT characteristics change on a line because of the excimer laser annealing (ELA) process, and it is confirmed as a Mura in the AM-OLED display. The ELA system employs a step-and-repeat crystallization process using a narrow width laser (Fig. 8), and TFT characteristics change due to the variation

of the crystallization ratio or the crystal size. To avoid this Mura, other crystallization processes have been proposed.

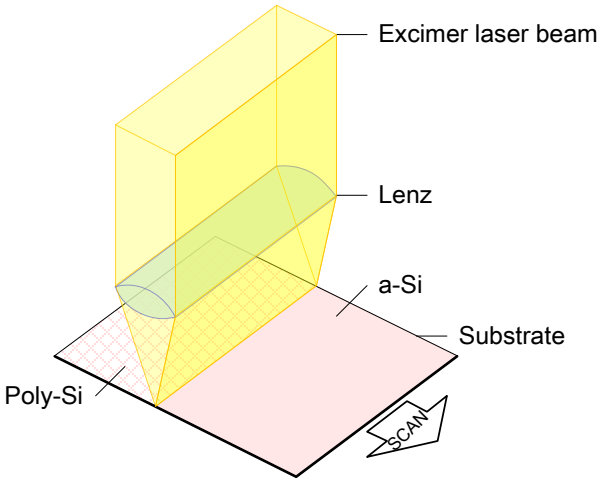


Fig. 8　ELA system and Si crystallization.

In the case of using a stepper apparatus in the photo-lithography process, the Cgs (: capacitance between gate and source) and Cgd (: capacitance between gate and drain) change near the stitching line due to the magnification error or the rotation error of the Mask (Fig. 9), and it is confirmed as a Mura. If the Cgs differs, the compensation ability differs. To avoid this Mura, self-alignment techniques have been proposed between gate and source/drain patterning.

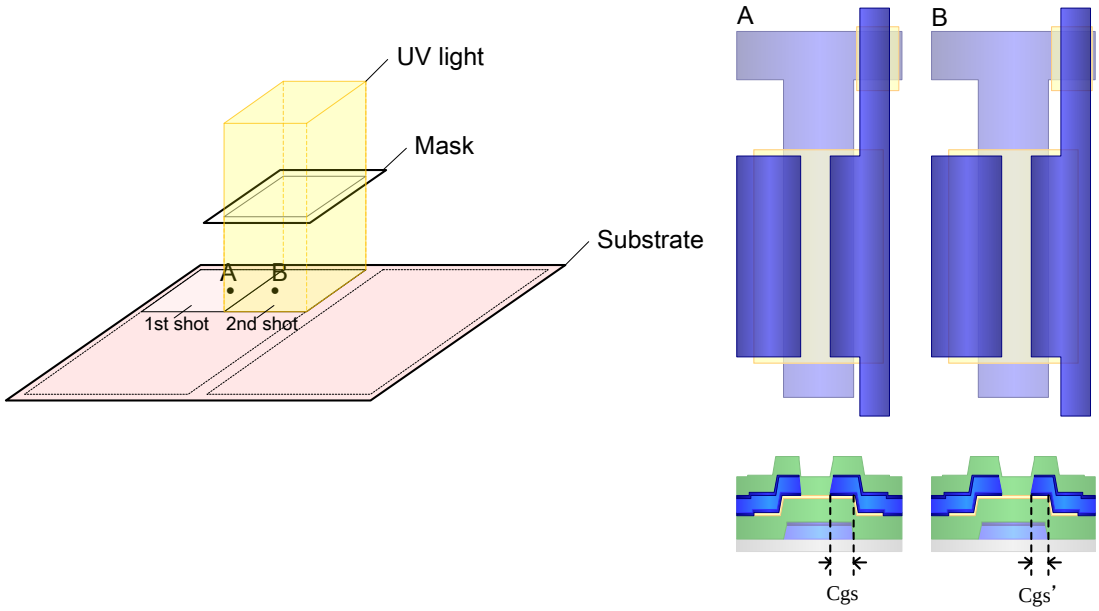


Fig. 9　Stepper process and the Cgs difference.

(c) Mobility

For the TFTs, high mobility is also required to drive the compensation circuit. This is because the write scan TFT needs to charge up to the storage capacitor and write a Vth compensated bias for the drive scan TFT. Fig. 10 shows the required mobility for each resolutions and frame rates in case of applying a conventional etching stopper type bottom-gate TFT for the top emission type AM-OLED television (TV) [10, 18]. This is calculated under a certain condition and changes if the required specification such as the brightness or the life-time change and also the luminous efficiency of the emission material improves, for example. In case of high resolution or high frame rate display, the WS TFT has to write the required bias in a short period; therefore, high mobility is required for the WS TFT. For example, mobility higher than 8 cm^2/Vs is required for 120 Hz 4k × 2k AM-OLED displays according to this simulation.

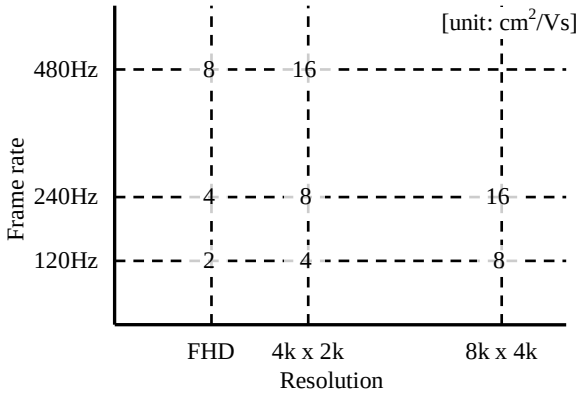


Fig. 10 Required mobility for each resolution and frame rate [10].

Moreover, it is necessary to improve the mobility of the TFT to lower the non-light emitting area around the display in the case of driver integration. However, when mobility is too high, the uniformity of the pixel transistors becomes worse and becomes a problem. Therefore, mobility from 30 cm^2/Vs to 50 cm^2/Vs would be preferable.

(d) Manufacturing cost

It is necessary to suppress the manufacturing cost to provide an AM-OLED display with a desirable panel price. The technique to reduce manufacturing cost is well studied in the manufacturing of the liquid crystal display (LCD), and following three items are important.

1. Productivity

The manufacturing easiness and the manufacturing yield are effective for the manufacturing cost. For the low cost manufacturing, the following items are effective.

- to avoid to use the low productivity apparatus.
- to avoid to use the apparatuses of high maintenance cost.
- to avoid to use high cost materials.
- to avoid to apply a process with a narrow process window.
- to avoid to apply uncontrollable process parameter.

2. Plate size

It is very effective to enlarge the plate size to reduce the manufacturing cost. By enlarging the plate size, the utilization efficiency of the materials can be improved. For example, if we use a large substrate with double length of the sides, the material consumption per area can be reduced to approximately 1/1.4. To use a large substrate, there are some difficulties such as the alignment accuracy or the film thickness uniformity; however, applying a larger plate size is effective for the low cost manufacturing.

Table 4 Substrate size for FPD manufacturing.

Generation	Plate size		Area	Area ratio (/Gen.4.5)	Operation year
	X [mm]	Y [mm]	[mm^2]		
1	300	400	120,000	0.2	1990
2	360	465	167,400	0.2	1993
3	550	650	357,500	0.5	1995
3.5	600	720	432,000	0.6	1997
4	680	880	598,400	0.9	2000
4.5	730	920	671,600	1.0	2000
5	1,100	1,250	1,375,000	2.0	2002
6	1,500	1,850	2,775,000	4.1	2003
7	1,870	2,200	4,114,000	6.1	2005
8	2,160	2,460	5,313,600	7.9	2006.8
8.5	2,200	2,500	5,500,000	8.2	2007.8
10	2,850	3,050	8,692,500	12.9	2009.1

3. Mask number

It is also very effective to shorten the process flow to reduce the manufacturing cost. Especially, the mask number reduction is most general way to shorten the process flow. To reduce the mask number, there

are some difficulties such as selective etching or double purpose use of a film; however, applying low mask number process is also effective for the low cost manufacturing.

In order to design a TFT array for AM-OLED display, it is required to consider these items to suppress the production cost.

1-7. The purpose of this thesis

The purpose of this thesis is to develop low cost, high performance TFT technology for the AM-OLED display.

Fig. 11 shows the outline of this thesis. This paper consists of four parts, and the two kinds of transistors are proposed for the backplane of AM-OLED display in chapter 2 and chapter 3.

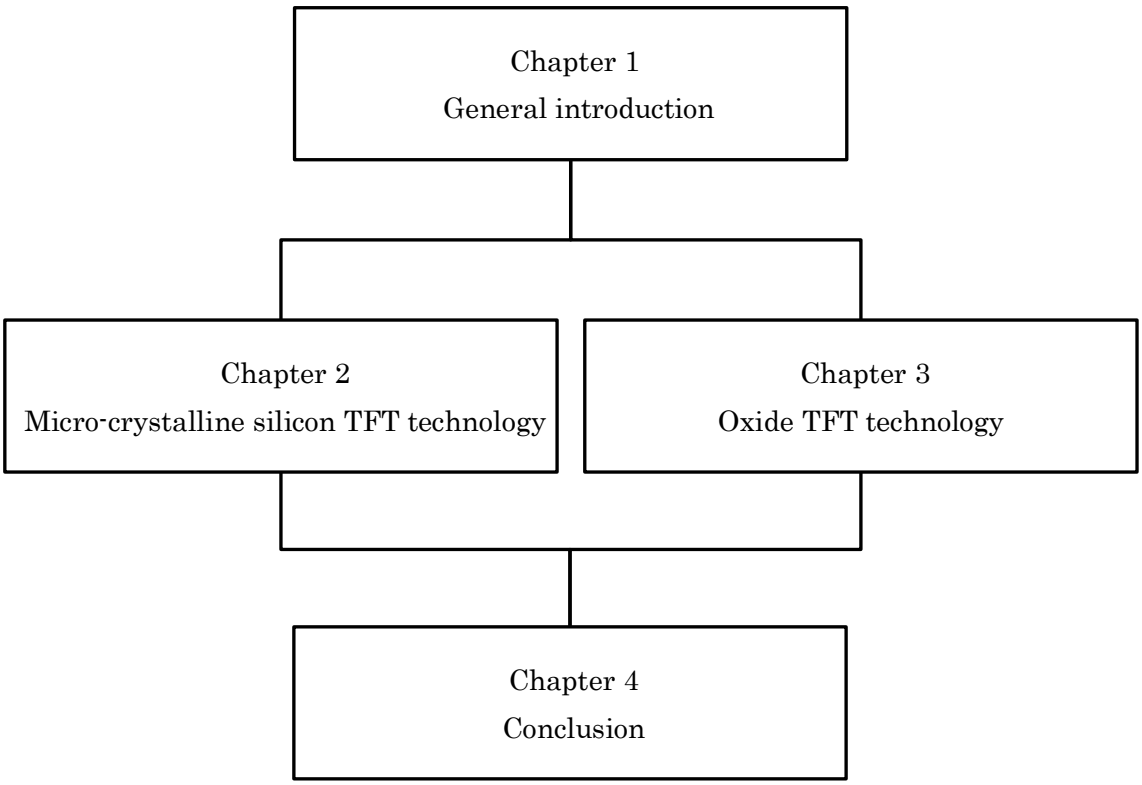


Fig. 11 Outline of this thesis

In chapter 1, the characteristics and the structural feature of AM-OLED display, the TFT candidates for driving AM-OLED display, the basics of EL device and its driving method, and the requirements for the TFT device, are described as basic knowledge.

In chapter 2, highly stable micro-crystalline silicon TFT with higher mobility than the conventional amorphous silicon (a-Si) TFT are developed using novel indirect laser annealing technique. To overcome the non-uniformity issue of the crystallized silicon, indirect laser annealing technique using Mo-capped silicon precursor and a stable continuous wave (CW) laser are adopted, and small grained uniform crystallization are stably realized. This process is realized by adding Mo-capping

process and laser annealing process to the conventional etching stopper type a-Si TFT process. It is valuable for the low cost manufacturing because of its simple process flow and the required small amount of additional investment to regenerate the conventional a-Si TFT manufacturing line.

In chapter 3, highly stable oxide TFTs with higher mobility than 10 cm^2/vs are developed. To overcome the reliability issue of the oxide TFT, alumina is adopted as a passivation and structural devices are also employed. In addition, several studies are done for

- high mobility oxide material for the gate driver integration,
- crystalline oxide material with high mobility,
- large substrate test run confirming the production applicability,
- advanced TFT structure with small parasitic capacitance,
- flexible and transparent AM-OLED displays featuring the properties of oxide TFT, and
- simplified backplane process for AM-OLED display merging S/D metal and anode metal.

As a result, a 5-Mask processed self-aligned top gate TFT is proposed as the most cost competitive, high performance TFT for the AM-OLED display.

Finally, chapter 4 summarizes the results of previous chapters, and describes the conclusions of this thesis.

Chapter 2 Micro-crystalline silicon TFT technology

2-1. Introduction

At the initial stage of the AM-OLED display, many manufacturers adopted LTPS TFT for its backplane, because the LTPS TFT is stable against high current flow and large current flow is necessary to the current-driven organic light emitting device [2, 5, 19, 20]. On the other hand, LTPS technology has demerits in production cost, the limitation in a mother glass size (< Generation 4), and the Mura caused by short-range non-uniformity of TFT performance due to the crystallization method using excimer laser annealing (ELA).

At the second stage, hydrogenated amorphous silicon (a-Si:H) TFT, which had been industrially grown as the backplane of LCD, was adopted [3, 21]. The amorphous silicon technology has advantages in production cost and the limitation in mother glass size, against the LTPS technology. However, amorphous silicon TFT has low mobility and low stability against the large current flow, which is required for the light emission of the OLED. Some manufacturers developed compensation circuit [11, 12, 13, 14, 15, 16] or fraction time negative bias driving method [22, 23, 24] to improve the stability of amorphous silicon. However, it is difficult to suppress the degradation of sub threshold slope (S) and to reset the Vth shift (ΔVth) by a certain negative bias insertion, because each pixel has different positive bias stress according to the luminance.

At the third stage, micro-crystalline silicon (μc-Si) TFT was adopted to the OLED backplane [25, 26]. By reducing the crystal size, the uniformity of the crystal seize is improved and the uniformity of the TFT characteristics is also improved. This technology has high potential to achieve low cost, high generation production and high stability, high uniformity in TFT characteristics.

However, there were several issues for the production. Especially, the stability in the formation of micro-crystalline film was the most difficult issue to be solved. A stable micro-crystalline film formation method was desired.

In this paper, a new crystallization technique using Diode Laser Thermal Annealing (dLTA) system and a low resistivity bus line technology in dLTA process are proposed for the large sized high definition TV production.

2-2. Conventional technologies

(a) PE-CVD

P. Roca's group had well established an as-deposited micro-crystalline silicon (μc-Si) technique using a conventional plasma enhanced chemical vapor deposition (PE-CVD) apparatus [27, 28]. The mobilities from 0.7 cm^2/Vs to 7.0 cm^2/Vs were obtained according to the layer-by-layer deposition technique or the fluorine and hydrogen effects. However, the deposition rates of those techniques are smaller than 0.1 nm/sec, and not suitable for the display manufacturing.

(b) Cat-CVD

A catalytic-CVD (Cat-CVD; often called Hot-Wire CVD) is an alternative technology to the PE-CVD, which is expected to overcome the issue of it [30, 31, 32]. A catalytic hot wire in a chamber improves the gas efficiency and increases the deposition rate. A micro-crystalline Si film with mobility over 10 cm^2/Vs is realized [32]. However, the catalyzers are required in a chamber and this special structure interferes in the chamber cleaning process and has a risk to increase the particles which are generated in a chamber.

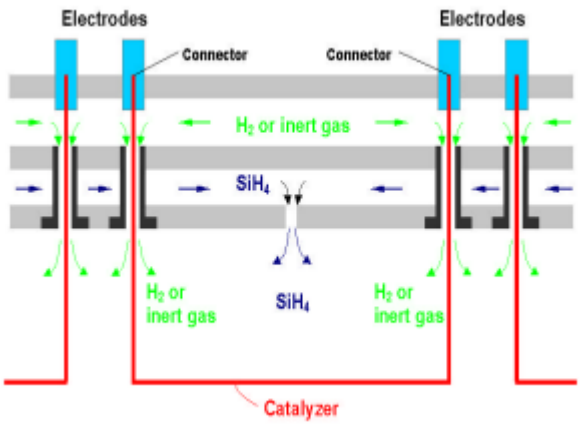


Fig. 12 Cross sectional chamber-structure of the Cat-CVD [32].

(c) ICP-CVD

An inductive coupled plasma-CVD (ICP-CVD) is also an alternative technology to the PE-CVD, which is expected to overcome the issue of it. High density plasma is generated by the inductively-coupled RF plasma source, and improves the deposition rate of the micro-crystalline silicon [33, 34]. However, it is difficult to generate high density, uniform plasma in a chamber, when the size of the chamber becomes large. A

technique to make the internal low-inductance antenna (LIA) units in a chamber was developed; however, the LIA also interferes in the chamber cleaning process and has a risk to increase the particles like CAT-CVD.

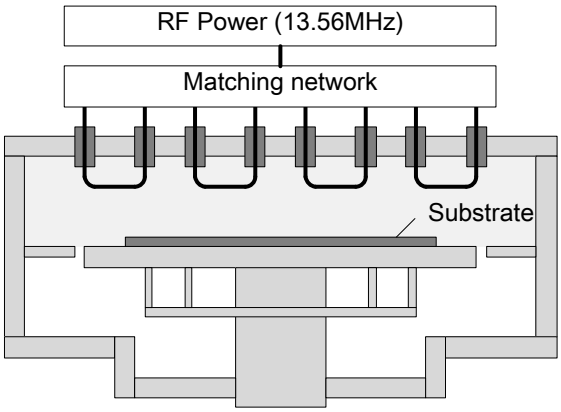


Fig. 13　Cross sectional chamber-structure of the internal LIA ICP-CVD.

(d) MSEP-CVD

To realize high density plasma, metal surface microwave excitation plasma-CVD (MSEP-CVD) is a good candidate. A rectangular shape plasma source was developed with 915 MHz microwave, and high density, low electron temperature microwave plasma was proved to form crystallized silicon without an incubation layer at the micro-crystalline Si/gate insulator interface. [35]. This plasma source is expected in the point that realized upsizing of the chamber size without the special structure in the chamber, which interferes in the chamber cleaning process. However, the mobility of the obtained micro-crystalline Si TFT (1.3 cm^2/Vs) was still low and needed to be improved.

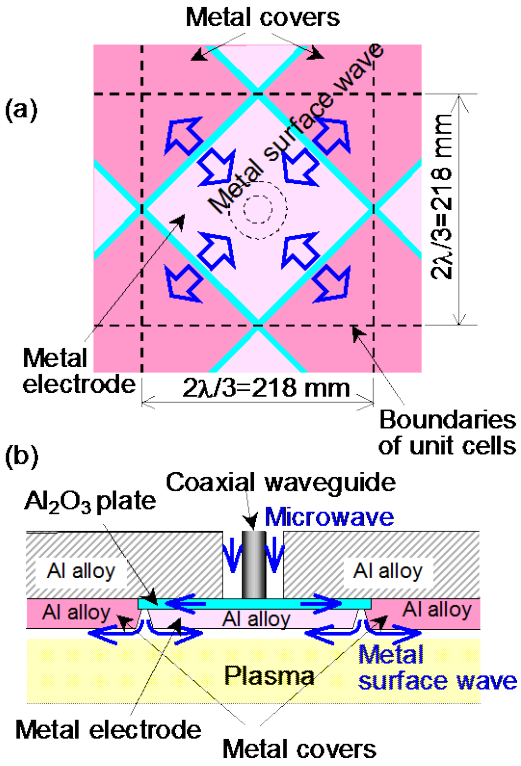


Fig. 14 (a) Bottom and (b) cross sectional chamber-structure of the MSEP-CVD [35].

(e) ELA

In the case of as-deposited micro-crystalline silicon, a stable film deposition is difficult because the initial part of the deposited film is easily affected by the chamber condition. The pre-deposited film on the surface of the chamber is supposed to be sputtered by the plasma and affects to the initial film formation. Therefore, a lot of techniques to crystallize the amorphous silicon by a laser irradiation or a thermal treatment are developed. The excimer laser annealing (ELA), which is generally used for LTPS TFT fabrication, is the most famous method for the crystallization of silicon. Fig. 15 shows the relationship between the laser power and the grain size of the crystallized silicon. When the laser power is high, the grain size becomes large and its variation also becomes large. The large variation in the grain size results in non-uniformity of the TFT characteristics and causes Mura problem in the AM-OLED display. To improve the uniformity, small grain is obtained by the low power ELA condition; however, the grain size and its variation are still large for the uniform micro-crystalline silicon formation.

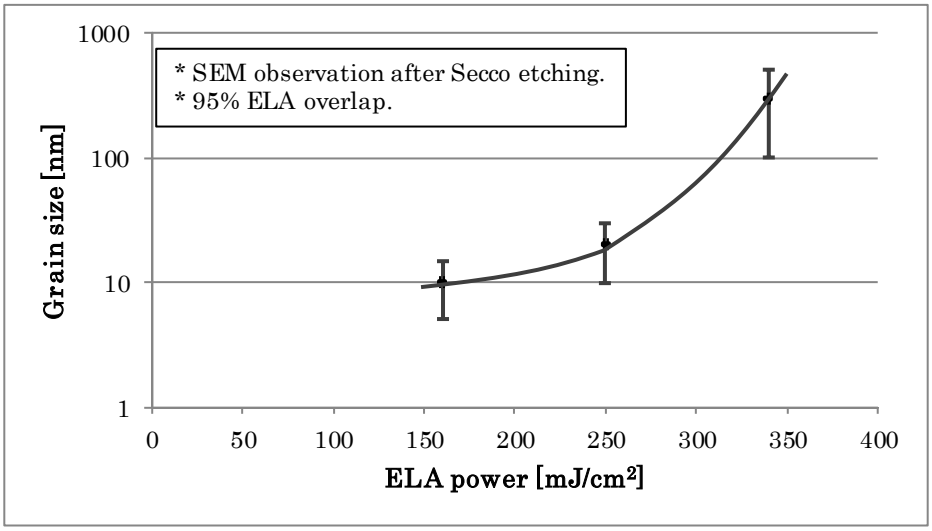


Fig. 15 Relationship between ELA power and grain size.

(f) SPC

A solid phase crystallization (SPC) technique was developed to achieve high mobility primarily by creating large size crystals; however, it can be applied for the micro-crystalline formation [25, 35, 36]. According to the applied temperature, the crystal size can be controlled. However, its process window is very small and there are some issues in the uniformity and plate-to-plate difference.

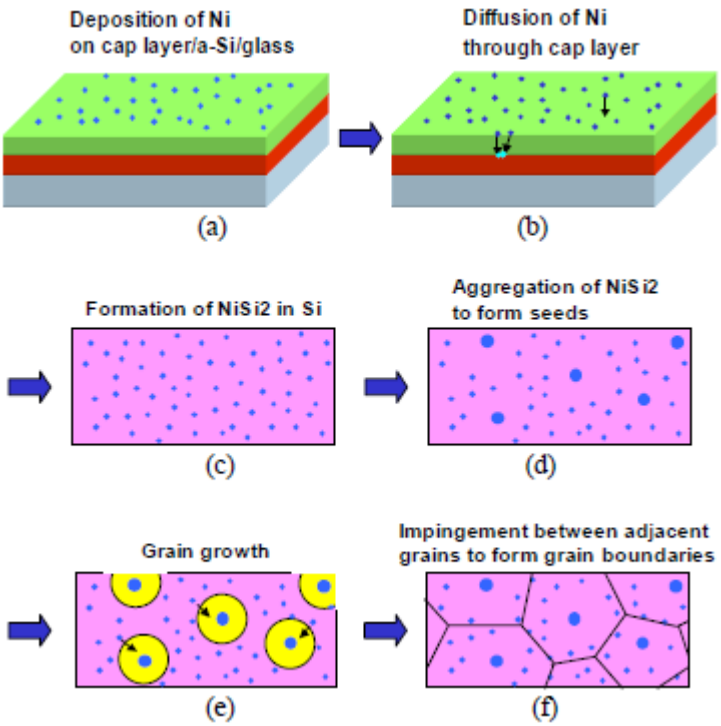


Fig. 16 Schematics of grain growth mechanism in SPC [25].

2-3. Key technologies for breakthrough

(a) Choice of crystallization method

Because the OLED is a current-driven device, the uniformity of the TFT characteristics is exceedingly important. A lot of techniques to form micro-crystalline Si were proposed [27, 28, 29, 30, 31, 32, 33, 34, 35]; however, there had been still some problems (, which are written in the previous paragraph) to apply them into production. To solve these problems, an in-direct annealing process using diode laser thermal annealing (dLTA) system was proposed [38, 39, 40, 41]. Here, a continuous wave (CW) laser is applied not a pulse laser used in the conventional ELA. A CW laser has far more stable output than the excimer laser in both the short term and the long term. N. Sasaki's group had reported TFTs with highly crystallized silicon and a high mobility of 566 cm^2/Vs by applying CW laser crystallization [42, 43, 44]; however, they left a problem for the uniformity that is necessary for the OLED driving. A dLTA system realizes uniform and stable laser irradiation and the laser is irradiated on the molybdenum film stacked on the amorphous silicon film. The amorphous silicon is crystallized by indirect heat from molybdenum film, which is heated by a laser, and forms a uniform crystalline silicon layer.

Table 5 Formation methods of micro-crystalline Si and issues for production.

Method		Issues				
		Deposition rate	Chamber cleaning	Crystallinity	Crystal uniformity	Process window
As-deposited	PE-CVD	Bad	OK	Fair	Good	Fair
	Cat-CVD	Fair	Difficult	Fair	Good	Fair
	ICP-CVD	Fair	Difficult	Fair	Good	Fair
	MSEP-CVD	Fair	OK	Fair	Good	Fair
Crystallization	ELA	—	—	Good	Bad	Bad
	SPC	—	—	Good	Fair	Bad
	dLTA	—	—	Fair	Good	Good

* Difficulty: High ← → Low

(b) TFT structure and crystallization method

As for the TFT for the FPDs, almost all are dominated by the amorphous silicon TFT because of its simple, low cost manufacturing process. Therefore, it is meaningful to improve the poor characteristics of the amorphous silicon TFT by changing its manufacturing process partially. A bottom-gate, back channel cut type TFT becomes to be widely applied for the backplane of LCD instead of etching stopper type TFT because of less manufacturing process steps. However, etching stopper type TFT

was chosen for the backplane of AM-OLED display because of its uniform TFT performance and less off-current. Fig. 17 shows the cross sectional view of the micro-crystalline silicon TFT by the dLTA system. A channel length (L) is determined by etching stopper width 8~10 micron, and channel width (W) is determined by source and drain width 20~100 micron, which is designed according to the panel specification, and channel thickness (d) is determined by deposited precursor thickness. In this design, TFT uniformity is mainly dominated by the variation of channel length L, promising high uniformity in large sized display.

A micro-crystalline TFT is fabricated by the following process. The molybdenum film was deposited on an alkali-free glass substrate by means of dc magnetron sputtering apparatus, and patterned to form the gate electrode using conventional photo lithography and dry etching method. The silicon nitride, silicon oxide, and amorphous silicon films are deposited by means of plasma enhanced chemical vapor deposition (PE-CVD) method to form a gate insulator and a precursor of the channel layer. A molybdenum film was deposited again to form the photo-thermal conversion layer. And then, the amorphous silicon film was crystallized by the dLTA system, which is composed of laser heads and a scanning stage (Fig. 18). More than 1W power continuous wave (CW) diode laser with 800 nm wavelength is used for the laser head. Irradiation process is performed by continuous oscillation of the laser and stage scanning of the glass substrate. The laser light absorbed in metal capping layer is converted to the heat, and the heat spreads to the lower layer. Finally it causes crystallization of silicon thin film from amorphous phase to micro-crystalline phase.
The exposed laser beam width was controlled to the width of channel region of each pixel, and the stage was scanned at a speed of about 150 mm/sec. After this crystallization process, the capping molybdenum film was etched off. Then, a silicon nitride film was deposited by means of PE-CVD method and patterned by the wet etching method to form an etching stopper of the TFT. A phosphorous-doped amorphous silicon (n+ a-Si) film was deposited by means of PE-CVD method. After the patterning of the silicon island by the dry etching method, the titanium-aluminum-titanium tri-layer films were deposited by means of dc magnetron sputtering, and patterned by the dry etching method to form the source and drain electrodes of the TFT. In this process, the n+ a-Si film on the etching stopper was also etched off. At last, a silicon nitride film was deposited by means of PE-CVD method as a passivation of the TFT.

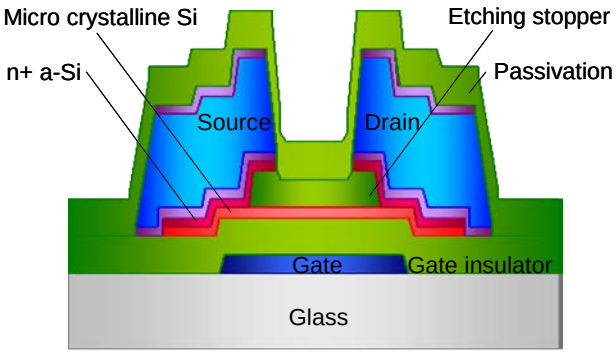


Fig. 17　Cross sectional view of the μc-Si TFT.

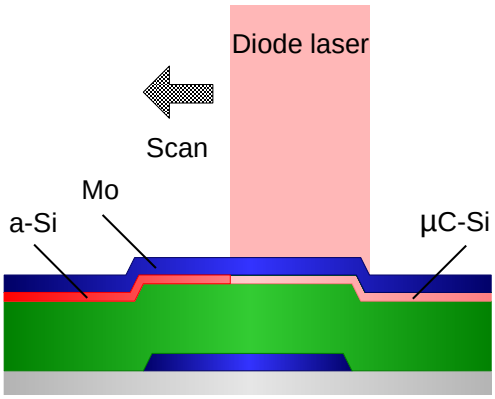


Fig. 18　Cross sectional view of the laser thermal crystallization.

Fig. 19 shows a process flow comparison between amorphous silicon TFT and micro-crystalline silicon TFT. The process flow of the micro-crystalline silicon TFT is almost same as that of amorphous silicon TFT. After the amorphous silicon deposition process, only the processes for photo-thermal conversion layer and crystallization are inserted. Only adding these processes, high mobility, uniform, and stable TFTs can be obtained.

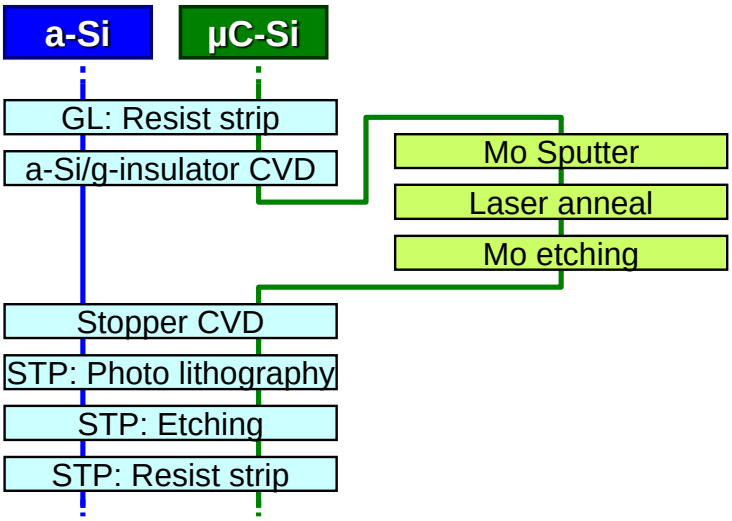


Fig. 19 Process flow comparison between a-Si TFT and µc-Si TFT.

(c) Film properties of micro-crystalline silicon

To realize uniform electrical properties, it is very effective to compose the TFT channel of micro-crystallite silicon, which is smaller than the size of TFT channel. The poly-crystalline silicon, which is formed by the crystallization method such as excimer laser annealing (ELA) method, has superior electrical properties and reliability, but its current uniformity is considerably worse because of the crystal size dispersion due to the pulse energy fluctuation of excimer laser. For the crystallization, metal capped diode laser thermal annealing (dLTA) method (Fig. 18) was employed. This laser has very stable output (<±1%) and long life (over 10000h), resulting in low maintenance cost in production. As for the a-Si:H film does not have large absorbance at the laser wavelength of 800 nm, a molybdenum film was deposited as a capping metal of the precursor a-Si:H film. The capping metal works as the photo-thermal conversion layer, and also works as a thermal diffusion layer contributing to the uniform crystallization. After removing the capping metal, the crystallinity of the micro-crystalline silicon was confirmed by Raman spectroscopy. A Jobin Yvon's LabRAM HR-800 system was used and the crystal fraction was calculated from the peak areas of decomposed peaks P1, P2, and P3 (P1: a-Si, P2: micro-crystalline Si, P3: poly Si). Fig. 20 shows the spectrum and decomposed three peaks located at 481 cm^{-1} (P1), 509 cm^{-1} (P2), and 518 cm^{-1} (P3), corresponding to the amorphous silicon phase, the micro-crystalline silicon phase and the poly-crystalline silicon phase, respectively. The crystal fraction was calculated using following formula, and was 70%.

$$\text{Crystal fraction} = (P2+P3)/(P1+P2+P3) \quad (1)$$

Fig. 21 shows the Secco etched micro-crystalline silicon film. Uniform 10~30 nm diameter crystalline was observed.

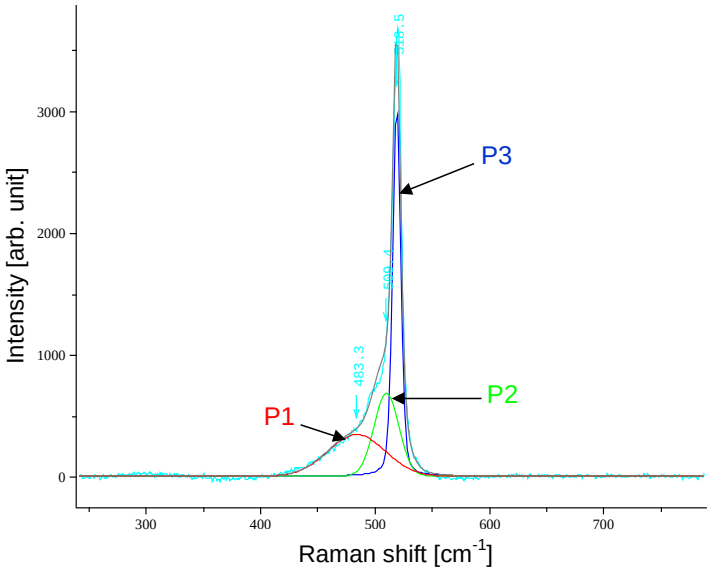


Fig. 20 Raman peak of micro-crystalline silicon and decomposed three peaks P1, P2 and P3.

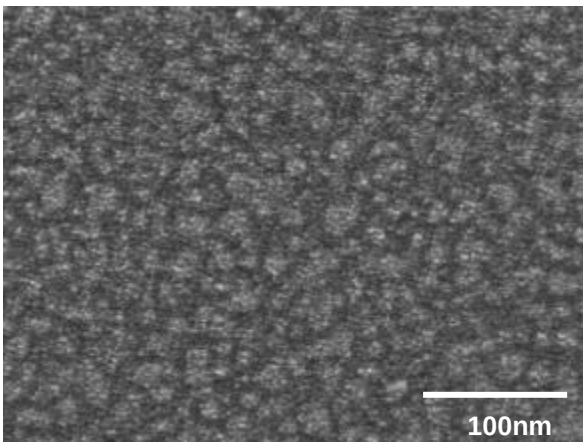
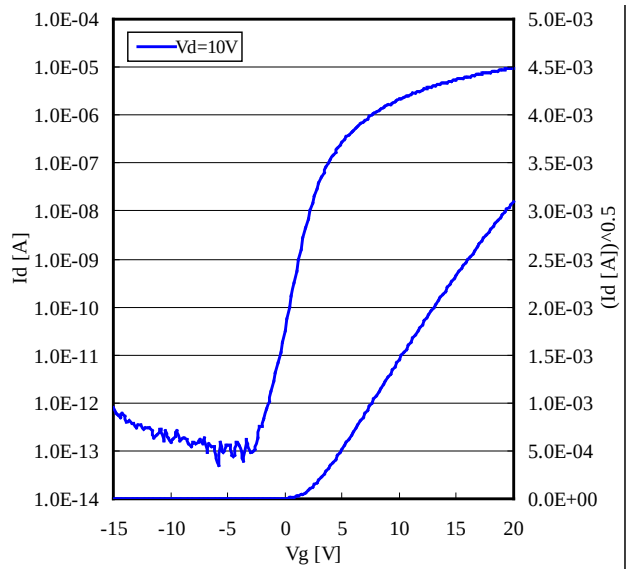


Fig. 21 SEM view of the Secco etched micro-crystalline silicon film.

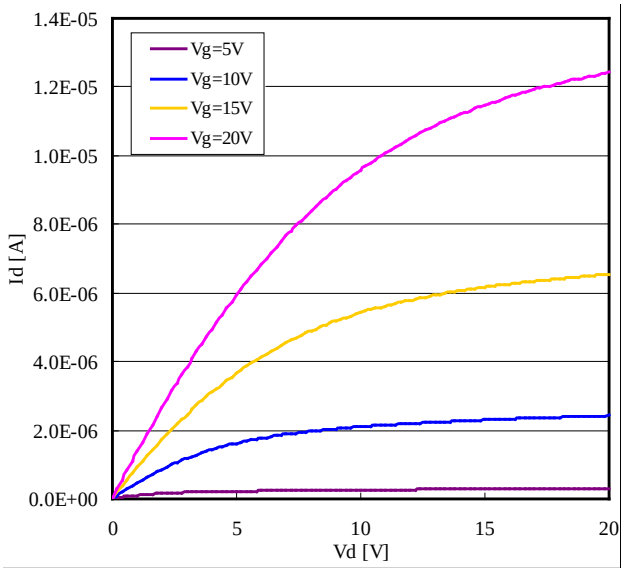
(d) Electrical properties of micro-crystalline silicon TFT

Fig. 22 shows I-V characteristics of the typical TFT. All the electrical properties were measured by the computer controlled Agilent 4156C precision semiconductor parameter analyzer. Its field effect mobility, threshold voltage (Vth), and sub threshold slope (S) were 3.1 cm^2/Vs, 2.3 V, and 0.93 V/decade, respectively. The crystallinity of micro-crystalline silicon is mainly affected by the thickness of precursor a-Si:H film or

the laser power of dLTA process, and those effects to the on-current are shown in Fig. 23 and Fig. 24. The thickness dispersion of the precursor a-Si:H film over the area of industrial manufacturing level is ±3%, meaning the ±2% variability in on-current. And the laser power dispersion of the dLTA system (, which includes the laser power dispersion and the scanning speed dispersion) is ±1%, meaning the ±3% variability in on-current. From these facts, the dLTA process is enough robust for mass-production.



(a) Vg-Id characteristics



(b) Vd-Id characteristics

Fig. 22 Electrical properties of μc-Si TFT.

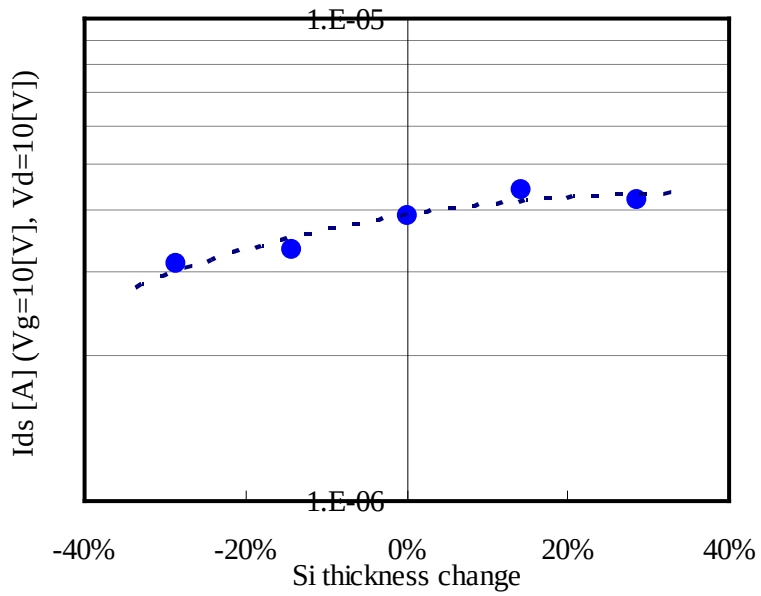


Fig. 23 Effect of precursor a-Si thickness to the on-current of μc-Si:H TFT.

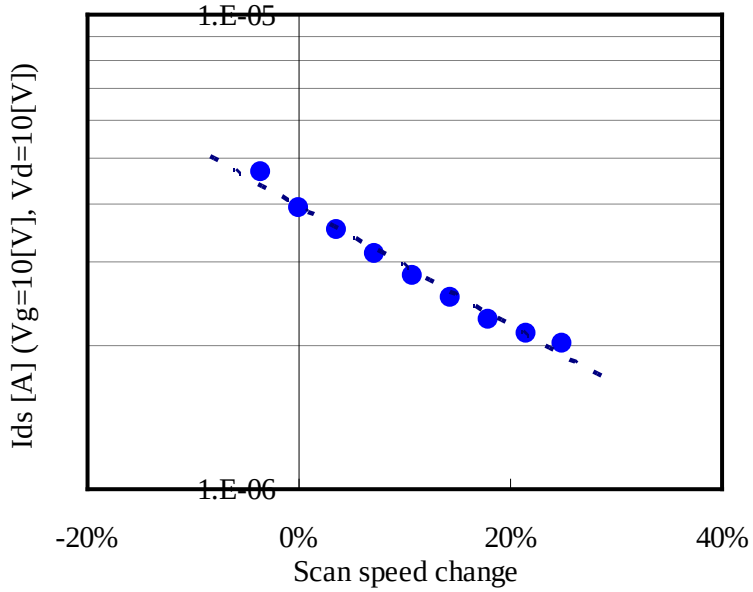


Fig. 24 Effect of laser scanning speed to the on-current of μc-Si:H TFT.

Fig. 25 shows the irradiating laser power dependence on Ids (Vg=Vd=10 V) of μc-Si TFT. Ids monotonously increased with the increase of the laser power. According to the curve, Ids can be precisely adjusted to the necessary value by controlling the driving current of the laser.

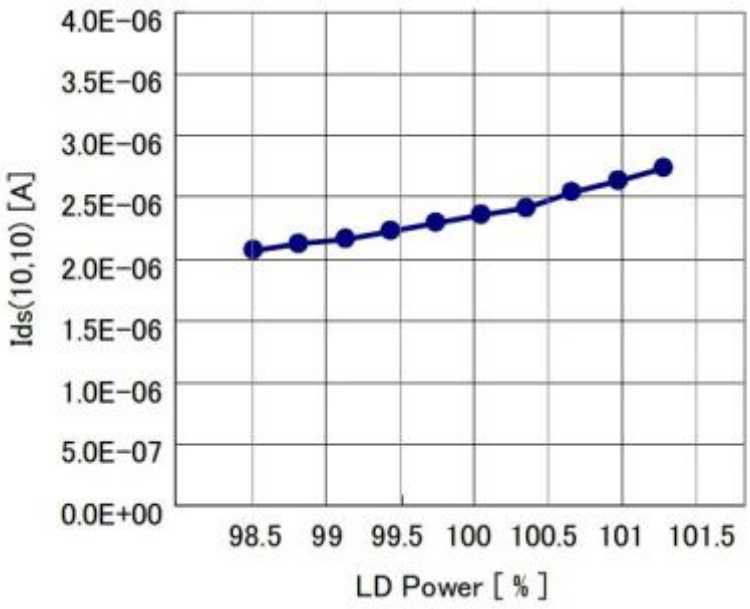


Fig. 25 Relationship between Ids and laser poser.

Fig. 26 shows the variation of Ids value (Vg=Vd=10 V) of adjacent 31 transistors in μc-Si TFT. The Ids dispersion of μc-Si TFT shows excellent uniformity. When the Ids dispersion of μc-Si TFT was compared with that of a-Si TFT under same device structure and same measuring condition, the Ids dispersion of μc-Si TFT showed almost the same value as that of a-Si TFT. The Ids dispersion originated with the micro-crystalline silicon crystallized by dLTA process is enough small for the OLED display.

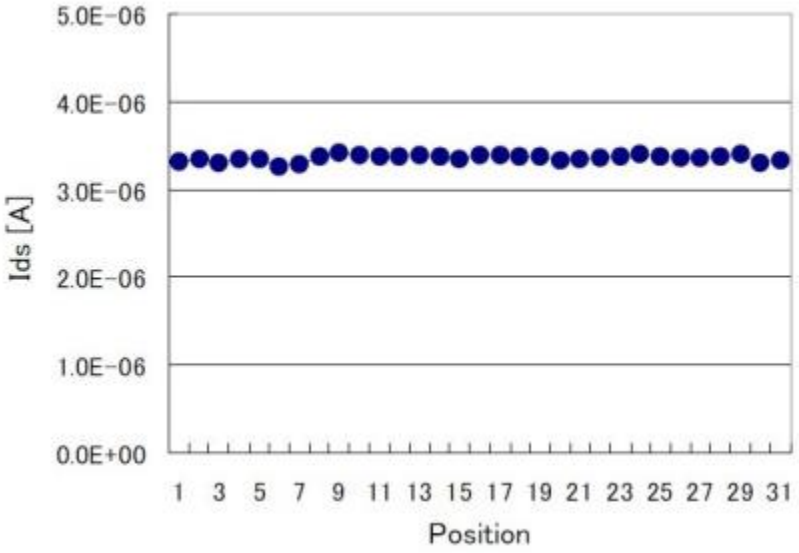


Fig. 26 Ids variation of adjacent 31 transistors.

(e) Technique to reduce off-current

This TFT has superior characteristics in the off-current even though using micro-crystalline silicon as channel. The laser thermal crystallization using metal capped structure and dLTA system realizes low lattice defect density, and the stopper type TFT structure realizes low process damage to the channel region after the crystallization process, and the thin channel has an advantage in off-current from the structural point of view. Moreover, proposed stacked n+ a-Si:H structure (Fig. 27) contributes to the extra low off-current even in the state of high drain voltage (Fig. 32). The off-current was easily reduced by reducing the phosphorous concentration of n+ a-Si:H layer with the reduction of on-current. This reduction of on-current was considered to be caused by the increase of the series resistance between the drain metal and the channel region. Therefore, extra low off-current was realized while maintaining high on-current by stacking the high phosphorous concentration layer on the low phosphorous concentration layer.

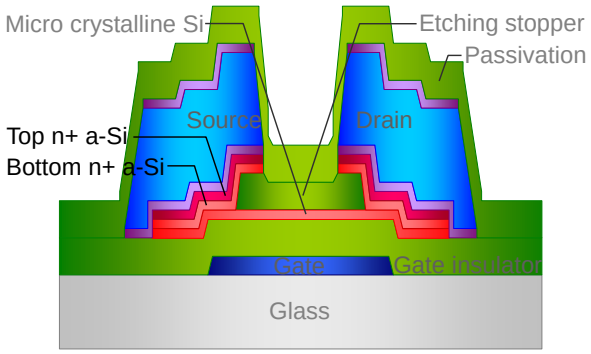


Fig. 27 Stacked n+ a-Si:H structure TFT.

Fig. 28 shows the on-current activation energy of the linear region characteristics of amorphous Si TFT and micro-crystalline Si TFT as a function of gate voltage. At the low gate voltage region around 5V, the activation energy of micro-crystalline Si TFT is smaller than that of amorphous Si TFT. Yet, as the gate voltage becomes larger than 15V, the activation energy of micro-crystalline Si TFTs get closer to that of amorphous silicon TFTs. Because the micro-crystalline Si TFTs have fewer defects than the amorphous Si TFTs, the micro-crystalline Si TFTs have smaller activation energy at the low gate voltage region. However, as the gate voltage becomes higher, the series resistance of the source and drain region becomes more dominant. Due to this series resistance, the activation energy of the two types of TFT becomes similar in value.

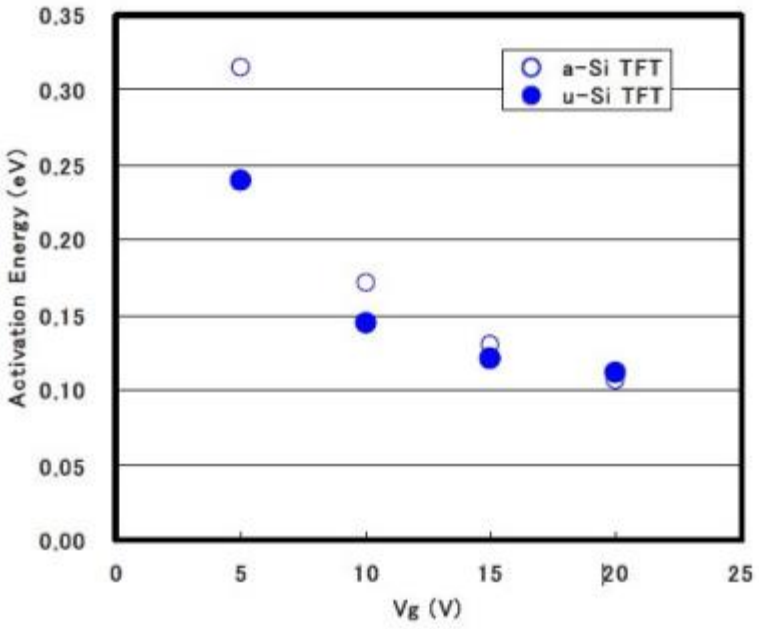


Fig. 28 On-current activation energy of a-Si TFT and μc-Si TFT.

Fig. 29 shows the relationship between on-current activation energy (Vg=20 V, Vd=10 V) and field effect mobility of micro-crystalline Si TFT. Each point has a different n+ a-Si layer deposition condition. To get a high mobility, it is considered that the n+ a-Si layer should be low resistance.

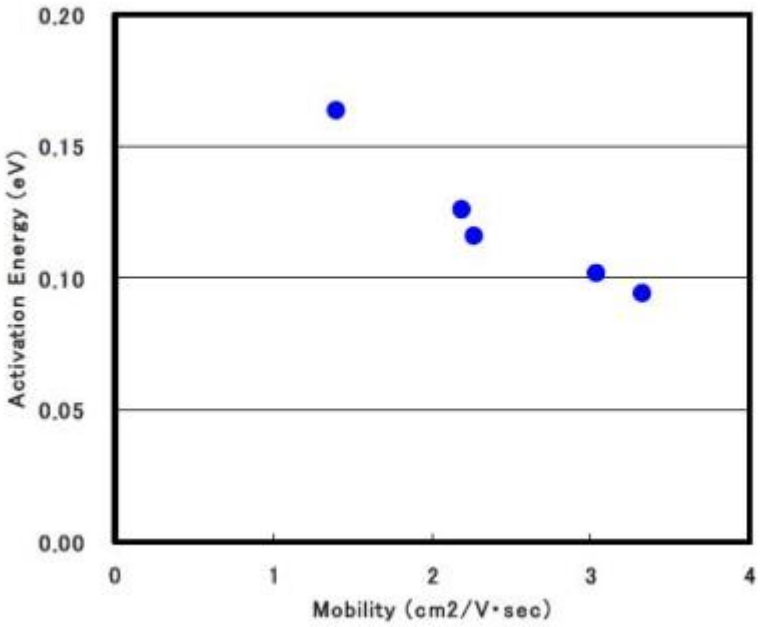


Fig. 29 Relationship between on-current activation energy and field effect mobility of μc-Si TFT.

Fig. 30 shows the effect of the phosphorus doping concentration on the on-current of micro-crystalline Si TFT. The phosphorous doping concentration was changed by the gas flow ratio of phosphine in the n+ a-Si layer deposition. As the concentration of phosphorus becomes higher, the on-current of micro-crystalline Si TFT becomes larger. Hence the reduction of the series resistance of source and drain region is very important to get a high drive current. Fig. 31 shows the relationship between the phosphorus concentration and the off-current of micro-crystalline Si TFT. Higher phosphorus concentration of n+ a-Si causes higher off-current of micro-crystalline Si TFT.

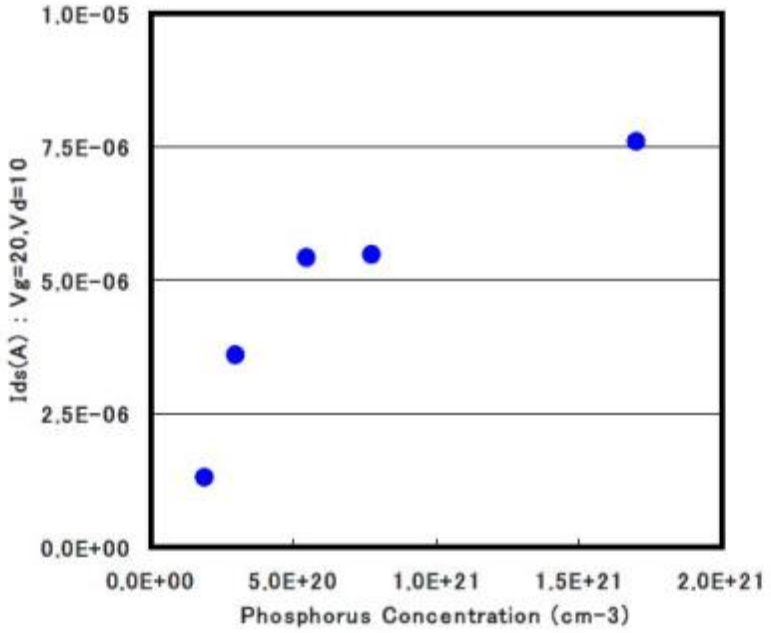


Fig. 30 Effect of phosphorus doping concentration on the on-current of μc-Si TFT.

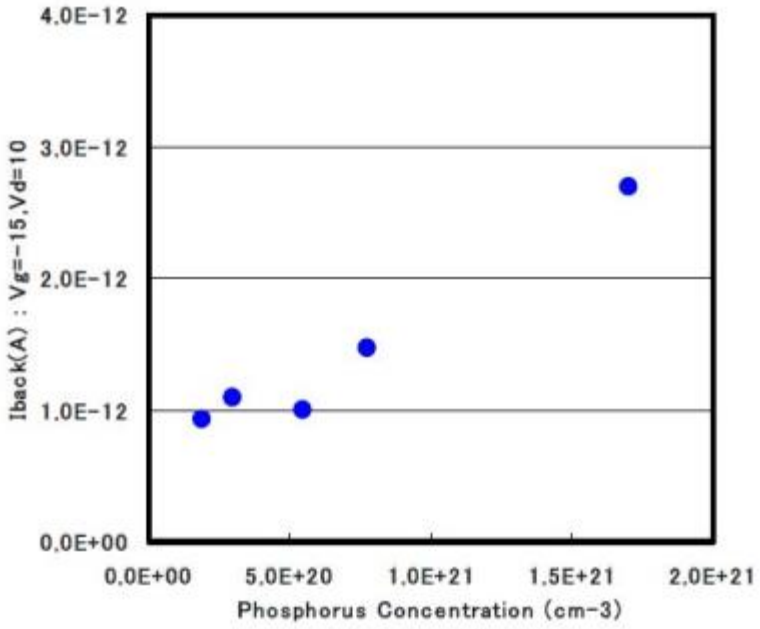


Fig. 31 Relationship between the phosphorus concentration and the off-current of μc-Si TFT.

To overcome this trade-off, a stacked source and drain structure (Fig. 27) was proposed for the micro-crystalline silicon TFT. This stacked source and drain layer

consist of a bottom layer with a low phosphorus concentration and a top layer with a high phosphorus concentration resulting in a lowered the electric field at the drain region. Also, the top source and drain layer lowered series resistance of source and drain region. Therefore, both of the high on-current and the low off-current are obtained according to this structure. Fig. 32 shows the Vg-Id characteristics both of a stacked source and drain structure and a conventional single source and drain structure. Even at a high drain voltage regime, a micro-crystalline silicon TFT with stacked source and drain structure shows both of the low off-current and the high on-current at the same time.

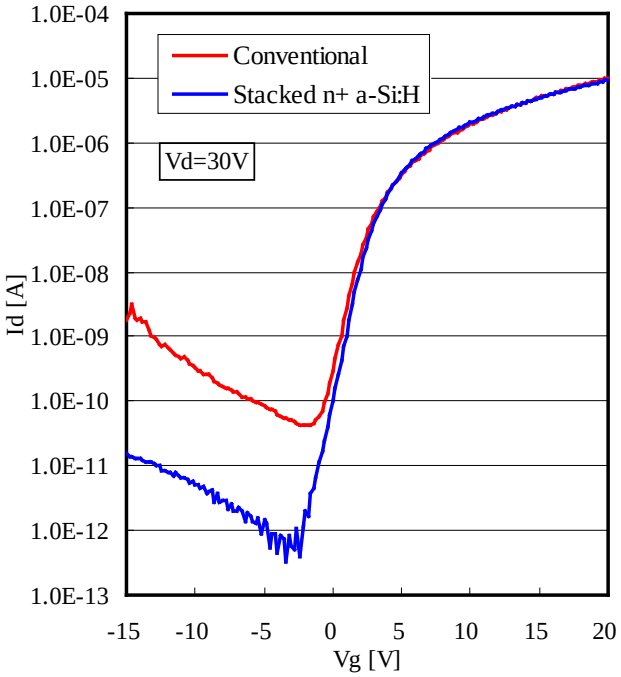


Fig. 32 Vg-Id characteristics of conventional and stacked n+ a-Si:H structure TFT.

Fig. 33 shows the bias temperature stress (BTS) test results of three types of TFTs: amorphous Si, micro-crystalline Si, and LTPS TFTs. For the television (TV) application as the toughest case, 100,000 hours reliability with an on-current of 10E−6 A at a temperature of 50 °C was considered for each TFT. Assuming the drive scan TFT in the compensation circuit of the pixel, the same bias was applied for gate (Vg) and drain (Vd) keeping 10E−6 A. A threshold voltage shift (ΔVth) was observed for 100,000 sec and extrapolated to 3.6E8 sec. The calculated ΔVth of micro-crystalline silicon TFT after 3.6E8 sec stress was only 1.77 V. Its value was two orders smaller than that of a-Si:H TFT (107.7 V), and only three times of that of LTPS TFT (0.52 V). In the fabrication flow of micro-crystalline silicon, there is no hydration process like LTPS;

however, it is supposed that the dangling bonds on the interface of micro-crystalline are terminated by the hydrogen, which comes from the upper CVD film formation.

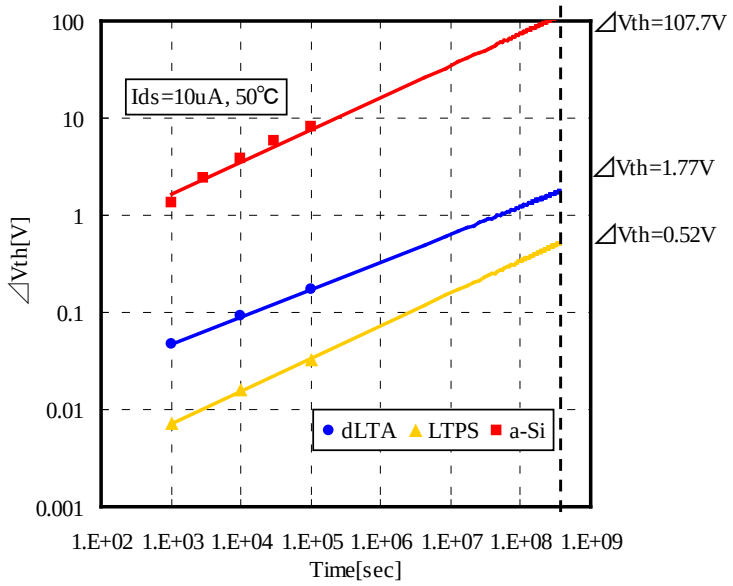


Fig. 33 Vth shifts (after BTS) of a-Si, μc-Si, and LTPS TFTs.

Fig. 34 shows the cross sectional TEM view of the micro-crystalline silicon. About 10 nm diagonal of grains are observed, and those grains are formed from the interface of the gate insulator. In general, as-deposited microcrystalline silicon often has amorphous incubation layer as the initial grown region and it causes the characteristics degradation by BTS. On the contrary, the microcrystalline silicon by the dLTA process has no incubation layer and therefore results in superior reliability against BTS. This must be an effect of the thermal crystallization method.

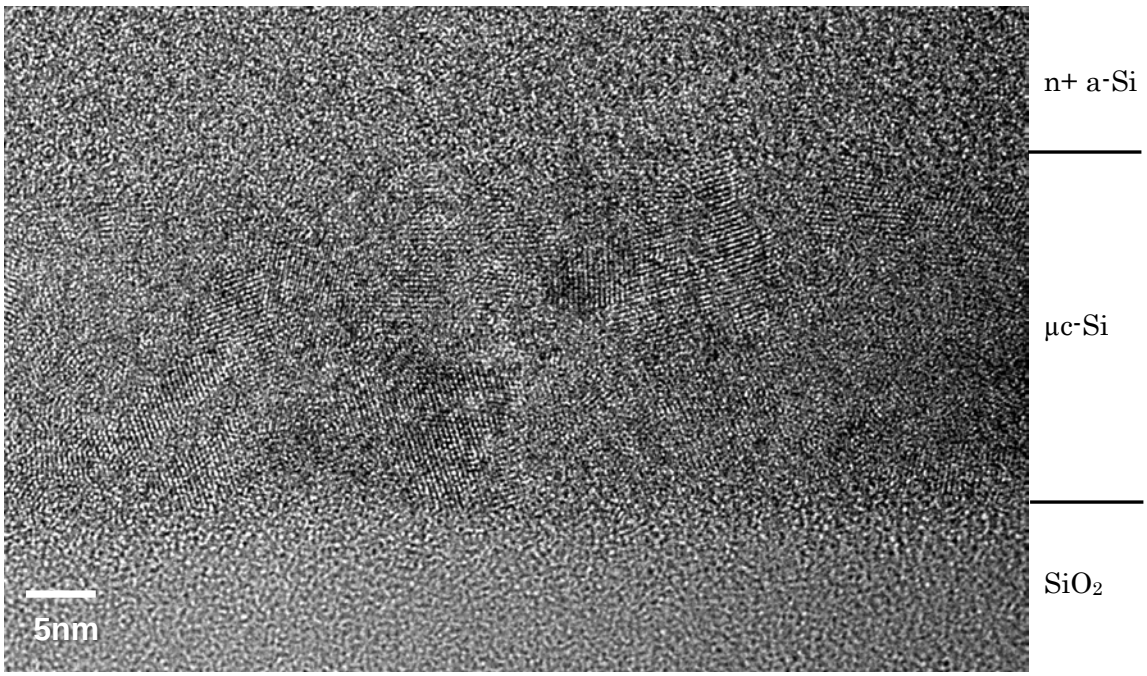


Fig. 34 Cross sectional TEM view of μc-Si.

(f) dLTA system for mass-production

Even though the scanning speed of the dLTA system is higher than 150 mm/sec, single head laser annealing is insufficient at a point of view of the productivity. A multi head laser annealing system (Fig. 35) is employed to reduce the takt-time. The scanning stage speed is designed from 150 to 300 mm/sec, and the laser power of each laser head is controlled to the same level, which results in no stitching Mura between two laser heads next to each other. Output laser light is formed to an appropriate beam shape with optical components and irradiate to a necessary area of the metal capping layer.

Fig. 36 shows the difference between dLTA system and ELA system. ELA system has wide laser width, but stepping speed is very low, because of its over-lapped stepping method. On the other hand, dLTA system has narrow laser width but scanning speed is very high. In case of ELA, panel size is limited by the laser width, and said 26" diagonal may be the maximum size. In case of dLTA, there is no size limitation, and takt-time can be reduced by increasing the laser head number and/or the scanning speed.

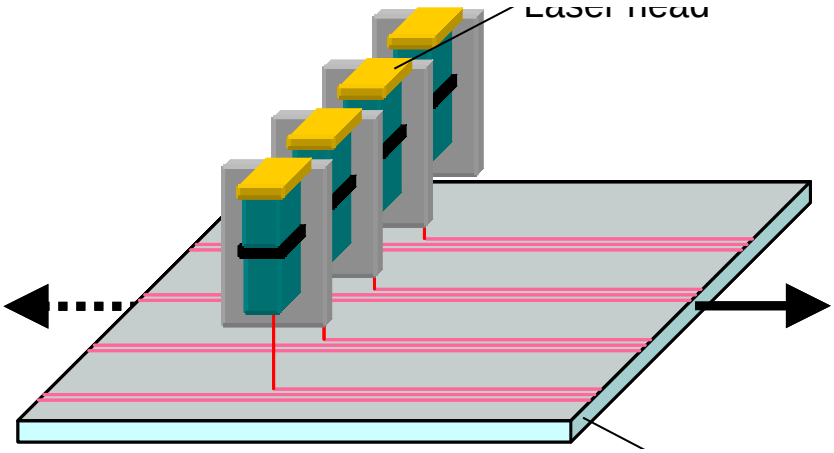


Fig. 35　Multi-head dLTA system.

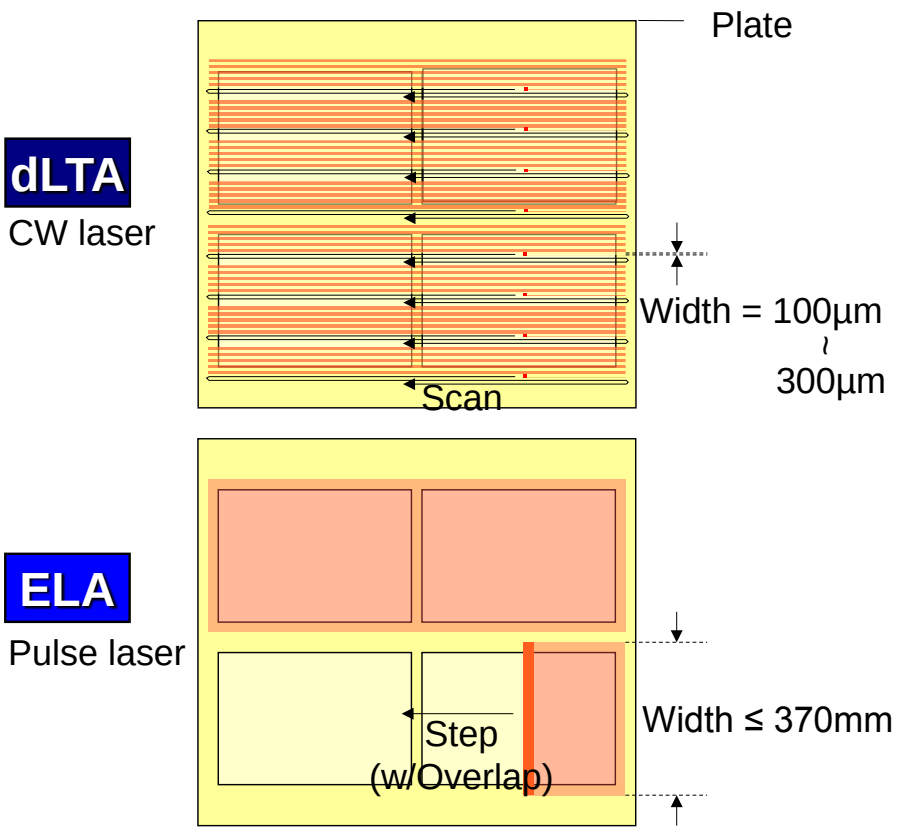


Fig. 36　Comparison of laser annealing method (CW laser vs. pulse laser).

(g) Low resistivity bus line for dLTA process

For the large size high resolution AM-OLED display, both vertical and horizontal bus lines should have low resistivity for the high current flow and the complicated driving signal. In the laser thermal annealing process, the gate metal of the bottom-gate TFT works as a heat sink. Therefore, a thermal capacity of gate metal is better to be small. Moreover, the conventional aluminum or aluminum alloy gate metal which is widely used in liquid crystal display can not be used in laser thermal annealing process, because even the aluminum alloy makes hillocks, whiskers, or voids as a result of thermal migration in the laser thermal annealing process (Fig. 37). Therefore, a molybdenum (Mo) film with a thickness of 90 nm is used as a gate metal, and the Mo/aluminum-neodymium alloy (AlNd) clad structure is used as a bus line (Fig. 38). Although this process requires additional photo-lithography process against the conventional a-Si:H TFT process, it realizes stable and high crystallinity of Si, and low resistivity bus line for large size, high resolution AM-OLED display.

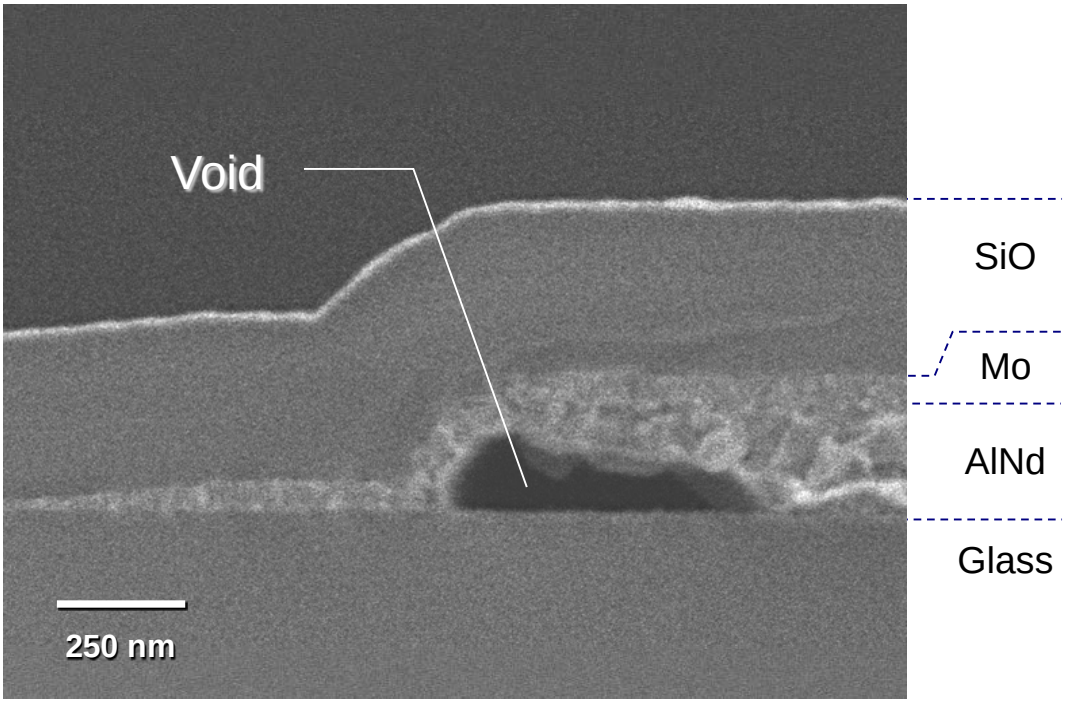
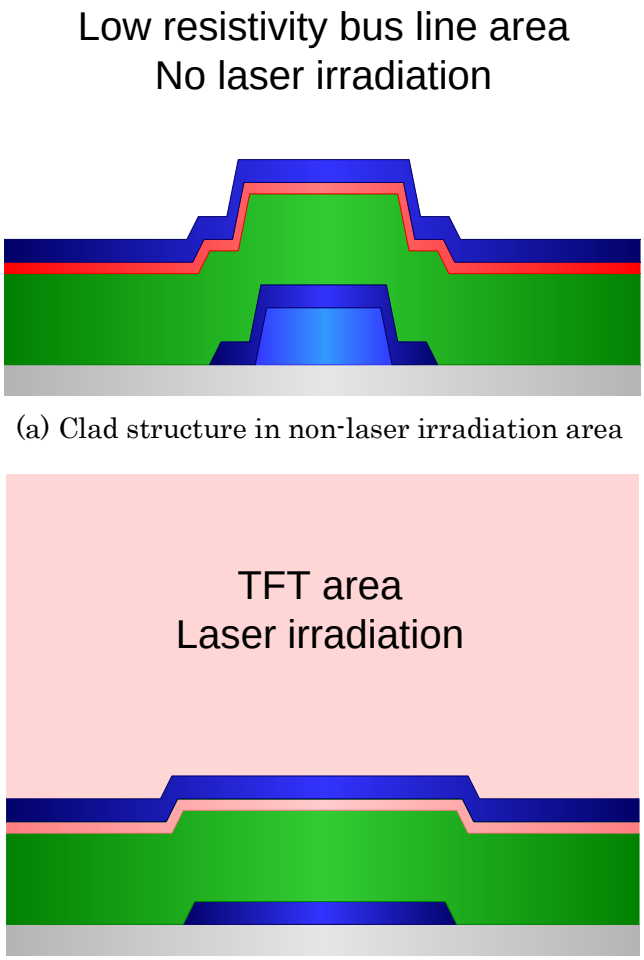


Fig. 37 Cross sectional SEM view of laser thermal annealed Mo/AlNd line. A void was created by the thermal stress migration.



(a) Clad structure in non-laser irradiation area

(b) Gate structure in irradiation area

Fig. 38　Cross sectional views of (a) Mo/AlNd clad structure in non-irradiation area and (b) Mo gate structure in irradiation area.

Fig. 39 shows the top view of a pixel. The “bus line area” and “TFT area” are divided, and the laser is irradiated only on the “TFT area”. Even if the TFTs constituting the compensation circuit increased, enough area can be prepared for the TFTs. There is no thermal damage on the low resistivity bus lines.

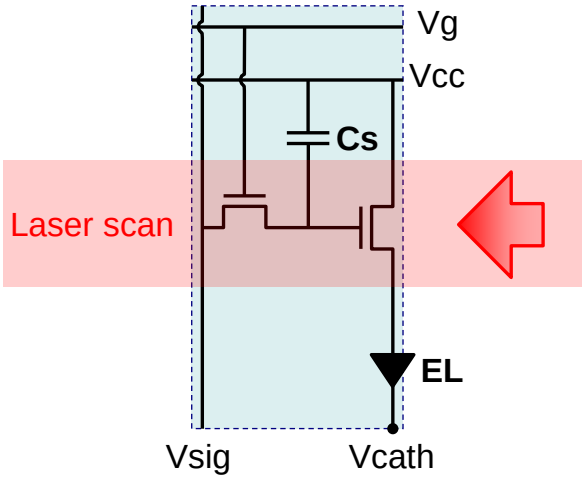


Fig. 39　Laser irradiation area in the sub-pixel for AM-OLED display.

Furthermore, its productivity can be improved to double by devising the pixel design. Fig. 40 shows the pixel design to do single laser scan for two pixel rows. The pixels are generally designed symmetrically in a matrix-shaped. By designing the two pixels next to each other for the gate bus line linear symmetry for the gate bus line, two pixels row can be crystallized simultaneously by single laser scan. A laser light is irradiated only on the “TFT area”, therefore, the gate bus line has no thermal damage by the laser irradiation. According to this method, the process takt-time can be reduced by a half.

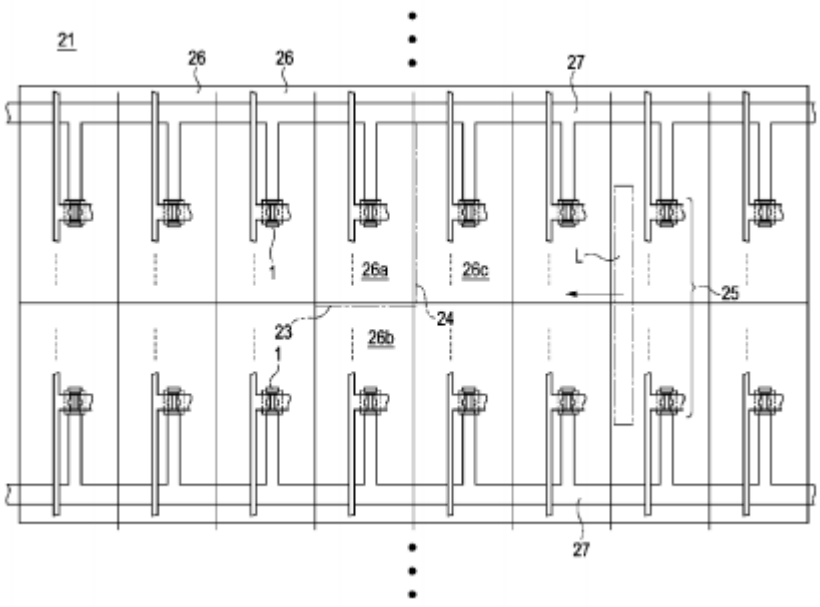


Fig. 40　US PAT. 8928638 [45].
(1: TFT, 27: gate wiring, L: laser light)

2-4. Fabrication of AM-OLED display

TFTs have very high uniformity both in the short range and in the wide range. Fig. 41 shows the brightness uniformity of the top emission OLED device on the DC mode. The channel regions of TFTs were horizontally annealed by dLTA system. In this case, only green EL material was deposited by vapor deposition method for all pixels to confirm the uniformity. All TFTs are driven in the saturation region and not compensated. No Mura was observed, and it indicates that TFTs have very uniform characteristics.

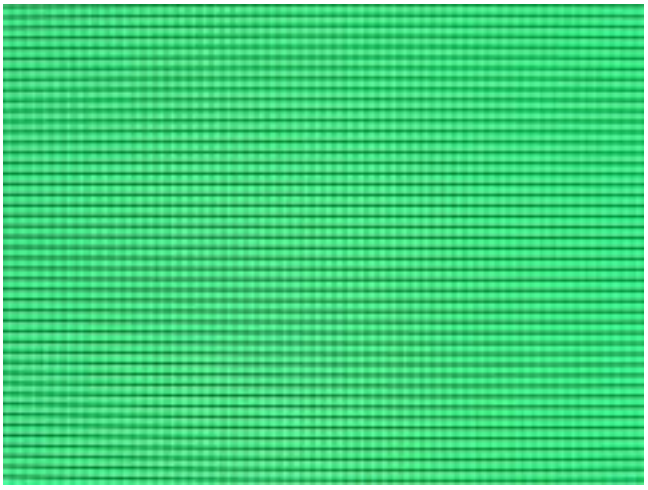


Fig. 41 Micrograph of AM-OLED screen driven in DC mode.

A 27.3-inch diagonal display, which has 1920 x 1080 pixels, was fabricated (Fig. 42). The micro-crystalline TFT by dLTA system and the low resistivity gate bus line by clad technology were applied to this display. A top emission type OLED structure was adopted and the EL materials were formed on the micro-crystalline TFT array by the laser-induced patternwise sublimation (LIPS) method with which the evaporated organic electroluminescence materials are pattern-wise transferred to the array substrate by laser irradiation [46]. Table 6 shows the specification of the display. The white peak luminance over 600 cd/m^2 and a color gamut exceeding 100% of NTSC triangle were achieved, and the reliable compensated driving by the stable micro-crystalline silicon TFT was confirmed.

Fig. 42　27.3-inch diagonal FHD μc-Si TFT driven AM-OLED display.

Table 6　Specification of the 27.3-inch diagonal μc-Si TFT driven AM-OLED display.

Panel size	27.3-inch (694 mm) diagonal
Format	Full HD (FHD)
Resolution	1920 RGB x 1080
Brightness	All white: 200 cd/m^2
	Peak : > 600 cd/m^2
Contrast	> 1000000 : 1 (Dark)
Number of colors	10 bit RGB
Color saturation	> 100% (NTSC)

2-5. Summary

A novel crystallization technology, which realizes uniform and superior electrical properties: field effect mobility of 3.1 cm^2/Vs, threshold voltage (Vth) of 2.3V, sub threshold slope (S) of 0.93 V/decade, and 8 orders of magnitude lower off-current than the on-current, was developed. From the BTS test, the calculated ΔVth of micro-crystalline silicon TFT after 3.6E8 sec of 10E−6 A stress was only 1.77 V. This value is 2 orders of magnitude smaller than that of a-Si TFT and only three times of that of LTPS.

Except for the dLTA system, all the process can be executed by the conventional manufacturing apparatus, which are commonly used in the manufacturing of a-Si TFT array. In other words, a few additional investments can change an existing amorphous silicon TFT manufacturing line to the new manufacturing line which comes to realize value added products. This technology is promised to contribute to the large size, high resolution, high frame rate, or the gate driver integrated AM-OLED displays.

Chapter 3 Oxide TFT technology

3-1. Introduction

A transistor for the AM-FPD had been completely dominated by the silicon-based semi-conductor technology. A micro-crystalline silicon TFT is a good candidate to realize both the electrical uniformity for the large substrate and the stability against bias stress; however, there is a trade-off relationship between the electrical uniformity and the mobility. When the necessary electrical uniformity is secured for the TFT, there is a problem that the mobility is suppressed by 3~5 cm^2/Vs. On the other hand, the high resolution or the high frame rate images increased from the late 2000s, and higher mobility came to be expected for the TFTs of AM-FPDs. In 2004, Hosono's group reported amorphous metal oxide-based semiconductor [47, 48, 49]. The proposed amorphous oxide semiconductor from the In-Ga-Zn-O system (a-IGZO) for the active channel has high mobility exceeding 10 cm^2/Vs, and is formed by the conventional dc-sputtering apparatus with low temperature deposition condition. It means that the oxide TFT can just follow the infrastructure of the amorphous silicon TFT production, and has a chance to realize low cost manufacturing with a large substrate.

Fig. 43 shows the schematic orbital drawings for the carrier transport paths in a) silicon semiconductors and b) metal oxide semiconductors [47], and Table 7 shows the comparison of amorphous silicon and amorphous metal oxide. In the case of silicon semiconductor, the band gap between the top of valence band and the bottom of conduction band are both composed of sp3 orbitals, which have strong directivity. Therefore, the bond angle fluctuations of amorphous silicon significantly suppress the band conduction, and the localized state conduction, which occurs via electrons hopping from one localized state to another, results in low mobility. In contrast, in the case of metal oxide semiconductors, the top of the valence band is composed of 2p orbitals of oxygen ions and the bottom of the conduction band is composed of the spacially spread metal s orbitals with isotropic shape. The neighboring s orbitals overlap even in the amorphous phase and contribute to the conduction, therefore amorphous oxide semiconductors exhibit high mobilities like crystalline.

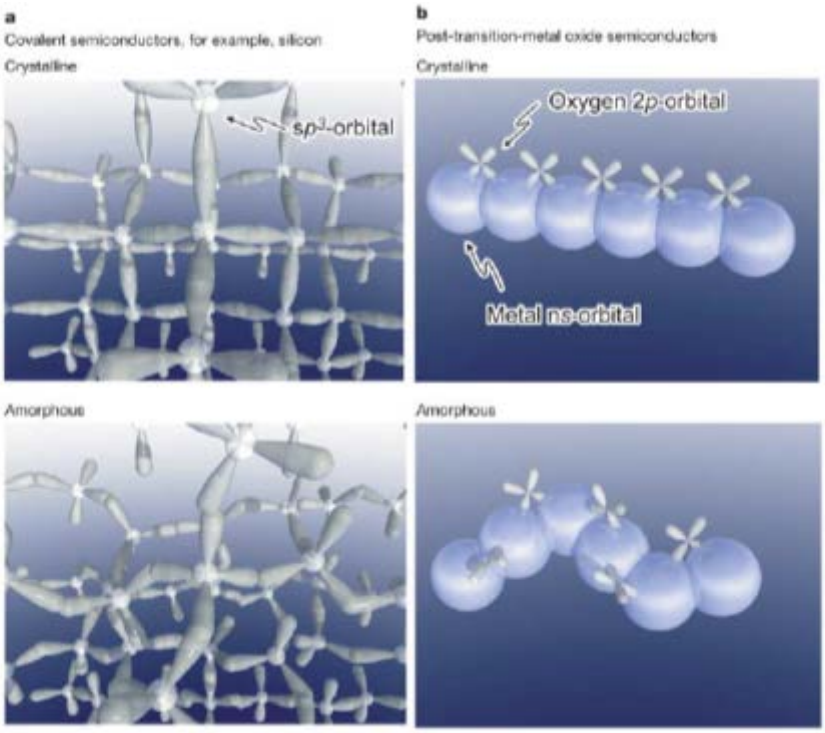


Fig. 43 Schematic orbital drawings for the carrier transport paths in a) silicon semiconductors and b) amorphous oxide semiconductors [47].

Table 7 Comparison of amorphous silicon and amorphous metal oxide (a-IGZO).

	a-Si	a-IGZO
Band gap [eV]	~1.7	~3.1
Mobility [cm²/Vs]	~0.5	~10
Chemical bond style	covalently	ionically
Carrier transport path	sp3 orbitals	s orbitals
Deposition temperature [°C]	~250	25~

3-2. Technologies in the early stage / Conventional technologies

Hosono's group reported the advantages of the amorphous In_2O_3–Ga_2O_3–ZnO system [47, 48, 49], and Fig. 44 shows the material properties of metal oxide semiconductors in the IGZO system.

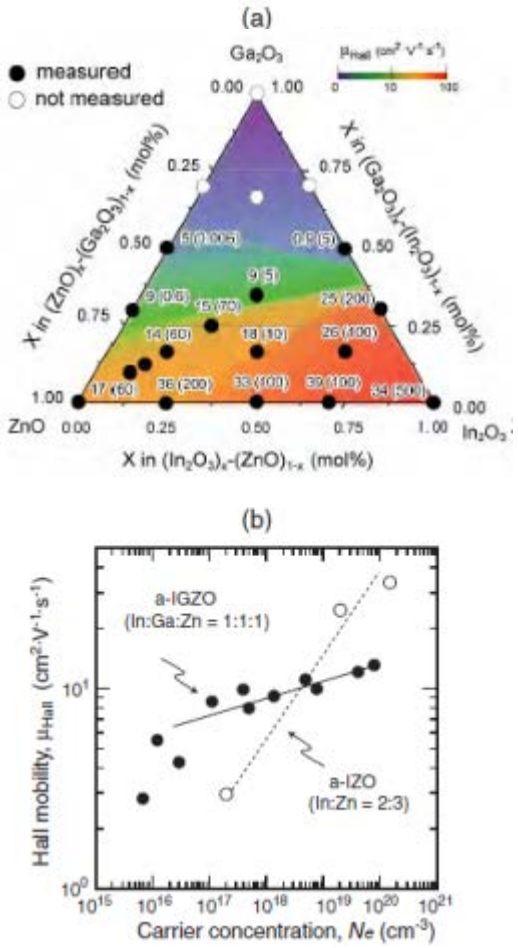


Fig. 44 Material properties of metal oxide semiconductors in the IGZO system [49]. (a) Room temperature Hall mobility and carrier concentration as functions of chemical composition. Values outside and inside parentheses show Hall mobility in cm^2/Vs and carrier concentration in 10^{18} cm^{-3}, respectively. (b) Relationships between Hall mobility and carrier concentration in a-IGZO and a-IZO films.

Each element has meanings to maintain good TFT characteristics. Indium (In) has an effect for high mobility; however, the excess In helps to crystallize resulting in non-uniformity and increases the carrier density too high for the semi-conductor. Gallium (Ga) has high oxygen-affinity and suppresses unintentional carrier generation; however, the excess Ga decreases mobility. Zinc (Zn) prevents poly-crystallization and

also has an effect for high mobility; however, the excess Zn helps to crystallize resulting in non-uniformity and increases the carrier density too high for the semi-conductor like In. Balance seems to be necessary for these three elements, and K. Nomura proposed the nominal chemical composition of $InGaZnO_4$ (In:Ga:Zn = 1:1:1) for the channel layer of TFT [49]. From the results shown in Fig. 44, Ga seems to have an important role; high Ga content results in too low mobility and low Ga content results in too high carrier density and uncontrollable Hall mobility. From initial stage of the study to the present, the composition that K. Nomura proposed is adopted extremely a lot.

The amorphous IGZO (a-IGZO) TFT has high mobility exceeding 10 cm^2/Vs and excellent on/off ratio exceeding 10^8. It has a strong potential to be used for high resolution, high frame rate AM-OLED display, which requires higher mobility than amorphous Si TFT and much higher uniformity than LTPS TFT. In order to apply oxide TFT to the AM-OLED display, most crucial point would be its stability.

Because the OLED is a current-driven device, both of the TFT and the OLED generate heat with the current flow and the emission of light. Actually, the TFT is placed under the severe bias-temperature stress (BTS) environment. In the case of amorphous Si TFT, the device instability has been attributed to two different mechanisms: charge trapping in the gate dielectric and the creation of the metastable dangling bond in the amorphous Si [50, 51, 52]. The former charge trapping mechanism is known to be also applicable to the oxide TFT [53, 54, 55, 56], therefore the formation of the gate insulator and the treatment of the interface between gate insulator and oxide semiconductor are important for the TFT stability.

Much severe instability due to the adsorption/desorption dynamics of water, oxygen, hydrogen, etc. are reported [57, 58, 59, 60]. In the case of OLED display, various materials for the OLED device are formed on the TFT and sealed, therefore the TFTs are affected by those materials or the environments, which they are formed. The photo illumination is known to affect to this instability.

Furthermore, the photo illumination also affects the instability. Despite of the wide band gap property, oxide semiconductor absorbs the light of short wave length resulting in leakage [61]. And, the effect of moisture on the photon-enhanced negative BTS instability is also reported [62].

To avoid these instabilities owing to various stresses (; bias, temperature, humidity, photo irradiation, etc.), annealing or passivating technologies have been proposed [63, 64, 65, 66, 67, 68]; however, simple and effective solutions are not found yet.

3-3. Key technologies for breakthrough

3-3-1. Bottom-gate TFT

As shown in Table 1, the oxide TFT attracted attention because of its high mobility and high uniformity; however on the other hand, there were several reliability issues, which were mentioned in the previous paragraph. The reliability improvement is a key for the wide use.

(a) TFT structure

It is well known that the properties of oxide semiconductor are highly dependent on the oxygen content, since oxygen vacancies provide the free carriers. Even in the case of In–Ga–Zn–O material, which is said to be a stable oxide semiconductor, the content of oxygen controls its film properties in applications from conductor to insulator. The oxygen in the oxide film may be absorbed or desorbed even after film deposition by the disclosed conditions such as heat, plasma, or a vacuum. Therefore a bottom-gate TFT structure was chosen so as to be affected as little as possible by the manufacturing process after the a-IGZO film deposition (Fig. 45) [64]. An etching stopper type TFT must have advantages for the stability, because the etching stopper acts as not only an etching stopper in the source/drain patterning but also a passivating film in the manufacturing process, an oxygen stabilizer for the oxide semiconductor, and a precise channel length promoter. For the gate insulator and an etching stopper, the conventional silicon oxide (SiO_x) films were deposited by chemical vapor deposition (CVD), and the very thin silicon nitride (SiN_x) film was inserted on the bottom of gate insulator to avoid the contamination from the lower layers.

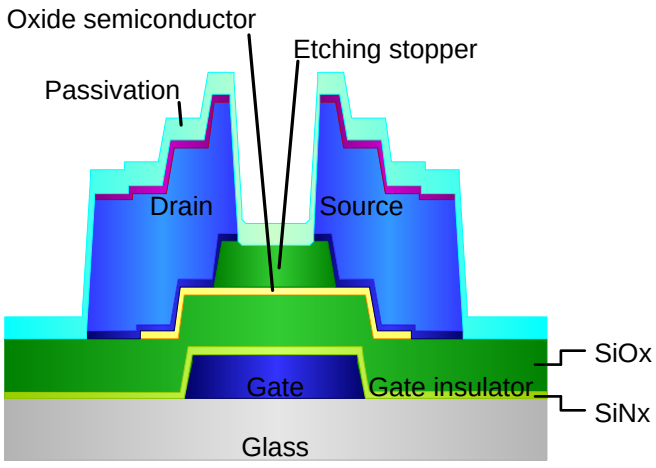
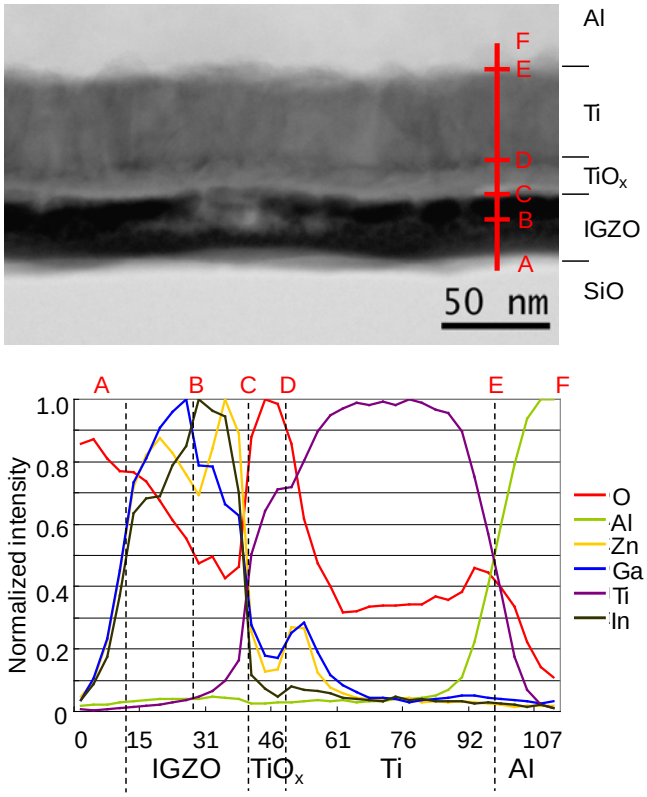


Fig. 45 Cross-sectional view of TFT.

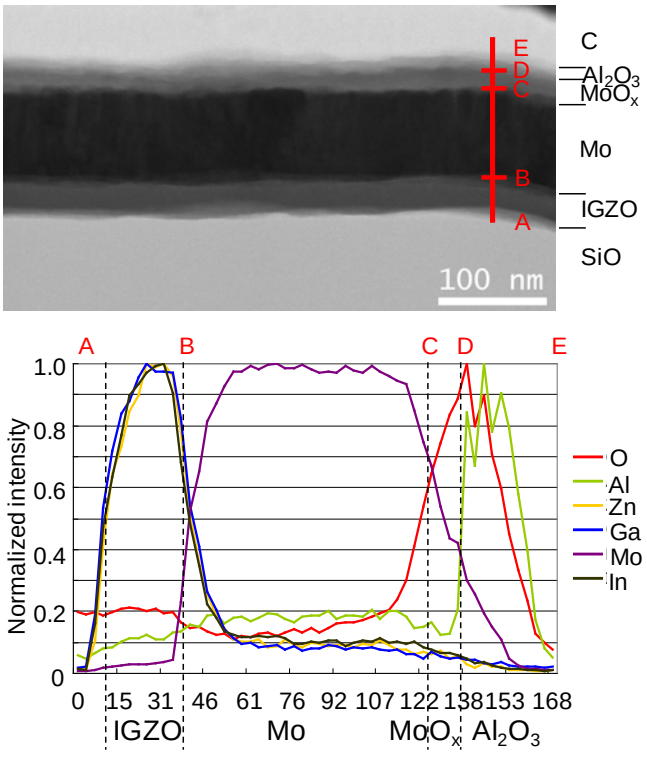
(b) Source/Drain material for high stability

In many cases, the source/drain has a structure of the stacked films to realize both low resistivity as a bus line and as electrical contact to the lower channel. Aluminum or copper is widely used as the core material of the source/drain because of their low resistivity. For the contact material, it has been reported that titanium (Ti) realizes better characteristics than other materials [65]. However, Ti has low ionization energy and is easily oxidized if oxygen exists in the contacting layer. Fig. 46 shows the cross-sectional TEM views and depth profiles of a Ti-contact and a molybdenum (Mo)-contact source/drain. With a Ti-contact, the interface of Ti reacts with oxygen from the a-IGZO layer and generates a TiO_x layer about 20 nm thick. A poor-oxygen region can be observed in the a-IGZO layer. It is supposed that the Ti extracted the oxygen from the a-IGZO layer during the thermal process, and its extraction was not so uniform. On the contrary, there was no oxidized layer between Mo and a-IGZO layers in case of Mo-contact source/drain, and high stability is expected.

Fig. 47 shows the Vth variations of Ti-contact TFTs and Mo-contact TFTs before/after thermal annealing. This annealing was done to stabilize the a-IGZO layer, and the annealing temperature was 250 °C. The Vths of initial TFTs were almost 0 V, but some TFTs in the plate had large negative Vth shifts only in the Ti-contact case. It is supposed that the oxygen extraction from the a-IGZO layer increased the oxygen vacancies in the a-IGZO layer near the channel region, and made the TFT channel to the depletion mode easily in some parts of the plate. If there is a poor-oxygen region near the channel region, the TFT should be instable.

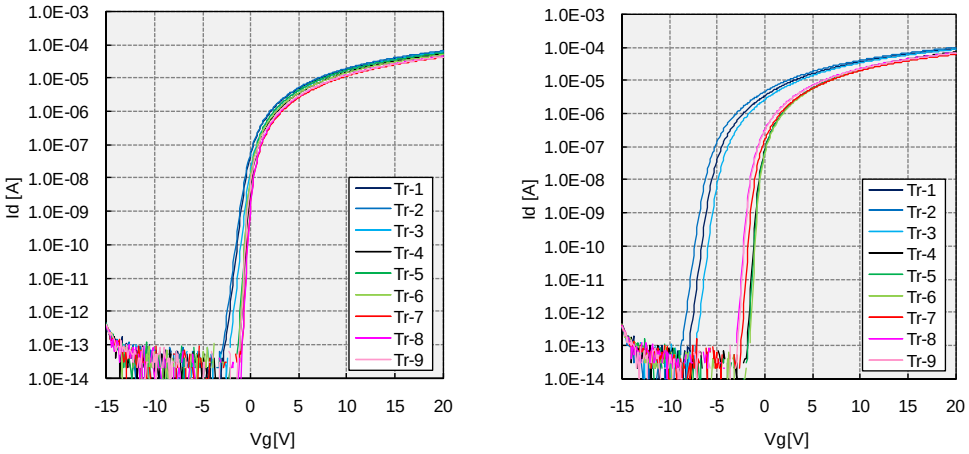


(a) Ti/Al/Ti source/drain.



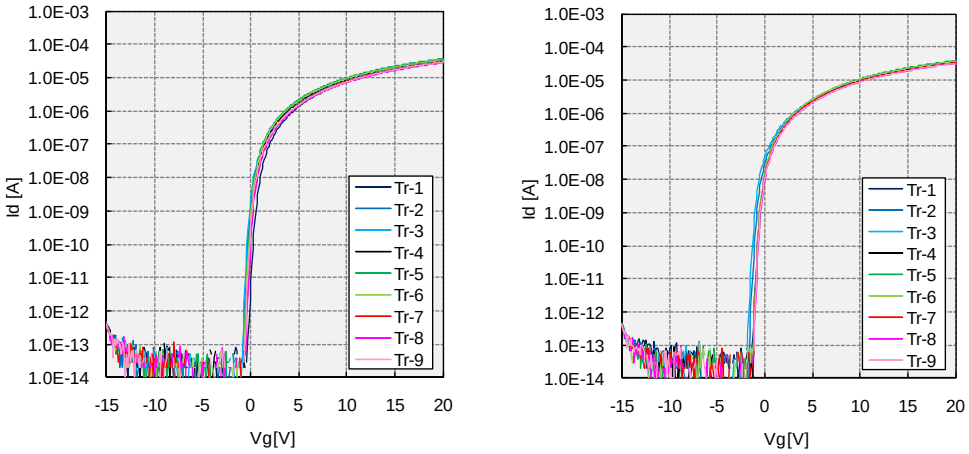
(b) Mo source/drain.

Fig. 46 Cross-sectional TEM views and EDX depth profiles of the source/drain.



<Before annealing> <After annealing>

(a) Transfer curves of Ti/Al/Ti source/drain.



<Before annealing> <After annealing>

(b) Transfer curves of Ti/Al/Mo source/drain.

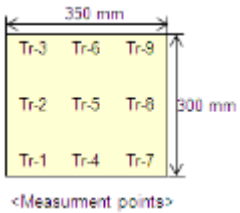


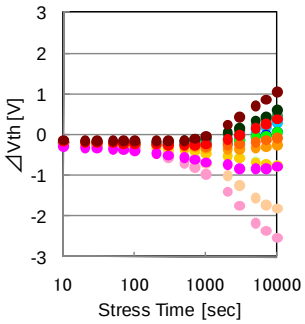
Fig. 47 Vth variation before/after thermal annealing.

In these measurements, Vd=10 V. TFTs of 9 points were located on the 300 × 350 mm substrates and were named from Tr-1 to Tr-9.

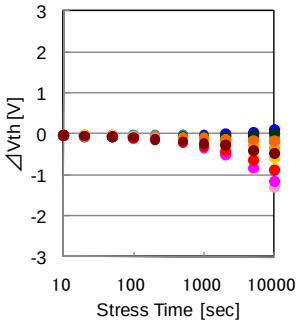
(c) Passivation material for high reliability

The passivating films for oxide semiconductor TFT are key technologies to improving reliability. A conventional SiN_x passivation deposited by CVD easily degrades TFT performance. It must be caused by its poor passivation ability in the face of oxygen or water penetration, and electron donors generated by the hydrogen in the SiN_x film or SiH_4 gas during film formation. Some researchers have reported that the Al_2O_3 (alumina) film deposited by atomic layered deposition (ALD) or SiO_x film deposited by rf sputter show good passivation properties [67, 68]. However, for large size FPD manufacturing, ALD and rf sputtering have several limitations for application in industry due to their difficulty of deposition over a large substrate. On the other hand, dc sputtering is widely adopted for FPD manufacturing, therefore a dc-sputtered Al_2O_3 was chosen as the passivation. Al_2O_3 is widely used as a surface protection material or a gas barrier film, and expected that it functions as the passivation material to the water and/or hydrogen diffusions, which change the properties of oxide semiconductor.

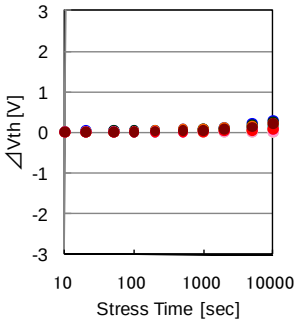
Fig. 48 shows the Vth shift after bias temperature stress (BTS). The bias, temperature, and period of BTS are Vg=0~15 V, Vd=0~15 V, 50 °C, 10,000 sec, respectively. The conventional SiN_x passivation with SiO_x underlayer showed large Vth shifts depending on the stress condition. These large shifts are supposed to be originated from the hydrogen diffusion from the SiN_x film. SiO_x passivation showed better reliability than the conventional CVD passivation, but had negative Vth shifts after BTS in the range of Vd larger than Vg. On the other hand, the Al_2O_3 passivation showed superior reliability in all bias ranges, and the Vth shifts after BTS were only 0.2 V at the maximum. Al_2O_3 is known to have negative fixed charge, however does not seem to adversely affect the TFT characteristics and the reliability. This might be caused by the TFT structure that the Al_2O_3 film is used as a passivation so as not to directly contact with the channel layer. When the current flow of the driving TFT was set to 2.2 μA with the TFT size of W (width)/L (length) = 20/8 μm, the extrapolated shift is smaller than 1 V even after 100,000 hours, if the square of the shift is in proportion to the square of the stress time (Fig. 49 (a)). Similarly, when the gate bias and drain bias were set to 15 V, the extrapolated shift is almost 1 V even after 100,000 hours, if the square of the shift is in proportion to the square of the stress time (Fig. 49 (b)). These values are enough small for driving AM-OLED displays.



(a) CVD SiN_x/SiO_x passivation.



(b) rf-sputtered SiO_x passivation.



(c) dc-sputtered Al_2O_3 passivation.

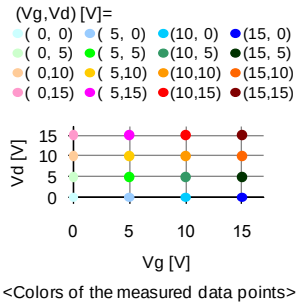
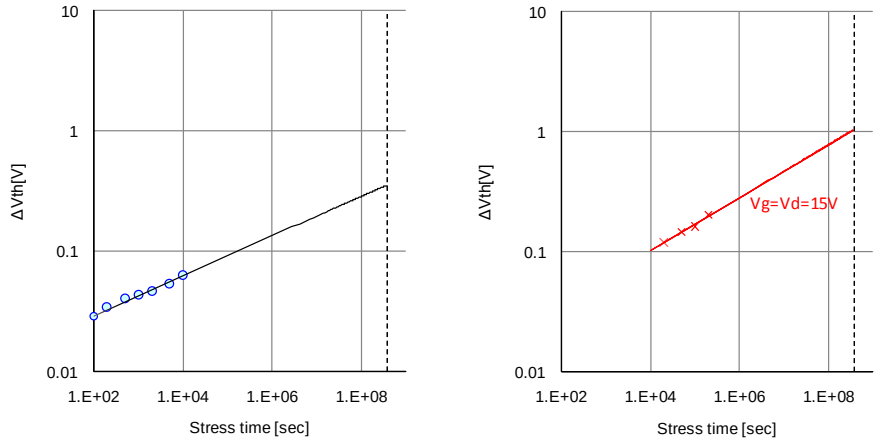


Fig. 48　Vth shifts for various passivation after BTS.

Vg and Vd were set from 0 V to 15 V at 5 V steps, and the stress temperature was 50˚C.



(a) Id=2.2 μA setting case (b) Vg=Vd=15 V setting case

Fig. 49 Estimated Vth shift after 10 years.
A solid line means the extrapolated Vth shift calculated from the data until 1E+04 sec.

Fig. 50 summarizes the BTS test results of five types of TFTs: LTPS, μc-Si, and a-Si TFTs as references, and Al_2O_3-passivated a-IGZO and SiNx/SiO_2-passivated a-IGZO TFTs. For the TV application, 100,000 hours reliability with an on-current of 10E−6 A at a temperature of 50 °C was assumed for each pixel. For the DS TFT in the compensation circuit of the pixel, the same bias was applied for gate (Vg) and drain (Vd) keeping 10E−6 A in case of LTPS, micro-crystalline, and amorphous Si TFTs. In case of oxide TFTs, 15 V was applied for both Vg and Vd, because the degradation of oxide TFT is mainly dominated by the Vg, and this bias stress condition was standardized for oxide TFTs. A threshold voltage shift (ΔVth) was observed for 10,000~200,000 sec and extrapolated to 3.6E8 sec. The calculated ΔVth of Al_2O_3-passivated a-IGZO TFT after 3.6E8 sec stress was only 1.0 V, which value is almost same as those of crystallized Si TFTs. In case of SiNx/SiO_2-passivated a-IGZO, the ΔVth was too high for the AM-OLED displays; however, it was smaller than that of a-Si TFT in the short range. It means that this structure can be applied for the LCDs from the reliability point of view. The inclination of the line for SiNx/SiO_2-passivated a-IGZO was quite different from those of other lines. This fact indicates that the degradation mechanism of the SiNx/SiO_2-passivated a-IGZO TFT includes different degradation factor from that of other TFTs; however it is not clarified here. The inclination of the line for SiNx/SiO_2-passivated a-IGZO was quite different from those of other lines. This fact indicates that the degradation mechanism of the SiNx/SiO_2-passivated a-IGZO TFT includes different degradation factor from that of other TFTs; however it is not clarified here.

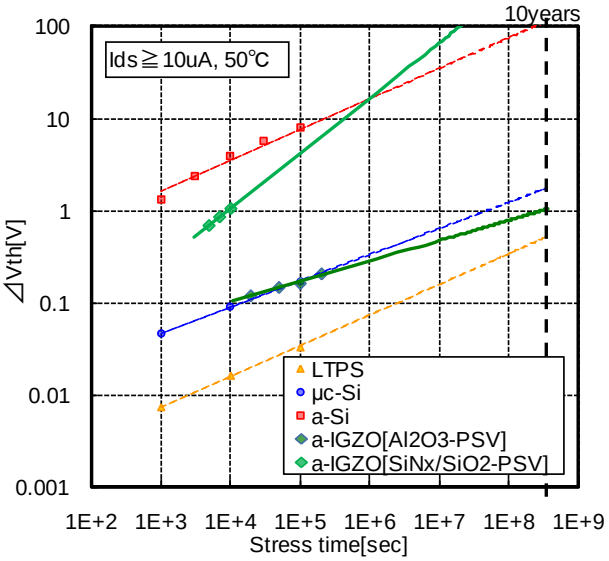


Fig. 50　Vth shifts after BTS tests of LTPS, μc-Si, and a-Si TFTs as references, and Al_2O_3-passivated a-IGZO and SiNx/SiO_2-passivated a-IGZO TFTs.

Fig. 51 shows the hysteresis of the transfer curve. In this measurement, the gate bias was swept from negative to positive and then positive to negative immediately. There was no difference in Vth between both directions, indicating that this TFT does not have severe charge trapping and has enough clean interfaces.

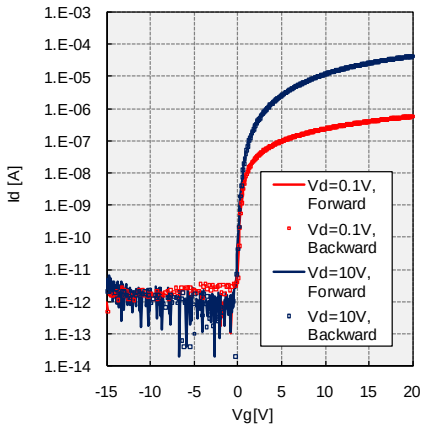


Fig. 51　Hysteresis of transfer curves.
Vg was swept from −15 V to +20 V, and then swept from +20 V to −15V immediately.
Vd was set at 0.1 V and 10 V.

It is known that the oxide TFT has photo leakage and negative Vth shift due to the shorter wave length light irradiation than about 440nm [61]. This value is due to

the band gap of oxide material, but the displays require the short wave length irradiation for the blue color image.

Fig. 52 shows the transfer curve under the light illumination. A 10,000 nit of cold cathode fluorescent lamp (CCFL) was irradiated from the top of TFT. CCFL is widely used as the backlight of LCD and emits wide range of wave length from 380nm to 720nm. However, its photo leakage and Vth shift were almost negligible (the Vth shift was smaller than −0.02 V).

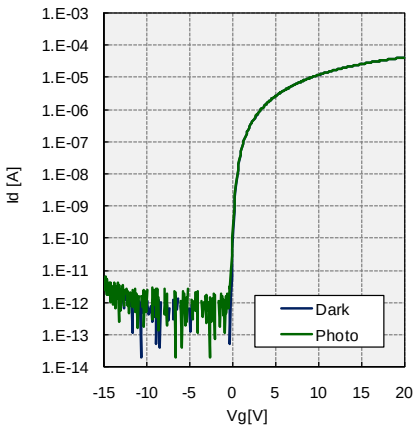


Fig. 52 Transfer curves in dark and photo irradiated conditions.
As a photo irradiated condition, 10,000 nit of CCFL was irradiated from the top of the TFT in the measurement of transfer curve.

And the bias stress test was executed under the light illumination. A negative gate bias instability under the light illumination is widely studied in these years [62]. All of the existing results show large negative Vth shifts by the negative gate bias stress under the light illumination. This instability is not only serious problem for LCD with high power backlight but also important for OLED, because the emitted light by EL layer can irradiate to the channel layer of TFT. Fig. 53 shows the result of negative gate bias stress test under light illumination. A negative gate bias stress test was executed irradiating a light from the top of the TFT. The stress conditions are −20 V of gate bias, 10 V of drain bias, and 10,000 nit of CCFL irradiation. Its Vth shift was only −0.2 V after 10,000 sec stress. This value is over 1 order of magnitude smaller than the reported values. It is supposed that the some of the measures for the BTS also affected to the negative gate bias stress under the light illumination, because the Vth shift by the negative gate bias under the light illumination has been known to be affected by the

environmental humidity [62], but the Al_2O_3 passivated TFT should not be affected so much by the environmental humidity due to the high passivation property of Al_2O_3.

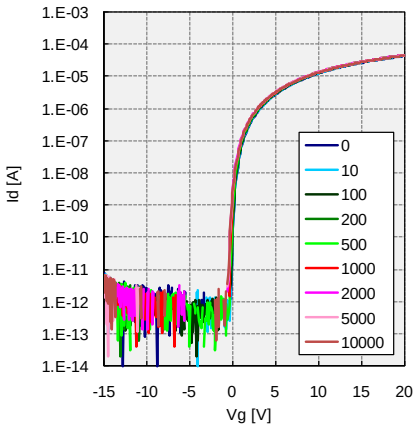


Fig. 53 Transfer curves after bias stress test under the light illumination. As a stress condition, Vg and Vd were set at −20 V and +10 V, and 10,000 nits of CCFL light was irradiated from the top of the TFT.

(d) Etching stopper and TFT design

When Al_2O_3 is used as the passivation, there are some issues in the Al_2O_3 deposition and patterning. To deposit Al_2O_3 film using dc sputtering, the deposition rate of Al_2O_3 film by Ar/O_2 reactive sputtering is not so high. Moreover, the etching rate of Al_2O_3 is low during patterning, so the Al_2O_3 film should be thin from the manufacturing point of view. Fortunately, even thin Al_2O_3 film around 10 nm has a good barrier property, but the source/drain must be relatively thick because of the need for complex driving of the compensation circuit, and this thickness results in a coverage problem at the edge of the source/drain. Here, the thickness of source/drain is designed to be from 450 nm to 900 nm, and the passivation is designed to be thinner than 300 nm. If the oxide semiconductor has poor passivation near the channel, the Vth easily shifts due to the stress during the fabrication process and the driving operation. Fig. 54 shows the Vth shifts of various source/drain designs. If the edge of the source/drain is directly mounted on the oxide semiconductor, the passivation ability is degraded because of the poor step coverage of thin Al_2O_3 film at the edge of pattern. The degradation of the passivation ability affects the Vth shift in the reliability tests. For example, Vth shifts after the temperature humidity storage (THS) test of Type A design and Type B design were very large. The temperature, humidity and period of THS were 60 °C, 90 %, and 100 hours, respectively. Therefore, the Type C design was chosen from the viewpoint of stability. In this case, the channel layer (the yellow area in Fig. 54) is covered with an etching

stopper or source/drain as the first layer, and covered again with the passivation as the second layer (Fig. 55). SiO_x is adopted for the etching stopper so as not to degrade the TFT performance, because this etching stopper also acts as a passivating film during the TFT manufacturing process. The etching stopper is not only relatively thinner than the source/drain and also has good tapered sides, so the passivation ability is better than the conventional design. The Vth shifts of the Type C design were very small and are applicable to the AM-OLED displays.

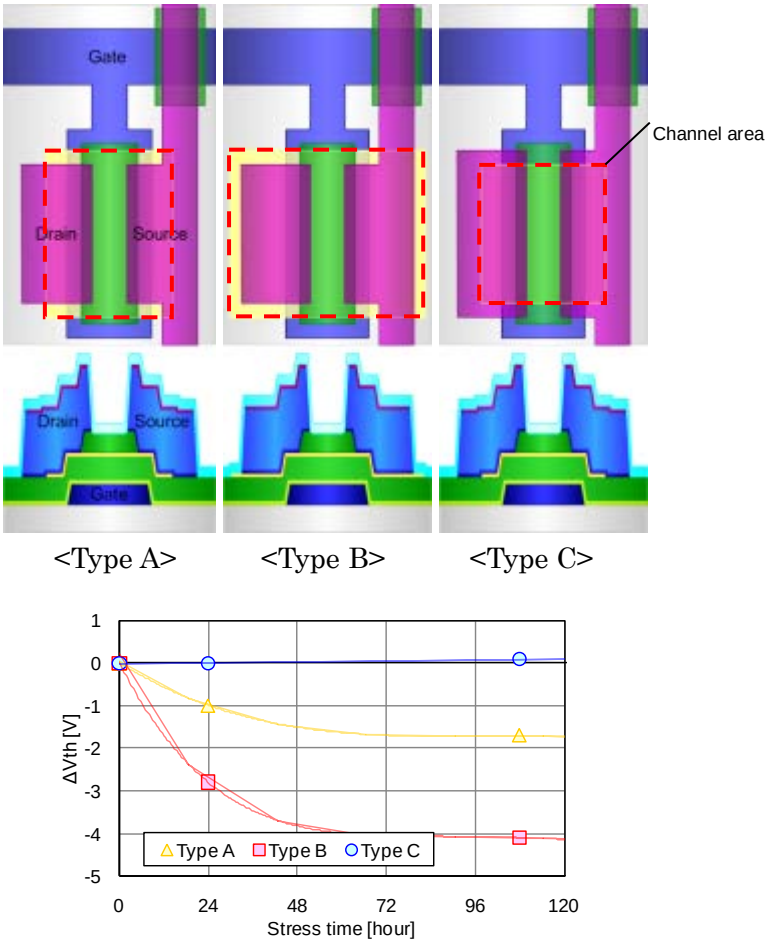


Fig. 54　Vth shifts of various TFT design in the HTS test.
Type A is a conventional design. In type B, the exposed channel area was expanded. In type C, the channel area was fully covered with etching stopper or source/drain.

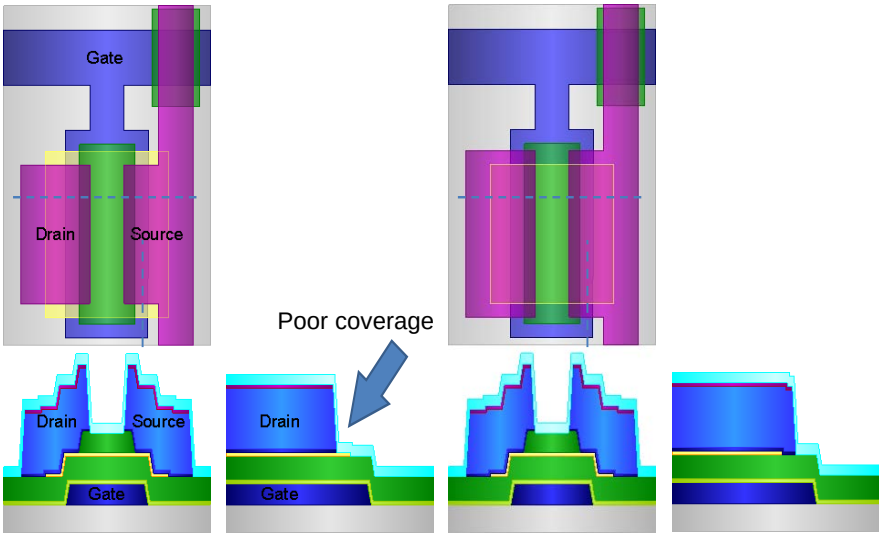


Fig. 55　Estimated design difference for the Vth degradation in the HTS test.

(e)　TFT uniformity

Fig. 56 shows the transfer curves of the optimized TFT structure and process. The mobility was 11.5 cm^2/Vs, the S factor was 0.27 V/decade, and the Vth was 0.3 V. TFTs have high uniformity both over the short range and the wide range. The wide range uniformity of on-current at 5 V of gate bias was smaller than 5 % in case of Gen. 1 substrate (300 mm x 350 mm). If the gate bias was higher than 10 V, the uniformity of on-current was smaller than 3 %. This uniformity is enough small even for the current driven AM-OLED displays.

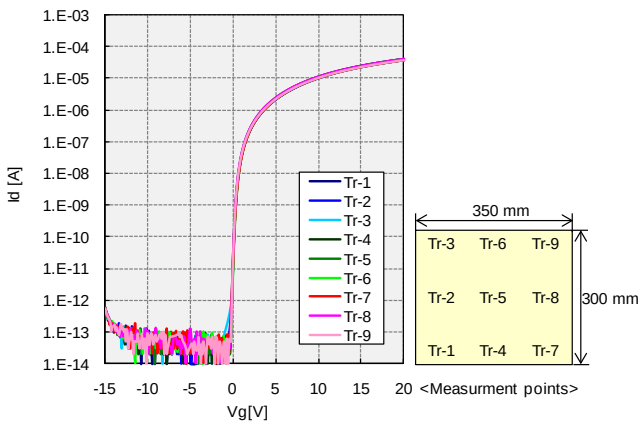


Fig. 56　Transfer curves and measurement points.
TFTs of 9 points were located on the 300 × 350 mm substrates and were named from Tr-1 to Tr-9.

(f)　11.7-inch diagonal AM-OLED prototype

Fig. 57 shows the compensation circuit with 2 transistors and 1 capacitor (2Tr1C) in a pixel. And a top emission structure was adopted for the EL device. According to these two technologies, high production yield by a simple pixel circuit and wide aperture EL emission which is not affected by the bottom layered pixel circuit were achieved. These two technologies also contribute to realize high resolution AM-OLED display.

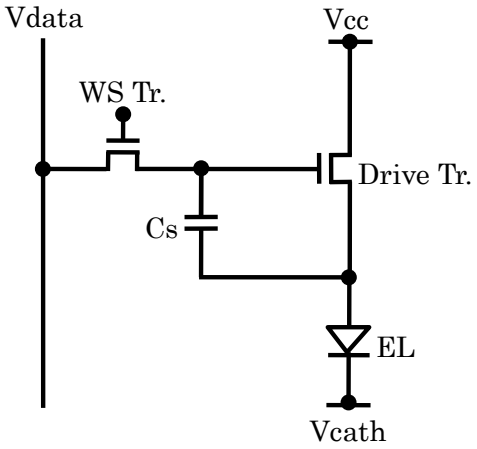


Fig. 57　2Tr1C pixel circuit.

Fig. 58 shows an 11.7-inch diagonal qHD a-IGZO TFT driven AM-OLED prototype and Table 8 shows its specification. Even in the dc mode driving, the brightness uniformity was only 10 % in wide distribution. This panel has a peak luminance over 600 cd/m^2 and a color gamut exceeding 100 % of the NTSC triangle.

Fig. 58　11.7-inch diagonal qHD a-IGZO TFT driven AM-OLED display.

Table 8　Specifications of the 11.7-inch diagonal a-IGZO TFT driven AM-OLED display.

Panel size	11.7-inch (297 mm) diagonal
Format	qHD
Resolution	960 RGB x 540
Brightness	All white: 200 cd/m^2 Peak : > 600 cd/m^2
Contrast	> 1000000 : 1 (Dark)
Number of colors	10 bit RGB
Color saturation	> 100% (NTSC)

(g) Summary

As a result, a highly reliable oxide semiconductor TFT for AM-OLED display was developed. A-IGZO was applied as the channel material and the TFT showed the mobility of 11.5 cm^2/Vs, the S factor of 0.27 V/decade, and the Vth of 0.3 V. A dc-sputtered Al_2O_3 passivation, an etching stopper type highly protective TFT structure, and a stable source/drain material realized superior reliability, indicating a possibility of a lifetime over 10 years. An 11.7-inch diagonal qHD AM-OLED display was fabricated using these technologies and demonstrated its performance. This highly reliable oxide semiconductor technology is expected to contribute to the spread of AM-OLED displays and high performance AM-LCDs.

3-3-2. High mobility oxide material

It has been reported that the TFT using amorphous In–Ga–Zn–O (a-IGZO) as a channel material has a higher mobility than 10 cm^2/Vs [47, 64, 69]. This value is enough for the pixel circuit of the ultra-high definition, 240 Hz driving AM-OLED display; however, higher mobility is expected for the higher definition, higher frame rate AM-OLED displays or the driver-circuit integration. A driver-circuit integration has been studied for the cost reduction and the increase of the panel-design flexibility [70, 71]. A mobility higher than 30 cm^2/Vs is expected for the driver-circuit integration because a higher current flow is required for the driver circuit than that for the pixel circuit. When a low mobility material is used for the driver circuit, it is necessary to make the gate-insulator thickness thinner and the TFT size larger to keep the power consumption; however, the former causes low breakdown voltage and a large parasitic capacitance at the electrode overlap and the latter causes a wide area occupied by the peripheral circuit.

To solve these problems, it is valuable to develop a high mobility TFT with high reliability for the circuit integration. A composition of In–Sn–Zn–O (ITZO) is a good candidate as a high mobility channel material [72, 73, 74, 75]; however, the TFT reliability for the driver-circuit of the AM-OLED display was an issue to be solved.

Here, a new composition ratio of ITZO is adopted as a channel material of the high mobility TFT and its reliability is studied and confirmed for the use of the inverter circuit [76, 77].

(a) Driver circuit integration

For the driver circuit integration, a scanner is designed with a combination of an inverter, a shift register, and a logic circuit. The oxide TFT is normally an n-channel transistor, because a high-performance p-type semiconductor is difficult to realize [78, 79]. Therefore, the inverter of the peripheral circuit must be formed by the n-channel inverter. Fig. 59 shows an n-ch inverter diagram for the driver circuit of the AM-OLED display. According to this circuit design and high performance TFT which has high mobility around 30 cm^2/Vs, the driver circuit can be integrated in several millimeters of width around the panel in case of UWXGA (1600 × 768 pixels) AM-OLED display.

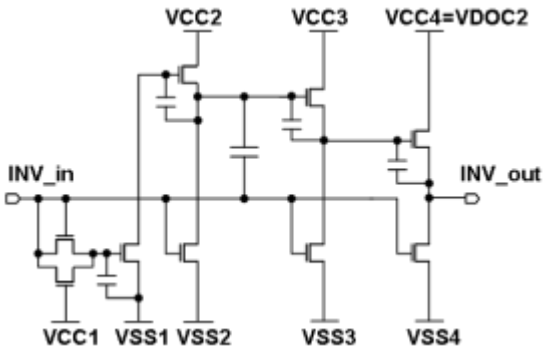


Fig. 59　n-ch inverter diagram.

An n-ch inverter is used in the driver circuit of the 8-in. UWXGA AM-OLED display.

(b)　a-ITZO TFT and its reliability

To realize high mobility TFT, a composition of ITZO was applied for the channel material. It has been reported that a TFT with ITZO channel material exhibited a high mobility of 24.6 cm^2/Vs [74] and a high reliability [75], but its composition ratio (In : Sn: Zn = 36.5 : 15 : 48.5; supplied by Idemitsu Kosan CO., Ltd) is formulated to achieve higher mobility than 30 cm^2/Vs to reduce the peripheral driver circuit area, and to achieve enough high reliability for the AM-OLED display driving. It is supposed that the carrier concentration in the channel increase by using Sn instead of Ga, and the mobility also increase. Fig. 60 shows hall mobility measurement data of the amorphous ITZO (a-ITZO) and a conventional a-IGZO. It indicates a-ITZO has higher hall mobility than a-IGZO. This might be caused by the fact that the 5s orbital of Sn is larger than 4s orbital of Ga.

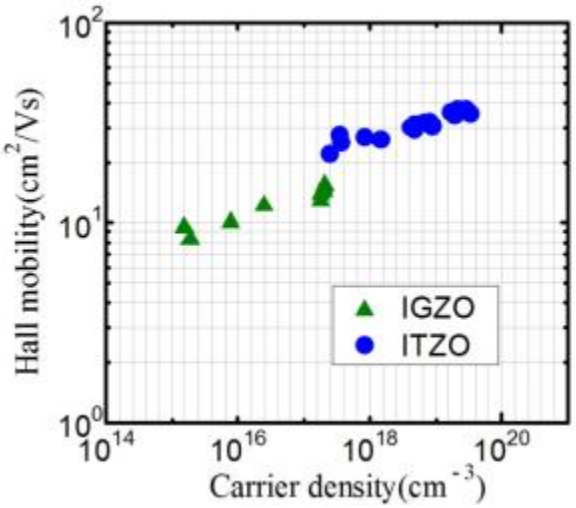


Fig. 60　Carrier density and hall mobility.

It is concerned that the weak binding energy between Sn and oxygen might affect the TFT performance, because the binding energy of SnO is 486 eV and is much smaller than 1118 eV for Ga_2O_3. However, by increasing the O_2 flow during deposition, a larger process window for the O_2 partial pressure than that of a-IGZO is confirmed with higher mobility than a-IGZO TFT (Fig. 61).

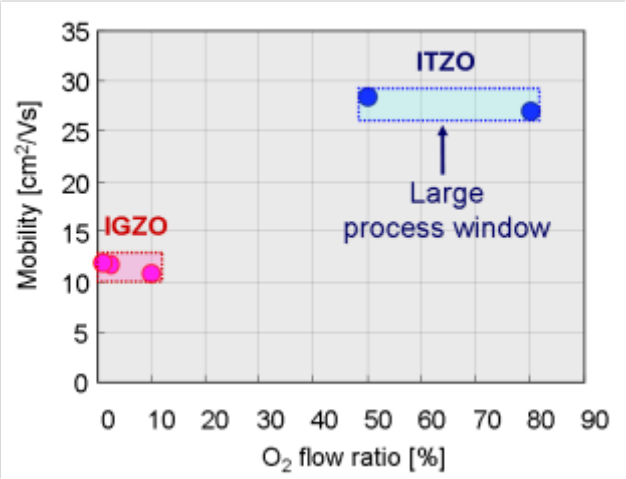
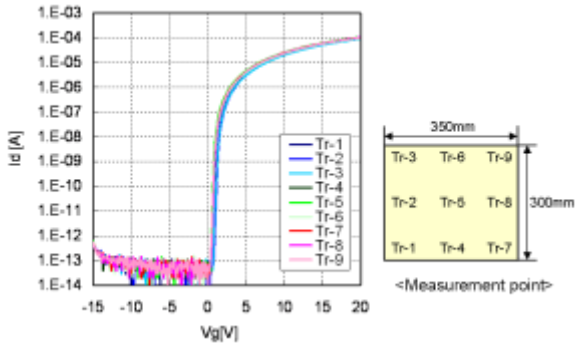
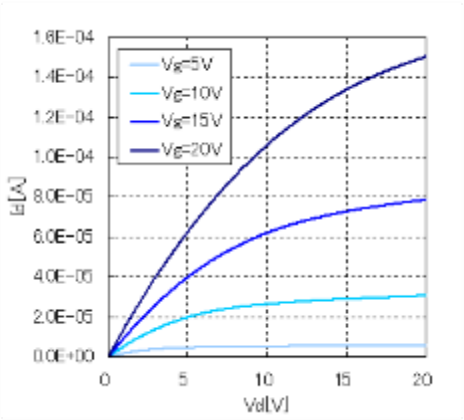


Fig. 61 Process window for the O_2 flow ratio.
The a-ITZO TFT realized high mobility with larger process window than a-IGZO.

Fig. 62 (a) shows the transfer curves of the optimized TFT structure and the process. The mobility was 30.9 cm^2/Vs, the sub-threshold swing value (S factor) was 0.21 V/decade and Vth was 0.97 V. The TFTs show a low off-current because they do not exhibit inversion p-channel operation by the negative gate bias due to a density of state (DOS) above the valence-band maximum (VBM) [78]. They also show very high uniformity. The wide-range uniformity of the on-current at Vg = 20 V was smaller than 4% for a first-generation substrate (300 × 350 mm). Fig. 62 (b) shows the output (Id–Vd) characteristics of one of the TFTs. It was confirmed that the TFT had good ohmic contact between the source/drain electrode and the channel material indicated by the linearity of the output characteristics near Vd = 0 V.



(a) Id-Vg characteristics.



(b) Id-Vd characteristics.

Fig. 62 TFT characteristics.

(a) Id–Vg characteristics with a drain bias of 10 V. TFTs of nine points were located on the 300 × 350 mm substrates and were named Tr-1 to Tr-9. (b) Id–Vg characteristics for a gate bias of 5~20 V.

Fig. 63 shows the time evolution of the threshold voltage shift (ΔVth) under a bias-temperature stress (BTS). The bias, temperature, and period of the BTS are Vg = 0~15 V, Vd = 0~15 V, 50°C, and 0~20,000 sec, respectively. As a result, the TFT exhibited superior reliability even though the low binding energy of SnO, and the ΔVth after BTS test were smaller than 0.1 V. Because it is greatly different from the a-IGZO film deposition in the oxygen partial pressure at the time of the a-ITZO film deposition, it is supposed to be important how to introduce oxygen in the a-ITZO film. When the current flow of the driving TFT of an AM-OLED pixel circuit was designed to 0.6 μA/μm (the current flow per unit width of a TFT), the extrapolated shift is smaller than 1 V even after 100,000 hours, if the model for the time evolution of ΔVth is a power-law approximated from a stretched exponential model (Fig. 64).

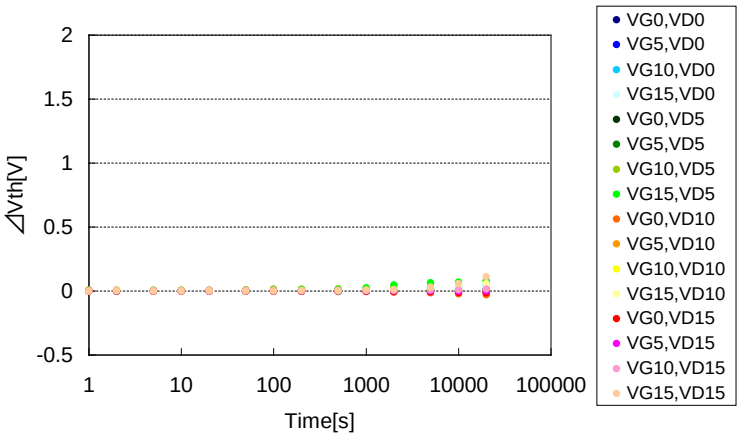


Fig. 63　Time evolution of ΔVth under BTS.
Vg and Vd were set from 0 to 15 V at 5V steps, and the stress temperature was 50°C.

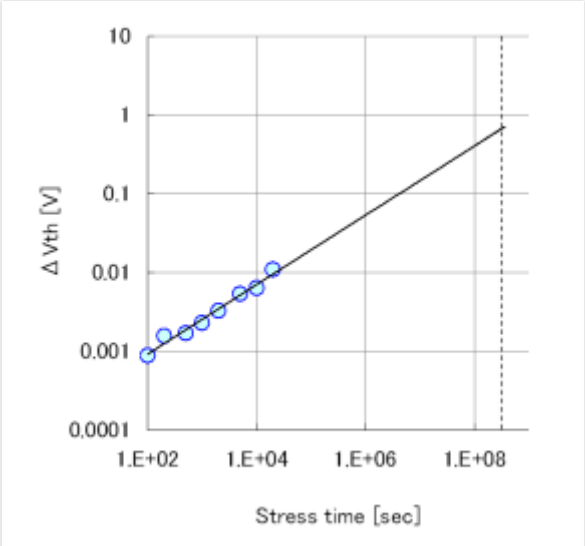


Fig. 64　Estimated Vth shift after 10 years.
The solid line represents the extrapolated Vth shift calculated from the data for 20,000 sec.

It has been reported that the light-induced hysteresis characteristic of oxide TFTs results from initially trapped charges at the deep trap site of the interface by effective trapping events due to the light illumination [79]. Therefore, the hysteresis characteristic of an a-ITZO TFT under photo-irradiated conditions was investigated.

Fig. 65 shows the hysteresises of the transfer curves for the dark state and the illuminated state. This TFT is different from the TFTs of Fig. 62. In this measurement, the gate bias was swept from negative to positive and then positive to negative

immediately and 10,000 nits of light from a cold-cathode fluorescent lamp (CCFL) was irradiated from the top of the TFT. There was no difference in Vth from both directions for each state. This indicates that this TFT does not show significant charge trapping and has a sufficient amount of clean interfaces.

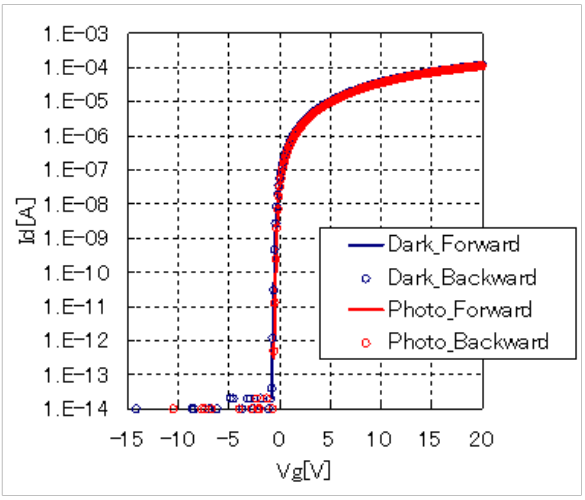


Fig. 65 Hysteresises of transfer curves.
Vg was swept from –15 to +20 V, and then swept from +20 to –15 V immediately. 10,000 nits of light from a CCFL was irradiated from the top of the TFT in the photo state.

(c) Scanner-integrated 8-in. UWXGA AM-OLED display

A scanner-circuit-integrated 8-in. UWXGA (1600 × 768 pixels) AM-OLED display was fabricated. It adopts high-mobility and high-reliability a-ITZO TFT (Fig. 66). The pixel circuit is composed of two transistors and one capacitor (2Tr1C), and the scanner is composed of a combination of the n-channel inverter, shift register, and logic circuits. The availability of a novel channel material with high mobility and high reliability allows the scanner to be integrated onto the TFT backplane.

Fig. 66　Scanner-integrated 8-inch diagonal UWXGA AM-OLED display.

Table 9　Specification of the scanner-integrated 8-inch diagonal AM-OLED display.

Panel size	8-inch
Format	UWXGA
Number of pixels	1600 × 768
Resolution	221 ppi
Pixel circuit	2Tr1C
Gate driver	Built-in

(d) Summary

As a result, a high mobility a-ITZO TFT driven driver-circuit integrated AM-OLED display was developed. A new composition of ITZO TFT realizes a high mobility of 30.9 cm^2/Vs, and the TFT achieves high reliability with a ΔVth smaller than 0.1 V after 20,000 sec of BTS. Its photo-stability was also high, and shows no hysteresis in the transfer curve measurement with the 10,000 nits of CCFL light irradiation. An 8-inch diagonal UWXGA AM-OLED display was fabricated using these technologies and demonstrated its performance. This driver-circuit integration technology with highly reliable high mobility oxide semiconductor TFT technology is expected to realize low cost, narrow bezel, flexible panel-designed AM-OLED displays.

3-3-3. Crystalline oxide material

As an oxide material for the TFT, several components of IGZO or ITZO have been widely studied in the amorphous phase [47-49, 63-66, 68, 72-77]. The feature of the amorphous oxide material is the high mobility in spite of the low temperature formation; however, its advantage against the crystalline oxide material would be the stability and the uniformity of the applied device. As the micro-crystalline Si TFT keeps the uniformity of amorphous Si TFT and the stability of LTPS TFT, it is supposed that a micro-crystalline oxide material may keep the stability and the uniformity in the TFT characteristics.

Here, a new crystalline In–Ga–O (c-IGO) material was adopted as a channel material of the TFT [81]. To maintain the low temperature fabrication process, its composition was formulated. An oxide TFT process, merging the fabrication processes of source/drain (S/D)-contact hole and gate contact hole was also proposed for the c-IGO TFT. The crystalline IGO has a high hall mobility and high etching selectivity to SiO_2 etchant (dilute HF; DHF), and metal etchant (phosphoric, acetic and nitric acid; PAN). When the etching stopper and the gate insulator are etched at the same time, the source/drain-contact areas of semiconductor have to be fabricated with high etching selectivity to underlayers. It is generally told that the grain boundary of poly-crystalline semiconductor interrupts the current conductivity. For example, the poly-crystalline ZnO is hard to be applied for TFT because of the low mobility due to the grain boundaries and the instability of the poly-crystalline structure [82]. However, the In_2O_3 based crystalline IGO maintains the high mobility even though it also has the grain boundaries. The c-IGO shows superior TFT characteristics.

(a) Crystalline IGO

A composition of IGO was evaluated as a poly-crystalline oxide semiconductor (supplied by Idemitsu Kosan CO., Ltd). It is well known that the role of Zn in IGZO is suppressing crystallization of In_2O_3, and the role of Ga is stabilizing oxygen for the strong binding energy. So IGO could be expected as a stable poly-crystalline semiconductor with high reliability. The features of this material are as follows. (1) By adjusting sputtering condition, the film state whether amorphous or poly-crystalline can be controlled, and the crystalline IGO is not etched by the HF treatment. (2) The hall mobility of this material is much higher than that of a-IGZO and has wide process window. Fig. 67 is the relationship between carrier concentration and hall mobility of poly-crystalline IGO and a-IGZO. The hall mobility of a-IGZO increased from 10 to 15 cm^2/Vs by decreasing the O_2 partial pressure at the deposition process. In the case of

c-IGO, the oxide films possess the higher mobility than a-IGZO at any deposition condition by optimizing the composition. Fig. 68 shows a relationship between hall mobility and etching rate by DHF (0.5%) of promising oxide semiconductors. Though the amorphous material like a-IGZO or a-ITZO is easily etched by DHF, only the poly-crystalline IGO has the high resistance to DHF with high hall mobility. Fig. 69 shows a relationship between the etching rate by DHF and the etching rate by PAN. Only the poly-crystalline IGO has the high resistance to both DHF and PAN. These chemical characteristics affect to the TFT fabrication methods. The c-IGO has a chance to create new TFT fabrication methods and decrease the photolithography processes.

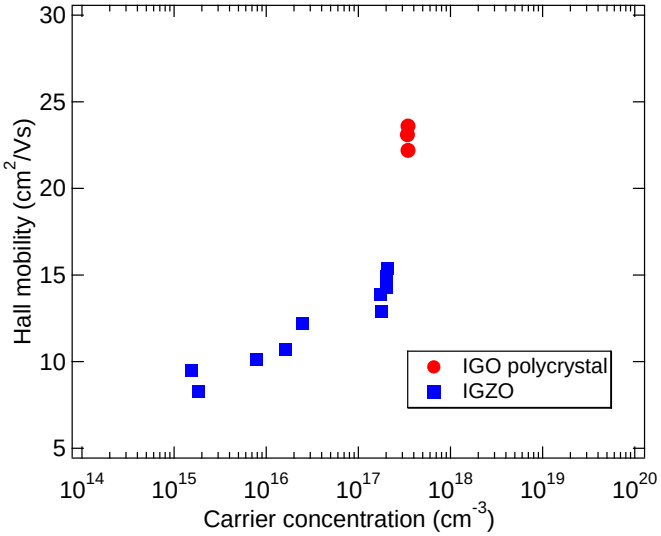


Fig. 67　Carrier concentration and hall mobility.

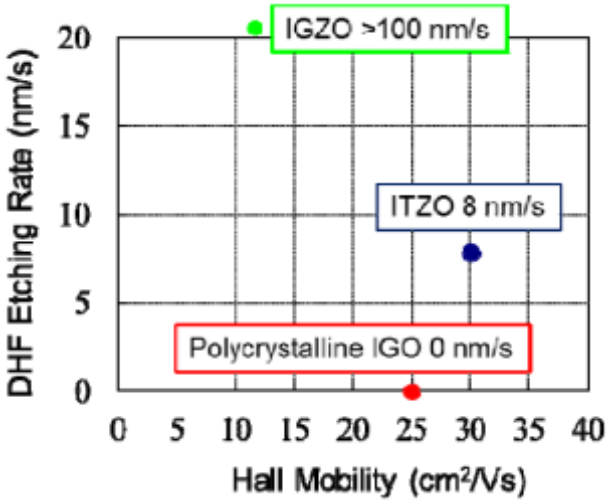


Fig. 68 Hall mobility and DHF (0.5%) etching rates of various oxide semiconductor materials.

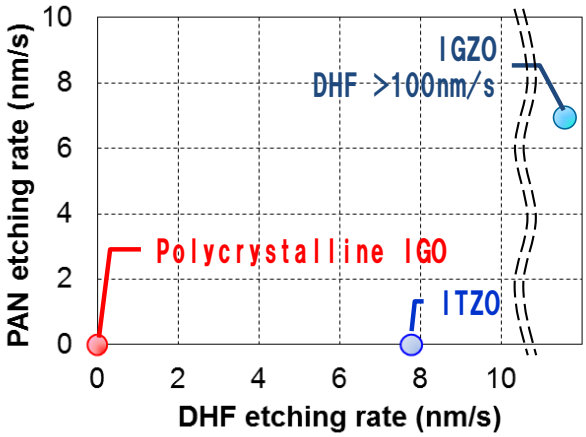


Fig. 69 Wet etching rate comparison of c-IGO, a-ITZO and a-IGZO.

Fig. 70 is an XRD spectrum of poly-crystalline IGO film. The peaks of plane In_2O_3 (222) and plane (400) indicate the high quality bixbyite structure. Fig. 71 is a top and cross-sectional view of the c-IGO film. The poly-crystalline IGO film is made up of large grains (surrounded by red solid line), the diameter is a few microns. And the large grain consists of a lot of rod-like structures with the asteriated alignment, the length and width are about 2 μm and a few hundreds nm respectively. In the rod-like structure, there are many sub-grains with the pillar structure. This complex sub-structure looks like the structure of ITO (In–Sn–O) film. In case of ZnO, the defects at the grain boundaries are thought to interrupt the carrier conduction. It causes low hall mobility to the thin ZnO film, because the grain size decreases in proportional with the film

thickness. But the hall mobility of c-IGO of which the thickness is less than 50 nm was high, about 25 cm^2/Vs. There is a possibility of two mechanisms about the origin of high mobility of c-IGO. One is explained by the amorphous IGZO theory, incorporation of heavy metal cations with large principal quantum number as reported by Hosono et al. [82]. The principal quantum number of In and Zn are 5 and 4 respectively, and the influence of crystalline axis mismatch may be small at the grain boundary of poly-crystalline IGO. The other is the difference of crystalline structure between In_2O_3 and ZnO. The symmetry of bixbyite structure is much lower than wurtzite structure of ZnO.

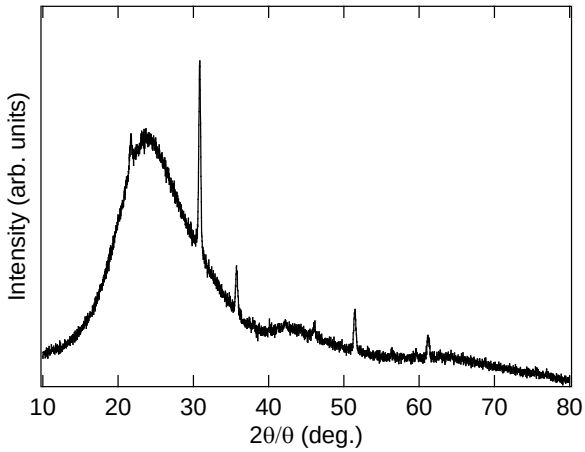
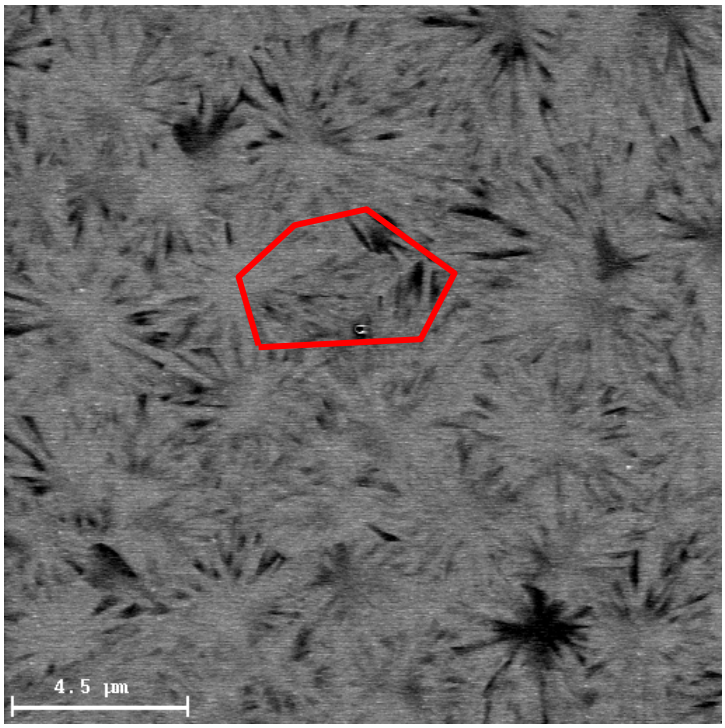
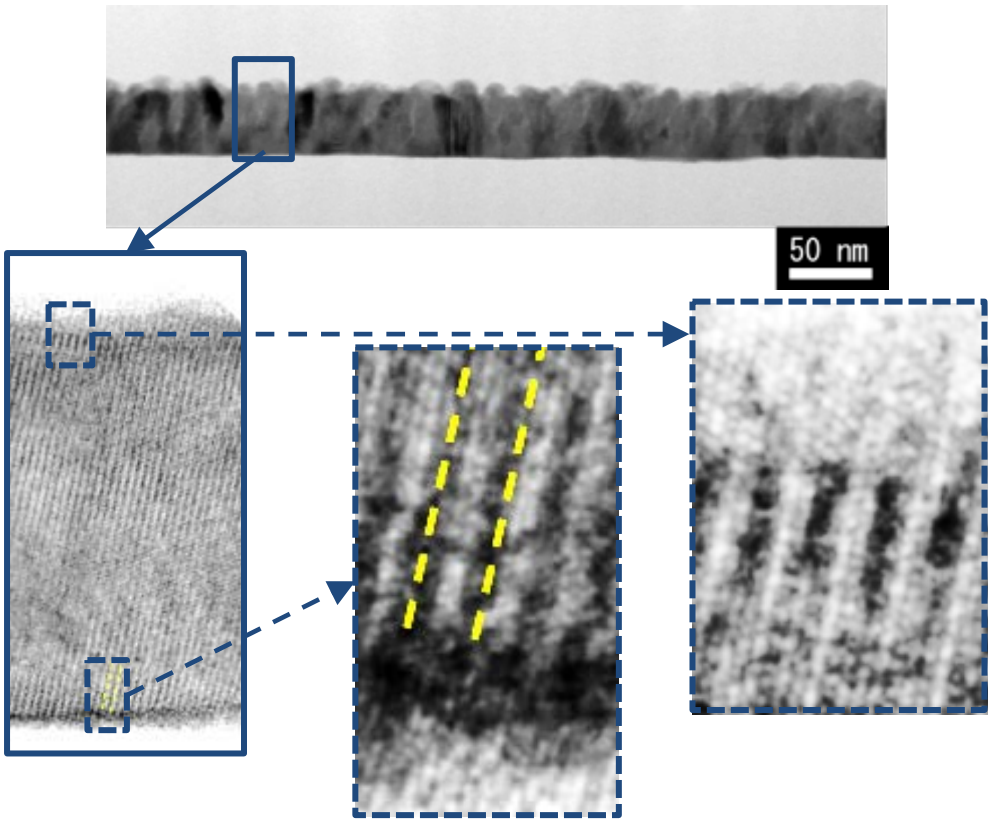


Fig. 70　XRD spectrum of poly-crystalline IGO film on glass.



(1) Top view



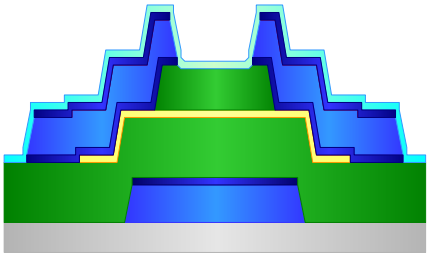
(2) Cross-sectional view

Fig. 71 (1) Top view of c-IGO film (red line : grain boundary of large grain) and (2) Cross-sectional TEM image of c-IGO films.

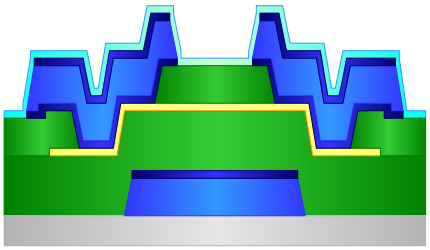
These mechanisms motivated the evaluation of poly-crystalline IGO-TFT with high mobility enough for the AM-OLED driving.

(b) TFT structure for c-IGO TFT

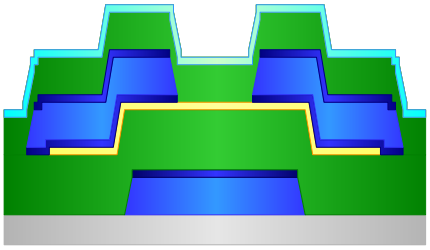
As a TFT structure, an etching stopper type was evaluated to achieve high reliability for the AM-OLED display driving [18, 75]. Fig. 72 indicates the cross section of etching stopper type TFT (1), etching stopper type TFT (2), and back channel etching type TFT. The etching stopper acts as not only an etching stopper but also a passivating film against the environmental effect. As the result of the back channel etching type TFT evaluation, the reliability and uniformity of transfer characteristics were not enough for the AM-OLED display, even though the back channel etching type TFT is preferable from the cost point of view. The etching stopper type TFT (1) requires the excess process for the fabrication of the etching stopper (Fig. 73 (A)), which indicates the increase of the process cost. Therefore, a cost down method for the etching stopper type TFT was evaluated. The SiO_2 films are used as the etching stopper and the gate insulator, and are etched by BHF (buffered HF). And the poly-crystalline IGO has high chemical resistance to BHF. By utilizing the character of poly-crystalline IGO, the processes of source/drain-contact holes fabrication (etching the stopper) and gate contact holes fabrication (etching the gate insulator) are merged (Fig. 73 (B); etch stopper type TFT (2)). This process realizes the low cost device with high reliability and uniform TFT characteristics.



(A) Etching stopper type TFT (1)



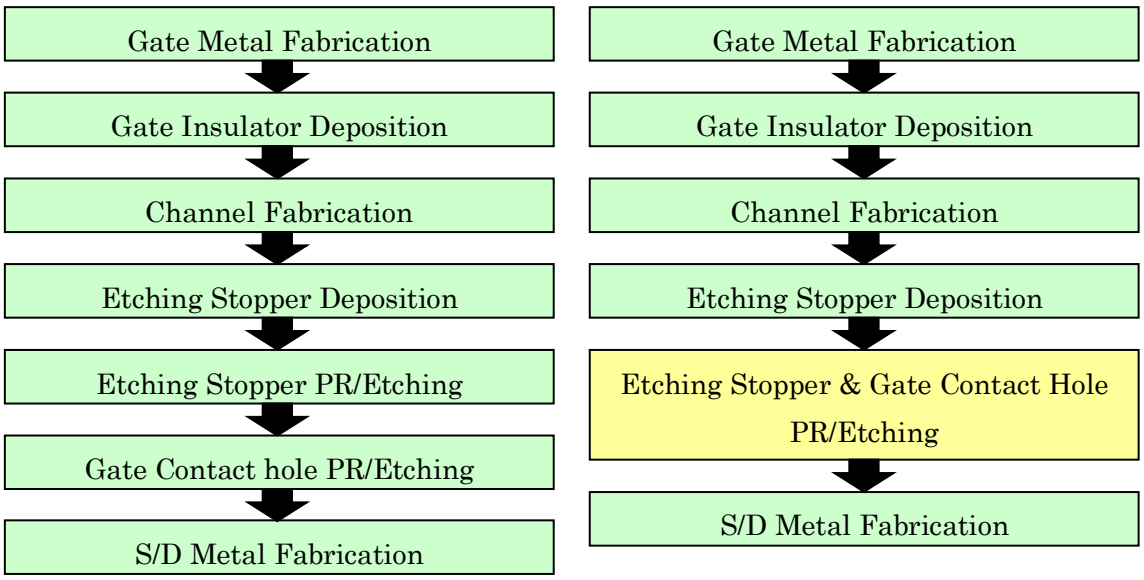
(B) Etching stopper type TFT (2)



(C) Back channel etching TFT

Fig. 72　Cross-sectional view of TFT.

Structure (B) and (C) realize the reduction of lithography process.



(A) Standard process flow (B) Merged process flow

Fig. 73 Process flow (A) standard process (B) merged process.

(c) Crystalline IGO TFT and its reliability

To fabricate the etch stopper type TFT (2), the damage at the source/drain-contact area during the etching process and the effect of grain boundary of poly-crystalline IGO were the key issues. Fig. 74 is a transfer characteristic of c-IGO TFT over Gen. 1 substrate fabricated with the structure of Fig. 72 (C). The mobility was 23.8 cm^2/Vs, Vth was −0.1 V and S-value was 0.30 V/dec. And the uniformity of the mobility over the Gen. 1 substrate (300 mmx350 mm) was ±0.86 cm^2/Vs. This high mobility agreed with the high hall mobility, meaning that the effects of grain boundaries were small.

Fig. 75 is the Vth shift after positive BTS (bias temperature stress) test. The bias, temperature and period of BTS are Vg=5~15 V, Vd=5~15 V, 50 °C, 10,000 s, respectively. The Vth shift was less than 0.3 V. Fig. 76 is the transfer characteristic after PBTS (Vg=Vd=15 V, 10,000 s). The Vth shift is so small that the c-IGO TFT can be applied to the backplane of AM-OLED display. And the result indicates that there are not serious damage at the S/D contact hole fabrication process and the defect nucleation at the grain boundary. The result of the Vth shift after positive BTS was a little worth than that of a-IGZO and a-ITZO. Shown in Fig. 71 (2), the rod-like structure of the c-IGO film is a little disordered in the initial grown region. The control of this incubation layer might be effective for the reliability improvement like the as-deposited micro-crystalline silicon; however it is not clarified in this study.

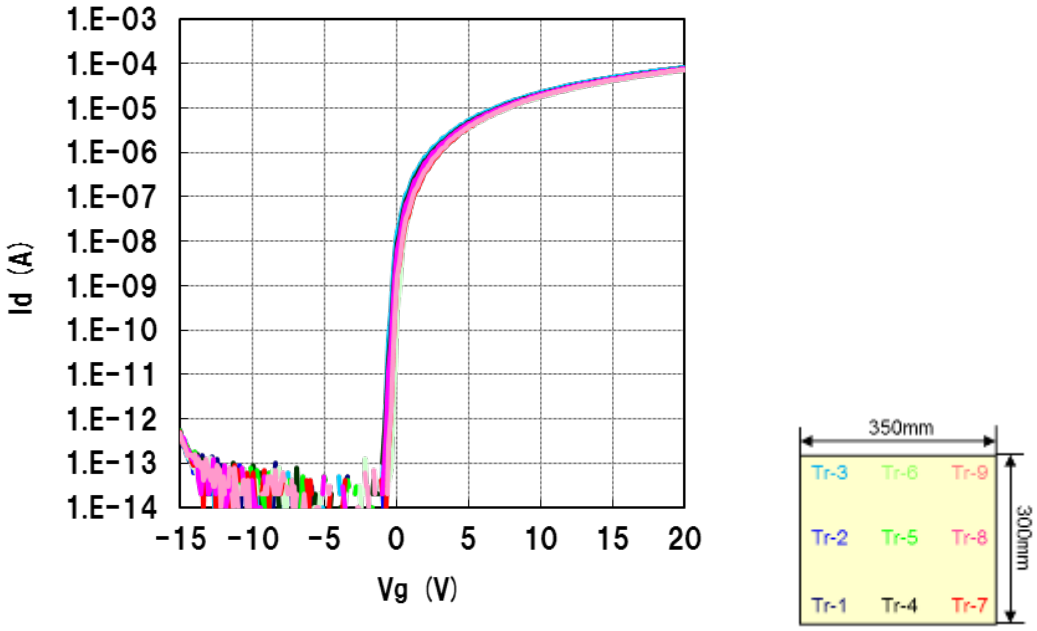


Fig. 74 Transfer characteristic of c-IGO TFT over Gen. 1 substrate (9 points).

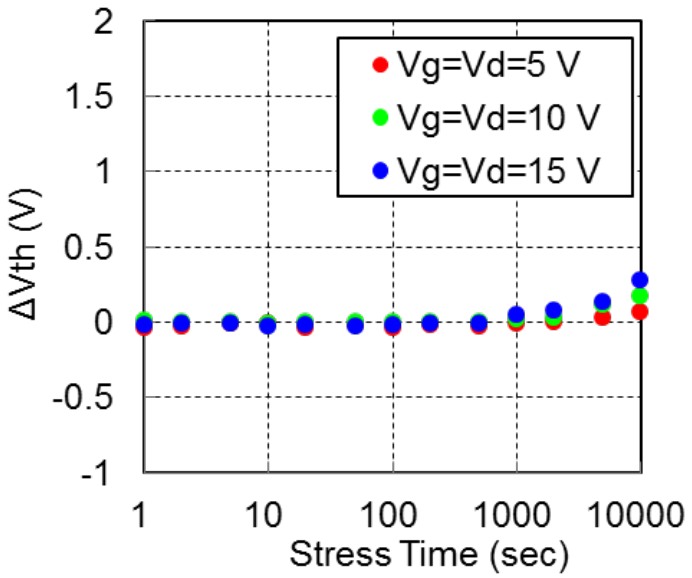


Fig. 75 Vth shift during the BTS.

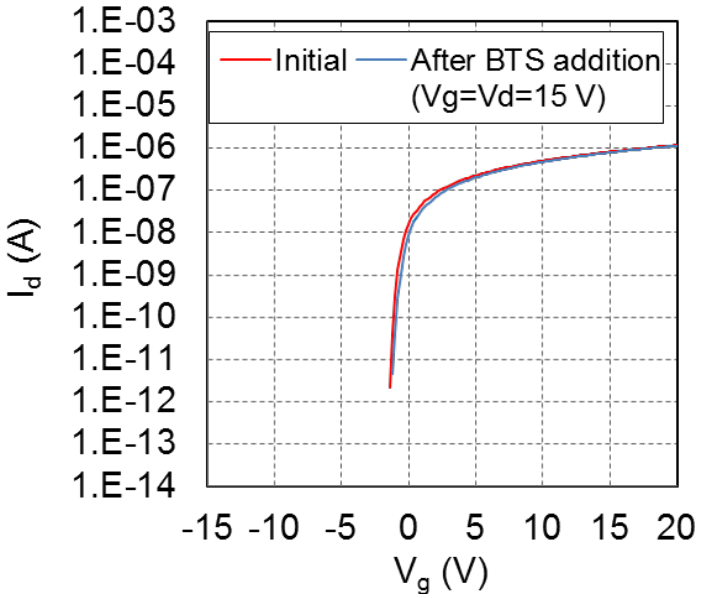


Fig. 76　Vth shift after PBTS (Vd=Vg=15 V, 10,000 s).

This high mobility and high reliability TFT with c-IGO channel is suitable for the AM-OLED display.

(d)　Crystalline IGO TFT driven 9.9-in. qHD AM-OLED display

By using these technologies, an AM-OLED display with c-IGO channel TFT was fabricated (Fig. 77). Table 10 shows the specification of 9.9-inch diagonal AM-OLED display. The pixel circuit consists of 2 transistors and 1 capacitor (2Tr1C).

Fig. 77　9.9-inch diagonal qHD AM-OLED display with c-IGO TFT.

Table 10　Specification of the 9.9-inch diagonal AM-OLED display with c-IGO TFT.

Panel size	9.9-inch diagonal
Format	qHD
Number of pixels	960(H)×540(V)
Resolution	111ppi
Pixel circuit	2Tr1C

(e)　Summary

A high mobility TFT with the poly-crystalline IGO channel was developed. This device reduced the photolithography process by merging the S/D-contact holes and gate contact holes fabrication. It demonstrated that the oxide material, which has high etching selectivity to the electrode or insulator, gives a potential to realize valuable functions to the TFT structure or process. The mobility of this TFT was about 3 times higher than that of the conventional TFT with a-IGZO channel, and the reliability at the BTS test was enough high for the TFT driving AM-OLED display. The 9.9-inch diagonal AM-OLED display with the improved TFT structure was fabricated. These results indicate that the c-IGO TFT is a promising candidate for the high performance and low cost AM-OLED display fabrication.

3-3-4. Issues in the manufacturing

According to the first report of a-IGZO TFT, it was known that the amorphous oxide semiconductors can achieve good TFT characteristics easily, and a lot of studies came to be done afterwards. Its reliability was the most serious issue for applying it into display manufacturing; however, several measures for the reliability came to be developed these days. However, there are some problems still more for manufacturing display devices, such as manufacturing cost or manufacturing stability.

(a) Cost reduction for the manufacturing

When applying the oxide TFT to the display industry, it is better to use the existing infrastructure for the conventional a-Si TFT or LTPS TFT to suppress the investment cost and to simplify the installation of the new oxide TFT process. Because of the similarity to the process flow of the oxide TFT, it is better to use a-Si TFT production line to save the additional investment cost. Table 11 shows the most distinctive differences in the process flow between a-Si TFT and oxide TFT.

Table 11 Most distinctive differences in the process flow between a-Si and oxide TFTs.

	a-Si TFT	Oxide TFT
TFT structure	Back Channel Etch type	Etching Stopper type
Differences		
1. Gate insulator	CVD: SiNx	CVD: SiOx
2. Channel	CVD: a-Si	PVD: Oxide
3. Contact layer	CVD: n+ a-Si	-
4. Etching stopper	-	CVD: SiOx
5. Passivation	CVD: SiNx	PVD: AlOx
6. Thermal anneal	~230˚C/N_2	~300˚C/Air,O_2

* SiNx: silicon nitride, SiOx: silicon oxide, AlOx: alumina.

In the case of a-Si TFT, a back channel etching type structure is often employed for the LCD to reduce the fabrication process steps. The insulators are deposited by chemical vapor deposition (CVD) apparatus and the silicon nitride is usually applied as insulator material because of its high dielectric constant for the high on-current or the high passivating properties. The channel layer is also deposited by CVD, and the n+ a-Si layer is required to be deposited on the channel, because of the reduction of the

contact resistance between channel layer and the source/drain metal, which will be deposited on the n+ a-Si layer. And the thermal annealing is required to make the TFT characteristics uniform. Lower temperature than 250˚C and the nitrogen-rich atmosphere is widely used.

On the other hand, in case of oxide TFT, an etching stopper type structure is normally employed to reduce the damages of the following fabrication processes to the channel oxide layer. The silicon oxide is usually applied as insulator material instead of the silicon nitride, because the highly concentrated hydrogen in the silicon nitride layer diffuses into the neighboring channel oxide layer and acts as electron donor, which makes the TFT leaky. The channel layer is deposited by a physical vapor deposition (PVD: Sputter) apparatus. An alumina is applied as the passivation because of its high passivating property, and this passivation layer is also deposited by the PVD apparatus [64]. Both the channel layer and the passivation layer are deposited by dc- or ac-mode to realize high deposition rate. The thermal annealing condition is also important and the high temperature, oxygen-containing thermal annealing is said to be better for improving the TFT reliability [59].

By utilizing the production infrastructure of the amorphous Si TFT, the production of the oxide TFT is enabled by only introducing PVD and high temperature annealing apparatuses basically (Fig. 78).

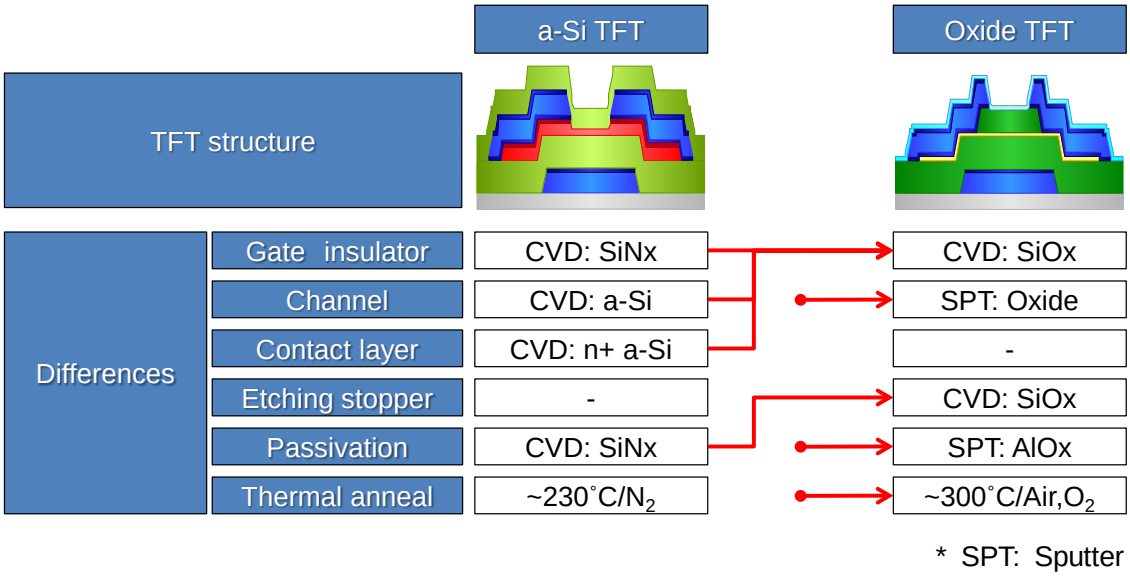


Fig. 78 Production shift from a-Si TFT to oxide TFT.

(b) Uniformity improvement in the large-substrate-based manufacturing

To realize oxide TFT driven large size display, the uniformity and the reliability of TFTs are the most important points. The slight variation in the TFT characteristics often leads to the large degradation of TFT reliability. However, high uniformity has not been required for the manufacturing of conventional a-Si TFT to drive an LCD. For the CVD, it is needed to change the insulator material from silicon nitride to silicon oxide to improve the reliability of the oxide TFT. Its film thickness, quality, and the plasma damage to the underlying channel layer are also effective to the TFT characteristics and the reliability; therefore, it is needed to develop the highly uniform deposition condition with high quality film properties. For the uniform CVD film deposition, it is expected to improve the plasma density uniformity and the gas flow uniformity in the process chamber of the CVD apparatus. For the PVD, it is needed to establish a highly uniform reactive sputtering method. In case of larger glass substrate than the Gen. 6 (1850 × 1500 mm), a multi cathode system is mainly employed [84, 85]. It is needed to find highly uniform deposition condition with this system, but the plasma variation due to the cathode position easily becomes an issue for the uniformity. For the uniform PVD film deposition, it is strongly expected to improve the plasma uniformity in the process chamber of the multi cathode type PVD apparatus. And for the thermal annealing, it is expected to install a new annealing apparatus with high temperature around 300˚C with oxygen-containing annealing condition.

As it has been mentioned above, though the process flow of the oxide TFT is similar to that of the a-Si TFT, some improvements of the production apparatuses are expected for the large size display production.

Recently, in view of the remarkable progress in the development of the oxide TFT technology [64, 18, 77, 81, 86], a trial of the oxide TFT technology installation to the high generation production line has been started. Fig. 79 and Table 12 show the improvement results of the TFT characteristics and the uniformity in the Gen. 6 (1850 × 1500 mm) production line. The conventional CVDs and PVDs, which are used for LCD manufacturing, were used for this study. The TFT characteristics of eight TFTs over the Gen. 6 plate are shown in a graph. Here, a-IGZO (In:Ga:Zn = 1:1:1) was employed as a channel material and an etching stopper type bottom-gate TFT was applied as a TFT structure. Although the TFT characteristics were worse than those of R&D line at the beginning (Step 1), but the uniformity could be improved by studying the deposition condition of CVD (Step 2). Since the reliability of this step was quite low, an Al_2O_3 passivation was applied (Step3) [64]. Finally, the uniform TFT characteristics over the large substrate with a Vth variation of 1 V could be achieved.

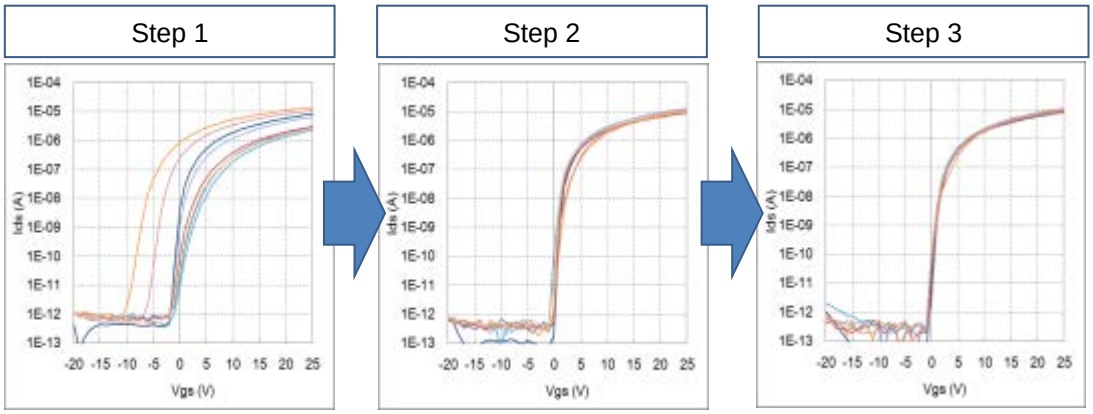


Fig. 79 Improvement results of TFT uniformity in the Gen. 6 production line.

Table 12 Improvement results of TFT uniformity in the Gen. 6 production line.

	Step 1	Step 2	Step 3
Vth LRU (V) (Max-min)	9.8	1.0	1.1
Ion LRU (%)	79	12	7.7
Mobility (cm^2/Vs)	2.1	11.6	10.1

* LRU: long range uniformity

As for the TFT performance, the reliability against the bias and humidity stresses was the most critical issue for the AM-OLED display. The reliability had been successfully improved drastically by adopting Al_2O_3 passivation [64]. However, it was the result of R&D with the small size substrate of Gen. 1. To achieve the similar results in the high generation production line, the process conditions after applying Al_2O_3 passivation process were optimized. Fig. 80 and Table 13 show the results of positive bias temperature stress (PBTS) test of the a-IGZO TFTs, which were fabricated in the Gen. 6 production line. Here, an etching stopper type bottom-gate TFT was employed as a TFT structure, and the positive gate bias was applied for the PBTS test so as to flow enough current for satisfying the highest luminance on the display specification. The threshold voltage shifts (ΔVth) were observed for 100 ~ 1,000,000 sec. The measured data tended to approximate into one line on the log-log plot, and were extrapolated to 3.16E8 sec from the last 3 data. When defining the lifetime of the display from the limit of the 3 V in ΔVth, the life time became in only 1,510 hours even if an Al_2O_3 passivation was applied (Step 2). This improvement ratio was around 3 orders in magnitude, but the lifetime was too short for AM-OLED display. Therefore, several manufacturing

processes were improved and finally 8.5 years lifetime could be achieved. Although this value is still worse than that of R&D result in Gen. 1 [64], enough to examine the AM-OLED display manufacturing start.

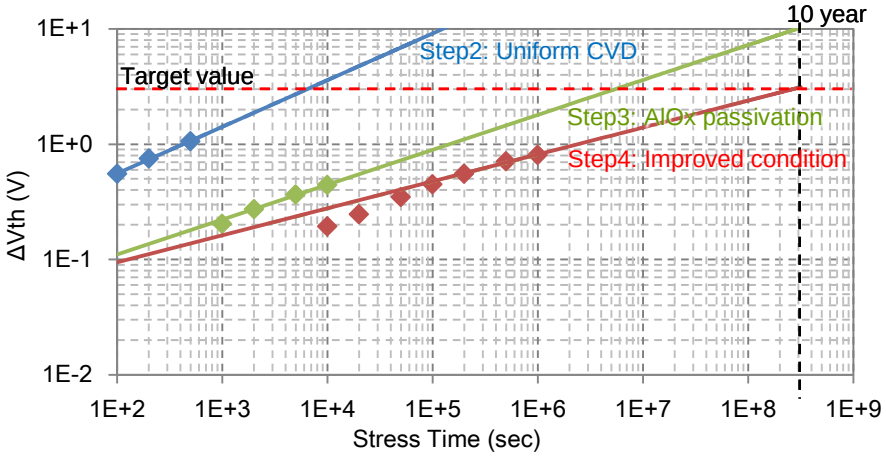


Fig. 80 Improvement results in Vth shifts after positive BTS tests.

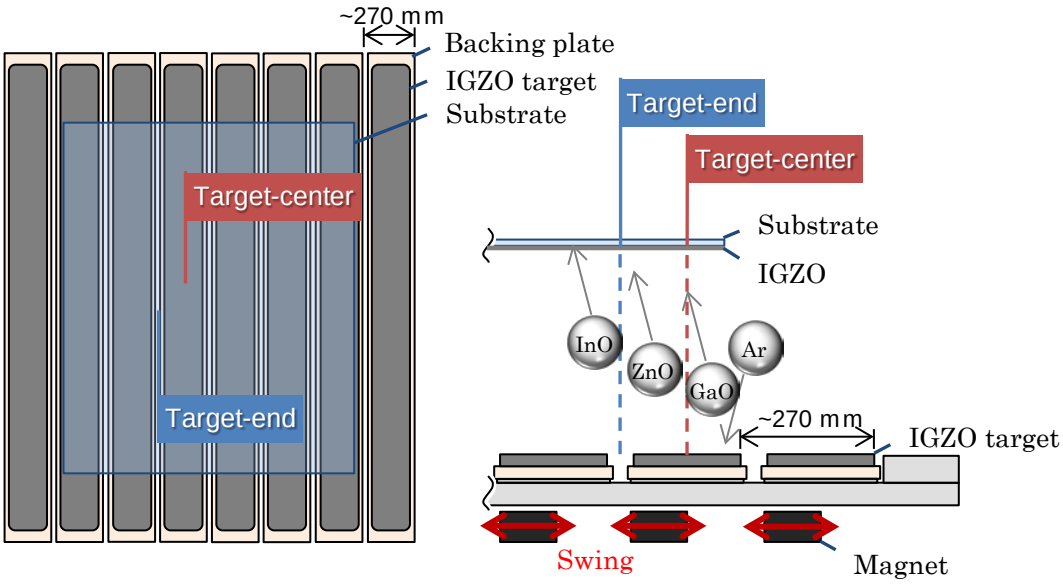
Table 13 Improvement results in the estimated life time.

	Step 1	Step 2	Step 3
Life time (hour) @ΔVth < 3 V	2	1,510	74,200

(c) Issue in the sputtering process

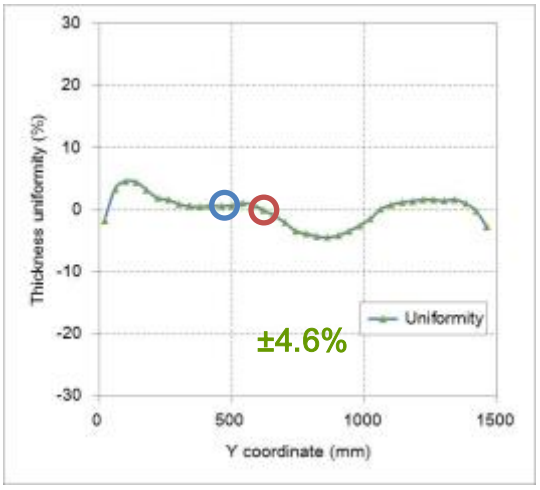
The uniformity and reliability became rather better than the initial, but further uniformity improvement was expected for PVD. In the a-IGZO sputtering, a multi-cathode type PVD system was used (Fig. 81 (a)). This system can realize globally uniform deposition over the large substrate; however, the sputtering conditions above the target-center and that above the target-end are supposed to be different (Fig. 81 (b)).

Fig. 82 shows the non-uniformity issue in the PVD system. Its thickness uniformity was ±4.6% for the horizontal direction (Y coordinate) measurement (Fig. 82 (a)). The thickness above the target-center and that above the target-end were almost same. However, the TFT characteristics had rather large non-uniformity (Fig. 82 (b), (c)). The threshold voltages of the TFTs varied more than 1V. The values of the threshold voltage had a periodicity in the Y coordinate, and the cycle was same as the target pitch. This non-uniformity is supposed to be caused by the plasma non-uniformity. By changing the sputtering condition, this value could be improved; however, further improvement is expected. It is expected to be developed a new PVD, which has uniform plasma over the large substrate entirely for the AM-OLED display.

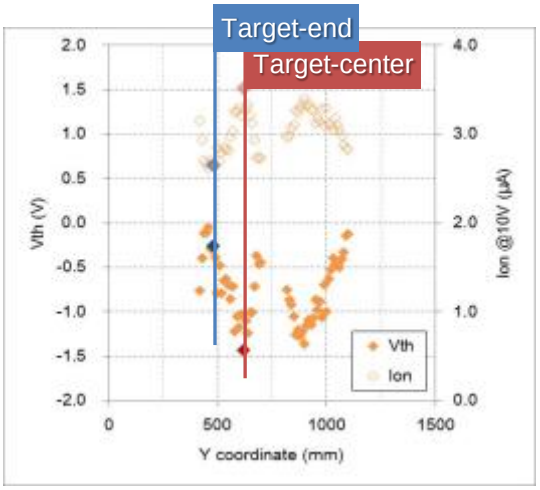


(a) Cathode structure (b) Sputtering diagram

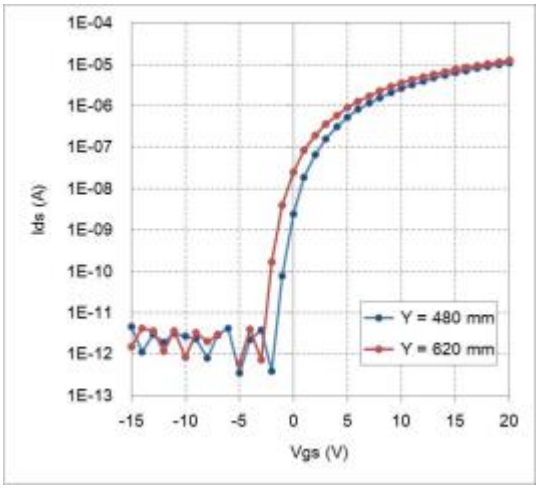
Fig. 81 Multi-cathode type PVD system.



(a) Thickness uniformity.



(b) Vth and Ion variations.



(c) Transfer curves of the TFTs at the target-center and the target-edge.

Fig. 82 Non-uniformity issue in sputtering.

(d) Large size AM-OLED prototypes

Fig. 83 shows 40-inch diagonal high resolution AM-OLED prototype, which was fabricated in the Gen. 6 production line. An etching stopper type TFT was employed as a TFT. This panel has a compensation circuit with two transistors in a sub-pixel, which is the minimum number for the compensation. This result indicated the potential of AM-OLED display manufacturing with a large substrate size.

Fig. 83 40-inch diagonal AM-OLED display fabricated in the Gen. 6 line..

Table 14 Specification of the 40-inch diagonal AM-OLED display fabricated in the Gen. 6 line.

Panel size	40-inch diagonal
Brightness	200 cd/m^2 (White) 600 cd/m^2 (Peak)
Color gamut	> 90% (NTSC)
Viewing angle	Brightness > 80%@45° $\Delta u'v' < 0.010$ @45°
Pixel circuit	2Tr2C

(e) Summary

A highly reliable oxide TFT technology for the AM-OLED displays was confirmed in the Gen. 6 production line. The uniformity improvement of the PVD system is still expected; however, the process conditions were improved and a large size AM-OLED prototype was successfully demonstrated. It indicated the possibility of low cost manufacturing of the AM-OLED display in the high generation production line.

3-3-5. New applications by oxide TFT driven AM-OLED display

The oxide TFT driven AM-OLED display is different from the existing a-Si or LTPS driven LCD both in the fabrication method and the device properties. Therefore, the new applications such as flexible [87, 88] or transparent [89] displays are expected using the unique properties of the oxide TFT or the OLED.

(a) Flexible AM-OLED display

As for the OLED is a self-emitting device, the OLED display does not need a back-light unit and has no viewing angle issue unlike LCD. Therefore, AM-OLED display is suitable for the flexible, foldable displays. It has been reported that flexible AM-OLED display using organic TFTs [90, 91], amorphous silicon (a-Si) TFTs [92], poly silicon TFTs [93, 94] and oxide TFTs [71, 95, 96] are developed over the past several years. Among these possibilities, oxide TFT is promising candidate for the backplane technology because of its high mobility, excellent stability and uniformity, simple fabrication process and possibility of large size backplane [64, 77, 81, 86]. Furthermore, the low process temperature of the oxide TFT process gives flexibility for the choice of the flexible substrate.

A flexible AM-OLED display has been demonstrated using etching stopper type bottom-gate oxide TFT. Fig. 84 shows the 9.9" diagonal qHD flexible AM-OLED display, and Table 15 shows its specification. Fig. 85 shows a schematic cross section of the display. A stacked top-emission structure was employed because it is advantageous to achieve a high resolution owing to the small footprint of a pixel in contrast to a side-by-side bottom-emission structure. The 20-μm-thick flexible substrate, on which oxide TFTs and OLEDs were integrated, and a 50-μm-thick color filter film were employed. As the flexible substrate, high heat-resistant resin with low thermal expansion coefficient was employed. TFT was fabricated on it with the same process as that for the glass substrate after the base coat process on the flexible substrate. The resultant thickness of the display was 110 μm. Comparing with the same type of display using a glass substrate, the weight and the thickness of the flexible display are less than one-fifth and less than one-tenth, respectively.

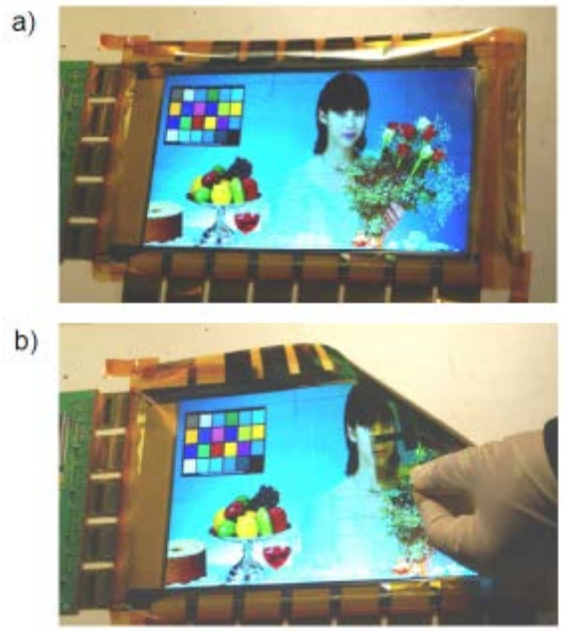


Fig. 84　9.9-inch diagonal qHD flexible AM-OLED display in (a) flat and (b) bending conditions.

Table 15　Specifications of the 9.9-inch diagonal flexible AM-OLED display.

Display Size	9.9”
Number of Pixels	960 × RGBW × 540 (qHD)
Pixel Size	228 μm × 228 μm
Resolution	111 ppi
Number of Colors	16,777,216
Operation Scheme	2Tr1C
Thickness	110 μm

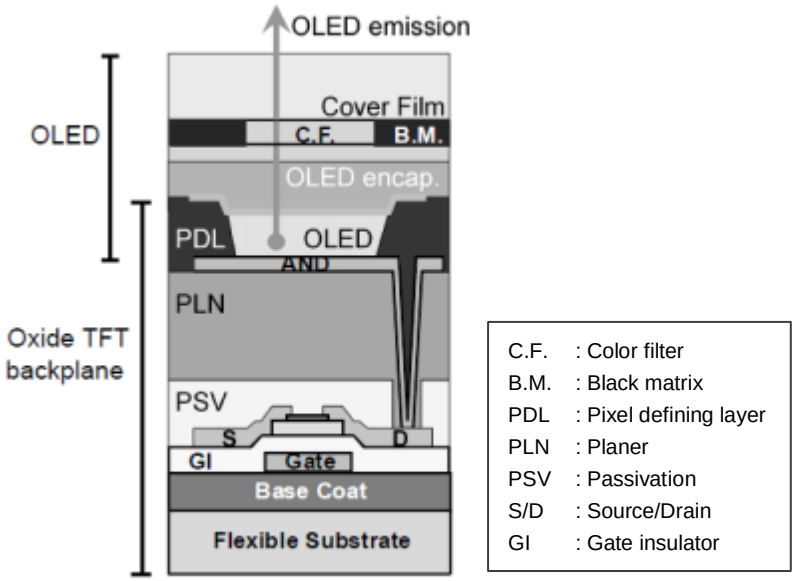


Fig. 85 Schematic cross section of the display.

(b) Flexible oxide TFT backplane

As a TFT, an etching stopper type bottom-gate TFT was employed for the flexible AM-OLED display. The TFTs were fabricated on a 300 mm × 350mm flexible substrate supported by glass substrate. A Mo film which was deposited by DC sputtering was used as a gate electrode. For the gate insulator, a silicon oxide film was deposited by plasma-enhanced chemical vapor deposition (PECVD) and then amorphous IGZO as a channel layer was formed by DC sputtering with Ar and O_2 gas mixture. The etching stopper film was deposited by PECVD. For source/drain (S/D) metal, titanium (Ti)/aluminum (Al)/Mo films were deposited by DC sputtering. After patterning of the S/D electrodes, DC sputtered Al_2O_3 as passivation (PSV) and a conventional photo-patternable resist as planarization layers (PLN) were formed. After the fabrication of through-holes, anode electrodes (AND) tied electrically to the drive TFT were formed and emission area was defined by the pixel-defining layer (PDL).

During the integration process, high overlay accuracy of less than ±1 μm was achieved because of the flexible substrate with low coefficient of thermal expansion (CTE), which is close to the glass substrate. As a result, a dense integration with a pixel pitch of 228 μm was achieved, which corresponds to a resolution of 111 ppi.

Fig. 86 (a) and Fig. 86 (b) show typical output and transfer characteristics of the oxide TFT after integration on the flexible substrate. The oxide TFT shows the field-effect mobility (μ), sub-threshold swing (S.S.) and on/off current ratio are 13.4 cm^2/Vs, 0.2 V/decade and 10^8, respectively (see Table 16). For a comparison of electrical

characteristics, the transfer characteristics of oxide TFT on the glass substrate are also plotted in Fig. 86 (b). It shows characteristics of oxide TFT on the flexible substrate is comparable to that on the glass substrate.

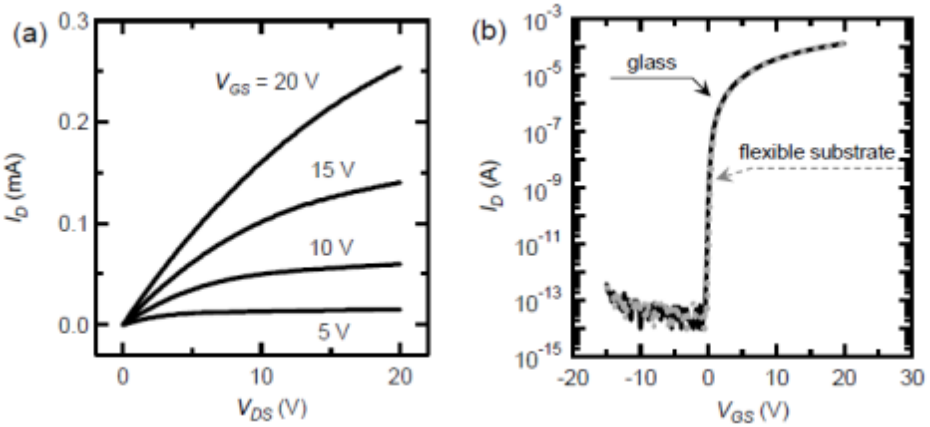


Fig. 86 (a) Output and (b) transfer characteristics of oxide TFT.

Table 16 Comparison of TFT performances on glass and flexible substrate.

Substrate	μ (cm^2/Vs)	S.S. (V/dec.)
glass	13.3	0.2
Flexible substrate	13.4	0.2

Fig. 87 (a) shows the transfer characteristics of 4 oxide TFTs after integration on the flexible substrate (300mm × 350mm). Uniform characteristics were achieved for oxide TFTs with a standard deviation of on-current of 5%. Fig. 87 (b) shows an optical micrograph of emission from the pixels in the display at the DC operation mode. The luminance of each pixel was uniform, which is strongly supported by the uniform characteristics of oxide TFT.

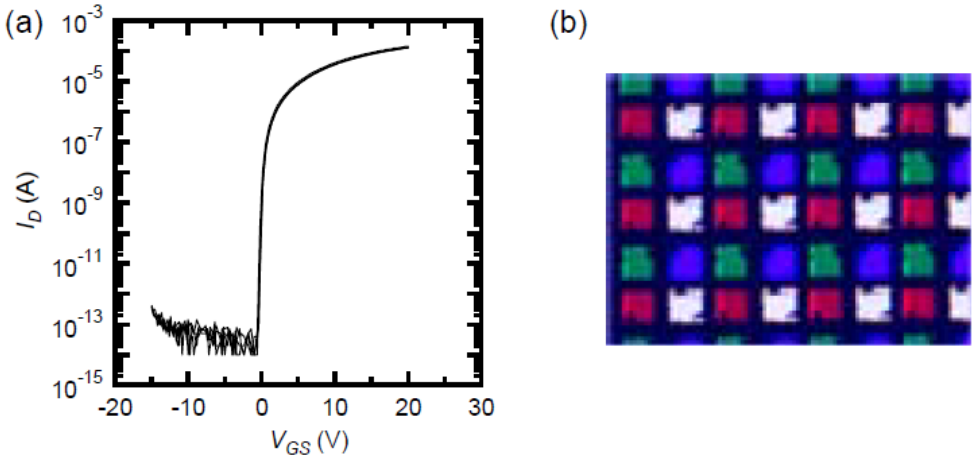


Fig. 87 (a) Transfer characteristic of 4 oxide TFTs fabricated on flexible substrate. (b) Optical micrograph of emission from pixels in the display.

A DC bias-temperature-stress test was performed on the oxide TFT after integration, under conditions which is similar to typical driving conditions for a drive TFT. Fig. 88 shows the time dependence of Vth in oxide TFT fabricated on the flexible substrate. The DC bias-temperature-stress after 10,000 sec caused a positive Vth shift of less than 0.1 V in the oxide TFT on the flexible substrate, which is comparable to that on the glass substrate [64]. This indicates that highly reliable oxide TFT were successfully fabricated on the flexible substrate.

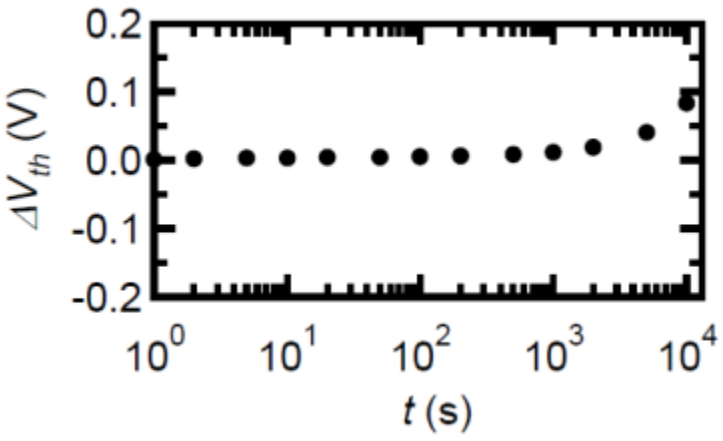


Fig. 88 Time dependence of Vth of oxide TFT.

The mechanical stability of the backplane is important because our backplane is released from glass carrier after integration. Fig. 89 shows the transfer characteristics of oxide TFT backplane, measured before and after the release process.

There is no significant change in transfer characteristics. This result indicates that our oxide TFT backplane can operate stably even after release process.

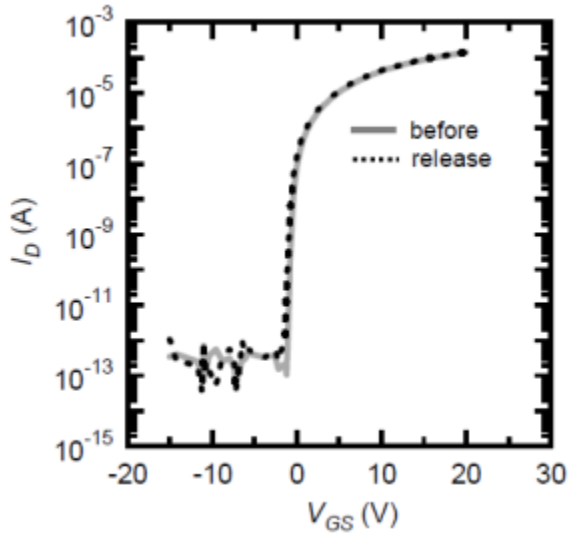


Fig. 89　Transfer characteristics of oxide TFT before (gray) and after (black) release process.

The TFT backplane was released from glass carrier after integration.

(c) Transparent AM-OLED display

As for the OLED is a self-emitting device, the OLED display does not need polarizers and a color filter like the LCD. It means that high transparency can be achieved. The transparent AM-OLED displays have been reported according to these features [67, 97]. Furthermore, the transparent property of the oxide semiconductor material gives a chance to increase the transparency by applying the transparent electrode made by the oxide electrodes.

A transparent AM-OLED display has been demonstrated using etching stopper type bottom-gate oxide TFT. Fig. 90 shows the 9.9" diagonal qHD transparent AM-OLED display, and Table 17 shows its specification. Its TFT was fabricated by the same process as that for conventional AM-OLED display. The bus lines and the electrodes of the TFT were fabricated by non-transparent metal; however, the pattern density of bus lines and TFTs of the pixel is smaller than 30% according to the applying simple 2Tr1C pixel circuit. The transmittance over 50% was achieved by this technology.

Fig. 90　9.9-inch diagonal qHD transparent AM-OLED display.

Table 17　Specification of the 9.9-inch diagonal transparent AM-OLED display.

Panel size	9.9-inch diagonal
Format	qHD
Number of pixels	960(H)×540(V)
Resolution	111ppi
Pixel circuit	2Tr1C
Channel material	a-IGZO
TFT type	Etching stopper type bottom-gate TFT
Transmittance	> 50%

(d) Summary

For the new applications using oxide TFT driven AM-OLED display, a flexible display and a transparent display were demonstrated. The oxide TFT was successfully integrated on the flexible substrate and it showed good performance, which is comparable to that on the glass substrate. The transparent property of the oxide material was confirmed to contribute to the transparency of the AM-OLED display, and the transmittance over 50% was achieved.

According to the unique property of the oxide material, it was proved that the oxide TFT has a potential to give new applications such as flexible displays and transparent displays.

3-3-6. Top-gate TFT

While the oxide TFT is attractive to the AM-OLED display driving due to its high mobility, the demands for the display size, the resolution, and the frame rate increase year by year. To driver such AM-OLED displays with the complex compensation driving method, small and uniform parasitic capacitances of TFT devices are valuable to enhance the compensating ability.

A self-aligned TFT structure is a good candidate to realize small and uniform parasitic capacitance. There have been a few reports on self-aligned structured oxide TFTs. In these reports, source and drain regions were made by hydrogen diffusion from silicon nitride films deposited by plasma-enhanced chemical vapor deposition (PECVD) [68, 98] or by plasma treatment [99, 100, 101, 102]. However, these self-aligned technologies seem to have difficulty in the stability of the TFT device performance. A highly reliable, small and uniform parasitic capacitance TFT is expected for the large size, high resolution, and high frame rate AM-OLED displays. To solve this issue, a novel aluminum (Al) reaction method was proposed to form stable source/drain regions in both sides of the channel region [86, 103-107].

(a) Self-aligned top-gate oxide TFT

A self-aligned top-gate TFT structure is a good candidate to realize small and uniform parasitic capacitance. The process flow of self-aligned top-gate oxide TFT was shown in Fig. 91. At first, oxide semiconductor as active layer was deposited by DC sputtering and was patterned by wet etching. A SiO_2 layer as the gate insulator was deposited by plasma-enhanced chemical vapor deposition on the active layer. Stacked layers of Al and Ti as the gate electrode were sequentially sputtered, and gate electrode and gate insulator were continuously dry etched using a gate pattern as shown in Fig. 91 (a). An Al layer as reactive metal was sputtered to make source/drain regions of the active layer as can be seen in Fig. 91 (b). Then, an annealing process was executed at 200 °C in the presence of oxygen atmosphere. As illustrated in Fig. 91 (c), source/drain regions and protection layer of aluminum oxide (Al_2O_3) were fabricated at the same time by the thermal diffusion (which will be discussed later) and the oxidation of aluminum, respectively. After that, an organic insulator layer was coated and patterned. Then Al_2O_3 layer was removed to contact with source/drain electrode by dry etching. Finally, a stacked layer of molybdenum (Mo) and Al as the source/drain electrode was sputtered and then patterned by wet etching.

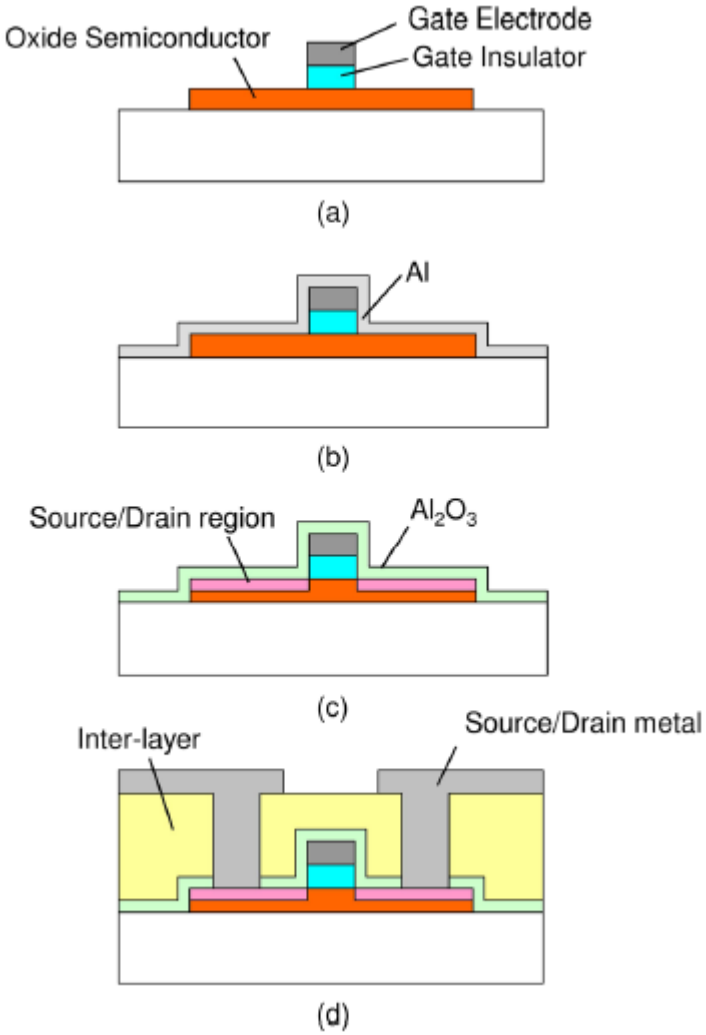


Fig. 91 Process flow for fabrication of self-aligned top-gate oxide TFT.

Fig. 92 shows the cross-sectional TEM views of TFT. In Fig. 92 (b), it is recognized that a uniform Al_2O_3 protection layer was formed on the a-IGZO layer.

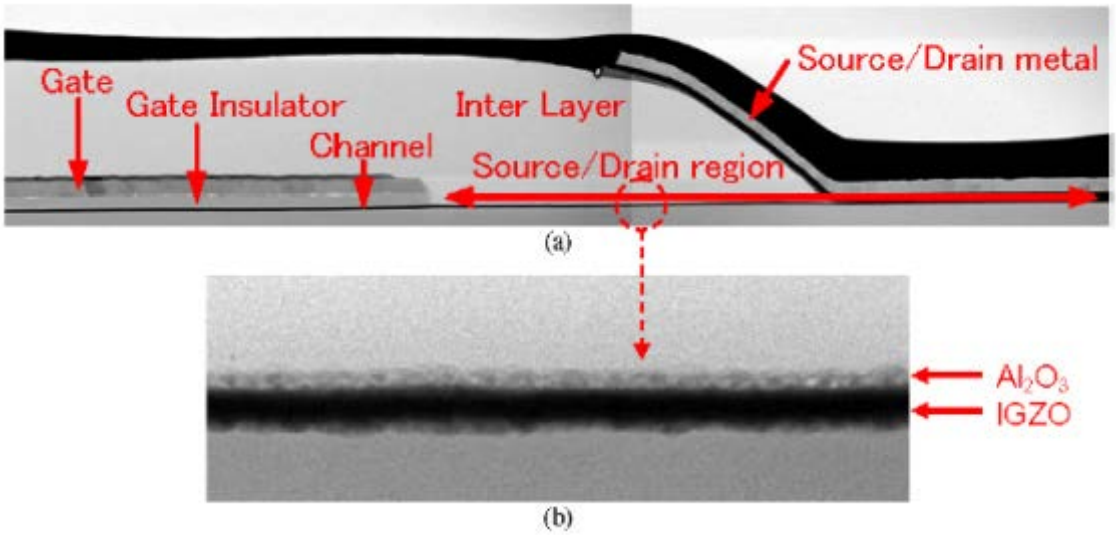
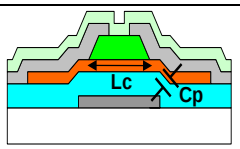
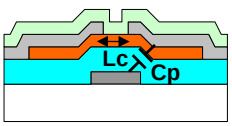
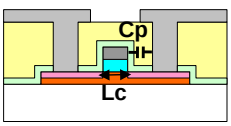


Fig. 92　Cross-sectional TEM views of self-aligned oxide TFT.

Table 18 shows typical TFT structures for the oxide TFT and those features. Three types of TFT structure have been proposed for the oxide semiconductor. An etching stopper (ES) type bottom-gate TFT is the most popular structure, because it is relatively easy to fabricate. However, many mask steps are needed in this structure. In addition, its channel length must be longer and parasitic capacitance must be larger than those of other structures due to large overlap regions. A self-aligned top-gate TFT is the most ideal structure because it requires fewer mask steps to fabricate. Furthermore, short channel length and small parasitic capacitance are also possible due to the self-aligned top-gate structure and the self-aligned structure, respectively.

Table 18　TFT structure comparison.

TFT structure	ES-type Bottom-gate	CE-type Bottom-gate	Self-aligned Top-gate
			
Mask count	6	5	4
Channel length (Lc)	Long	Short	Short
Parasitic capacitance (Cp)	Large	Medium	Small

(b) Al reaction method for the source/drain region formation

To obtain high-mobility and highly reliable TFTs, the source and drain region should have low sheet resistivity. To solve this issue, a metal reaction method was proposed [86]. According to this process, the resistivity of the oxide semi-conductor is reduced by the chemical reaction with the deposited metal.

Fig. 93 shows the annealing temperature dependence of the sheet resistivity with a stacked layer of metal and oxide semiconductor. When Al was used as the reactive metal, a much lower sheet resistivity was obtained than that when Ti was used. Furthermore, the sheet resistivity of the films with the Al stack decreased with the annealing temperature and showed a minimum value of 9.5×10^2 Ω/sq. at 200 °C. The increase in the sheet resistivity after 200 °C may be attributed to the oxidation of the amorphous In−Ga−Zn−O (a-IGZO) layer. On the other hand, the sheet resistivity of the films with the Ti stack was always over 30 kΩ/sq. regardless of the annealing temperature. From this result, Al reaction with oxide semiconductor is an effective way to obtain low-resistive source and drain regions for top-gate oxide TFTs. Fig. 94 shows typical transfer curves of self-aligned top-gate TFTs with a channel width (W) and length (L) of 10 and 4 μm, respectively. In these TFTs, a-IGZO was used as the channel material. The on-currents of the TFTs without any reactive metal and with Ti are about three orders lower than those with Al as a reactive metal. Their low on-currents would be due to the high series resistivity of the source and drain regions. The TFT with Ti stacked onto the source and drain exhibits about one order higher off-current than the other TFTs. It is suggested that the quality of the TiO_2 film formed by thermal oxidation is not sufficient to prevent surface leakage current.

The TFT with the Al reactive metal exhibits good transfer characteristics at a drain voltage of 10 V such as a sub-threshold swing of 0.22 V/decade, a minimum off-current of 10 fA, a threshold voltage (Vth) of −1.5V, a field effect mobility of 9.8 cm^2/Vs, and an on/off current ratio of over 10^{10}. The extremely low off-current of the TFT indicates that the surface leakage current in the Al_2O_3 layer was negligibly small.

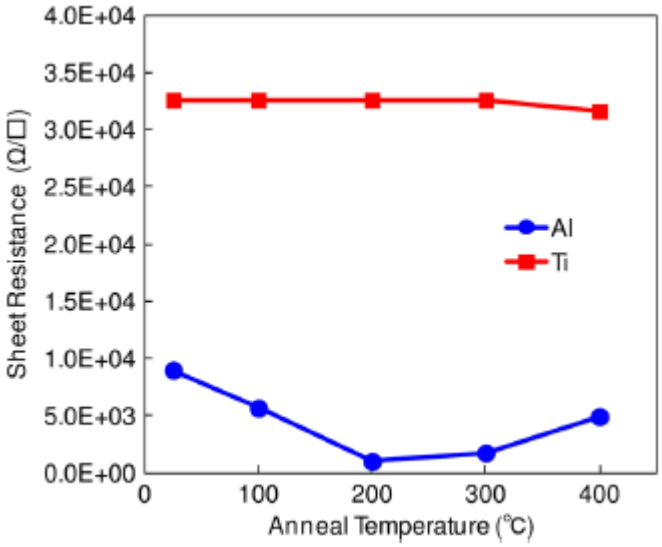


Fig. 93 Sheet resistance of stacked layer of metal and oxide semiconductor depending on annealing temperature.

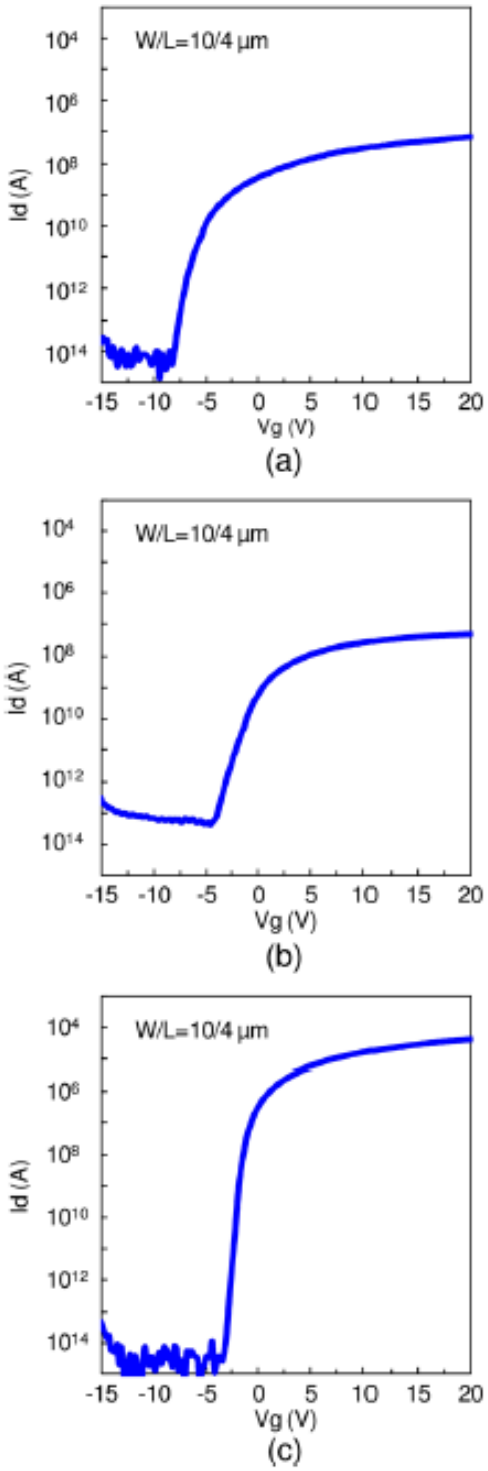


Fig. 94 Representative transfer characteristics of self-aligned TFT (a) without reactive metal, (b) with Ti reactive metal, and (c) with Al reactive metal with W/L=10μm/4 μm.

Fig. 95 shows output characteristics of self-aligned top-gate TFT with Al reactive metal. The TFT exhibited excellent output characteristics with steep rise in low Vds region. This suggests that good ohmic characteristics were obtained.

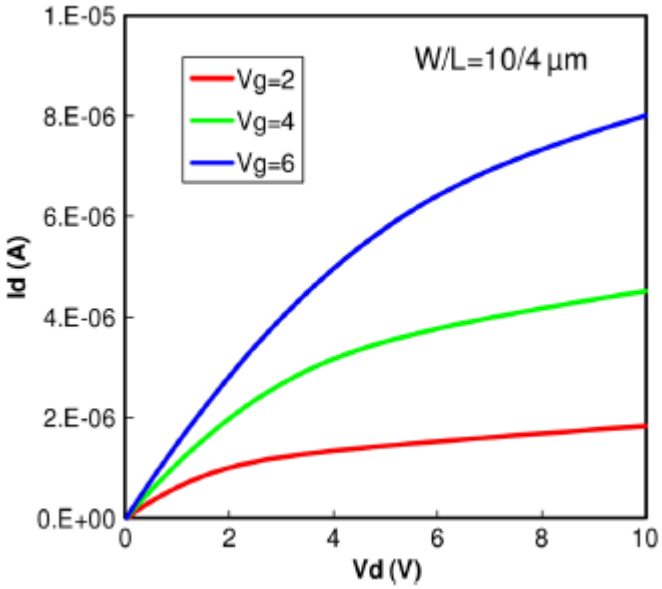


Fig. 95 Output characteristics of self-aligned TFT with Al reactive metal with W/L=10µm/4 µm.

Fig. 96 shows the depth profile of Al_2O_3 and a-IGZO layer measured by EDX analysis. The significant amount of aluminum was diffused into the a-IGZO layer after the TFT fabrication process. From this result, it is considered that the diffused Al works as a donor in the a-IGZO film and reduces the sheet resistivity of a-IGZO film. It is well known that aluminum can be worked as a donor in the zinc oxide (ZnO) and the Al decreases the sheet resistivity of ZnO film [108]. It is supposed that the same mechanism of reduction of the sheet resistivity works in the case of a-IGZO film. Another possible mechanism of the decrease of sheet resistivity of a-IGZO is due to the increase of O-vacancy. However. if the increase of O-vacancy in the a-IGZO film reacted with metal is the main reason of the decrease of sheet resistivity, the sheet resistivity of a-IGZO film reacted with Ti would also decrease. Therefore, O-vacancy would not be the main reason to decrease the resistivity of a-IGZO films.

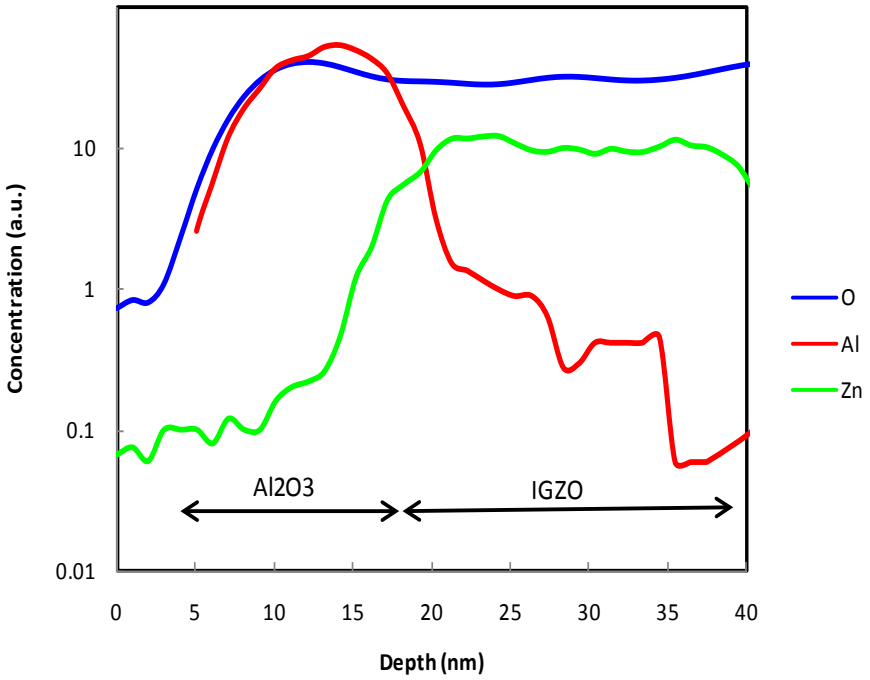


Fig. 96 Depth profile of S/D region by EDX.

To detect the Al and O profiles in the a-IGZO layer, laser-assisted atom probe tomography (APT) analysis was used. APT can avoid interfacial-mixing artifacts (knock-on effects) during the secondary ion mass spectroscopy sputter depth profiling measurement. APT can be utilized as a practical method for 3D characterization of individual element positions in semiconductor-based transistors with close to atomic resolution [109,110].

A schematic diagram of APT measurement is shown in Fig. 97. Evaporations are initiated by using short pulse and application of high voltage. The mass to charge ratios of individual atoms are determined by measuring the time of flight of individual ions. Thus, the two-dimensional (2D) detector enables to draw the 2D element map of the specimen surface. Then, reconstruction of a series of 2D element maps with a graphics workstation enables to draw a 3D element map of the specimen.

The mechanism of the Al reaction method was examined using APT analysis. The analyzed sample was made by the following process. A 40-nm-thick a-IGZO layer was deposited on a substrate by DC sputtering. A thin Al layer as a reactive metal was then sputtered on the a-IGZO layer. Annealing at 200 °C was then performed in an oxygen atmosphere. The sheet resistivity was changed from 1.2×10^5 to 9.5×10^2 Ω/sq. after the annealing process. Thus, sufficient lowering of the sheet resistivity for the source/drain region can be achieved by the annealing process. Fig. 98 shows the depth

profile of Al and O in the oxide semiconductor measured by APT analysis before and after annealing. Al diffusion into the a-IGZO layer was evident after annealing. Al can act as a donor in ZnO and decrease the sheet resistivity of ZnO films [108]. It is supposed that the same mechanism for the reduction of the sheet resistivity is applied to the a-IGZO film with the incorporation of Al. The oxidization of the Al layer by annealing was also confirmed. It is expected that this Al_2O_3 layer functions as a protective layer against impurities, such as moisture.

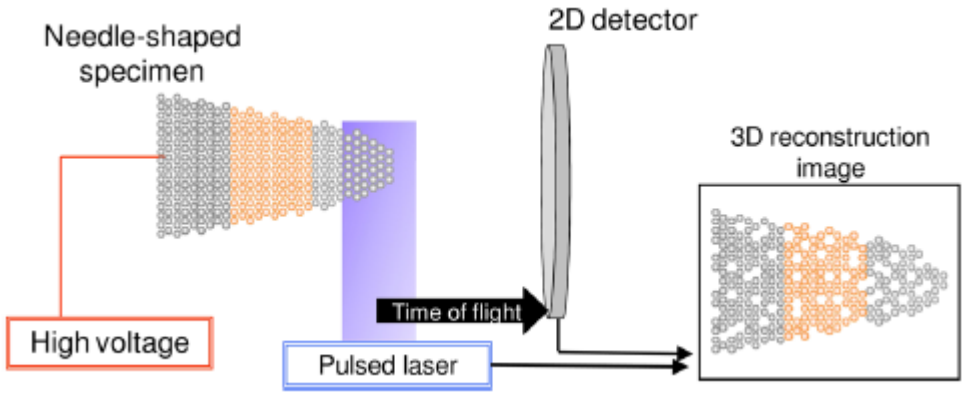


Fig. 97　Configuration of APT measurement setup.

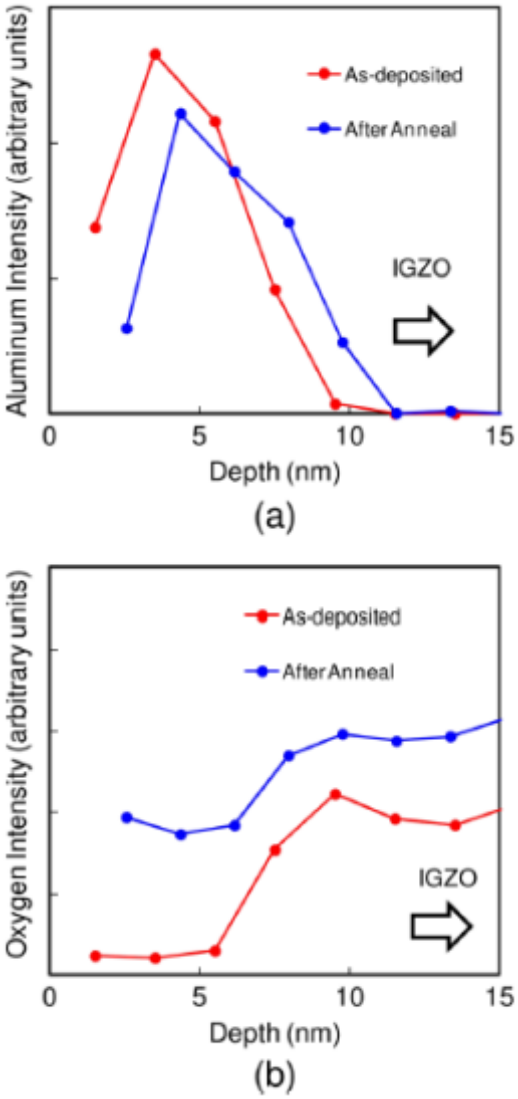


Fig. 98 Depth profiles for Al and O before and after annealing.

The effect of the annealing temperature on the reliability of the TFTs was examined. Thermal annealing processes were executed after device fabrication and in an oxygen atmosphere. Fig. 99 shows Vth shift curves after bias temperature stress (BTS). The stress bias voltage was set to two conditions of Vg = 10 V and Vd = 10 V. The stress temperature was set to 50 °C, and the stress period was 10,000 sec. As a result, the TFT annealed at 300 °C showed much better reliability than that annealed at 200 °C.

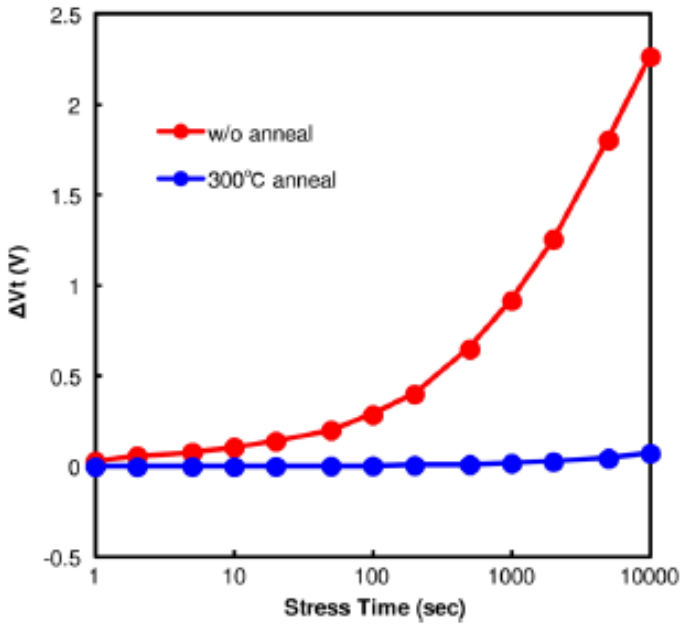


Fig. 99　Vth shift curves for TFTs annealed after BTS.

To clarify the reason for the difference in reliability, depth profiles of In and O in the oxide semiconductor were examined by APT analysis after the TFT fabrication process. Fig. 100 shows the depth profiles of In and O in the channel region of the TFT (a) annealing at 200 °C and (b) annealing at 300 °C. The depth profile of O is almost constant in the oxide semiconductor annealed at 300 °C. However, the interfacial oxygen concentration at the center position of the TFT annealed at 200 °C is higher than that in the bulk. It is supposed that the excess oxygen was diffused from the interface, and uniform oxygen depth profile was obtained after annealing at 300 °C. The excess oxygen in the oxide semiconductor may form trap states and deteriorate the reliability characteristics of the TFT annealed at 200 °C. In contrast, the TFT annealed at 300 °C has a homogeneous oxygen depth profile, and thus has superior reliability characteristics. Therefore, the oxygen concentration in the channel must be controlled to obtain excellent electrical reliability.

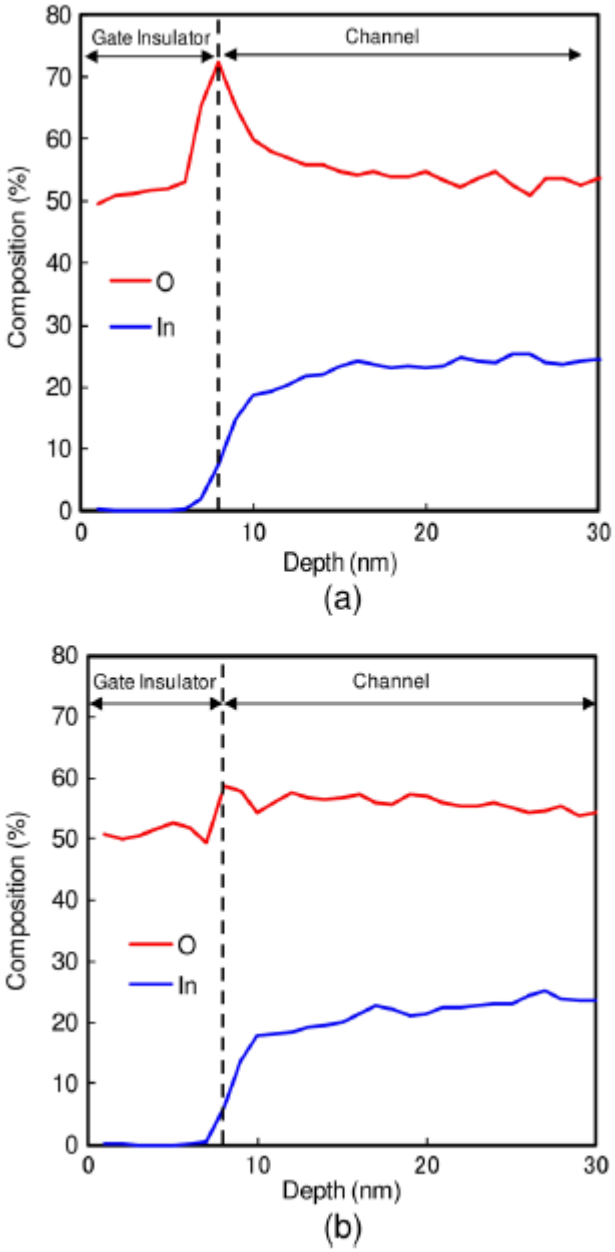


Fig. 100　Depth profiles for In and O in the channel region, (a) annealing at 200 °C and (b) annealing at 300 °C.

(c) TFT characteristics and reliability

Fig. 101 shows typical transfer curves of the self-aligned top-gate TFT with a channel width/length of 10/4 μm. It exhibits good transfer characteristics at a drain voltage of 10 V, such as a sub-threshold swing of 0.22 V/decade, minimum off-current of 10 fA, threshold voltage (Vth) of –1.5 V, field-effect mobility of 9.8 cm^2/Vs, and on/off ratio in the order of 10^{10}.

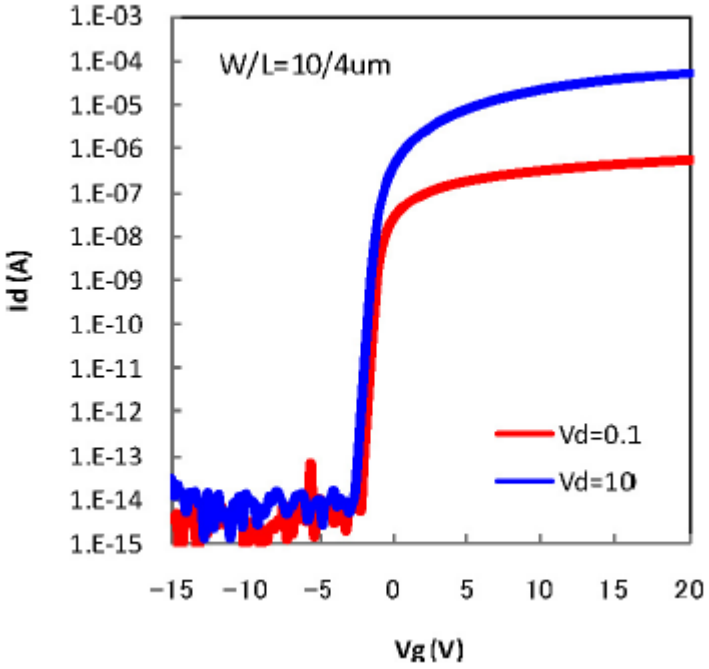


Fig. 101 Transfer curves of the self-aligned top-gate TFT.

The parasitic source-to-drain resistances (Rsd) and the differences in channel length (ΔL) of fabricated TFTs were evaluated by using a channel resistance method [101]. Fig. 102 shows the dependency of the total resistivity (Rtot) on the channel length (L) of TFTs with W = 10 μm at Vgs = 10~20 V. The coordinates of the intersection of the straight lines fitted to each Rtot, which is dependent on L and Vgs, give Rsd = 2.0 kΩ and ΔL = 0.8 μm, respectively. The width-normalized Rsd (RsdW) is thus calculated to be 2 Ωcm. Those values are lower than those of the previous reports: Rsd = 330 Ωcm [102], and Rsd = 51 Ωcm and ΔL = 1.6 μm [98]. This observation confirms that self-aligned top-gate TFTs by the Al reaction method have good ohmic characteristics. The shrinkage of the channel length, ΔL = 0.8 μm, would be attributed to the critical-dimension loss during patterning of the gate electrode and gate insulator and/or to the decrease in channel length induced by aluminum diffusion from the source/drain regions.

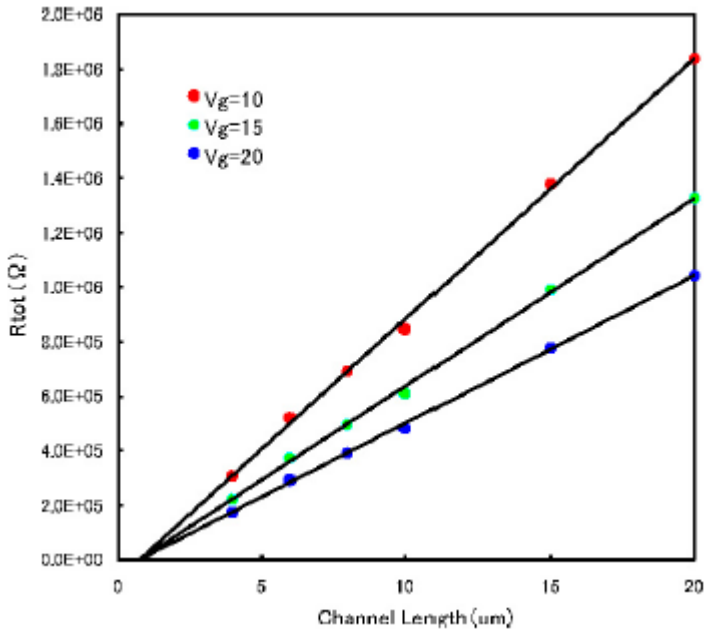


Fig. 102 Dependence of Rtot on L of TFTs with W = 10 μm at Vgs = 10~20 V.

One of the indispensable properties of TFTs for the AM-OLED display applications is to have heat resistance against thermal annealing processes. To examine the amount of sheet-resistance change, the self-aligned top-gate TFTs were fabricated by two different methods. One is the self-aligned TFT fabricated by our proposed Al metal reaction method and the other is a self-aligned TFT using argon (Ar) plasma treatment to make source/drain regions. The Ar plasma was treated for 90 sec before the inter-layer formation. Fig. 103 shows the sheet resistance of source/drain regions by two different source/drain fabrication processes after using different annealing temperature. Thermal annealing was conducted in the presence of oxygen atmosphere for 1 hour. The sheet resistance with the Ar plasma treatment was low before the thermal annealing process just after TFT fabrication. However, the resistance increased drastically after thermal annealing above 200°C. On the other hand, the sheet resistance caused by the aluminum metal reaction slightly changed after thermal annealing process. If the sheet resistance of the source/drain regions is lower than 10 kΩ/sq., it is possible that the source/drain regions are used as connecting layers in the pixels of the display. Therefore, TFTs fabricated by using the Al reaction method is applicable to connecting layers in pixel circuits after the thermal annealing process.

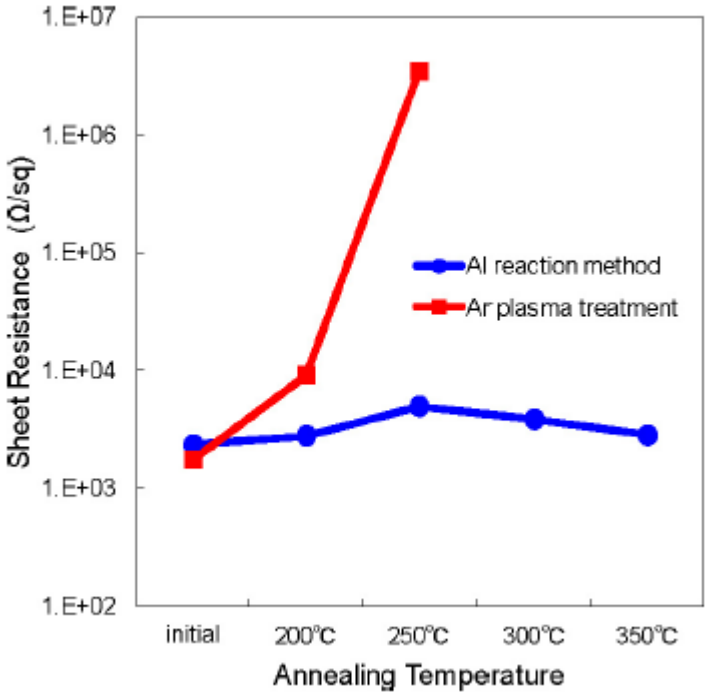


Fig. 103 Dependence of sheet resistance on annealing temperature.

Fig. 104 shows Vth-shift curves after bias temperature stress (BTS) test. The stress-bias voltage was set to two conditions: Vgs = 15 V, Vds = 0 V and Vgs = 15 V, Vds = 15 V. The stress temperature was set to 50°C and the stress period was 10,000 sec. The effect of the thermal annealing temperature on the reliability of the TFTs was examined. Thermal annealing processes were executed after device fabrication and in an oxygen atmosphere. Both in Fig. 104 (a) and Fig. 104 (b), the TFT with thermal annealing at 300°C showed much better reliability than that at 200°C. Since an oxide semiconductor is very sensitive to impurities such as water or oxygen or hydrogen, a high-temperature annealing process to decrease the impurities in TFTs is necessary in order to obtain highly reliable TFTs. Therefore, an Al-reaction process with high temperature annealing is very suitable for obtaining self-aligned top-gate TFTs with high reliability.

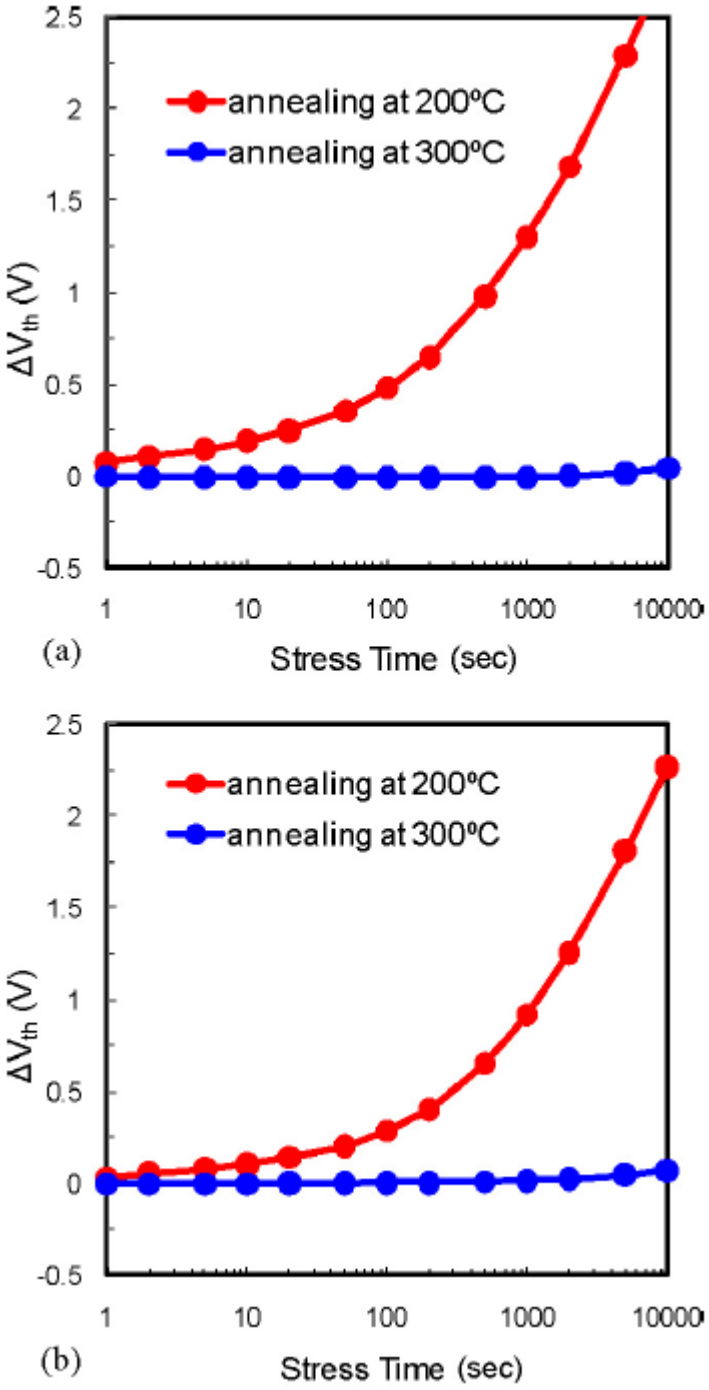


Fig. 104 Vth shift as a function of time on a logarithmic scale for TFTs annealed at different temperatures after BTS.
Stress voltage condition with (a) Vgs = 15 V, Vds = 0 V and (b) Vgs = 15 V, Vds = 15 V.

The device structure affects the reliability [111]. Fig. 105 shows the cross-sectional view of the top emission AM-OLED device. In case of top-gate TFT

structure, there is no need to deposit thick gate insulator because the step height of the underneath oxide layer is small. The high gate electric field due to thin gate insulator gives high current flow; however, it tends to accelerate the threshold voltage shift in the positive bias temperature stress (PBTS) test. On the other hand, in case of top emission AM-OLED device, there are several organic layers around the channel region. These organic layers contain impurities such as hydrogen and water. Especially, the upper layers tend to contain impurities more because of those lower baking temperature. They diffuse through the device to the channel region and let the threshold voltage negative shift. These kinds of impurities often accelerate the threshold voltage shift in the negative bias temperature stress (NBTS) test. Fig. 106 shows the difference in diffusion-origin degradation due to the TFT structure. In the case of top-gate TFT, the gate electrode acts as a passivation. Moreover, there is a thin alumina passivation layer on the oxide semi-conductor layer as a by-product of the source/drain formation process. An alumina has an excellent passivating property even though thin thickness; therefore this top-gate TFT tends to have excellent reliability against NBTS.

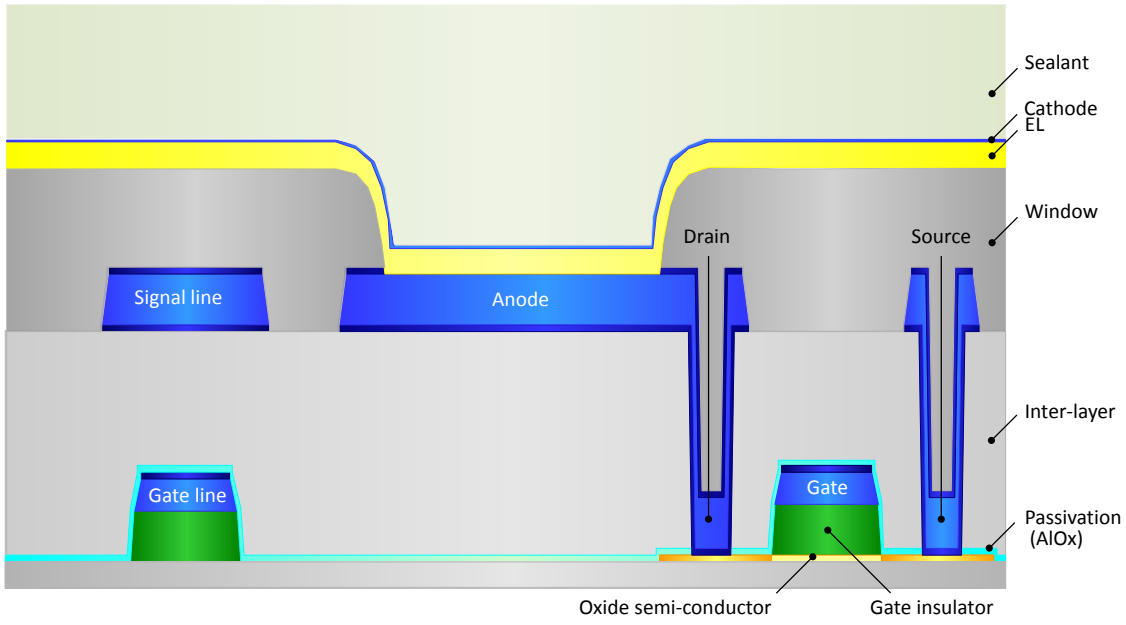


Fig. 105 Cross-sectional view of the top emission AM-OLED device.

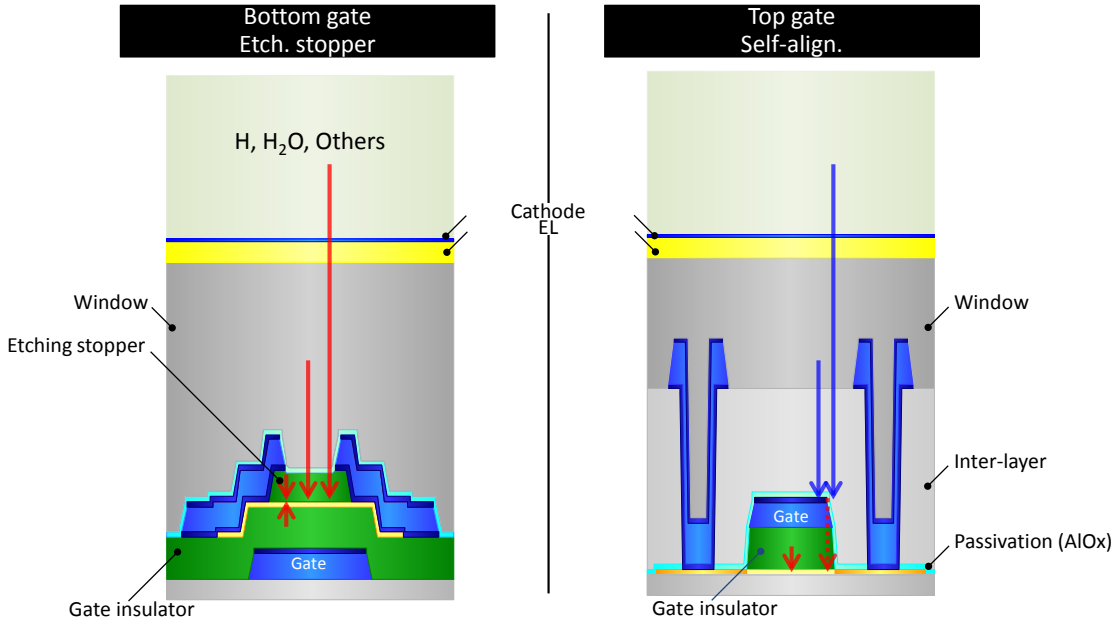


Fig. 106 Difference in diffusion-origin degradation due to the TFT structure.

Fig. 107 shows the results of PBTS and NBTS tests. The stress bias voltages were set to Vgs = ±15 V and Vds = 15 V. The stress temperature was set to 50°C and the stress period was 10,000 sec. In the case of original process, the threshold voltages after PBTS and NBTS tests were 1.04 V and 0.16 V, respectively. To improve the TFT stability, the conditions of organic layers, inorganic layers near the oxide semiconductor layer, annealing process, and the treatment of the interface between oxide semiconductor and gate insulator were optimized. After the optimization, the threshold voltages after PBTS and NBTS tests became 0.05 V and 0.05 V, respectively. These values are enough small for the OLED driving.

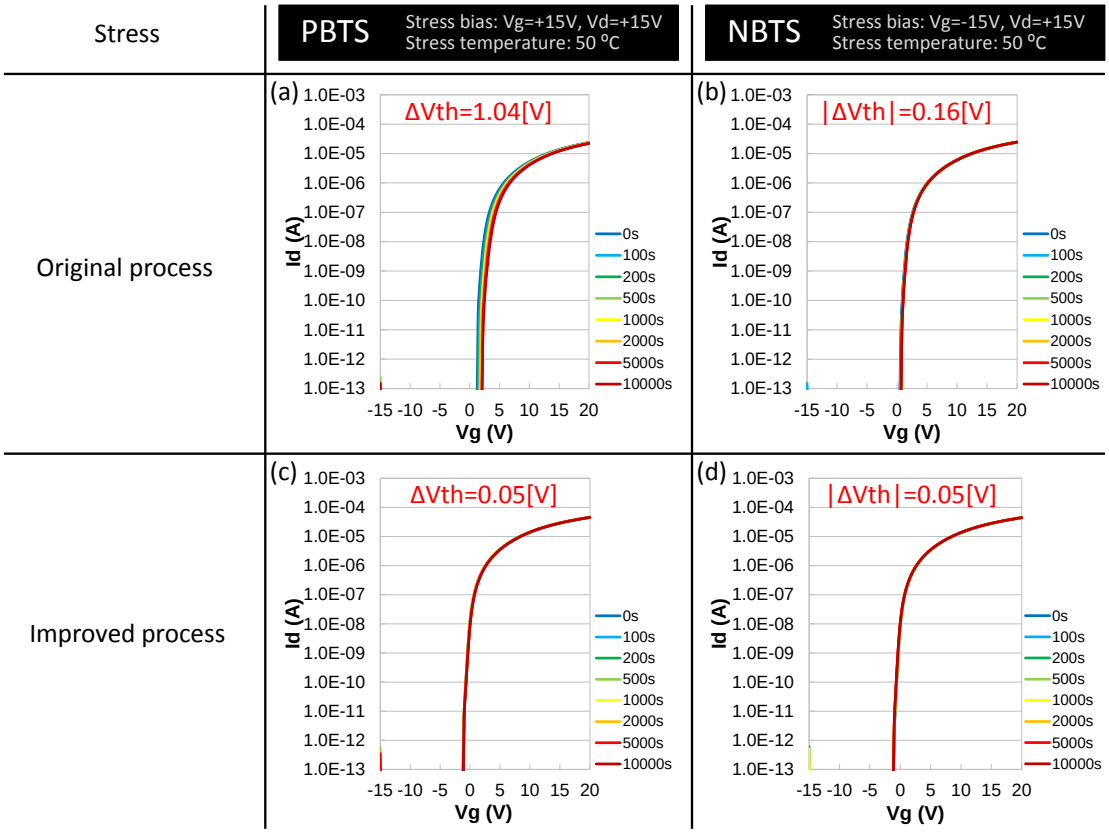


Fig. 107 Results of PBTS and NBTS tests.

And the available bias range for this device was evaluated. Fig. 108 shows the results of PBTS tests for the wide bias range. The stress bias voltages were set to Vgs = 0~50 V and Vds = 0~50 V. The stress temperature was set to 90°C and the stress period was 5,000 sec. In area-A, the TFT showed excellent TFT reliability; however in area-B, some of the TFTs showed large threshold voltages shifts. This fact indicates that the degradation mode changes in this area, and this device can be used in area-A conditions. This area is enough large for AM-OLED display, even if using for the gate driver.

Fig. 109 shows the Arrhenius plot for the threshold voltage shift in PBTS test, indicating the stability against temperature. The stress bias voltages were set to Vgs = 40 V and Vds = 0 V. The stress temperature was set to 50~125°C and the stress period was 2,000 sec. According to these data, the activation energy is 73 meV. It is enough stable for the temperature in this temperature range. This result suggests that this transistor is also applicable for the high temperature application over 100°C.

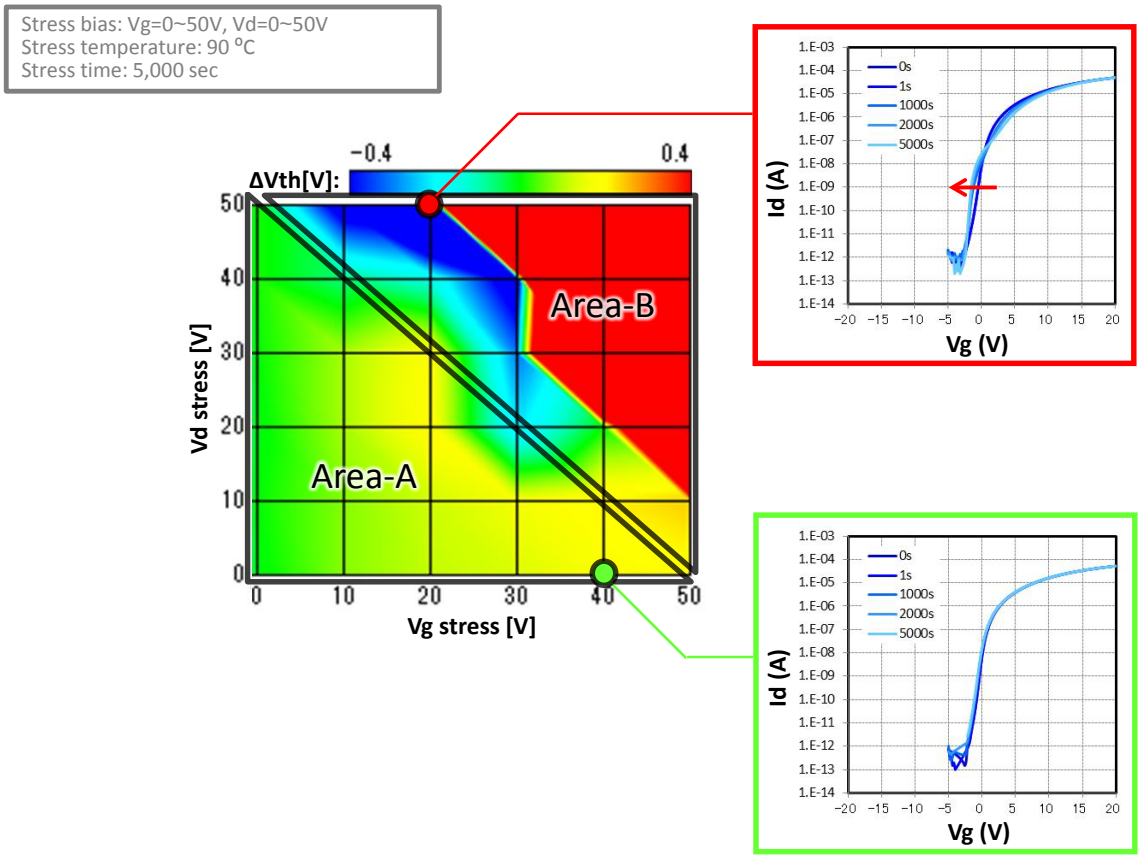


Fig. 108 PBTS test results for the wide bias range.

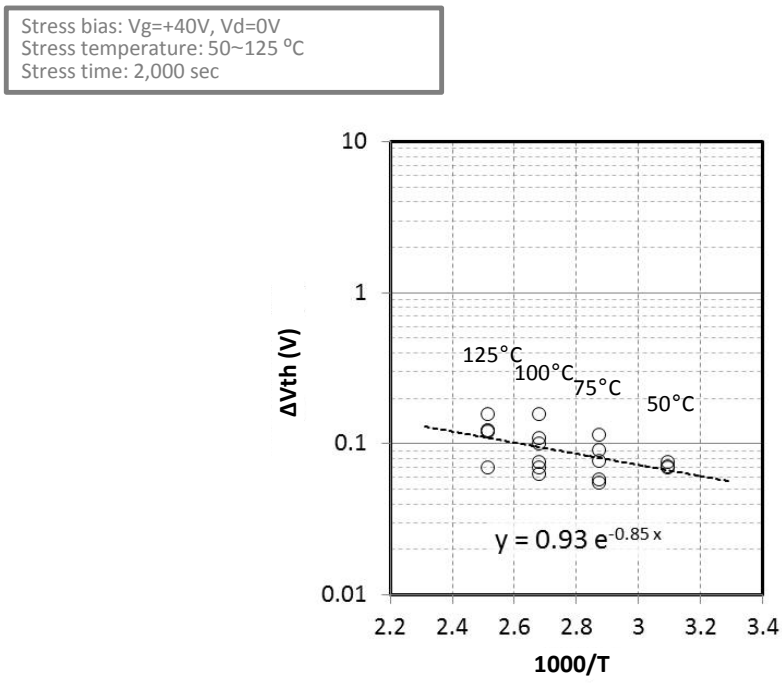


Fig. 109 Stability against Temperature (Vth shifts of PBTS tests).

(d) High mobility materials

To make AM-OLED panels with integrated gate and data drivers on glass substrate, oxide TFTs with higher mobility are desired. That can be achieved by using oxide-semiconductor materials with higher carrier density.

At first, another IGZO material that has a different composition from IGZO (2:2:1) was employed as an active layer. As shown in Fig. 110, the TFT exhibits excellent transfer characteristics, such as a field effect mobility of 21.4 cm^2/Vs, Vth = –1.6 V, and a sub-threshold swing of 0.12 V/decade.

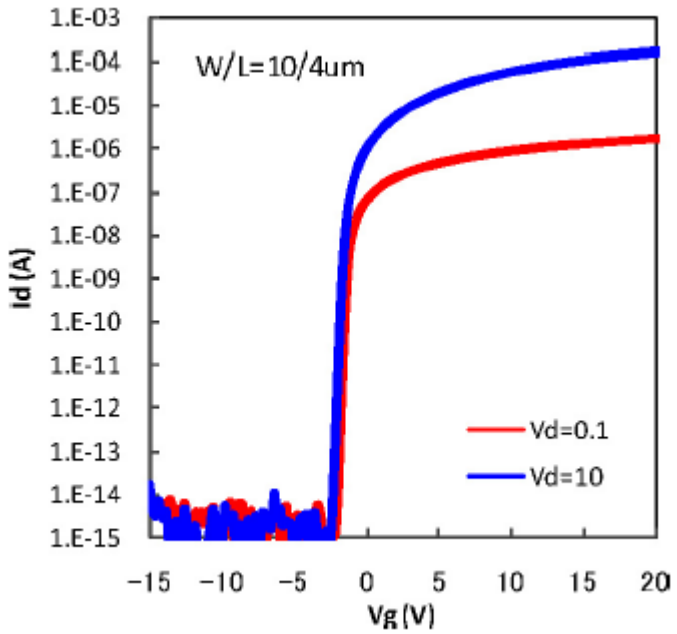


Fig. 110 Transfer curves of self-aligned TFTs with different IGZO composition from IGZO (2:2:1).

Next, a-ITZO was employed as an active layer of the self-aligned top-gate oxide TFT. Fig. 111 shows that these TFTs exhibit excellent transfer characteristics, such as a field effect mobility of 32.0 cm^2/Vs, a Vth of −0.09 V, and a sub-threshold swing of 0.12 V/decade. In addition, these TFTs have excellent uniformity with a 4-μm channel length. From these results, Al reaction method was successfully applied with a-ITZO to obtain low resistivity source/drain regions of self-aligned top-gate TFTs.

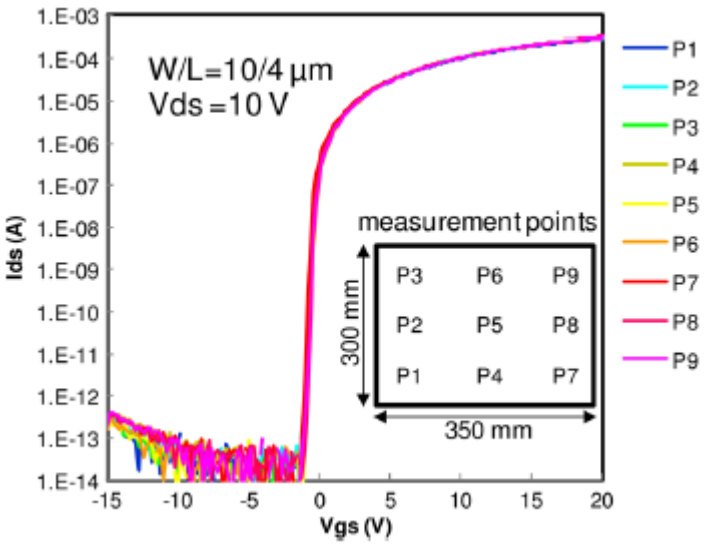


Fig. 111 Transfer curves for self-aligned top-gate a-ITZO TFT.

The parasitic source-to-drain resistance (Rsd) and the differences of channel length (ΔL) for the fabricated TFTs were evaluated using the channel resistance method [101]. Fig. 112 shows the transfer characteristics of the self-aligned top-gate a-ITZO TFT with various L and W=10 µm at Vds = 0.1 V.

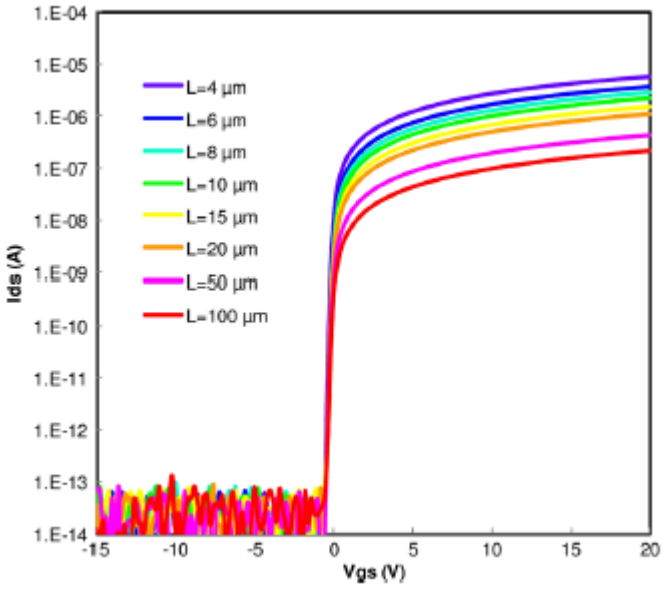


Fig. 112 Transfer characteristics for self-aligned top-gate a-ITZO TFT with various L and W=10µm at Vds = 0.1V.

Fig. 113 shows the dependence of the total resistance (Rtot) on the channel length (L) of TFTs with W=10 μm at Vgs = 10~20 V. The coordinates of the intersection of the straight lines fitted to each Rtot, which is dependent on L and Vgs, give Rsd = 0.5 kΩ and ΔL = 0.4 μm. The width-normalized Rsd (RsdW) is thus calculated to be 1Ωcm. These values are lower than those of previous reports: Rsd = 330 Ωcm [102], and Rsd = 51 Ωcm and ΔL = 1.6 μm [98], which confirm that self-aligned top-gate TFTs fabricated by the Al reaction method have good ohmic characteristics. In addition, the shrinkage of the channel length, ΔL = 0.4 μm, is rather small; therefore, this process is suitable for the fabrication of short channel TFTs for high-resolution displays.

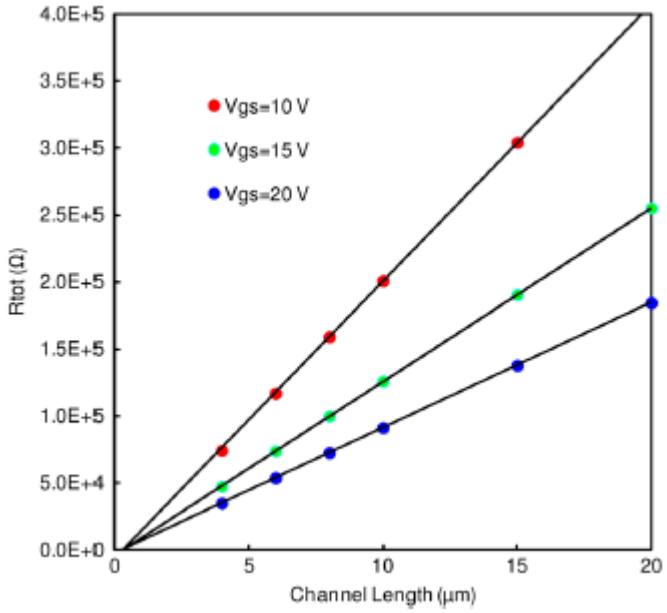


Fig. 113 Dependence of Rtot on L for the TFT at Vgs = 10~20V.

With respect to the TFT performance, the reliability against the bias stresses is the most critical issue for the AM-OLED display. The measured data tended to approximate a straight line on the log–log plot and were extrapolated to 3.16×10^8 s (10 years) in Fig. 114. When the lifetime of the display is determined from the 3V limit of ΔVth in the PBTS test of Vg = Vd = 10 V, it becomes 5.2×10^8 sec, which is sufficiently long for the TFT application of the AM-OLED displays.

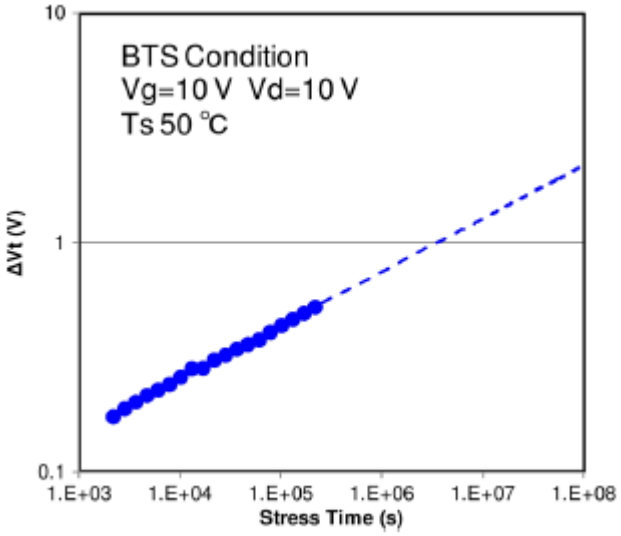


Fig. 114 Vth shift after positive BTS test.

(e) 5 Mask TFT backplane for AM-OLED display

It is desirable to reduce the mask steps for the backplane of the AM-OLED display to reduce panel cost. In the case of self-aligned top-gate TFT using an organic interlayer, the mask steps of the oxide TFT for AM-OLED device can be reduced to five by merging the anode electrode process to the source/drain electrodes process, as shown in Fig. 115. This structure is very promising not only because it has good electrical characteristics but also because it strengthens the cost competitiveness of the AM-OLED display.

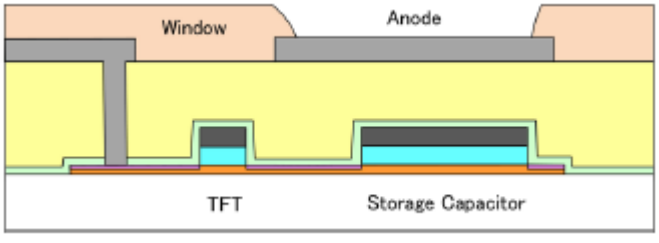


Fig. 115 Cross-sectional view of the five-mask processed backplane for AM-OLED device..

(f) 9.9-in. qHD AM-OLED prototypes

As shown in Fig. 116, a certain circuit to drive the electrical current is fabricated on each pixel of the AM-OLED display. When the parasitic capacitances are large or non-uniform in this circuit, brightness uniformity deteriorated because the

pixel circuit cannot work properly and the variation of the parasitic capacitances worsens the uniformity of the image. Fig. 117 shows the brightness uniformity at a low gray level of the AM-OLED panel, depending on the TFT structures. On the panel driven by etching stopper (ES) type bottom-gate TFTs, the brightness variation depending on the panel position was detected. On the other hand, the panel driven by self-aligned TFTs shows excellent uniformity. The brightness uniformity of the AM-OLED panel is degraded by the variation of the TFT characteristics of each pixel. As a result, in AM-OLED displays, compensation pixel circuits are used to achieve uniform brightness. On the panel using ES-type bottom-gate TFTs, pixel circuits cannot compensate for the variation of the TFT characteristics due to the large parasitic capacitance. However, on the panel with self-aligned TFTs, uniform brightness can be obtained due to the small parasitic capacitances. To realize high frame rate driving such as 240 Hz or 480 Hz, RC delay is a crucial issue that leads to brightness non-uniformity due to the signal delay. Above-proposed self-aligned TFTs can drive the AM-OLED panel with a much higher frame rate than the conventional ES-type bottom-gate TFTs. Because the self-aligned TFTs have lower interlayer capacitance owing to a thicker organic insulator compared to the ES-type bottom-gate TFTs as shown in Fig. 117. In addition, because the organic insulator has small relative permittivity, the interlayer capacitance of the self-aligned TFT decreases more. To this point, the proposed TFT structure has an advantage over the conventional ES-type TFT structure in achieving higher frame-rate operation.

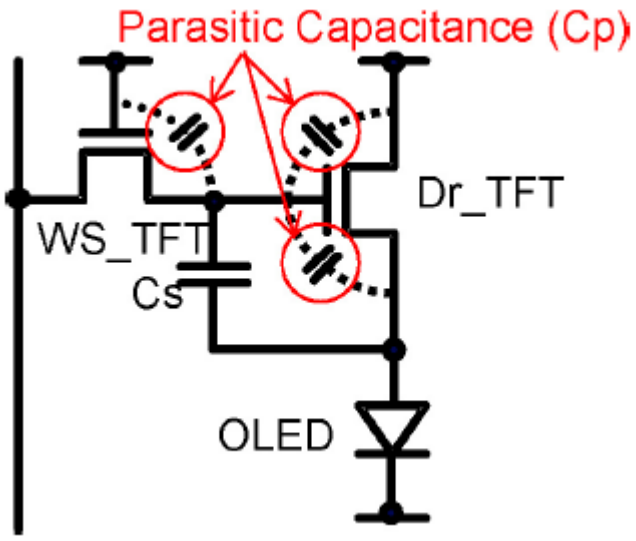
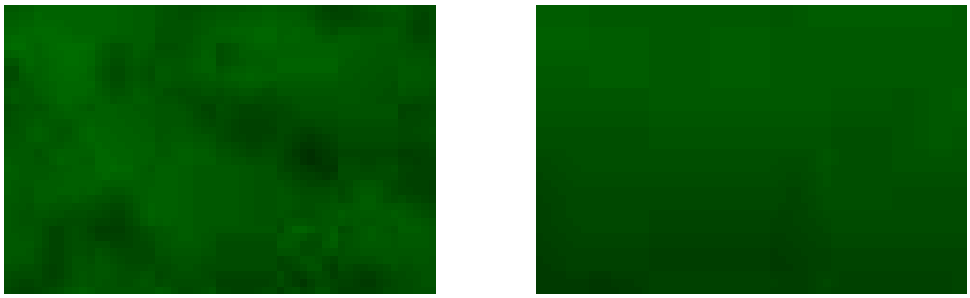


Fig. 116 Equivalent pixel circuit of the AM-OLED display.



(a) AM-OLED panel by ES-type TFT (b) AM-OLED panel by self-aligned TFT

Fig. 117 AM-OLED panels with different TFT structures at low gray levels.

Fig. 118 shows the cross-sectional views of ES-type TFT and self-aligned TFT, and Fig. 119 shows the 9.9-in.-diagonal AM-OLED prototype driven by 5-Mask processed self-aligned top-gate TFTs using an Al-metal reaction method to make the source/drain regions. IGZO (In:Ga:Zn = 2:2:1) was used for the active layer of TFT in this panel. This panel has a compensation circuit with two transistors and one capacitor in a pixel. This panel has a peak luminance over 600 cd/m^2 and a color gamut of 96% of the NTSC triangle.

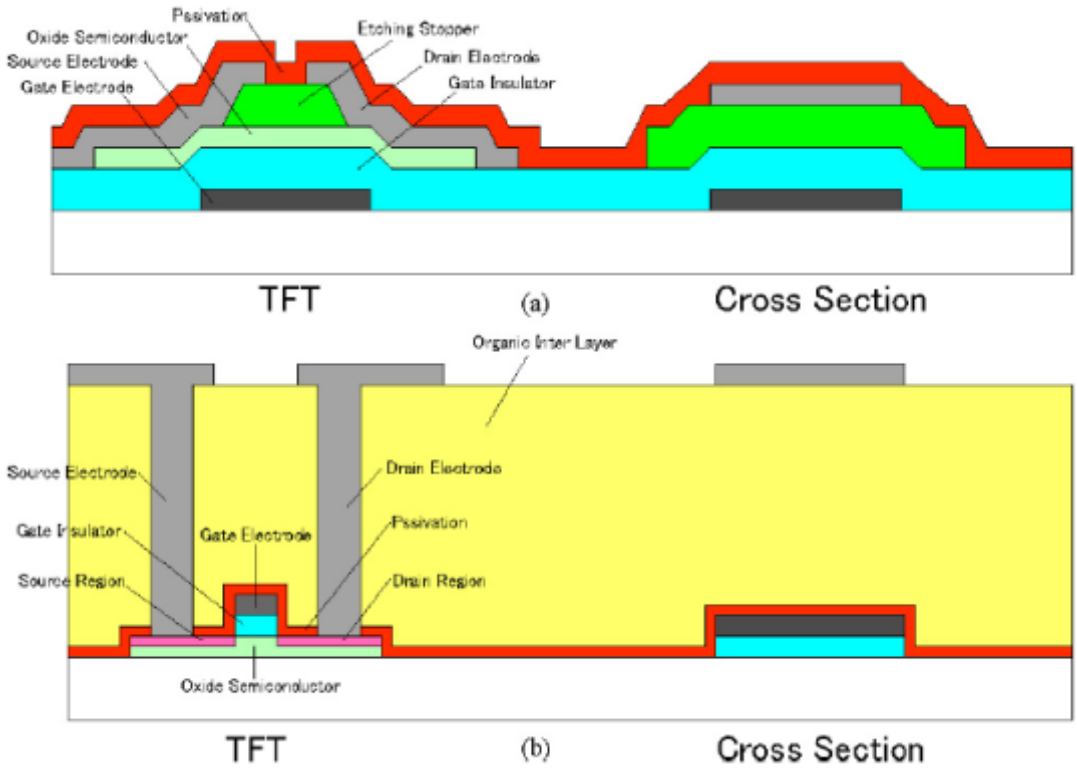


Fig. 118 Cross-sectional views of ES-type TFT and self-aligned TFT.

Fig. 119　9.9-inch diagonal qHD AM-OLED display by 5-Mask processed self-aligned top-gate a-IGZO TFT.

Table 19　Specification of the 9.9 inch diagonal AM-OLED display.

Panel size	9.9-inch diagonal
Format	qHD
Number of pixels	960(H)×540(V)
Resolution	111ppi
Luminance	All white: 200 cd/m^2
	Peak : > 600 cd/m^2
Contrast ratio	> 1,000,000 : 1 (Dark)
Color saturation	96% (NTSC)
Pixel circuit	2Tr1C

Fig. 120 shows the 9.9-in. diagonal AM-OLED prototype driven by 5-Mask processed self-aligned top-gate TFTs. A-ITZO was used for the active layer of TFT in this panel. This panel has a compensation circuit with two transistors and one capacitor in a pixel. The peak luminance is over 600 cd/m^2, and the color gamut is 102% of the National Television System Committee (NTSC) triangle. Owing to small parasitic capacitance of the self-aligned TFT structure, this panel shows the excellent brightness uniformity. In this panel, a metal-insulator-semiconductor (MIS) structure was adopted for the storage capacitor. When plus bias was applied to the gate electrode of storage capacitor, a large amount of electron was accumulated in a-ITZO layer. An enough capacitance was obtained using this MIS structured storage capacitor with appropriate

bias voltage to the electrode and the excellent image quality of AM-OLED panel was realized using this structure.

Fig. 120　9.9 inch diagonal qHD AM-OLED panel by 5-Mask processed self-aligned top-gate a-ITZO TFT.

(g) Summary

To realize low cost, large size, high resolution, high frame rate AM-OLED display, a self-aligned top-gate oxide TFT technology was developed. The Al-reaction method is suitable for making stable source/drain regions of a self-aligned TFT. The high temperature annealing process stabilizes the source/drain regions without increasing the sheet resistance. As the channel material, IGZO (In:Ga:Zn = 2:2:1), higher mobility IGZO, and ITZO were evaluated, and the mobility of 9.8, 21.4, and 32.0 cm^2/Vs were confirmed, respectively. When the lifetime of the display is determined from the limit of 3 V in ΔVth, it becomes 5.2×10^8 sec (over ten years). It is sufficiently long for TFT application to the AM-OLED displays. According to these technologies, 9.9-in. diagonal qHD AM-OLED displays with a-IGZO channel and a-ITZO channel were fabricated and demonstrated. This 5-Mask processed self-aligned top-gate oxide TFT would be the most cost competitive TFT backplane with superior reliability for the top emission AM-OLED display at this moment.

Chapter 4 Conclusion

In this thesis, a micro-crystalline silicon TFT and an oxide TFT were studied for the AM-OLED display. The main concept in creating novel TFT technology is based on the low cost manufacturing of the high performance TFT for the AM-OLED display. Several technologies for high reliability, high uniformity, high mobility, and low parasitic capacitance were examined and confirmed for the manufacturing, and those capabilities were confirmed with prototypes. The main conclusions of this thesis are summarized as follows.

4-1. Micro-crystalline silicon TFT technology

(a) dLTA process

Because the OLED is a current-driven device, the driving TFT tends to degrade by the high bias, high current flow condition for the emission of the OLED device. A crystallized silicon is a good candidate as the channel of TFT to achieve high reliability; however, the conventional LTPS TFT with poly-crystalline silicon channel has issues in the uniformity and the manufacturing cost. The proposed crystallization method “dLTA (diode laser thermal annealing)” applying the Mo-capped silicon precursor and the scanning CW laser annealing system realizes small grained uniform micro-crystallized silicon and low cost manufacturing process like a-Si TFT.

(b) Micro-crystalline silicon TFT

According to the dLTA process, a micro-crystalline silicon TFT with high mobility and 10 years of lifetime for AM-OLED display was developed. Its field effect mobility, threshold voltage (Vth), and sub threshold slope (S) were 3.1 cm^2/Vs, 2.3 V, and 0.93 V/decade, respectively. And the calculated threshold voltage shift after 3.6E8 sec of current flow stress was only 1.77 V. The process flow of the a-Si TFT manufacturing is followed to achieve low cost manufacturing. Only adding Mo-capping process and laser annealing process to the conventional etching stopper type a-Si TFT process flow, a micro-crystalline TFT process is realized. Its mobility is low for the 240Hz frame rate driving, the 4k resolution, or the driver integration; however, a stable TFT for the AM-OLED driving can be achieved by the small amount of additional investment to the conventional a-Si TFT manufacturing line.

4-2. Oxide TFT technology

(a) Bottom-gate oxide TFT

In 2000's the amorphous oxide transistor had a serious issue in the reliability while it showed superior transistor properties. To solve this issue, it was found that the AlOx passivation applied etching stopper type TFT realizes superior TFT characteristics and reliability. Its mobility, S factor, and Vth were 11.5 cm^2/Vs, 0.27 V/decade, and 0.3 V, respectively. The extrapolated threshold voltage shift under the 15 V of gate and drain bias stress for 100,000 hours was almost 1V. It is enough low for 10 years lifetime of AM-OLED display. The low cost manufacturing is achieved by using the scalable and efficient production tools which are commonly used in the a-Si TFT manufacturing. The process flow of the etching stopper type oxide TFT is composed by 5-Mask steps. It is supposed to be competitive with that of a-Si TFT for the AM-LCD.

(b) High mobility oxide materials: a-ITZO and c-IGO

The generally used IGZO (In:Ga:Zn = 1:1:1 ~ 2:2:1) has a mobility around 10 cm^2/Vs. This value is enough for the pixel circuit of the ultra-high definition, 240 Hz driving AM-OLED display; however, higher mobility is expected for the higher definition, higher frame rate AM-OLED displays or the driver-circuit integration. For this purpose, a-ITZO and crystalline IGO were evaluated, and higher mobilities than a-IGZO were confirmed with enough high reliability for AM-OLED display. The mobility, sub-threshold swing value (S factor), and threshold voltage of a-ITZO TFT were 30.9 cm^2/Vs, 0.21 V/decade, and 0.97 V, and those of c-IGO TFT were 23.8 cm^2/Vs, 0.30 V/decade, and −0.1 V, respectively. The threshold voltage shifts under the 15V of gate and drain bias stress for 10,000 sec were 0.1V and 0.3V, respectively. This difference in threshold voltage shift looks small: however, the crystallinity itself may not be meaningful for the reliability. The dissoluble property to the Al etchant is sometimes valuable for the TFT structure or the production yield of the TFT; however, a-ITZO may be a better candidate for the higher mobility with high reliability, thinking for the limitation of the c-IGO in the stable micro-crystallized film formation. The crystallinity is affected by the chamber condition; therefore, it is important to control the chamber condition for the stable crystallized film formation.

(c) Issues in the manufacturing

When applying the oxide TFT to the display industry, it is better to use the existing infrastructure for the conventional a-Si or LTPS TFT to suppress the investment cost and to simplify the installation of the new oxide TFT process. Because

the OLED is a current-driven device, the uniformity of the TFT device would be the most serious issue to be solved at the early stage. As well as the uniformity of the TFT characteristics, the uniformity of the TFT reliability is important. Particularly, the non-uniformity caused by the multi-cathode type PVD system was found to affect the uniformity of the TFT characteristics and reliability. By optimizing the sputtering condition, it could be improved; however, further improvement is expected. It is expected to develop a new PVD, which has uniform plasma over the large substrate entirely for the AM-OLED display.

(d) New applications by oxide TFT driven AM-OLED display

A flexible panel and a transparent panel were demonstrated in order to utilize the low temperature nature of the manufacturing process and the transparent feature of the oxide semiconductor materials. Because the OLED is a self-emitting device, a flexible OLED display is expected due to no back-light system and no viewing angle issue unlike LCD. From the same reason, a transparent OLED display is expected due to no polarizer, no color filter structure unlike LCD. Therefore, AM-OLED display is suitable for the flexible and transparent displays. The oxide TFT was successfully integrated on the flexible substrate and it showed the same performance with that on the glass substrate. And the transparent property of the oxide material was confirmed to contribute to the transparency of the AM-OLED display, and the transmittance over 50% was achieved. According to the unique property of the oxide material, it was proved that the oxide TFT has a potential to give new applications such as flexible displays and transparent displays.

(e) Top-gate oxide TFT

When competing with the a-Si TFT for LCD at a point of the manufacturing cost, a self-aligned top-gate structure is effective. A TFT can be fabricated by only four Masks; moreover, 5-Mask processed TFT backplane for AM-OLED display is available by merging the source/drain metal and anode metal (Fig. 121). The self-aligned top-gate TFT would be the best TFT structure for the AM-OLED display from the manufacturing cost point of view.

Because the OLED is a current-driven device, the compensation driving is required for the uniform emission of light over the screen front. Due to the complex signal operation for the compensation driving, RC delay is the serious issue for the accurate compensation. To solve this issue, the minimization of the parasitic capacitances is extremely valuable (Fig. 122). Moreover, it is also valuable for the accurate compensation driving to suppress the variation between Cgs and Cgd, which

is occurred by the alignment error of the photo-lithography process. According to these reasons, the self-aligned top-gate TFT structure is ideal for the TFT of the AM-OLED display, especially for large size, high resolution, and high frame rate specification. In the case of a-IGZO TFT, the mobility, S factor, and Vth were 9.8 cm^2/Vs, 0.22 V/decade, and –1.5 V, respectively. In the case of a-ITZO TFT, the mobility, S factor, and Vth were 32.0 cm^2/Vs, 0.12 V/decade, and –0.09 V, respectively. When the lifetime of the display is determined from the 3V limit of the threshold voltage shift in the PBTS test of Vg = Vd = 10 V, it becomes 5.2×10^8 sec, which is sufficiently long for the TFT application of the AM-OLED displays.

The low cost, small parasitic capacitance, and highly reliable self-aligned top-gate oxide TFT would be the best candidate for the TFT backplane of the AM-OLED display.

Display mode		<LCD>	<OLED display>		
Structure		Bottom gate Back channel etch.	Bottom gate Etch. stopper	Top gate (Standard)	Top gate (Anode merge)
Process step (Photo-lithography)	TFT	Gate Si S/D PSV PIX	Gate Oxide Etch. stopper S/D PSV	Oxide Gate IL S/D	Oxide Gate IL S/D, Anode
	Anode		PLN Anode WIN	PLN Anode WIN	WIN
Channel material		a-Si	Oxide	Oxide	Oxide
Mask number (for TFT only)		5 (5)	8 (5)	7 (4)	5 (4)

Fig. 121 Standard TFT process flows and proposed 5-Mask process flow.

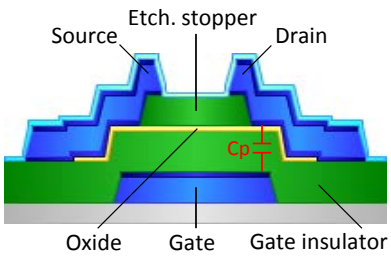
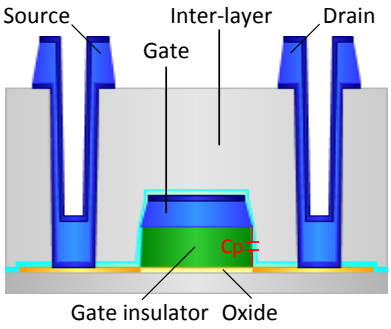
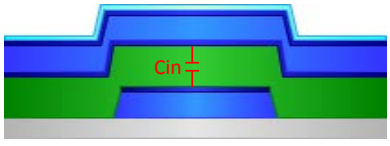
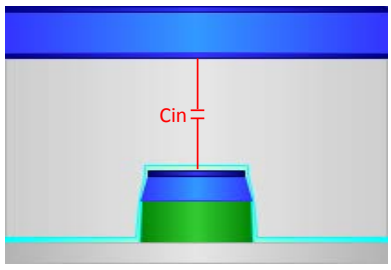
Structure		Bottom gate Etch. stopper	Top gate Self-align.
Cross section	TFT		
	Crossing		
Cp		1	~ 1/3
Cin		1	~ 1/5

Fig. 122 Cross-sectional views and parasitic capacitances of etch. stopper type bottom-gate TFT and self-aligned top-gate TFT.

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Acknowledgement

First of all, I sincerely thank my academic supervisor Prof. Yukiharu Uraoka, Nara Institute of Science and Technology, for his exhaustive and painstaking instructions on accomplishing this thesis. In addition, I deeply thank Prof. Jun Ohta, Prof. Hisao Yanagi, and Assic. Prof. Yasuaki Ishikawa for their precious comments and advices to my study and thesis.

Almost all studies in this thesis had been done from 2004 to 2015, when I worked in Sony Corporation Atsugi technology development center. I would like to thank Mr. Tetsuo Urabe, who gave me a chance to develop the micro-crystalline silicon TFT for AM-OLED display, and Mr. Tatsuya Sasaoka, who gave me a chance to develop the oxide TFT for AM-OLED display.

In the development of the micro-crystalline silicon TFT technology, I would like to thank Mr. Koichi Tatsuki, Dr. Narihiro Morosawa, Mr. Kazuhiko Tokunaga, Mr. Yasunobu Hiromasu, Mr. Koji Hidaka, Mr. Tetsuo Nakayama, Mr. Atsuya Makita, Mr. Motohiro Toyota, Mr. Naoki Hayashi, Mr. Yusuke Yoshimura, Mr. Ayumu Sato, Mr. Kimiyasu Namekawa, Mr. Hirokazu Yamada, Mr. Takayuki Ito, Mr. Hajime Kaneko, Mr. Hiroshi Musha, Mr. Yoshio Inagaki, Mr. Nobuhiko Umezu, Mr. Katsuya Shirai, Mr. Makoto Yoshizaki, Mr. Satoshi Bannai, Mr. Masaaki Abe, Mr. Koichi Tsukihara, Mr. Shin Hotta, Mr. Tsuyoshi Matsunobu, Mr. Kosuke Kamiya, and the manufacturing technology development group of Sony corporation, for their valuable comments and devoted cooperation.

In the development of the oxide TFT technology, I would like to thank Mr. Kazumasa Nomoto, Mr. Yoshito Shiraishi, Dr. Narihiro Morosawa, Mr. Kazuhiko Tokunaga, Mr. Yasuhiro Terai, Mrs. Eri Fukumoto, Mr. Takashige Fujimori, Mr. Tetsuo Nakayama, Mr. Yoshihiro Oshima, Mr. Mitsuo Morooka, Mr. Tomoatsu Kinoshita, Mr. Masanori Nishiyama, Mr. Ayumu Sato, Mr. Junji Iwasaki, Mr. Keiichi Akamatsu, for their valuable comments and devoted cooperation, and the materials analysis center of Sony corporation for their support in analysis, and Idemitsu Kosan corporation for their supply of the valuable new oxide semiconductor materials. And I would like to also thank Mr. Yoshito Shiraishi, Mr. Yasunobu Hiromasu, Mr. Takahide Ishii, and the joint development members of AU Optronics Corporation in Taiwan, for their devoted activities in the FAB in Taiwan.

Finally, I deeply thank my family for their understanding and supports for accomplishing this thesis.

List of publications

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