Oxide Semiconductor Thin Film Transistors with High-K Dielectric Material Fabricated by Solution Process

(溶液プロセスによる高誘電率材料を用いた酸化物系薄膜トランジスタの作製)

Li Lu

Graduate School of Materials Science

Nara Institute of Science and Technology

Supervisor: Prof. Yukiharu Uraoka

March 2013

Contents

Chapter 1

Introduction

"Active-matrix" and "passive-matrix" displays are two main types of flat-panel display.[1)] The most common type of active-matrix display is based on a technology known as thin film transistor (TFT). TFTs act as switching devices to turn each pixel in the display “on” (light) or “off” (dark). A TFT is generally constituted of gate electrode, gate dielectric layer, active semiconductor channel layer, and source/drain electrodes. Materials of gate dielectric and semiconductor channel layer, and their fabrication methods play important roles on TFTs’ performances. SiO_2 is a conventional gate dielectric. In order to miniaturize the device size and obtain low operating voltage subsequently decrease energy consumption, high-k materials like HfO_2, Al_2O_3, Ta_2O_5 were intensively studied.[2-10)] For the semiconductor channel layer, the material changing from Si to oxide material also happened based on the versatile needs of displays such as low temperature fabrication.[11-12)] In order to fabricate these materials, vacuum-based methods of sputtering and chemical vapor deposition are traditional adopted. Although high quality thin films can be fabricated by the use of these vacuum-based methods, the cost is high and the process is complicated.[13-18)] An alternative method of solution process which is simple and low cost appeared on the stage recently.

1.1 TFT

1.1.1 Passive- and active-matrix displays

Passive-matrix display is a common type of flat-panel display consisting of a grid of horizontal and vertical wires (Fig. 1-1(a)).[1)] At the intersection of each grid is an liquid crystal display (LCD) element which constitutes a single pixel, either letting light through or blocking it. The simplicity of the passive-matrix system is good, but it has significant drawbacks, notably slow response time and imprecise voltage control. An active-matrix display has a higher quality, which uses a transistor to control each pixel (Fig. 1-1(b)).[1)] Active-matrix displays could refresh the screen more frequently than in conventional passive-matrix displays. The most common type of active-matrix display is based on a technology of TFT.

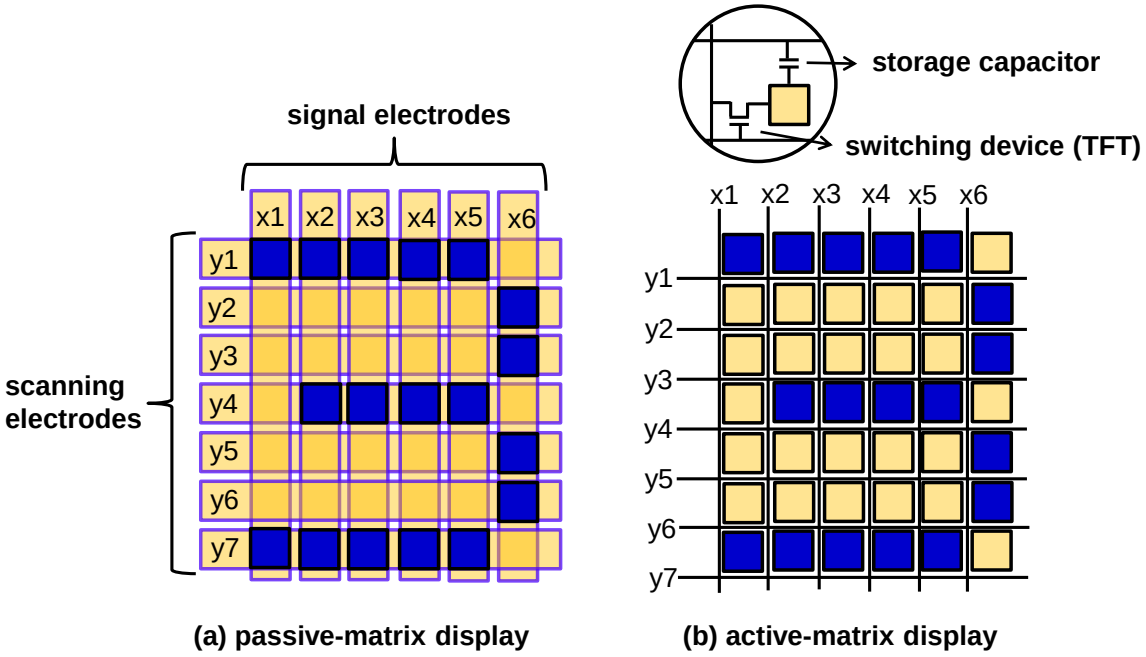


Fig. 1-1 Schematic diagrams of (a) passive-matrix and (b) active-matrix displays.

1.1.2 Basic structure of TFT

TFT is a special kind of metal-oxide-semiconductor field-effect transistor (MOSFET) made by depositing thin films of an active semiconductor channel layer as well as the gate dielectric layer and metallic contacts over a supporting substrate (Fig. 1-2).[19-20] A common substrate is glass, since the primary application of TFTs is in LCDs. This differs from the conventional transistor where the semiconductor material typically is the substrate, such as a silicon wafer. A TFT whose active, current-carrying layer is a thin film, in contrast to MOSFETs, which is made on Si wafer and use the bulk-silicon as the active layer. In a flat-panel display, light must be able to pass through the substrate material to reach the viewer. Glass is the most commonly used starting substrate because it is highly transparent and is compatible with conventional semiconductor processing steps.

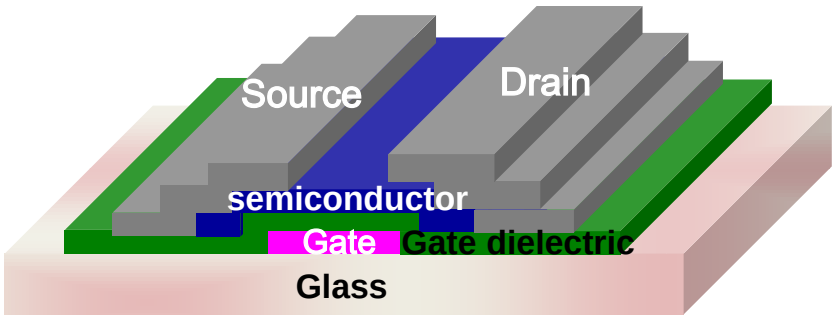


Fig. 1-2 Schematic diagram of TFT device structure.

The actions of TFTs are shown in Fig. 1-3. In a simple TFT, for example n-channel TFT, when a negative voltage is applied on the gate, electrons are depleted in the channel, hence almost no current is present. When a positive voltage is applied on the gate; negative charges are induced on the semiconductor channel, which are in the region between source and drain; these negative charges flow from drain to source to make the channel conductive. Thus, TFTs act as switches to turn each pixel "on" (light) or "off" (dark) on the display.

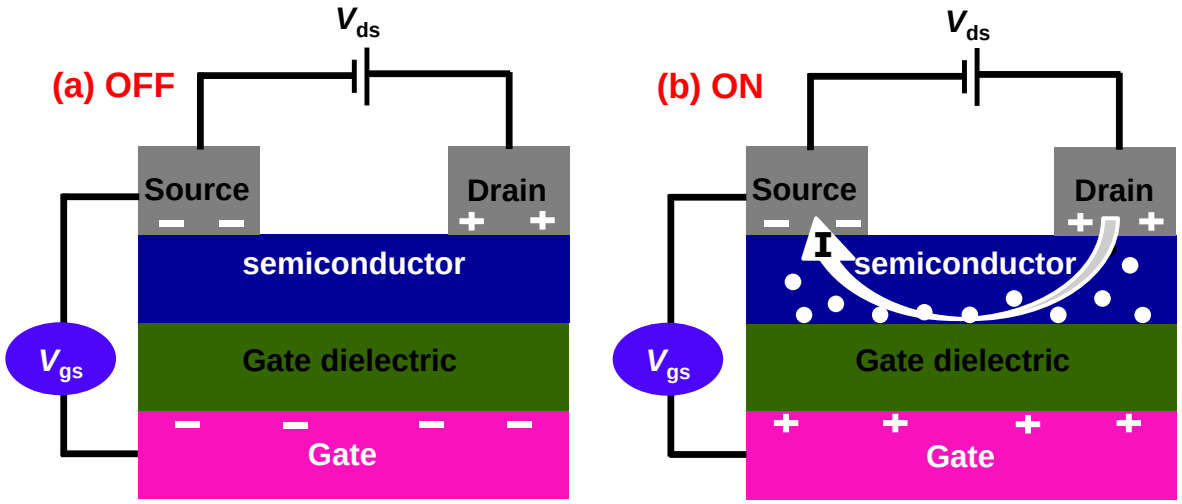


Fig. 1-3 Actions of TFTs: (a) off-state and (b) on-state. V_{gs} is the gate voltage and V_{ds} is the drain voltage. The arrow in (b) delegates the direction of current (I) in the channel.

1.1.3 Important parameters for evaluating characteristics of TFTs[1, 20-21)]

The electrical characteristics which determine TFTs' performance are evaluated in terms of several parameters such as field effect mobility (μ_{FET}), on-off current ratio (I_{on}/I_{off}), threshold voltage (V_{th}), and subthreshold swing (S), as shown in Fig. 1-4.

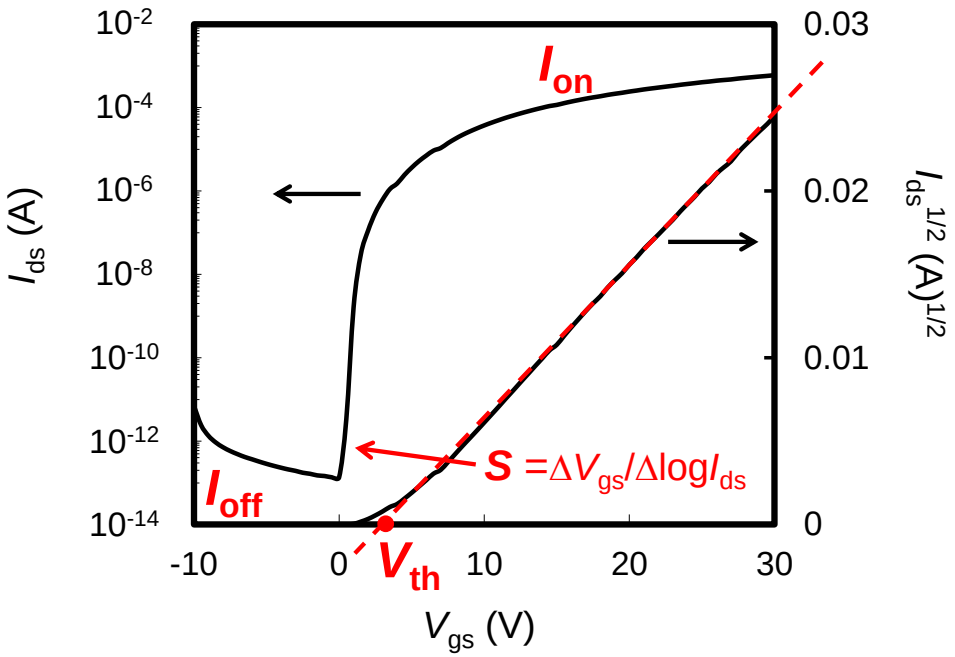


Fig. 1-4 Schematic diagram of various parameters.

A. μ_{FET} (unit: $cm^2/(V\cdot s)$)

The μ_{FET} is the average charge carrier drift velocity per unit electric field and measure of how easily large carriers can move in the device. Large mobility is required for reliable operation of transistor. Mobility increases with increase in channel length and active semiconductor layer thickness. By measuring the drain current (I_{ds}) with respect to V_{gs}, the μ_{FET} can be obtained from

$$\mu_{FET} = \frac{g_m}{\frac{W}{L}C_i V_{ds}} \quad , \tag{1-1}$$

where V_{ds} is the source-drain voltage, C_i is the capacitance of the gate dielectric per

unit area, W is the channel width and L is the channel length. The g_m is trans-conductance, which is calculated by $g_m = \frac{\partial I_{ds}}{\partial V_{gs}}$.

B. I_{on}/I_{off}

The ratio of current in the accumulation mode over the current in the depletion mode is called I_{on}/I_{off}. In this research, the I_{on} and I_{off} were defined as the highest and the lowest I_{ds} in the measured range. Current ratio depends upon various factors such as materials, channel length, and thickness of semiconductor. It should be more than 10^6 for memory and display devices.

C. V_{th} (unit: V)

The V_{th} of a MOSFET is usually defined as the V_{gs} where an inversion layer forms at the interface between the gate dielectric layer and the substrate (semiconductor body). The formation of the inversion layer allows the flow of electrons through the gate-source junction. Lower V_{th} is useful in lowering device power consumption and useful in producing portable devices. There are several methods to extract the V_{th} value. In general, the V_{th} value was extracted from linear fittings to the plot of the square root of I_{ds} versus V_{gs}. This was adopted in this research.

D. S (unit: V/decade)

When the V_{gs} is below the V_{th} and the semiconductor surface is in weak inversion or depletion, i.e., subthreshold region, the corresponding I_{ds} is called the subthreshold current. The subthreshold region tells how sharply the current drops with V_{gs} and is particularly important for low-voltage and low-power applications. The subthreshold current exponentially depends on the V_{gs} as well as the V_{ds} because below V_{th} the free carrier density exponentially depends on the local voltage. Therefore, a plot of logarithmic I_{ds} versus V_{gs} with drain, source, and bulk voltages fixed will exhibit approximately linear behavior in the MOSFET operating regime. The S is defined by the inverse of the slope of this plot. By this definition, S is calculated by[20-21)]

$$S = \frac{\partial V_{gs}}{\partial \log I_{ds}} \quad . \tag{1-2}$$

The S of a typical MOSFET is limited by $(kT/q)\ln 10$, roughly 0.06 V/decade at room temperature, where k is the Boltzmann's constant, T is the temperature and q is

the electronic charge.

These parameters strongly depend on the device structure and fabrication process, the semiconductor materials, and the gate dielectrics or interconnect metals in contact with the semiconductor. Because fast switching is the key role of TFT devices in electronic applications, one would in general target high μ_{FET} and I_{on}/I_{off}, V_{th} close to zero, and S as small as possible. To extract information about impurity concentrations, interface states and traps, it is common practice to use V_{th} and subthreshold current as device evaluation parameters.

1.2 Oxide semiconductor TFTs

Conventional active-matrix flat panel displays are based on amorphous or single and poly-crystalline Si. Although hydrogenated amorphous silicon (a-Si:H) have been extensively investigated for flexible electronics, the carrier mobility of a-Si:H is typically 1 $cm^2/(V\cdot s)$ which is lower by two or three orders of magnitude than that of single-crystalline Si (200 $cm^2/(V\cdot s)$). Device performance is limited by the low mobility of the channel materials. The carrier transport in a-Si:H is controlled by hopping between localized tail-states, and band conduction.[11] As shown in Fig. 1-5(a), in Si, carrier transport paths composed of strongly directive sp3 orbital, so structural randomness greatly degrades the magnitude of bond overlap, i.e., carrier mobility. Therefore, when Si is in amorphous state, the mobility significantly decreased. On the other hand, Si-based devices are of less interest for transparent circuits because they are not transparent, owing to the small bandgap.

In the last few years, several metal oxide based TFTs have been reported. The first reports of transistors based on polycrystalline ZnO.[12] Fortunato *et al.* and Nomura *et al.* presented the first fully transparent TFTs produced at room temperature using ZnO and amorphous InGaZnO (IGZO), respectively.[12] Compared to a-Si:H TFT, oxide based TFTs could provide mobility exceeding 10 $cm^2/(V\cdot s)$ even deposited at room temperature using sputtering.[1] Amorphous oxide semiconductors composed of post-transition-metal cations.[11] As shown in Fig. 1-5(b) (spheres denote metal s orbitals), the contribution of oxygen 2p orbitals is small. Direct overlap between neighbouring metal s orbitals is rather large, and is not significantly affected even in an amorphous structure.

Furthermore, in contrast to Si-based material, these oxide materials have larger bandgap which provide the possibility of transparent application. Because of such remarkable characteristics, oxide semiconductor TFTs are excellent candidate switching elements for large area, ultra definition (UD), and fast frame rate active-matrix LCD panels. By properly implementing IGZO TFT arrays, Samsung

Electronics successfully developed a 70-inch 240 Hz 3-dimensional UD TV prototype that was presented at FPD International 2010 in November. In addition to active-matrix LCDs, oxide semiconductor TFTs are also promising alternatives to low temperature poly-silicon TFTs that are used as driving elements in active-matrix organic light-emitting diode displays.

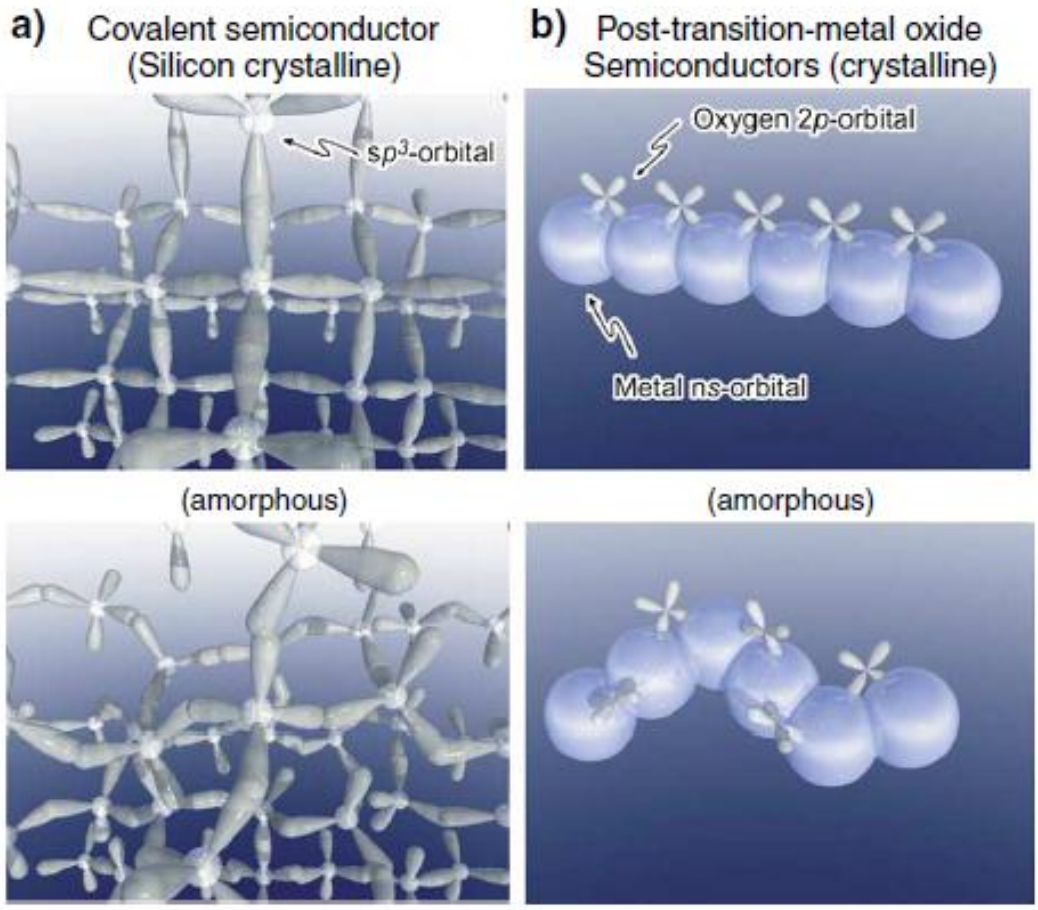


Fig. 1-5 Schematic orbital structure of the conduction-band minimum in (a) Si and in (b) ionic oxide semiconductor.[11)]

1.3 High-k material

Amorphous, thermally grown silicon dioxide (SiO_2) has been used as a gate dielectric material for decades. The use of SiO_2 as the gate dielectric offers a stable, high quality Si-SiO_2 interface as well as superior electrical isolation properties.

However, as transistors have decreased in size, the thickness of the SiO_2 gate dielectric has steadily decreased to increase the gate capacitance and thereby drive current, raising device performance. As the thickness scales below 2 nm, leakage currents due to tunneling increase drastically, leading to high power consumption and reduced device reliability. Replacing the SiO_2 gate dielectric with a material with high dielectric constant k or ε (as compared to SiO_2), i.e., high-k material, allows increased gate capacitance without the associated leakage effects.

Many materials systems are currently under consideration as potential replacements for SiO_2. However, very few materials are promising with respect to all guidelines which including dielectric constant, band gap and band alignment to silicon, thermodynamic stability, film morphology, interface quality, process compatibility and reliability. The industry has employed oxynitride gate dielectrics since the 1990s, wherein a conventionally formed silicon oxide dielectric is infused with a small amount of nitrogen. The nitride content subtly raises the dielectric constant and is thought to offer other advantages, such as resistance against dopant diffusion through the gate dielectric. In early 2007, Intel announced the deployment of hafnium-based high-k dielectrics in conjunction with a metallic gate for components built on 45 nanometer technologies, and has shipped it in the 2007 processor series codenamed Penryn. Except the high-k materials mentioned above, Ta_2O_5, Al_2O_3, ZrO_2 and other materials were also researched a lot.[2-10)]

By the use of high-k materials as gate dielectrics of TFTs, it is possible to drive TFTs at low gate voltage according to the following equation[1)]

$$I_{\mathrm{ds}} = \frac{WC_{\mathrm{i}}}{L}\mu_{\mathrm{FET}}\left[\left(V_{\mathrm{gs}} - V_{\mathrm{th}}\right) - \frac{V_{\mathrm{ds}}}{2}\right]V_{\mathrm{ds}} \quad . \tag{1-3}$$

Assumed the μ_{FET} and I_{ds} are constants, increase of the C_{i} could decrease V_{gs} and V_{ds}. Consider a parallel plate capacitor, $C_{\mathrm{i}} = \frac{\varepsilon\varepsilon_0 \mathrm{A}}{d}$,[2)] where ε_0 is the permittivity of free space (=8.85×10^{-12} F/m), A is the area of the capacitor, and d is the thickness of the dielectric. The C_{i} is proportional to the ε while A and d are constants.

1.4 Solution process

For depositing dielectric and semiconductor thin films, vacuum-based processes of sputtering, chemical vapor deposition, atomic layer deposition, pulsed laser deposition and molecular beam epitaxy are generally used. However, these vacuum-based processes are complicated and expensive. Alternatively, solution

process allows for the deposition of films at atmospheric pressure with minimal equipment cost. The first chemical solution deposited electronic oxide thin films were prepared in 1980s.[22] The solution process also allows for uniform, large-area coverage, and easy compositional control of multicomponent materials, which is important for high through-put industrial applications.[23]

1.4.1 Deposition of thin films[24-26]

Several solution coating and patterning techniques are shown in Fig. 1-6. Coating techniques can be classified into two categories: direct growth of the material on the substrate during deposition or liquid coating that requires additional processing to remove solvent and yield the desired phase.

Direct growth methods include electrochemical and electroless chemical bath deposition (CBD). CBD methods rely on the controlled reaction and precipitation of reagents in solution. Nucleation and film growth occurs on the surface of a substrate immersed in the solution bath. However, the main drawback of CBD is the quantity of solution waste. Spin-coating is extensively used for smaller, laboratory-scale device processing due to its simplicity and high reproducibility. During the process, the substrate is secured to the spin-coater by a vacuum chuck, and an excess of solution is applied to the surface. Then the substrate is rapidly accelerated (typically to several 1000 rpm), which drives solution flow radially outward. A uniform, thin film is left after spin-off and solvent evaporation. Dip-coating involves the entrainment of a solution layer on a substrate as it is withdrawn from a solution reservoir, either in batches or in a continuous roll-line.

During doctor blading (knife-over-roll coating), the film thickness is controlled by gap between the blade and the substrate. Instead of a blade, a wire-wound metering rod (referred to as a Mayer/Meyer rod) can also be used. The amount of coating left on the substrate is determined by the diameter of the wire on the rod. Slit, slot, and die casting involve flowing the solution through a slotted head above the substrate. The line speed is frequently much faster than the speed of the extrusion, which enables coatings to be considerably thinner than the width of the slot. These methods can be used for high solids loading solutions (5–50000 cP) and are easily scaled to a roll-to-roll production line.

Spray-coating is an attractive non-contact, large-area deposition method. It can be used as either a liquid coating method or for the direct growth of films if the substrate temperature is above the decomposition temperature of the precursors. This method is commonly referred to as spray pyrolysis. In general, an atomized solution is generated pneumatically or ultrasonically and then directed onto the substrate with

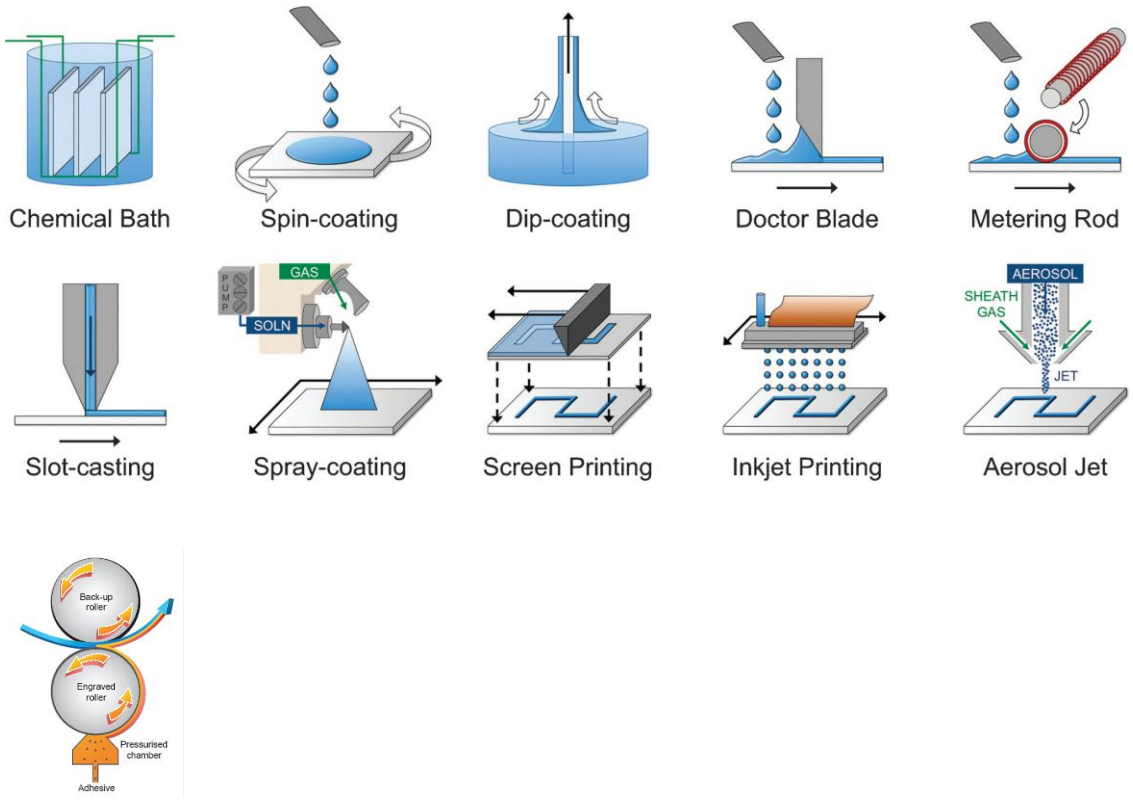


Fig. 1-6 Depiction of various solution deposition methods.[24-25)]

a carrier gas. Spraying requires low viscosity solutions (typically 10 cP).

Patterning from solution has been traditionally performed by contact methods such as screen-printing with a mask or stamping. These methods require a degree of force for application and require high viscosity solutions. Direct-write methods such as inkjet printing and aerosol jet are attractive alternatives. These methods offer several advantages, including the ability to deposit multilayer structures without the need of photolithography and non-contact processing for use with fragile thin-film substrates. Furthermore, these drop-on-demand deliveries allow for maximum material utilization.

The gravure coater has become one of the most popular types of coaters in use today due to its ability to apply less coating with more precision than other methods. The gravure coating process relied on an engraved roller running in a coating bath, which fills the engraved dots or lines of the roller with the coating material. The excess coating on the roller is wiped off by the doctor blade and the

coating is then deposited onto the substrate as it passes between the engraved roller and a pressure roller.

1.4.2 Precursors of spin-coating method[22)]

Since the spin-coating is extensively used for smaller, laboratory-scale device processing, it was used for the deposition of thin films in this research. The process of spin-coating starts with the preparation of suitable precursors that are often salts, typically, carboxylates, or other metallo-organic compounds, usually, alkoxides. The precursors are dissolved in appropriate solvents and mixed in a stoichiometric ratio that yields the desired composition of the final film. In some cases, additives such as chemical stabilizers are included during solution synthesis and additional processing steps are employed to adjust the properties of the coating solution.

The chemical interactions that occur between the starting reagents during solution synthesis will depend on the reactivity of the compounds and the solution preparation conditions, such as reflux temperature. In classical sol-gel processing routes, the reactivity of the reagents is high, and if alcohol exchange occurs, or if modifying ligands are used, the structure of the species in solution can bear little resemblance to the starting compounds. In this case, the species that are generated are frequently oligomeric in nature and can contain more than one type of cation. In contrast, for long-chain carboxylate compounds, which have been historically used in metal organic decomposition (MOD) routes, reactivity is low and the chemical interactions between the different precursor compounds is minimal. In addition to manipulation of reaction conditions to control precursor species characteristics, the viscosity, solute concentrations, and solvent system must also be adjusted at this stage for the coating technique that will be employed and the type of substrate. Depending on the procedures utilized during coating solution preparation, the gelation behavior of the deposited film, and the reactions that take place during thermal annealing, the various chemical routes utilized for electronic oxide film fabrication can be generally grouped into three principal categories:

- Classical sol-gel processes that use alkoxide precursors that undergo primarily hydrolysis and polycondensation. Since they do not contain polymeric materials such as organic acids, and the principal constituents of the solution are themselves precursors, they are generally excellent for low-temperature film formation.
- MOD routes that utilize carboxylate precursors that do not undergo significant condensation reactions during either solution preparation or film deposition. Chemical reactions occur on the substrates by heating. This is a simple method of

forming a thin oxide film.

- Hybrid routes that exhibit condensation reactions at several process stages; frequently, this route is used when multicomponent oxide films, e.g., perovskite materials, are prepared from multiple precursor types or when chelating ligands are added to solutions with multiple precursor types.

After the deposition of the coating solution on the substrate by spin coating, the (wet) as-deposited film is dried, pyrolyzed, crystallized, and (optionally) post-annealed for further densification or microstructure manipulation. The term 'pyrolysis' is normally defined as the conversion of solid organic materials, into gases and liquids by indirect heat under exclusion of air, or oxygen, respectively, which is predominantly used to describe the decomposition of the organic matrix in air or oxygen. The conversion of the wet, as-deposited film into the desired film is induced through controlled thermal processes, which typically employ either a hot plate and conventional furnace, or a rapid thermal annealing (RTA) oven. If the desired film thickness is not obtained in the first coating cycle, the deposition and thermal process sequence are repeated to prepare thicker films.

1.5 Background and objective of this research

Since ZnO-based oxide semiconductors have wide bandgap and high mobility even though fabricated at low temperatures, ZnO-based semiconductors were used as the active channel layer material of TFTs in this research.[2-10)] In order to obtain superior performance TFTs, sputtering, pulsed laser deposition and plasma enhanced chemical vapor deposition are generally used for the production of ZnO-based thin films.[13-18)] Recently, there has been substantial interest in the use of solution process for the fabrication of these materials. However, the performance of the fabricated TFTs is still not high enough for the application of displays.[13-18)] In particular, when the annealing temperature is lower than 400 ^{o}C, device characteristics become very poor because large amounts of organic residues remains in thin films at low annealing temperatures.[13-18)] Therefore, high performance TFTs using solution process-derived ZnO-based semiconductors as channel layers were expected to be fabricated at temperatures lower than 400 ^{o}C in this research.

On the other hand, high operating voltages are often required to achieve high mobility and high I_{on}/I_{off} for ZnO-based TFTs. In order to solve this problem, high-k materials of amorphous (Ba,Sr)TiO_3, TiO_x, Al_2O_3 were alternatively used as gate dielectrics.[4, 6-7)] Certain Ta_2O_5-based material, $SrTa_2O_6$ (STA), was regarded as a promising candidate because it has a high ε of about 100-110 in crystalline state and

about 30-40 in amorphous state.[27-32] These values of ε are higher than many high-k materials now being used. STA also shows low leakage current which could ensure low power consumption and avoid information loss on electrical devices. Another Ta_2O_5-based material, $BaTa_2O_6$ (BTA), also had a high ε of about 20-30 in amorphous state.[33] However, since there were limited reports on STA and BTA thin films, their potential on the application of TFTs was not clear. In particular, the material mixed by STA and BTA, i.e., $(Ba,Sr)Ta_2O_6$, have not been reported until now. Consequently, the properties of the material $(Ba,Sr)Ta_2O_6$ were expected to be clearly understood in this research. Suitable compositional $(Ba,Sr)Ta_2O_6$ thin films would be used as the gate dielectric for realizing low-operating-voltage TFTs.

Meanwhile, in these limited reports, the fabrication method of STA and BTA thin films were mainly vacuum process. Therefore, solution process would be used for fabricating BSTA thin films. Both channel layer of ZnO-based semiconductor thin films and gate dielectric of BSTA thin films were expected to be fabricated by solution process.

1.6 Structure of this thesis

This thesis was constituted by the following six chapters. Fig. 1-7 shows the structure of this thesis.

Chapter 1 Materials that were used for the semiconductor channel layer and gate dielectric of thin film transistors, and the deposition methods of these materials were introduced.

Chapter 2 Dielectric and leakage current properties of solution-process derived high-k materials of $(Ba,Sr)Ta_2O_6$ thin films were introduced. Composition effect, temperature dependency and low-temperature fabrication process of UV/O_3-assisted annealing were discussed.

Chapter 3 Characteristics of TFTs using solution process-derived InZnO thin films as channel layers and thermally oxidized SiO_2 thin films as gate dielectrics were introduced. Organic and aqueous solutions were used to fabricate InZnO thin films.

Chapter 4 Characteristics of sputtered-InGaZnO, aqueous solution-derived InZnO and organic solution-derived InZnO TFTs using $SrTa_2O_6$ thin films as gate dielectrics were introduced. Low-operating-voltage TFTs were obtained by use of $SrTa_2O_6$ thin films.

Chapter 5 Gate voltage stress instability of TFTs using aqueous solution-derived InZnO thin films as channel layers and thermally oxidized SiO_2 thin films as gate dielectrics were evaluated. In order to improve the instability, atomic layer deposition derived Al_2O_3 thin films were used to passivate the back-channel

region of TFTs.

Chapter 6 Conclusions and future works

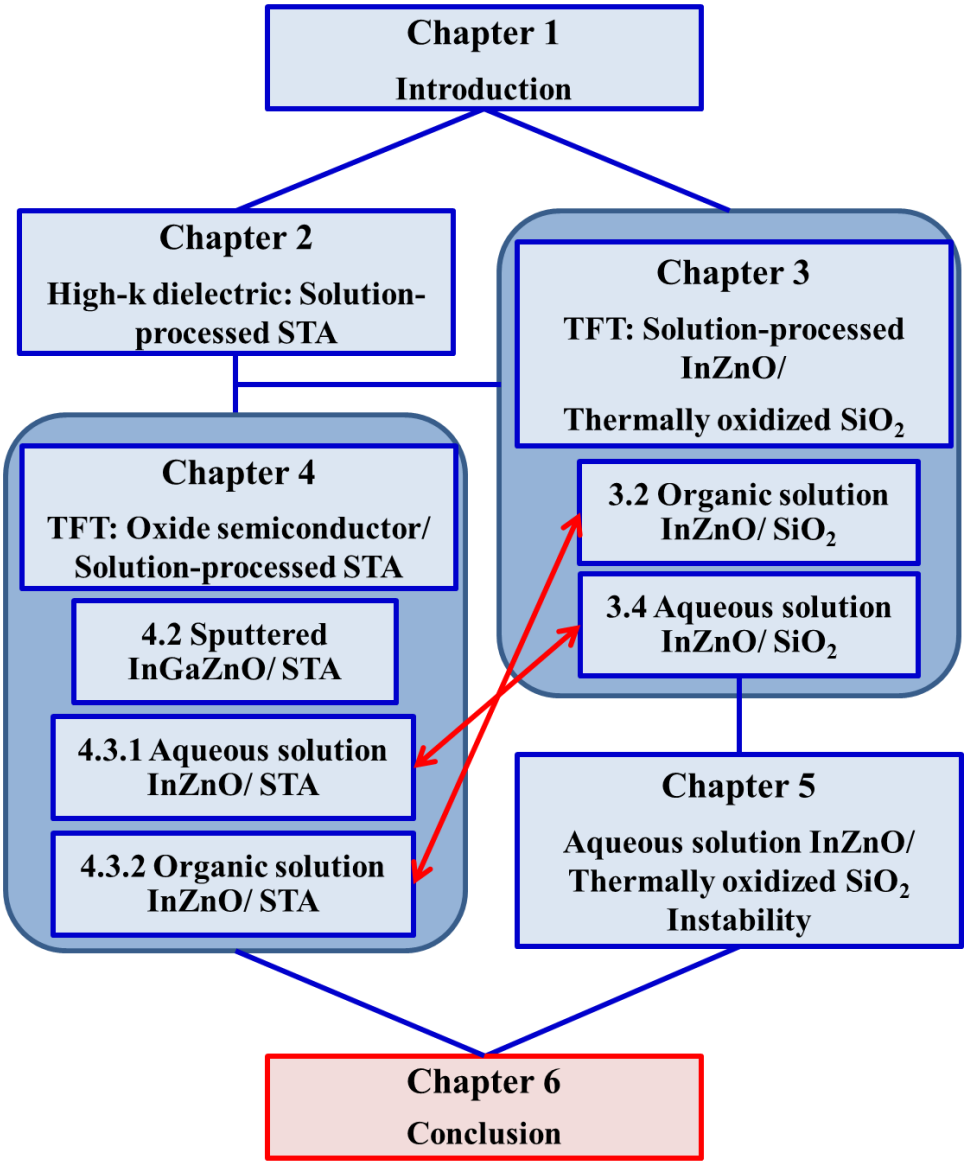


Fig. 1-7 Structure of this thesis.

[References]

1) Thin Film Materials & Devices Meeting: Thin-film transistor (Corona, Tokyo, 2008) P1, 7, 13-15, 49, 52, 68 [in Japanese]

2) H. R. Huff, and D. C. Gilmer: High Dielectric Constant Materials: VLSI MOSFET Applications (Springer, Berlin, 2005) P254, 263

3) J. Robertsona: Eur. Phys. J. Appl. Phys. **28** (2004) 2654)

4) J. Siddiqui, E. Cagin, D. Chen, and J. D. Phillips: Appl. Phys. Lett. **88** (2006) 212903

5) J. B. Kim, C. F.-Hernandez, and B. Kippelen: Appl. Phys. Lett. **93** (2008) 242111

6) J.-S. Park, J. K. Jeong, Y.-G. Mo, and S. Kim: Appl. Phys. Lett. **94** (2009) 042105

7) J.-M. Lee, I.-T. Cho, J.-H. Lee, W.-S. Cheong, C.-S. Hwang, and H.-I. Kwon: Appl. Phys. Lett. **94** (2009) 222112

8) K. Kishiro, N. Inoue, S.-C. Chen, and M. Yoshimaru: Jpn. J. Appl. Phys. **37** (1998) 1336

9) S. Ezhilvalavan, and T.-Y. Tseng: J. Appl. Phys. **83** (1998) 4797

10) W. S. Lau, K. K. Khaw, P. W. Qian, N. P. Sandler, and P. K. Chu: Jpn. J. Appl. Phys. **35** (1996) 2599

11) K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono: Nature, **432** (2010) 488

12) A. Facchetti and T. Marks: Transparent Elecronics: From Synthesis to Applications (Wiley, Wiltshire, 2010) P152

13) H. S. Shin, G. H. Kim, W. H. Jeong, B. D. Ahn, and H. J. Kim: Jpn. J. Appl. Phys. **49** (2010) 03CB01

14) Y.-J. Chang, D.-H. Lee, G. S. Herman, and C.-H. Chang: Electrochem. Solid-State Lett. **10** (2007) H135

15) C. G. Choi, S.-J. Seo, and B.-S. Bae: Electrochem. Solid-State Lett. **11** (2008) H7

16) C. Y. Koo, K. Song, T. Jun, D. Kim, Y. Jeong, S.-H. Kim, J. Ha, and J. Moon: J. Electrochem. Soc. **157** (2010) J111

17) D.-H. Lee, Y.-J. Chang, G. S. Herman, and C.-H. Chang: Adv. Mater. **19** (2007) 843

18) S. J. Kim, G. H. Kim, D. L. Kim, D. N. Kim, and H. J. Kim: Phys. Status Solidi A **207** (2010) 1668

19) H. Matsunami: Semiconductor Engineering (Shokodo, Tokyo, 1999) 2nd ed., P167, 171 [in Japanese]

20) J. S. Park, W.-J. Maeng, H.-S. Kim, and J.-S. Park: Thin Solid Films **520** (2012) 1679

21) S. M. Sze, and K. K. Ng: Physics of Semiconductor Devices (Eiley, New Jersey,

2007) 3rd ed., P205, 315
22) R. W. Schwartz, T. Schneller, and R.Waser: C. R. Chimie **7** (2004) 433
23) W. Sakamoto, Y.-S. Horie, T. Yogo, and S.-I. Hirano: Jpn. J. Appl. Phys. **40** (2001) 5599.
24) R. M. Pasquarelli, D. S. Ginley, and R. O'Hayre: Chem. Soc. Rev. **40** (2011) 5406
25) http://www.eikos.com/coating-deposition.html
26) N. Kapur: Chemical Engineering Science **58** (2003) 2875
27) V. Ya. Kunin, Yu. K. Tarnopol'skii, and N. A. Shturbina: Sov. Phys. J. **32** (1989) 556
28) M. Silinskas, M. Lisker, B. Kalkofen, and E. P. Burte: Mater. Sci. Semicond. Process. **9** (2006) 1102
29) W.-J. Lee, I.-K. You, S.-O. Ryu, B.-G. Yu, K.-I. Cho, S.-G. Yoon, and C.-S. Lee: Jpn. J. Appl. Phys. **40** (2001) 6941
30) D.-O. Lee, P. Roman, C.-T. Wu, P. Mumbauer, M. Brubaker, R. Grant, and J. Ruzyllo: Solid-State Electron. **46** (2002) 1671
31) E. Tokumitsu, G. Fujii, and H. Ishiwara: Appl. Phys. Lett. **75** (1999) 575
32) E. Tokumitsu, K. Okamoto, and H. Ishiwara: Jpn. J. Appl. Phys. **40** (2001) 2917
33) Y. S. Kim, Y. H. Lee, and M. Y. Sung: Solid-State Electron. **43** (1999) 1189

Chapter 2

Electrical properties of solution process-derived $(Ba,Sr)Ta_2O_6$ thin films

Various compositional $(Ba,Sr)Ta_2O_6$ (BSTA) thin films were fabricated using the spin-coating method. Electrical properties including dielectric constant (ε), loss tangent (tan δ), capacitance-voltage (*C*–*V*) stability and leakage current property were evaluated by metal-insulator-metal (MIM) capacitors. Among various compositional BSTA thin films, the $SrTa_2O_6$ (STA) thin film, i.e., Ba undoped thin film, showed the highest ε, the lowest tan δ and the lowest leakage current. Thus, the STA was regarded as the best composition for the application of gate dielectric. Then, the annealing temperature dependency of electrical properties was investigated for STA thin films. For these thin films, the 700 ^oC annealed STA thin film showed a high ε, the lowest leakage current and the best *C*–*V* stability. However, the annealing temperature of 700 ^oC was too high for glass substrate application. Therefore, an additional UV/O_3 treatment for the 500 ^oC annealed STA thin film was proposed to improve its electrical properties. Significant improvement of leakage current property was obtained by the UV/O_3 treatment.

2.1 Fabrication and evaluation of BSTA thin film capacitors

2.1.1 Fabrication of BSTA thin films

STA and $BaTa_2O_6$ (BTA) sol-gel solutions were prepared by Mitsubishi Materials Corporation. The molar ratios of Sr/Ta and Ba/Ta were 1:2 and the metal alkoxide concentrations were 7 wt.%. In order to obtain expected compositions of Sr/Ba, the mixed precursors were stirred at room temperature for about 1 h to ensure chemical homogeneity. The prepared precursors were spin-coated onto Pt/TiO_2 (or Ti)/SiO_2/Si (purchased from Panasonic Corporation and Tanaka Kinzoku Kogyo Corporation) substrates at 3000 rpm for 30 s. Here, the Pt layer worked as bottom electrode of MIM capacitor. The TiO_2 (or Ti) layer was used to enhance the adhesion between the Pt electrode and the SiO_2/Si substrate.[1)] Thicknesses of Pt and TiO_2 (or Ti) layers were about 30 and 10 nm, respectively. After spin coating, the deposited thin films were dried at 100 °C for 5 min and pyrolyzed at 450 °C for 4 min on hot plates in air. The coating and heat treatment procedures were performed several times

until the films reached expected thickness. At last, thin films were annealed in a tube furnace to improve electrical properties. The fabrication process of BSTA thin films is shown in Fig. 2-1.

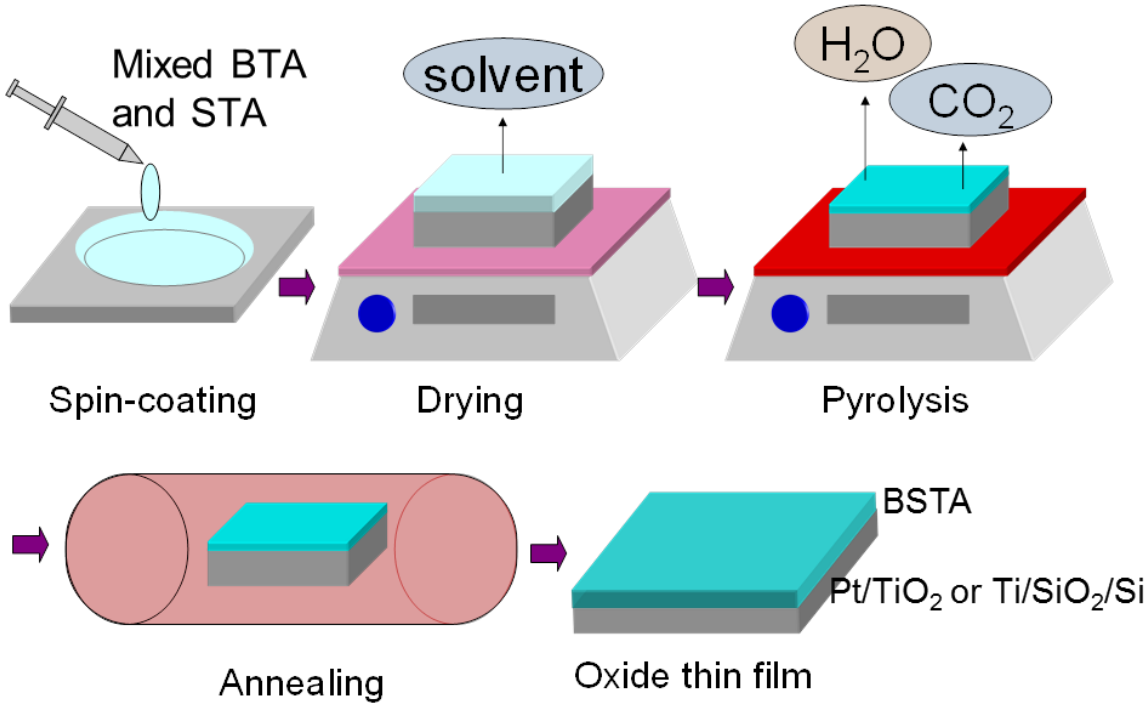


Fig. 2-1 Schematic diagram of fabrication process of BSTA thin films.

2.1.2 Fabrication of MIM capacitor

Since the metal of Pt has very stable chemical property and a higher work function than many other metals, the Pt was used as electrode material for MIM capacitors. Schematic diagram of fabricated MIM capacitor is shown in Fig. 2-2. Pt top electrodes of about 200 nm thick were deposited through a shadow mask by sputtering.

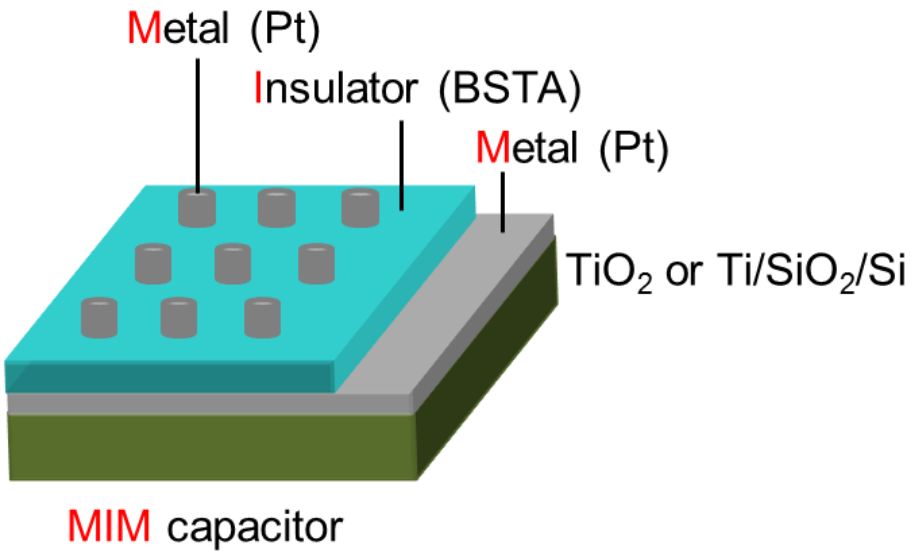


Fig. 2-2 Schematic diagram of fabricated MIM capacitor.

2.1.3 Evaluation of thin films and capacitors

Capacitance–frequency (*C–F*) and *C–V* properties were evaluated using a 50 mV signal by an impedance analyzer (Hewlett-Packard, HP4149A). Under the frequency of 100 kHz, the polarization includes the space charge polarization, which associated with mobile and trapped charges in thin films.[2-3] The space charge polarization mainly derived from various defects in thin films.[2-3] In order to exclude the effect of space charge polarization on the values of ε and tan δ, they were extracted from the *C–F* and *C–V* measurement results at the measurement frequency of 100 kHz. Leakage currents were measured using a programmable electrometer (Keithley, 617). All of the electrical properties were measured at room temperature.

Deposited film thicknesses were determined by scanning electron microscopy (JEOL, JSM-6301F). Crystal structures were evaluated by X-ray diffractometry (XRD: X'pert MRD, PANalytical or Rigaku RINT-TTR Ⅲ/NM) using Cu Kα radiation. The compositions of obtained thin films were evaluated by X-ray fluorescence (MagiX Pro, PANalytical). Refractive indices of thin films were measured by spectroscopic ellipsometry (Horiba Jobin-Yvon, UVISEL ER AGMS-NSD). Surface morphologies were observed with atomic force microscopy (AFM: SPA400, Seiko Instruments). For accuracy several points were measured on each sample. The depthwise distribution of elements was analyzed by secondary

ion-microprobe mass spectrometry (SIMS: Ion-Microprobe Atomika-6500) using Cs or O ion beams. Transmission electron microscopy (TEM: JEOL JEM-3100FEF) was used to investigate the microstructures of thin films.

2.2 Composition effect of BSTA thin films

In addition to $BaTa_2O_6$ (BTA) and $SrTa_2O_6$ (STA) thin films preparation three other composition thin films, i.e., $(Ba_{0.75}Sr_{0.25})Ta_2O_6$ (BSTA75), $(Ba_{0.5}Sr_{0.5})Ta_2O_6$ (BSTA50), and $(Ba_{0.25}Sr_{0.75})Ta_2O_6$ (BSTA25), were also fabricated. After drying and pyrolysis, thin films were annealed at 800 ^oC for 1 h in air and O_2 atmospheres using a tube furnace. Film thicknesses of BTA, BSTA75, BSTA50, BSTA25, and STA were about 130, 130, 130, 130, and 150 nm, respectively. The diameters of the Pt top electrodes were approximately 0.26 mm.

2.2.1 Effects of annealing atmosphere on electrical properties of BTA thin films

Many reports described that an appropriate annealing atmosphere is effective for improving the electrical properties of Ta_2O_5 thin films,[4-6] therefore, the annealing atmosphere was expected to affect the electrical properties of BSTA thin films. In order to understand the effect of annealing atmosphere on electrical properties of BSTA thin films, one simple composition thin film, BTA thin film, was firstly chosen to investigate possible defects and to search for an appropriate annealing atmosphere for BSTA thin films. Heat-treated BTA thin films were annealed in air and O_2 for 1 h at 800 ^oC. In both cases, the films were crystallized and had the same crystal structure. ε and tan δ of air- and O_2-annealed thin films are listed in Table 2-1. BTA thin film annealed in O_2 shows higher ε of about 66 and lower tan δ of about 0.8 %. This value of ε is about twice that of amorphous BTA thin films.[7] Therefore, O_2 atmosphere annealing is more appropriate for the fabrication of BTA.

Table 2-1 ε and tan δ of BTA thin films annealed in air and O_2 atmospheres at 800 ^oC for 1 h and measured at 100 kHz.

	ε	tan δ (%)
Air	42	2.8
O_2	66	0.8

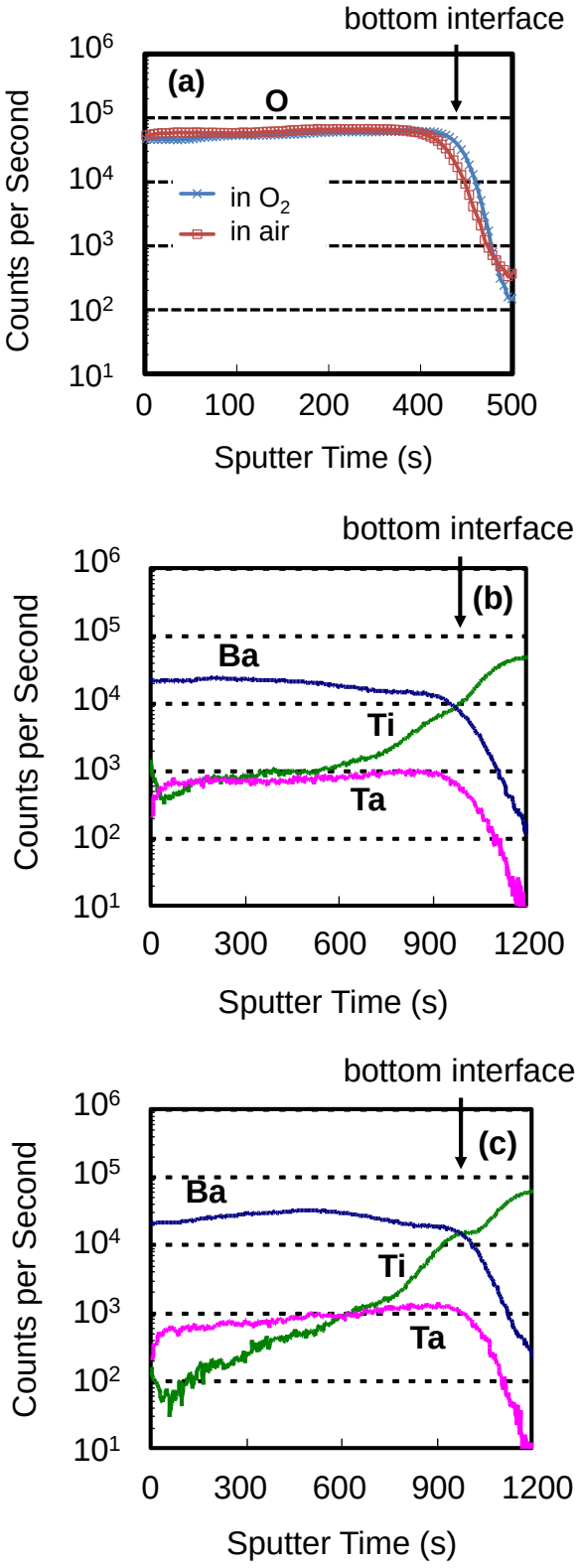


Fig. 2-3 (a) SIMS profiles of O in BTA thin films annealed in air and O_2, measured using a Cs ion beam. SIMS profiles of Ba, Ti and Ta in BTA thin films annealed in (a) air and (b) O_2, measured using an O ion beam.

SIMS investigation was performed to elucidate the change in the depthwise distribution of elements depending on the different annealing treatments. No obvious difference in the concentration of O elements was found between the two thin films, which were investigated using a Cs ion beam (as shown in Fig. 2-3 (a)). SIMS profiles of Ba, Ta, and Ti, which were investigated using an O ion beam are shown in Fig. 2-3(b) and 2-3(c). The concentrations of Ba and Ta elements were almost the same in these two thin films. The detected Ti elements are inferred to have diffused from the underlying Ti substrates into the BTA thin film through the thin Pt layer (30 nm) during the high-temperature annealing. The diffusion of Ti in the two thin films under the two annealing atmosphere conditions was different, as indicated by the Ti curves in Figs. 2-3(a) and 2-3(b). Under both conditions, relatively high amounts of Ti were detected near the bottom interface, however under the O_2 annealing atmosphere condition, lower counts of Ti were detected with nearness to the surface.

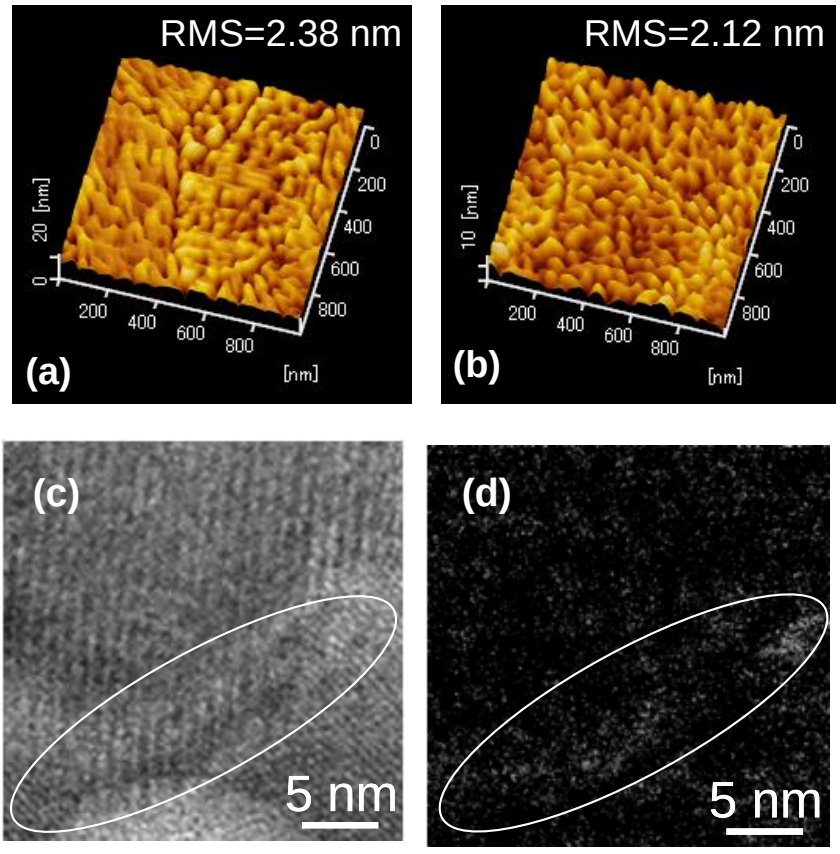


Fig. 2-4 AFM images of BTA thin films annealed in (a) air and (b) O_2 atmospheres. (c) Cross-sectional TEM images and (d) Ti EELS map at the same place in the BTA thin film annealed in the air. The ellipse reveals that larger amounts of Ti were observed in the grain boundary.

Surface morphologies of these two thin films were investigated by AFM, as shown in Figs. 2-4(a) and 2-4(b). The root mean square (RMS) roughness of thin films annealed in air and O_2 were 2.38 and 2.12 nm, respectively. The thin film annealed in O_2 showed better and denser surface morphology. The O_2 annealing was expected to be more effective to exclude the organic impurities in dielectric thin films,[8-9] thus thin films grew better.

TEM and Electron energy-loss spectroscopy (EELS) mapping was carried out on the BTA thin film annealed in air to investigate the diffusion of Ti. Figures 2-4(c) and 2-4(d) show the cross-sectional TEM image and the elemental Ti map at the same place in the thin film. Larger amounts of Ti were detected in the grain boundary, which is marked with an ellipse in Figs. 2-4(c) and 2-4(d). It was concluded that Ti diffused mainly through grain boundaries in BTA thin films. O_2 annealed thin film is denser than air annealed thin film and effective in preventing the diffusion rates of Ti. Since the Ti impurity is the only clear difference between these two thin films, the difference in the dielectric properties was considered to be mainly due to the different diffusion rates of Ti. Less Ti contamination leads to higher ε and lower tan δ in the O_2-annealed thin film. Therefore, BSTA thin films of other compositions were also annealed in O_2 atmosphere.

2.2.2 Effects of composition on electrical properties of BSTA thin films

The crystal structures of BSTA thin films of various compositions were investigated by XRD, as shown in Fig. 2-5. Diffraction peaks were found for all composition thin films, which showed that they all crystallized at the annealing temperature of 800 ^{o}C. The crystalline BSTA thin films have orthorhombic tungsten bronze structures.[10-12] Traditional ε vs. frequency and tan δ vs. frequency (ε and tan δ values were obtained from *C–F* measurements) properties show that both ε and tan δ decreased as frequency increased for all compositions of BSTA thin films. The change rates of ε in the measured frequency range for all thin films are lower than 4 %, as shown in Fig. 2-6(a). This indicates that all films have excellent frequency properties in the low-frequency region.[13]

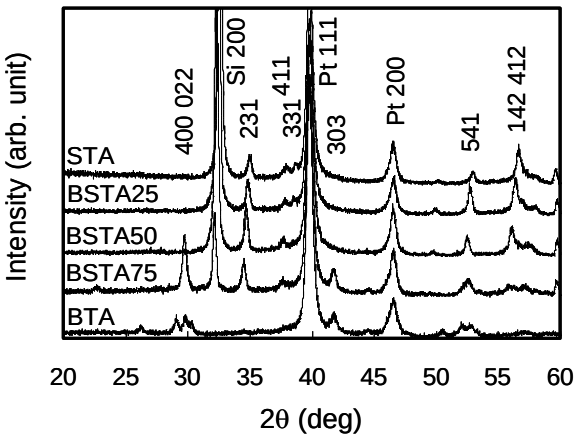


Fig. 2-5 XRD patterns of BSTA thin films measured by the thin film diffraction technique. The angles of incidence were set at 5 °.

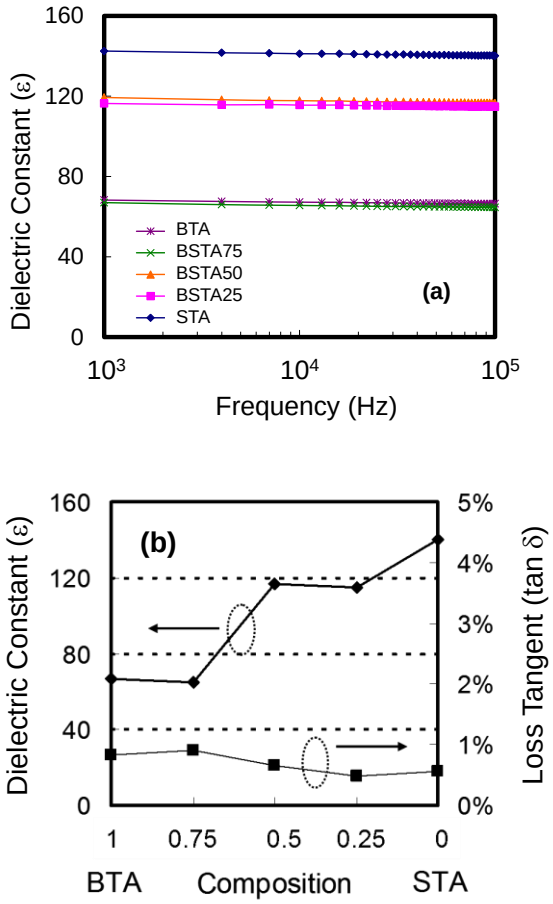


Fig. 2-6(a) ε of BSTA thin films as a function of frequency. (b) ε and tan δ of BSTA thin films as a function of composition.

The values of ε and tan δ of BSTA thin films as a function of composition measured at 100 kHz are shown in Fig. 2-6(b). The values of ε and tan δ of BTA, BSTA75, BSTA50, BSTA25, and STA are 66 and 0.8 %, 65 and 0.9 %, 117 and 0.7 %, 115 and 0.6 %, and 140 and 0.6 %, respectively. The ε values of all thin films are higher than Ta_2O_5,[4-5] and tan δ values of all thin films are lower than 1 %. Meanwhile, ε tends to increase as the component of Sr increases, but no obvious change was found in tan δ.

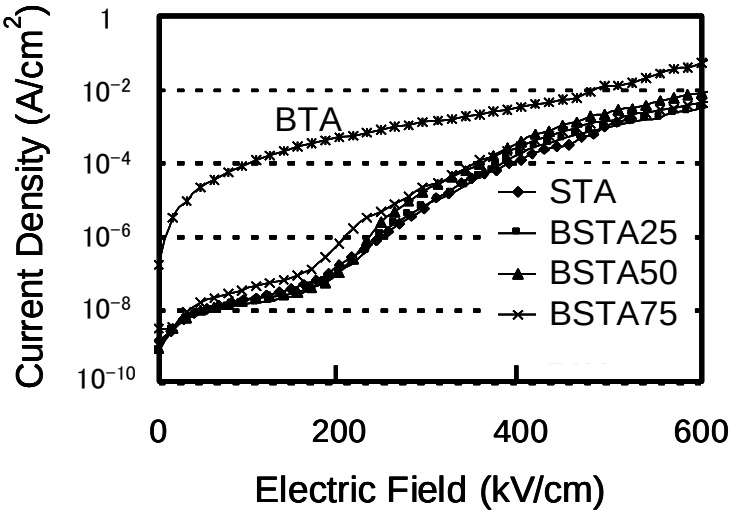


Fig. 2-7 Leakage current properties of BSTA thin films.

Leakage currents as a function of the electric field of BSTA thin films of various compositions are depicted in Fig. 2-7. The hold time of 20 s was selected for eliminating the relaxation process effects. BTA shows the highest leakage current, however, it is considerably improved after the substitution of Sr. Low leakage currents of about 10^{-7} A/cm^2 (at 200 kV/cm) were observed for all thin films except that of BTA. Almost no difference was found among BSTA75, BSTA50, BSTA25, and STA in the higher electric field range. The value of BSTA75 in the low electric field range is just slightly larger than those of BSTA50, BSTA25, and STA. The characteristics of these curves show that the electrical conduction mechanism in BSTA75 is the same as that in BSTA50, BSTA25, and STA, but different from that in BTA.

Because they are a key parameter in determining the leakage current properties of thin films, the surface morphologies of BSTA thin films were investigated by AFM,

as shown in Fig. 2-8. RMS roughness of the surfaces for BTA, BSTA75, BSTA50, BSTA25, and STA are 2.12, 0.70, 0.79, 0.70, and 0.89 nm, respectively. BTA has a large grain size of about 50 nm and the worst surface morphology. BSTA75, BSTA50, BSTA25, and STA have similar grain sizes of about 20 nm and similar surface morphologies. The component of Sr improved the surface morphology. The higher leakage current in BTA may be due to current flowing through these grain boundaries.

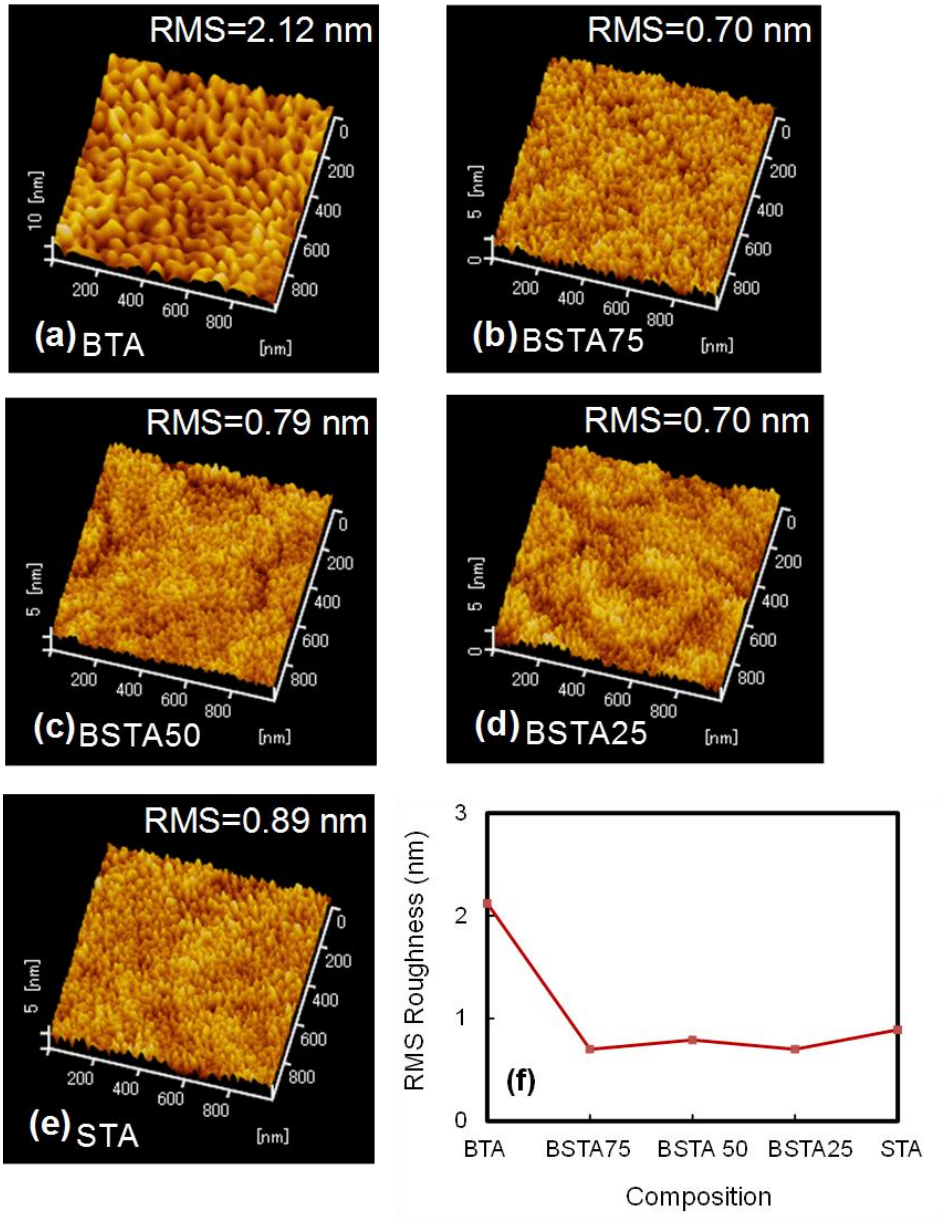


Fig. 2-8 Surface morphologies of (a) BTA, (b) BSTA75, (c) BSTA50, (d) BSTA25, and (e) STA thin films. (f) RMS roughness of various composition BSTA thin films.

Since the STA thin film showed the highest ε, the lowest leakage current, the lowest tan δ and good surface morphology among various composition BSTA thin films, it was regarded as the best choice of gate dielectric for thin film transistors (TFTs). The temperature effect of STA thin films was further investigated.

2.3 Temperature dependency of STA thin films

Deposited STA thin films were annealed in O_2 atmosphere at 500, 600, 700, and 800 °C for 1 h. Film thicknesses were about 150 nm. Diameters of Pt top electrodes were about 0.09 mm.

Figure 2-9 shows XRD patterns of STA thin films annealed at various temperatures. No diffraction peak was found for the thin films annealed at 500, 600 and 700 °C. It indicates that the STA thin films were in amorphous state under 800 °C annealing. The calculated lattice constants are a = 12.43 Å, b = 12.74 Å, and c = 3.87 Å. The crystallization temperature and the crystal structure are the same as those of metal organic chemical vapor deposition (MOCVD) thin films.[10] Diffraction peaks of the bottom Pt electrode and the Si substrate were also observed, which implies that the Si and Pt layers also crystallized and that the Pt layer is oriented with the (111) face. No diffraction peaks were observed from the other components of the overlay structures (i.e., the TiO_2 and SiO_2 layers).

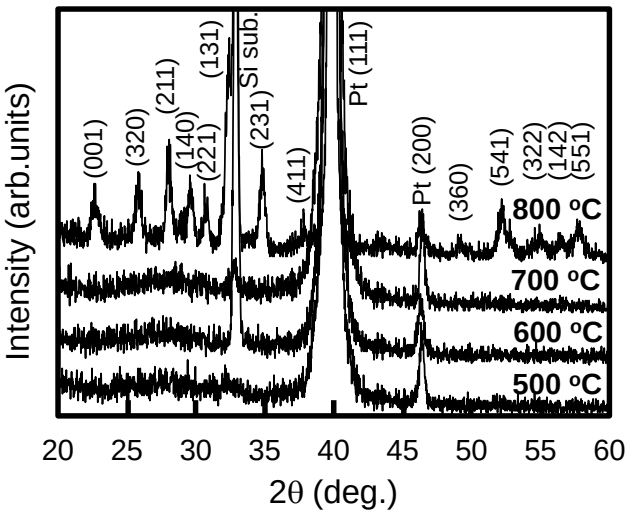


Fig. 2-9 XRD patterns of STA thin films annealed at various temperatures. STA thin films were in amorphous states at annealing temperatures of lower than 700 °C.

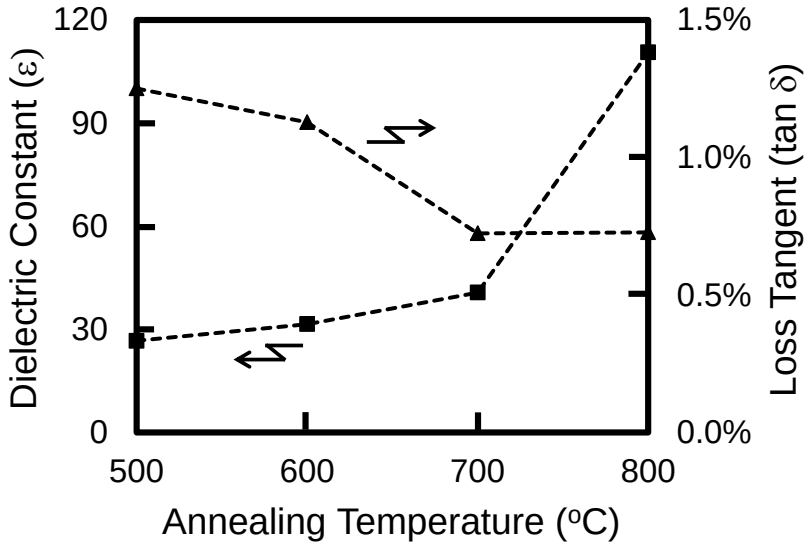


Fig. 2-10 The values of ε and tan δ of STA thin films annealed at various temperatures. ε increases with increasing annealing temperature while tan δ decreases with decreasing annealing temperature.

Figure 2-10 shows the values of ε and tan δ measured at 100 kHz of the STA thin films that had been annealed at various temperatures. The crystalline STA thin film that had been annealed at 800 °C (STA-800) exhibited a high ε of about 110, which is comparable to those of MOCVD and atomic layer deposition derived thin films.[10, 14] ε decreased significantly to 41, 31, and 26 for amorphous STA thin films that had been annealed at 700 °C (STA-700), 600 °C (STA-600), and 500 °C (STA-500), respectively. Of these three amorphous thin films, STA-700 had the highest ε of 41; although this is approximately 40 % that of the crystalline STA thin film, it is still higher than that of many other high-k materials[15-17]. In contrast, tan δ tended to decrease with increasing annealing temperature. STA-700 and STA-800 had the lowest tan δ of 0.7 %. STA-500 and STA-600 had a slightly higher tan δ of about 1 %, but this is still very low. These values are comparable to those of MOCVD STA thin films,[10] which suggests that soution process-derived STA thin films were well fabricated.

C–V measurements were conducted to determine the stability of the STA thin films under an applied electric field. Figure 2-11(a) shows the change in the

capacitance measured at 100 kHz of each thin film relative to that at 0 kV/cm [$C(0)$] as a function of the electric field strength; in other words, $\Delta C = C(E)–C(0)$ as a function of E, where $C(E)$ is the capacitance at an electric field strength of E. For the crystalline STA thin film (STA-800), the capacitance decreased with increasing electric field strength, as indicated by the negative curvature of the $\Delta C/C(0)$ curve. In contrast, the capacitances of the three amorphous thin films (STA-700, STA-600, and STA-500) increased with increasing electric field strength, as indicated by the positive curvatures of their $\Delta C/C(0)$ curves. The capacitance of STA-800 changes much more with electric field strength than those of STA-700, STA-600, and STA-500. No obvious difference was found in the capacitance changes of STA-700, STA-600, and STA-500, as shown in Fig. 2-11(b). These results imply that the capacitances of the amorphous STA thin films were more stable as a function of the applied voltage than that of the crystalline STA thin film and that the capacitances of crystalline and amorphous STA thin films change by different mechanisms.

The voltage capacitance coefficient was used to evaluate the stability of the capacitance as a function of voltage. It is given by[15-16, 18-20)]

$$\Delta C/C_0 = \alpha V^2 + \beta V, \qquad (2\text{-}1)$$

where α and β are respectively the quadratic and linear voltage capacitance coefficients. In practice, β can be more easily compensated by the circuit design than α since α is more indicative of the intrinsic properties of the material.[15-16)]

Since STA-700 exhibits the same $C–V$ characteristics as STA-500 and STA-600, the calculated values of α for STA-800 and STA-700 were compared. The value of α for STA-800 was calculated to be about –1027 ppm/V^2; it exhibits no dependence on the frequency, as shown in Fig. 2-12(a). In contrast, α were 36, 27, 19, and 15 ppm/V^2 at 10, 100, 500 kHz, and 1 MHz for STA-700, respectively. The variation decreased with increasing frequency in STA-700, as shown in Fig. 2-12(b). For most high-k materials, α lies in the range 100–1000 ppm/V^2. In a few years, applications will require α < 100 ppm/V^2 according to the International Technology Roadmap for Semiconductors.[16)] The STA-700 thin film has a much lower α than most other high-k materials and it is sufficiently low to satisfy the requirement set by the International Technology Roadmap for Semiconductors.[16)]

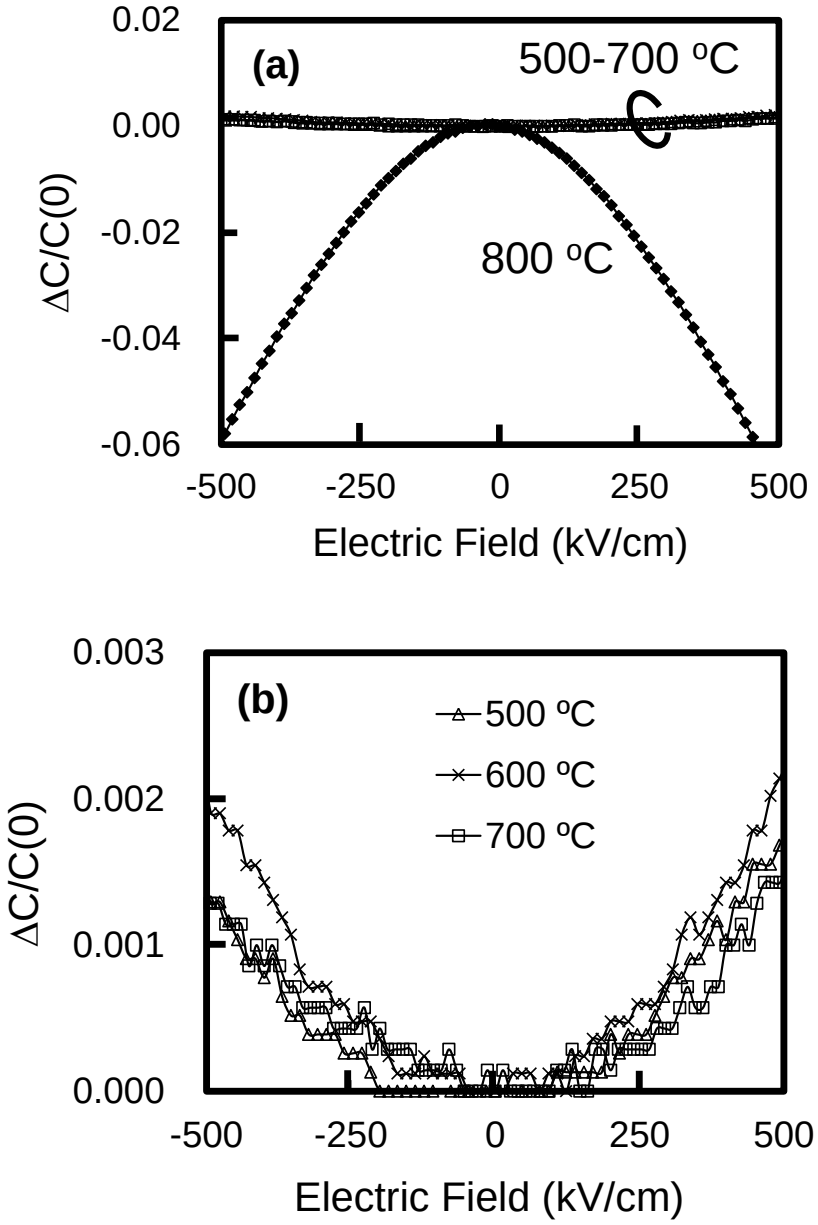


Fig. 2-11 (a) The change in capacitance relative to the capacitance at 0 kV/cm for each STA thin film, which was calculated from $[C(E)–C(0)]/C(0)$ for STA thin films annealed at various temperatures. The crystalline STA thin film annealed at 800 °C shows a negative curvature, whereas amorphous STA thin films annealed at 500, 600, and 700 °C show positive curvatures. (b) An enlarged figure of $[C(E)–C(0)]/C(0)$ for STA 500–700 thin films. No obvious changes were observed between these thin films.

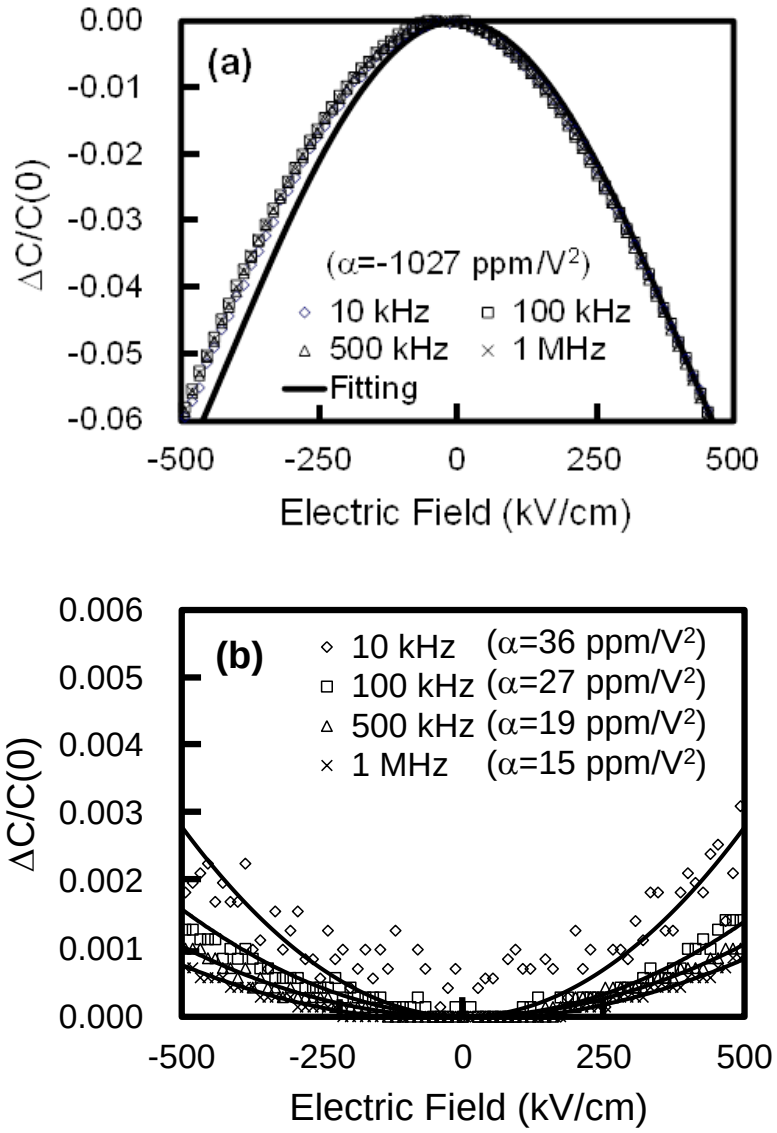


Fig. 2-12 The change in the capacitances of (a) STA-800 and (b) STA-700 thin films relative to their capacitances at 0 kV/cm (i.e., [$C(E)$–$C(0)$]) as a function of frequency. The α was calculated using eq. (2-1). No frequency dependence was observed for STA-800, whereas α decreased with increasing frequency for STA-700.

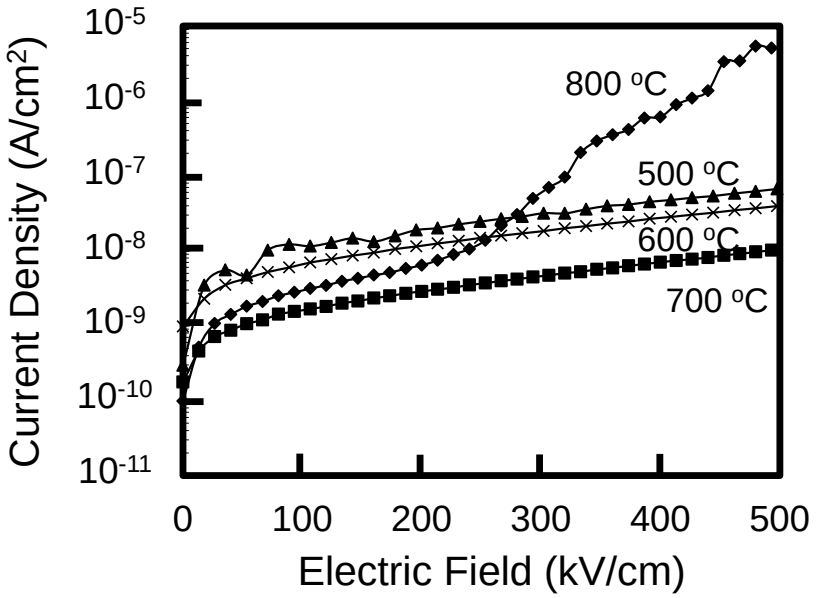


Fig. 2-13 Leakage currents of STA thin films annealed at various temperatures. Amorphous thin films annealed at temperatures lower than 800 °C show similar characteristics as each other. The STA thin film annealed at 700 °C has the lowest leakage current of the amorphous thin films.

Figure 2-13 shows the leakage current as a function of the electric field strength for STA thin films that had been annealed at various temperatures. The leakage current of STA-800 increased slowly with increasing electric field strength at electric fields lower than about 210 kV/cm, but it increased rapidly at higher electric fields. This indicates that two mechanisms mainly determine the leakage current of STA-800. STA-500 and STA-600 had higher leakage currents than STA-800 at electric fields lower than about 250 kV/cm. However, they increased slowly with increasing electric field, so that STA-500 and STA-600 had lower leakage currents than STA-800 at higher electric fields. STA-700 had the lowest leakage current over the whole measurement range and a low value of about 10^{-8} A/cm^2 at 500 kV/cm. This leakage value is comparable to that of a MOCVD STA thin film.[10)] The three amorphous STA thin films exhibited similar leakage current characteristics and the leakage current decreased with increasing annealing temperature. STA-800 had similar leakage current characteristics as those of the three amorphous STA thin films at low electric fields. This suggests that the same mechanism may dominate at low electric fields in all four STA thin films, but that different mechanisms dominate at high electric fields

in crystalline and amorphous STA thin films. Table 2-2 lists the obtained parameters for the fabricated STA thin films.

Table 2-2 Obtained parameters of STA thin films annealed at various temperatures.

Annealing temperature (^{o}C)	Microstructure	Dielectric constant ε	Loss tangent $\tan\delta$ (%)	Quadratic voltage capacitance coefficient α (@100 kHz) (ppm/V^2)	Leakage current density (@500 kV/cm) (A/cm^2)
800	crystalline	110	0.7	-1027	5.4×10^{-6}
700	amorphous	41	0.7	27	1.0×10^{-8}
600	amorphous	31	1.1	51	4.0×10^{-8}
500	amorphous	26	1.2	40	6.7×10^{-8}

Leakage current in a dielectric thin film can be owing to several conduction mechanisms including Schottky emission (SE), Poole-Frenkel (PF) emission, Fowler-Nordheim tunneling, and a space charge limited current.[17, 20-22] The current density due to SE can be expressed as follows

$$J \propto T^2 \exp\left[\frac{q\left(-\Phi_B+\sqrt{\frac{qE}{4\pi\varepsilon}}\right)}{kT}\right] \quad (2\text{-}2)$$

In addition, the current density due to PF emission can be written as

$$J \propto E \exp\left[\frac{q\left(-\Phi_B+\sqrt{\frac{qE}{\pi\varepsilon}}\right)}{kT}\right] \quad (2\text{-}3)$$

Space charge limited current (SCLC) is generally expressed by

$$J = \frac{9\varepsilon\mu V^2}{8d^3} \quad (2\text{-}4)$$

The tunneling is the most-common conduction mechanism through dielectrics under high fields. It is expressed by

$$J \propto E^2 \exp[-\frac{4\sqrt{2m}\,(q\,\Phi_B)^{3/2})}{3qhE}] \quad (2\text{-}5)$$

where J denotes current density, T represents absolute temperature, k is Boltzmann constant, q denotes electronic charge, E represents electric field strength, Φ_B is barrier height, m denotes effective mass, μ is the carrier mobility in the absence of traps and h is the plank constant.

The SE is a process where thermionic emission over the metal-insulator barrier is responsible for carrier transport. The plot of $\ln(J/T^2)$ versus $1/T$ yields a straight line with a slope determined by the barrier height. The PF emission is due to emission of trapped electrons into the conduction band. The supply of electrons from the traps is also through thermal excitation. It is generally occurs at a higher electric field. The SCLC results from carrier injected into the dielectric, where no compensating charge is present. For a given dielectric, each conduction process may dominate in certain temperature and voltage range, i.e., several kinds of conduction process may be occur in one dielectric at different temperatures and voltages.[22)]

To clarify the mechanism that determines the leakage currents of the crystalline and amorphous STA thin films, Figs. 2-14(a) and (b) respectively show plots of the SE [i.e., $\log(J/T^2)$–$E^{1/2}$] and PF emission [i.e., $\log(J/E)$–$E^{1/2}$]. Since the amorphous STA thin films exhibit similar characteristics to each other, STA-800 and STA-700 were compared. Fitting with straight lines resulted in almost the same slopes for STA-800 at low electric fields and STA-700 over the whole range of measured electric fields in the SE plot (Fig. 2-14(a)). The refractive indices (n) calculated from these slopes are about 2.4, which agrees well with that (1.8–2.2) measured by ellipsometry. This indicates that SE mechanisms are dominant at low electric fields (<210 kV/cm) for both the crystalline and amorphous STA thin films over the whole range of measured electric fields. The PF emission plot (Fig. 2-14(b)) was used to analyze the leakage current of STA-800 at high electric fields (>210 kV/cm). A good linear fit was obtained with n = 1.5, which also agrees well with the measured value. The PF emission mechanism is thus considered to dominate in STA-800 at high electric fields.

Equation (2-1) is a phenomenological expression that is generally used to describe the capacitance as a function of voltage, but the origin of the capacitance change has been unclear until now.[15-16, 18-19, 21)] Blonkowski *et al.* proposed a model in which a negative α was explained as being due to dipolar relaxation.[21)] In their study, the dielectric properties of Ta_2O_5 thin films showed no frequency dependence and PF emission was dominant. STA-800 showed an SE mechanism at low electric fields and a PF emission mechanism at high electric fields. Therefore, the variation in

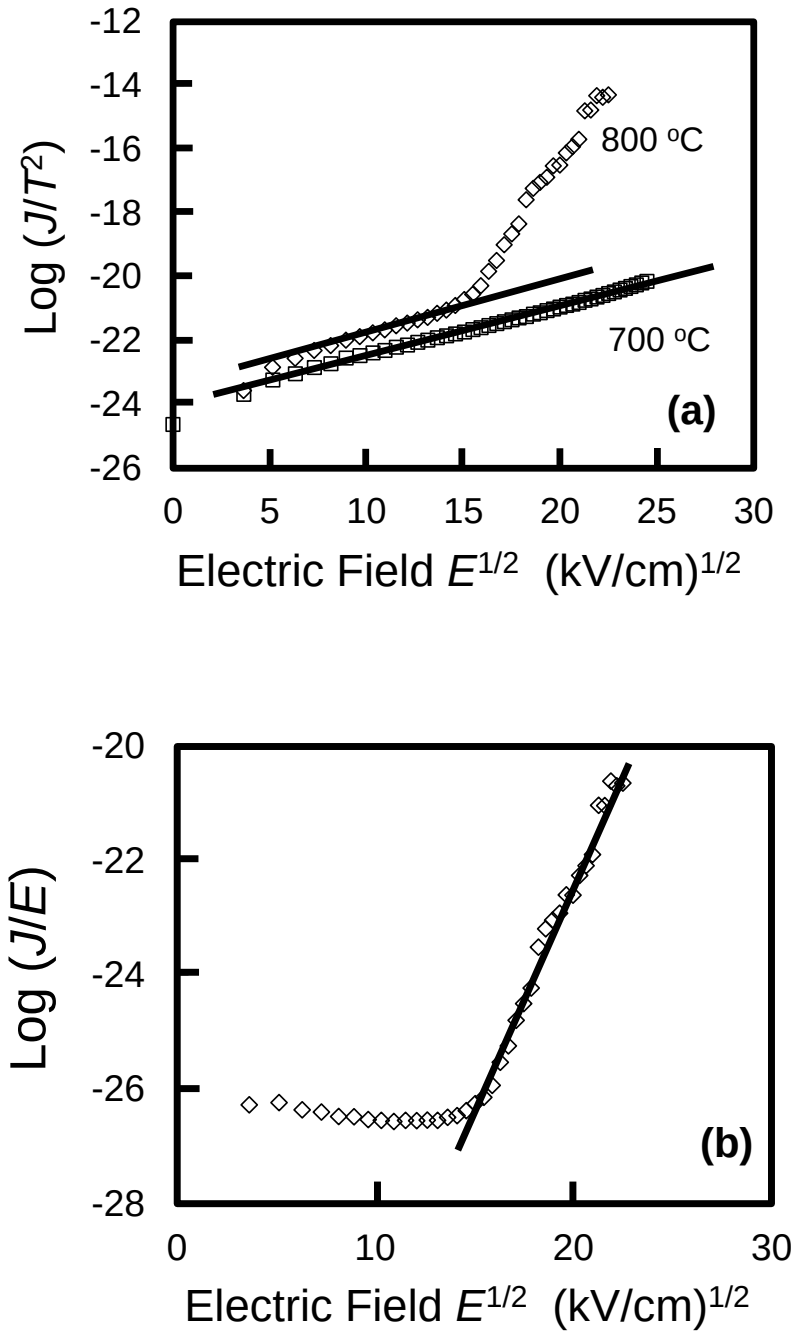


Fig. 2-14 (a) SE plot of STA thin films annealed at 700 °C (STA-700) and 800 °C (STA-800) and (b) PF emission plot of the STA-800 thin film. SE mechanism dominates in STA-700 over the whole range of measured electric fields and in STA-800 at low electrical fields. The PF mechanism dominates at high electrical fields in the STA-800 thin film.

the capacitance of the STA-800 thin film may also be due to dipolar relaxation. To investigate the dependence of the dielectric properties on dipolar relaxation, the variation of $\Delta C/C(0)$ of STA-800 was calculated using[18, 21)]

$$\frac{\Delta C}{C(0)} = \frac{2n_2 nE^2 + n_2^2 E^4}{\varepsilon} \quad (2\text{-}6)$$

where ε is the measured dielectric constant, n is the measured linear refractive index, and n_2 is the second-order nonlinear refractive index. The calculated value of $\Delta C/C(0)$ agrees very well with the measured value, as shown in Fig. 2-12(a). The calcuated n_2 is about -2.4×10^{-16} m^2/V^2. It is higher than that of Ta_2O_5 thin films,[14)] which is reasonable since the STA thin films have a much higher ε than the Ta_2O_5 thin films. Thus, it was concluded that dipolar relaxation caused the capacitance variation of STA-800.

On the other hand, Gonon *et al.* suggested that in many high-k materials the change in the capacitance with positive α is related to the electrode polarization in which mobile (hopping) carriers form an accumulation layer at the electrodes resulting in a voltage-dependent double-layer capacitance. This change in the capacitance can be expressed by[15, 19)]

$$\frac{\Delta C}{C} \propto Af^{-2m}\sigma^{2m} \quad (0 < m < 1), \quad (2\text{-}7)$$

where A is a parameter related to the contact conditions, f is the frequency, σ is the conductivity, and m is a parameter related to the Jonscher response. For ohmic contact, $A \approx 0$, so that C is almost constant,[19)] whereas for blocking contact, $\Delta C/C$ should decrease with increasing frequency and increase with increasing leakage current. Since the SE mechanism dominates in STA-700 (i.e., there is blocking contact), the variation in the capacitance and the leakage current of STA-700 agree with eq. (2-7). Electrode polarization induced by oxygen vacancies or other defects is expected to explain the variation in the capacitance as a function of voltage in STA-700 and other amorphous STA thin films.

Although the amorphous STA thin films had much lower ε than the crystalline STA thin film, the variation of capacitance with voltage demonstrated decreased. Of the amorphous thin films, STA-700 exhibited the best electrical properties including the highest dielectric constant of 41, the lowest leakage current of 10^{-8} A/cm^2 (500 kV/cm) and a very good capacitance stability with changing voltage with α = 27

ppm/V^2. The value of 41 was much higher than many other studied high-k materials. Therefore, the best annealing temperature was regarded as 700 ^oC. However, the temperature of 700 ^oC limits the application on transparent and flexible displays which the TFTs should be fabricated on glass and flexible substrates. Therefore, low-temperature processes for fabricating electronic devices urgently need to be developed. A method involving ultraviolet (UV)-assisted annealing in an ozone atmosphere (UV/O_3 treatment) has been reported for several materials, including SiO_2, Ta_2O_5, ZrO_2, and TiO_2.[23-25] UV/O_3 treatment was found to be effective for realizing lower fabrication temperatures and for producing sol-gel-derived thin films with low leakage currents.[23-27] However, no studies have been investigated for improving the electrical properties of STA thin films fabricated at low temperatures. Ishikawa *et al.* reported that Si diffusion could be enhanced by UV irradiation at low temperatures.[28] The effect of impurities on the STA is not clear. Therefore, UV/O_3 treatment was carried on STA thin films in order to improve leakage current properties. The effect of generated impurities was also studied.

2.4 Low temperature fabrication using UV/O_3 treatment

STA Thin films were firstly annealed at 500 °C in O_2 for 1 h in a tube furnace and then subjected to UV/O_3 treatment (UV & Ozone Dry Stripper, Samco Inc.) with heating temperatures of room temperature (RT), 70, 170, and 290 °C. These thin films will be abbreviated as STA-RTUVO_3, STA-70UVO_3, STA-170UVO_3, and STA-290UVO_3, respectively, according to the variation of heating temperature under UV/O_3 treatment. Since the highest heating temperature of this equipment is 290 ^oC, no higher temperatures were carried out. The UV irradiation was performed using wavelengths of 185 and 254 nm. The UV/O_3 treatment time was 1 h. The thin film that had not been subjected to UV/O_3 treatment will be abbreviated as STA-NOUVO_3. The UV/O_3 treatment process is shown in Fig. 2-15. Wavelengths of irradiated UV lights were 185 and 254 nm.

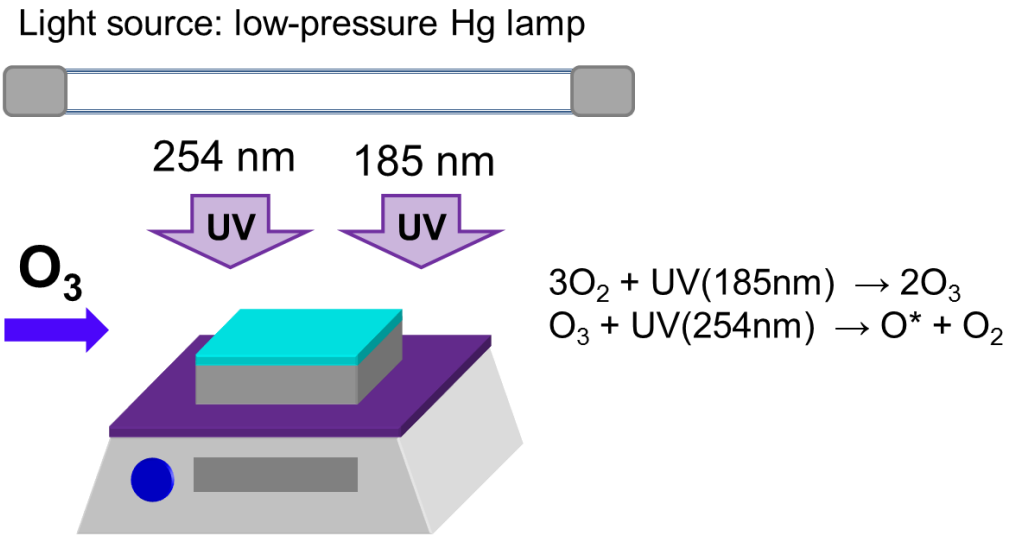


Fig. 2-15 Schematic diagram of UV/O_3 treatment.

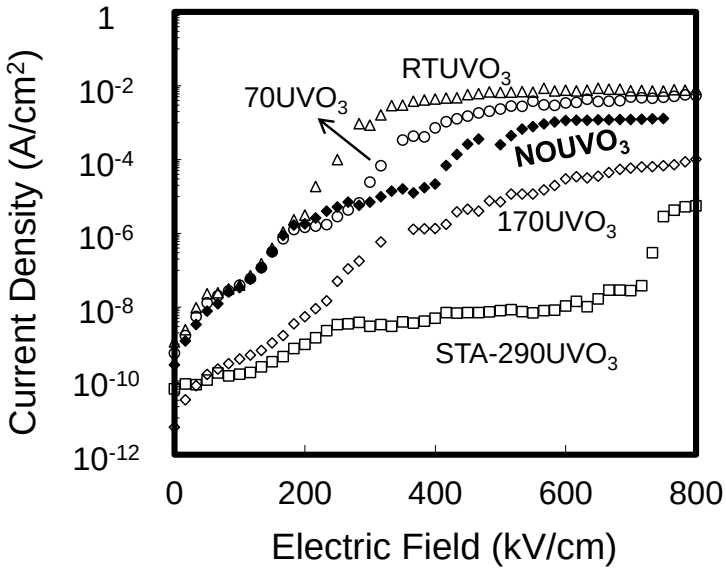


Fig. 2-16 Leakage currents of STA thin films that had been UV/O_3 treated at various temperatures and without UV/O_3 treatment.

Figure 2-16 shows the leakage currents of an untreated STA thin film and STA thin films that had been treated by UV/O_3 at various temperatures. The STA-RTUVO_3 and STA-70UVO_3 had higher leakage currents than that of the STA-NOUVO_3. However, the leakage current decreased with increasing the treatment temperature. For the STA-170UVO_3, the leakage current was about two orders of magnitude lower than that of the STA-NOUVO_3. In particular, for the STA-290UVO_3, a very low leakage current value of about 10^{-9} A/cm^2 at 500 kV/cm was obtained, which is six orders of magnitude lower than that of the untreated STA thin film. This value is lower than that of plasma enhanced ALD-derived STA thin films that were annealed at 500 °C.[14] Therefore, UV/O_3 treatment at an appropriate temperature is considered to be a very effective way to improve the leakage currents of solution process-derived STA thin films. The leakage currents of capacitors with STA thin films which were treated by UV only (which will be abbreviated as STA-290UV) and O_3 only (which will be abbreviated as STA-290O_3) were also investigated. The leakage currents of STA-290UV and STA-290O_3 were about 1.3×10^{-4} and 1.9×10^{-4} A/cm^2 at 500 kV/cm, respectively. They were almost the same to that of the STA-NOUVO_3, i.e., 2.5×10^{-4} A/cm^2 at 500 kV/cm. No obvious improvements of leakage currents were found for UV only and O_3 only treatment.

No diffraction peaks were observed in the XRD patterns of any of the STA thin films, irrespective of whether they had been subjected to UV/O_3 treatment or not (Fig. 2-17). These XRD patterns suggested that all thin films were in amorphous states. Almost no changes in the surface state and the RMS roughness were observed, except that the RMS roughness of the STA-290UVO_3 was slightly higher (0.1 nm) than that of the STA-RTUVO_3. Since the crystalline states and surface morphologies of the UV/O_3 treated STA thin films were almost unaltered, their different leakage currents are considered to be independent on the crystalline states and surface morphology.

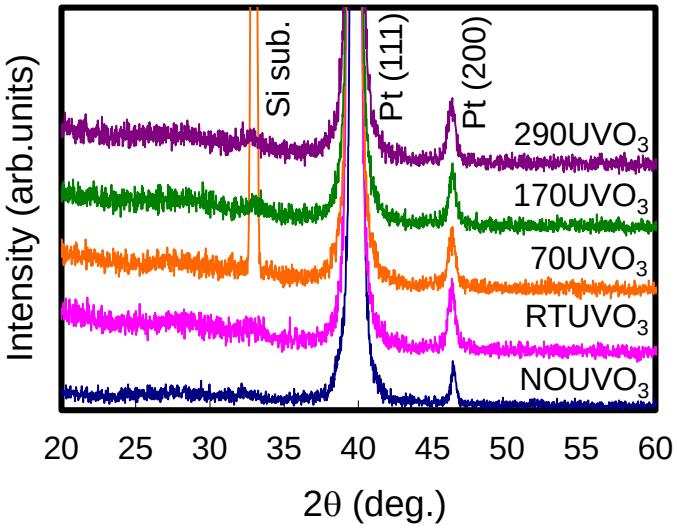


Fig. 2-17 XRD patterns of STA thin films that had been UV/O_3 treated at various temperatures and without UV/O_3 treatment.

Figs. 2-18(a)–(e) show depth profiles of carbon (C), oxygen (O), hydrogen (H), Si and Ti of STA-NOUV/O_3, STA-RTUVO_3, STA-70UVO_3, STA-170UVO_3, and STA-290UVO_3, respectively. Impurities of C and H mainly originated from the organic precursor. Different C, H, and O distributions were observed in the untreated and UV/O_3 treated STA thin films. In the STA-NOUV/O_3, C, H, and O were uniformly distributed throughout the whole film. However, the concentrations of these three elements constantly decreased from the STA/Pt interface to the STA surface. In contrast, no obvious variations in the concentrations of these three elements were found in the UV/O_3 treated STA thin films. During UV irradiation, O radicals (O*) were generated according to the equation $O_3 + h\nu$ (254 nm) $\rightarrow$ O* + O_2.[27, 29] The chemically active O* radicals diffused into the STA thin films and bonded with C, generating CO_2, which escaped from the STA thin film. Therefore, reduced concentration of C was observed close to the STA thin film surface. Excess O* diffused deep into the STA thin film, giving rise to the higher oxygen intensities observed at the bottom STA/Pt interface.[27, 29] The higher H concentration may be due to absorption of H_2O from the air, which subsequently diffused throughout the STA thin film.

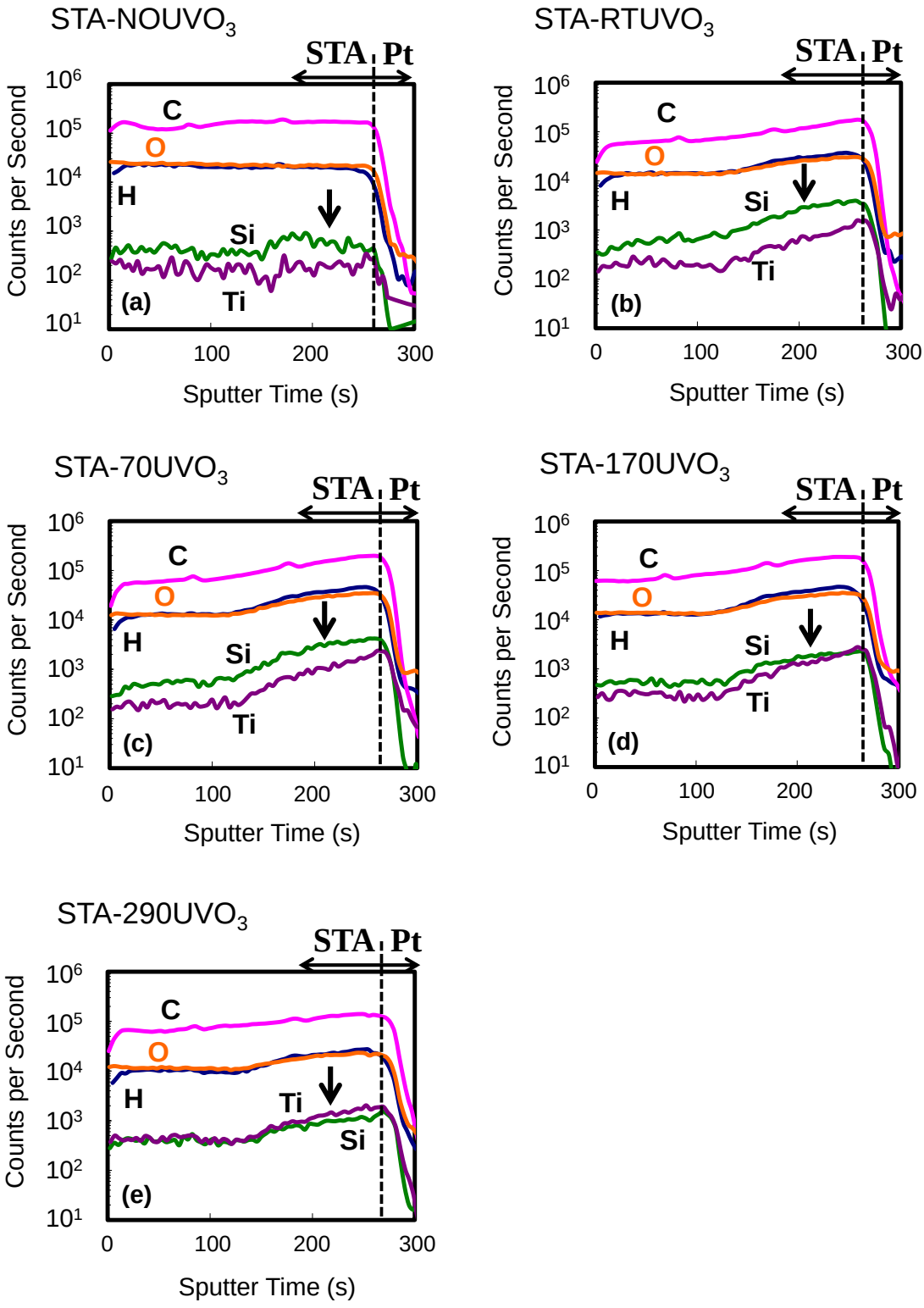
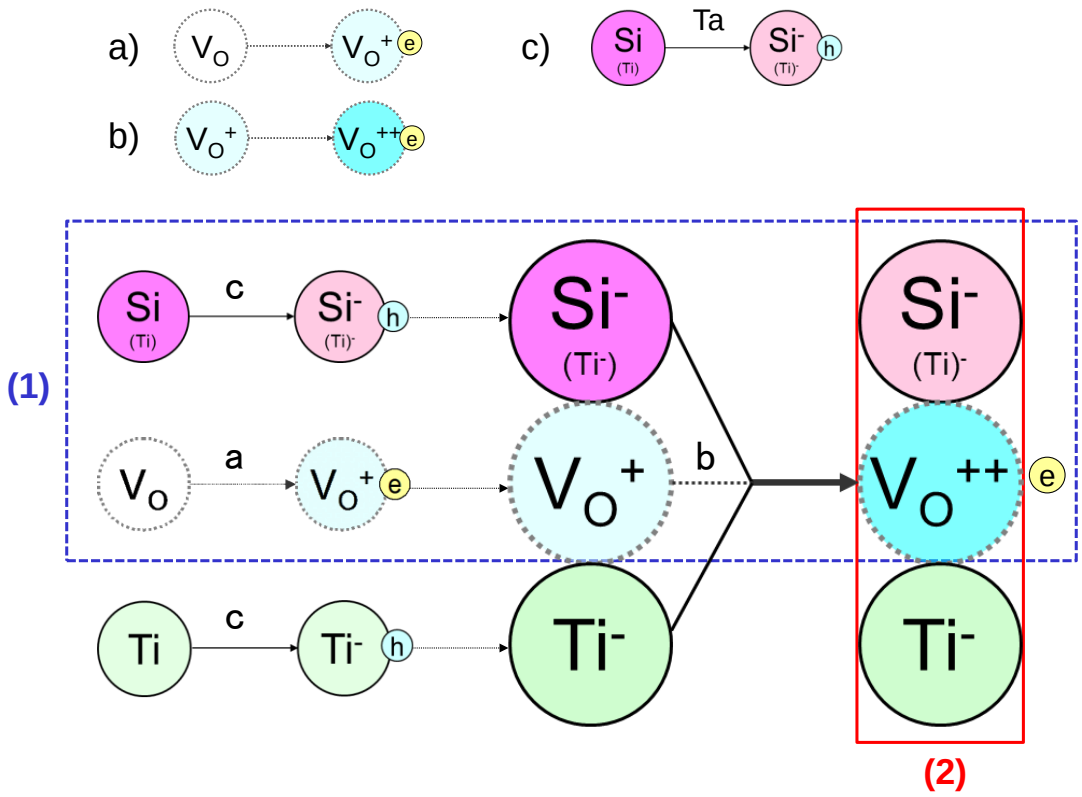


Fig. 2-18 Depth profiles of various elements in (a) STA-NOUVO$_3$, (b) STA-RTUVO$_3$, (c) STA-70UVO$_3$, (d) STA-170UVO$_3$, and (e) STA-290UVO$_3$.

On the other hand, Ti ions were found to diffuse from TiO_2 into Ta_2O_5 thin films under rapid thermal annealing.[30] In light of the above-mentioned enhanced Si diffusion under UV irradiation in ref. 28, impurities of Si and Ti in the STA thin films were measured because the substrate had SiO_2 and TiO_2 layers below the Pt bottom electrode. Furthermore, the energies of UV lights of 185 nm (6.70 eV) and 254 nm (4.88 eV) are enough to dissociate the bonding of Si-O (4.61 eV) in SiO_2 and Ti-O in TiO_2 (6.30 eV), thus generate free ions of Si^{4+} and Ti^{4+}. Relative to the STA-NOUV/O_3, the STA thin films that had been UV/O_3 treated clearly had higher Si and Ti ion concentrations close to the bottom STA/Pt interface. The concentration of diffused Ti ions increased and the concentration of diffused Si ions decreased with increasing treatment temperature. The diffusion of Ti ions appears to suppress the diffusion of Si ions. Ti ions diffused throughout the STA-290UV/O_3. The small increase in the surface roughness of the STA-290UV/O_3 may be due to Ti ions diffusing deep into the film.

Although the C concentration in the STA thin film was decreased by UV/O_3 treatment at RT, the leakage current increased. The C and H concentrations remained almost constant in the UV/O_3 treated STA thin films with increasing treatment temperature, whereas the leakage current decreased with increasing treatment temperature. It was considered that diffused impurities of Si and Ti ions mainly affected the leakage current. Since these STA thin films were in amorphous state, the Si and Ti were not mainly diffused through grain boundaries. Oxide thin films usually contain oxygen vacancies (V_o). These V_o generate V_o^+ and V_o^{++}, and produce one or two free electrons (process (a) and (b) in Fig. 2-19).[31-32] These oxygen vacancies increase leakage currents in oxide thin films.[31-32] Si^{4+} and Ti^{4+} which were originated from the substrates diffused into Ta^{5+} sites where they generated Si^- and Ti^-, and produced one hole (process (c) in Fig. 2-19).[31-32] The generated Si^- and Ti^- could combine with V_o^+ to produce active donors of $(Si^- – V_o^+)^+$ and $(Ti^- – V_o^+)^+$ (process (1) in Fig. 2-19), which are shallower than V_o^+.[31-32] The model of the substitution of Sr^{2+} by Ti^{4+} and Si^{4+} was also considered. Since Sr^{2+}, Ta^{5+}, Ti^{4+}, and Si^{4+} respectively have radii of 0.127, 0.073, 0.068, and 0.039 nm, it was considered that Ti^{4+} and Si^{4+} prefer to enter Ta^{5+} sites than to enter Sr^{2+} sites. Meanwhile, Ti^{4+} was also thought to enter Ta^{5+} sites much more readily than Si^{4+}. At lower treatment temperatures (i.e., in STA-RTUV/O_3 and STA-30UV/O_3), too few Si^- and Ti^- were generated, they could not completely neutralize the active donors of $(Si^- – V_o^+)^+$ and $(Ti^- – V_o^+)^+$, meanwhile, additively generated electrons moved in the thin films, thus the leakage currents increased. However, at higher temperatures (i.e., in STA-170UV/O_3 and STA-290UV/O_3), the Ti concentration increased and sufficiently many Ti^- ions combined with $(Si^- – V_o^+)^+$ and $(Ti^- – V_o^+)^+$ to generate $(Si^- – V_o^+)^+ – Ti^-$



(1) generation of active combination of (Si^{-} (or Ti^{-})–V_o^{+})$^{+}$:

$(a + c) \rightarrow b$

(2) generation of inactive combination of (Si^{-} (or Ti^{-})–V_o^{+})$^{+}$–Ti^{-}:

$(a + 2c) \rightarrow b$

Fig. 2-19 Model of the UV/O_3 treatment effect on the variation of leakage current.

and (Ti^{-}–V_o^{+})$^{+}$–Ti^{-} inactive combinations, meanwhile, additively generated electrons and holes neutralized, thus, giving rise to lower leakage currents (process (2) in Fig. 2-19).[32] In particular, in the STA-290UV/O_3 thin film, many Ti^{4+} diffused throughout the whole STA thin film and neutralized active donors that contained oxygen vacancies. Thus, the leakage current of this film was significantly lower than that of the STA-NOUV/O_3 thin film. On the other hand, at higher treatment temperatures, more Ti^{4+} diffused into the STA thin film and occupied the Ta^{5+} sites, suppressing the diffusion of Si ions so that lower diffusion of Si ions was observed.

No obvious improvement in the STA-290UV and STA-290O_3 was considered to be mainly due to the effect of the C impurities. The C was hard to be excluded in the STA-290UV. Meanwhile, the diffusion of Si^{4+} and Ti^{4+} could not occur without UV irradiation in the STA-290O_3. Therefore, no obvious improvement was obtained in the STA-290O_3. These results suggested that an appropriate concentration of Ti impurities is effective to improve the leakage current properties of STA thin films; this is consistent with many studies that found that Ti is suitable for insulating Ta_2O_5 thin films.[31-35] However, in Ref. 32, high-temperature annealing at 1000 °C was used to realize Ti diffusion, making it unsuitable for low-temperature fabrication. In the present study, Ti diffusion occurred at a low temperature of 290 °C with UV/O_3 treatment and the leakage current was significantly improved.

2.5 Conclusion

BSTA thin films were fabricated by a solution process. The effects of annealing atmosphere and composition on the electrical properties of crystalline BSTA thin films were investigated for the first time. O_2-atmosphere annealing improved the surface morphology and prevented large amounts of Ti diffusion into the BTA thin film, and subsequently improved the dielectric properties. Among five compositions of BSTA thin films, the STA thin film shows the highest ε of about 140, the lowest tan δ of about 0.6 %, and the lowest leakage current of about 10^{-7} A/cm^2, and was regarded as the most promising for application in TFTs.

Although amorphous STA thin film showed much lower ε than the crystalline STA thin film, the capacitance variation with voltage significantly decreased. Of the amorphous thin films, the STA-700 exhibited the best electrical properties including the highest dielectric constant of 41 and the lowest leakage current of 10^{-8} A/cm^2 (500 kV/cm). These electrical properties are comparable to those of MOCVD derived STA thin films. The amorphous STA thin films showed similar *C–V* and leakage-current characteristics with each other, but these characteristics differed from those of the crystalline STA thin film. The SE mechanism dominated in the amorphous STA thin films over the whole range of measured electric fields and in the crystalline STA thin film at electric fields lower than about 210 kV/cm. The PF emission mechanism dominated in the crystalline STA thin film at electric fields higher than about 210 kV/cm. In the crystalline STA thin film, the negative α that was independent of frequency and the PF leakage current mechanism imply that dipolar relaxation causes the change in the capacitance under with a change in voltage. On the other hand, the amorphous STA thin films had a positive α that decreases with increasing frequency and an SE leakage current mechanism, which suggests that

electrode polarization dominates in them.

In order to decrease the leakage current of STA thin film which was annealed at a lower temperature of 500 ^{o}C, an assisted UV/O_3 treatment was carried out. Different concentrations of Si and Ti impurities diffused into STA thin films when they were assisted by UV/O_3 treatment with different heating temperatures. Leakage current of STA thin films decreased with increasing treatment temperature of UV/O_3 treatment. The leakage current of a STA thin film subjected to UV/O_3 treatment at a temperature of 290 °C was six orders of magnitude lower than that of an untreated STA thin film. The improvement mechanism on leakage current under UV/O_3 treatment was analyzed. Si^{4+} and Ti^{4+} diffused to Ta^{5+} sites where they generated Si^{-} and Ti^{-}, which affected the leakage current properties. For UV/O_3 treatment at relatively low temperatures, Si^{-} and Ti^{-} combined with V_o^{+} to generate active shallow donors of $(Si^{-}–V_o^{+})^{+}$ and $(Ti^{-}–V_o^{+})^{+}$ combinations and consequently the leakage current increased. However, sufficiently Ti^{-} ions were generated at higher treatment temperatures and they combined with $(Si^{-}–V_o^{+})^{+}$ and $(Ti^{-}–V_o^{+})^{+}$ combinations to generate inactive $(Si^{-}–V_o^{+})^{+}–Ti^{-}$ and $(Ti^{-}–V_o^{+})^{+}–Ti^{-}$ combinations. Thus, low leakage currents were obtained. These results suggested that an appropriate concentration of Ti in STA thin films could improve the leakage current properties. Since a high quality STA thin film could be fabricated at 500 ^{o}C, solution process derived STA thin film is possible to be applied on the fabrication of transparent displays.

[References]

1) T. P.-C. Juan, S. -M. Chen, and J. Y. -M. Lee: J. Appl. Phys. **95** (2004) 3120.

2) K. C. Kao: Dielectric Phenomena in Solids (Elsevier Academic Press, London, 2004) P75

3) K. Okazaki: Exercise on Electrical Engineering Materials (Gakken Marketing, Tokyo, 1969) P76 [in Japanese]

4) W. S. Lau, K. K. Khaw, P. W. Qian, N. P. Sandler, and P. K. Chu: Jpn. J. Appl. Phys. **35** (1996) 2599

5) K. Kishiro, N. Inoue, S.-C. Chen, and M. Yoshimaru: Jpn. J. Appl. Phys. **37** (1998) 1336

6) W. S. Lau, K. K. Khaw, T. Han, and N. P. Sandler: Appl. Phys. Lett. **89** (2006) 262901

7) Y. S. Kim, Y. H. Lee, and M. Y. Sung: Solid-State Electron. **43** (1999) 1189

8) H.-C. Kim, Y.-S. Kim, Y.-B. Kim, D.-K. Choi: J. of Non-Cryst. Solids **336** (2004) 107

9) H. Shinriki, M. Nakata, Y. Nishioka, and K. Mukai: IEEE Electron Device Lett. **10** (1989) 514

10) S. Regnery, R. Thomas, P. Ehrhart, and R. Waser: J. Appl. Phys. **97** (2005) 073521

11) G. K. Layden: Mater. Res. Bull. **2** (1967) 533.

12) ICDD 00-020-0146.

13) T. Nozaka, Y. Mizutani, B. Gun, M. Echizen, T. Nishida, H. Takeda, K, Uchiyama, and T. Shiosaki: Jpn. J. Appl. Phys. **47** (2008) 7494

14) W.-J. Lee, I.-K. You, S.-O. Ryu, B.-G. Yu, K.-I. Cho, S.-G. Yoon, and C.-S. Lee: Jpn. J. Appl. Phys. **40** (2001) 6941

15) A. Paskaleva, M. Lemberger, A. J. Bauer, W. Weinreich, J. Heitmann, E. Erben, U. Schröder, and L. Oberbeck: J. Appl. Phys. **106** (2009) 054107

16) C. Jorel, C. Vallée. P. Gonon, E. Gourvest, C. Dubarry, and E. Defay: Appl. Phys. Lett. **94** (2009) 253502

17) F.-C. Chiu, J.-J. Wang, J. Y.-M. Lee, and S. C. Wu: J. Appl. Phys. **81** (1997) 6911

18) Y. H. Jeong, J. C. Kim, J. B. Lim, K. P. Hong, S. Nahm, H. J. Sun, T. H. Ghong, Y. D. Kim, and H. J. Lee: J. Appl. Phys. **101**(2007) 084108

19) P. Gonon, and C. Vallée: Appl. Phys. Lett. **90** (2007) 142906

20) T.-H. Perng, C.-H. Chien, C.-W. Chen, P. Lehnen, and C.-Y. Chang: Thin Solid Films **469** (2004) 345

21) S. Blonkowski, M. Regache, and A. Halimaoui: J. Appl. Phys. **90** (2001) 1501

22) S. M. Sze and K. K. NG: Physics of Semiconductor Devices (John wiley & Sons,

Inc., Hoboken, 2007) 3rd ed., P227
23) S. Maekawa, K. Okude, and T. Ohishi: J. Sol-Gel Sci. Tech. **2** (1994) 497
24) S. Hirai, K. Shimakage, and M. Sekiguchi: J. Am. Ceram. Soc. **82** (1999) 2011
25) N. Tohge, K. Shinmou, and T. Minami: J. Sol-Gel Sci. Tech. **2** (1994) 581
26) M. L. Calzada, I. Bretos, R. Jiménez, H. Guillon, and L. Pardo: Adv. Mater. **16** (2004) 1620
27) S. Tanimoto, M. Matsui, K. Kamisako, K. Kuroiwa, and Y. Tarui: J. Electrochem. Soc. **139** (1992) 320
28) Y. Ishikawa, and T. Tamagawa: Electronics and Communications in Japan, **79** (1996) 78
29) M. Matsui, S. Oka, K .Yamagishi, K. Kuroiwa, and Y. Tarui: Jpn. J. Appl. Phys. **27** (1998) 506
30) I. S. Kim, S. J. Jeong, J. S. Song, and P. S. Shin: Met. Mater. Int. **8** (2002) 577
31) W. S. Lau, and T. han: Appl. Phys. Lett. **83** (2003) 2835
32) W. S. Lau, T. S. Tan, P. Babu, and N. P. Sandler: Appl. Phys. Lett. **90** (2007) 112903
33) A. Paskaleva, M. Tapajna, E. Atanassova, K. Frohlich, A. Vincze, and E. Dobrocka: Appl. Surf. Sci. **254** (2008) 5879
34) K. M. A. Salam, H. Fukuda, and S. Nomura: Mater. Sci. Semicond. Process. **6** (2003) 531
35) C. S. Chang, T. B. Wu, W. C. Shih, and L. L. Chao: Jpn. J. Appl. Phys. **38** (1999) 6812

Chapter 3

Low temperature fabrication of InZnO thin film transistors using solution process

InZnO (IZO) thin film transistors (TFTs) were fabricated by the spin-coating method using the thermally oxidized SiO_2 as gate dielectric material. For the fabrication of IZO thin films, both organic and aqueous solutions were adopted. By the use of the organic precursor, a high annealing temperature should be used for obtaining high performance TFTs. In order to decrease the annealing temperature of IZO thin films, UV/O_3-assisted annealing was used. Under the UV/O_3-assisted annealing, TFTs with 290 ^oC annealed IZO thin film as channel layer showed almost the same properties to that of the TFTs with 700 ^oC annealed IZO thin film as channel layer which was not assisted by UV/O_3 treatment. However, although the properties significantly improved by the UV/O_3-assisted annealing at a low temperature, they were still not good enough for the application of displays. Large amounts of carbon (C) impurities still remained in the UV/O_3-assisted annealed IZO thin films, which were considered to mainly induce the insufficient performance. Therefore, an aqueous solution using the water as solvent and inorganic metal salts as solutes were adopted. Significantly decreased C was found in the IZO thin film. An extremely high field effect mobility (μ_{FET}) of 19.5 $cm^2/(V\cdot s)$ was obtained by the use of this aqueous solution even though the annealing temperature was as low as 300 ^oC.

3.1 Fabrication of IZO TFTs

A bottom-gated structure for TFT fabrication was adopted. The fabrication process of IZO TFTs is shown in Fig. 3-1. A low resistivity ($\rho < 0.004\ \Omega$) P^+-Si wafer was used as the substrate. Because of the low resistivity, the Si substrate was also used as the gate electrode. Thermally oxidized SiO_2 thin films with thickness of 50 or 100 nm were used as gate dielectrics, thus good interfaces were obtained between the gate electrode and gate dielectric. The IZO thin films were fabricated by spin-coating method. A metal organic decomposition (MOD) solution (Kojundo Chemical) and an aqueous solution were used to fabricate IZO thin films. In order to obtain expected thickness, the spin-coating process was repeated several times. After spin-coating, various annealing processes were used to improve the properties of deposited thin films. Traditional photolithography of applying photoresist, exposing to UV light

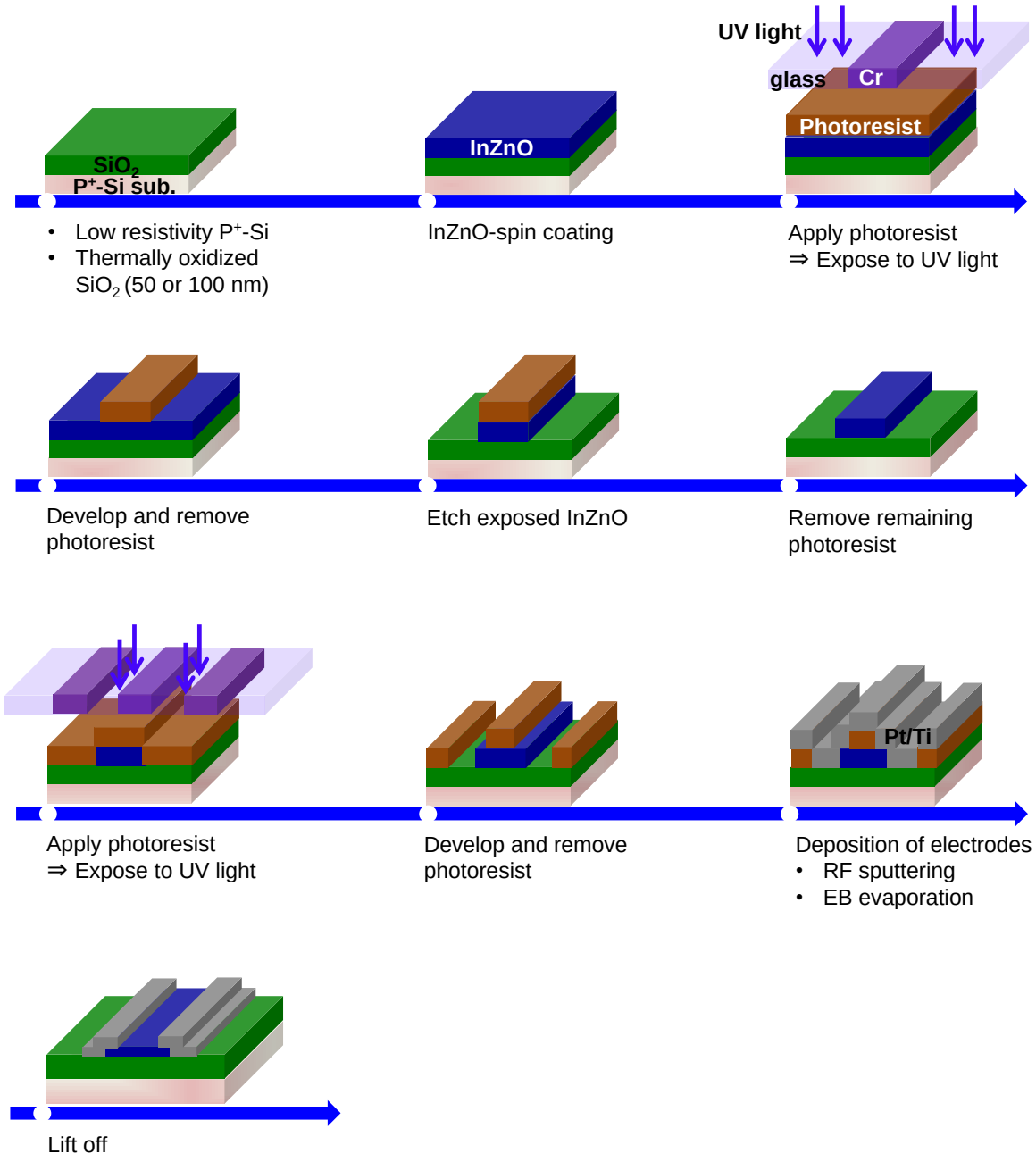


Fig. 3-1 Fabrication process of the solution process-derived IZO TFTs.

through a mask, removing photoresist, etching exposed IZO thin film, deposition of electrodes and lift off was used for the fabrication of TFTs. Diluted HCl with the concentrations of about HCl:H_2O=1:199 and 1:99 were used to etch unnecessary organic and aqueous solution derived IZO thin films, respectively. Source and drain electrodes were deposited by sputtering or electron-beam evaporation. Characteristics of fabricated TFTs were measured in the dark at room temperature using a precision semiconductor parameter analyzer (Agilent 4156C).

3.2 Temperature dependency of organic solution-derived IZO TFTs

When organic solutions are used, high annealing temperatures (400 °C or higher) are commonly required to decompose the organic additives and to crystallize the semiconducting oxides to obtain high performance TFTs.[1-6] Therefore, the annealing temperature dependency of IZO TFTs was firstly investigated.

The concentrations of $InO_{1.5}$ (SYM-IN02) and ZnO (SYM-ZN20) MOD solutions were 0.2 and 2 mol/l, respectively. To ensure chemical homogeneity, the mixed solution was stirred at room temperature for 1 h. The molar ratio of In to Zn was about 4 to 1. The thicknesses of fabricated IZO thin films were about 20 nm. Fabricated TFTs with the channel width/length of about 500/50 μm were used to evaluate the properties.

The thermal behavior of the mixed IZO precursor was monitored under air atmosphere from room temperature to 500 ^oC by thermogravimetry-differential thermal analysis (TG-DTA; EXSTAR TG/DTA6000), as shown in Fig. 3-2. A first endothermic reaction was observed with a large weight loss in the range below 88 °C; this was primarily caused by low-temperature solvent evaporation. An exothermic peak around 337 ^oC was observed, which was interpreted as the alloying of metal hydroxides to multicomponent oxides.[4] No significant weight loss occurred at temperatures above 348 ^oC. These results indicated that the semiconducting characteristics would be hard to discern, except that the annealing temperature was higher than 348°C. Therefore, the annealing temperatures of IZO thin films were carried out at 400, 500, 600, 700 and 800 ^oC. They will be abbreviated as IZO-400, IZO-500, IZO-600, IZO-700 and IZO-800, respectively.

Microstructures of various temperatures annealed IZO thin films were investigated by X-ray diffractometry (XRD), as shown in Fig. 3-3. For all thin films, diffraction peaks were found. Thus, all of these IZO thin films crystallized. According to the positions and relative intensity of diffraction peaks, crystal structures were decided as bixbyite structures. As annealing temperature increased, the intensity of diffraction peaks increased. It was considered to attribute to the

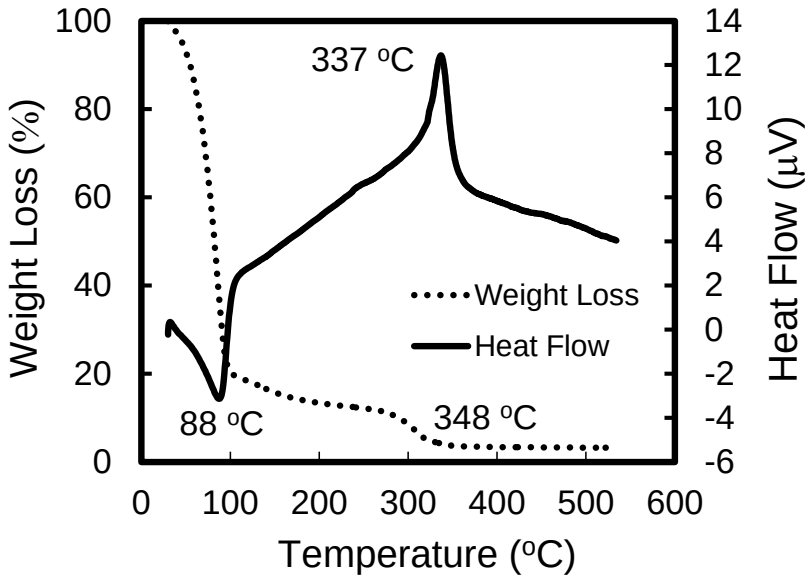


Fig. 3-2 TG-DTA result of IZO organic solution.

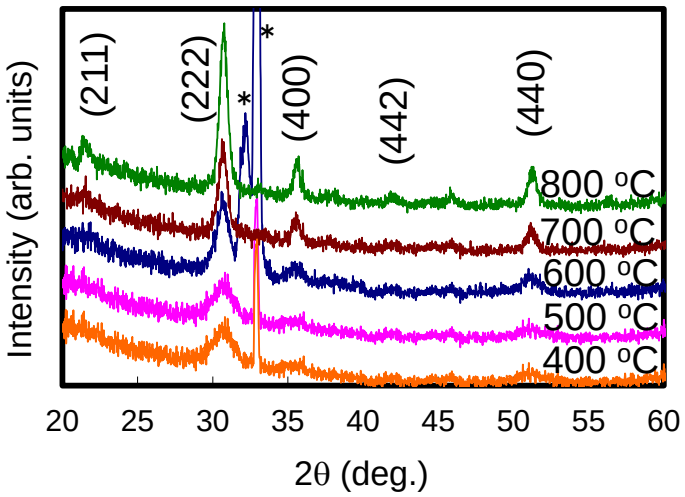


Fig. 3-3 XRD patterns of various temperatures annealed IZO thin films.
*Diffraction peaks of the Si substrate. These peaks were not observed in IZO thin films which were annealed at 700 and 800 °C due to the forbidden of X-rays' reflection.[7)]

growth of crystal grains.

Surface morphologies of all thin films are shown in Fig. 3-4. Surface roughness of IZO-400, IZO-500, IZO-600, IZO-700 and IZO-800 were 0.16, 0.21, 0.23, 0.35 and 0.77 nm, respectively. All of them showed roughness lower than 1 nm, which suggested that IZO thin films were well fabricated on substrates. As annealing temperature increased, the surface roughness increased. It was due to the grain growth. From 400 to 700 ^{o}C, the roughness uniformly increased, however, a large increase was found from 700 to 800 ^{o}C.

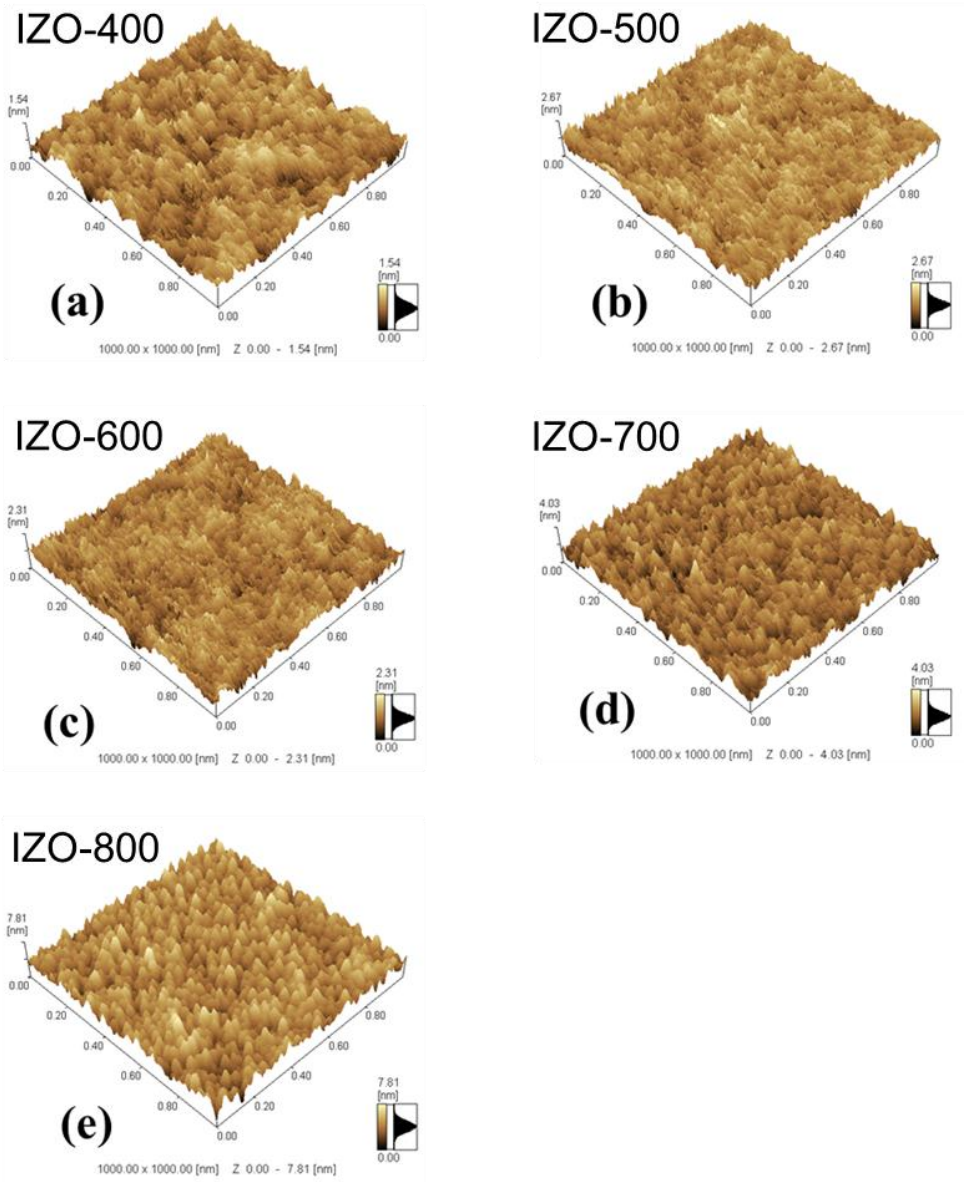


Fig. 3-4 Surface morphologies of IZO thin films which were annealed at (a) 400, (b) 500, (c) 600, (d) 700 and (e) 800 ^{o}C.

Transfer characteristics at a drain voltage (V_{ds}) of 10 V of TFTs with various temperatures annealed IZO thin films are shown in Fig. 3-5. No off-states, i.e., intensively negatively shifted threshold voltage (V_{th}), were found in IZO-400 and IZO-500 TFTs in the measured voltage range. This will be discussed later. The off-current of the IZO-700 TFT was almost the same to that of the IZO-800, and lower than that of the IZO-600. Meanwhile, the IZO-700 TFT showed the highest on-current. Electrical parameters of IZO-600, IZO-700 and IZO-800 TFTs are shown in Table 3-1. The IZO-700 TFT showed the highest μ_{FET} of 2.25 $cm^2/V \cdot s$, highest on/off current ratio (I_{on}/I_{off}) which exceeded 10^8 and lowest sub-threshold swing (S) of 0.44 V/decade. Therefore, 700 ^oC was the best annealing temperature for the fabrication of IZO thin films.

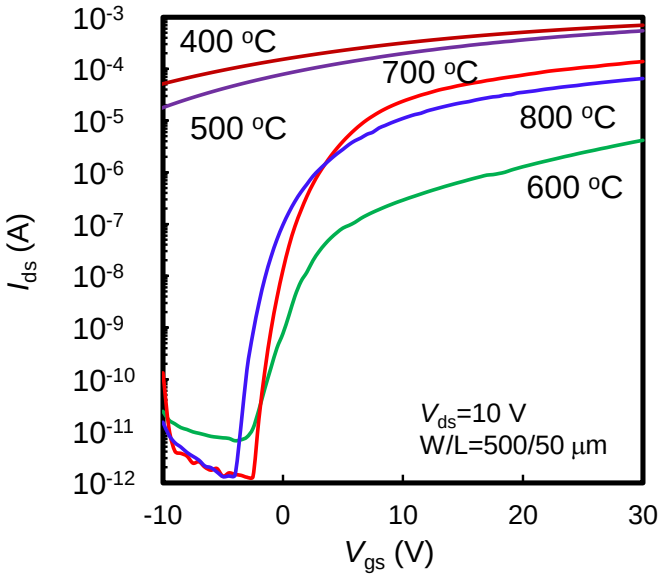


Fig. 3-5 Transfer characteristics of TFTs with various temperatures annealed IZO thin films.

Table 3-1 Parameters of 600, 700 and 800 ^oC annealed IZO TFTs.

T (^oC)	600	700	800
μ_{FET} ($cm^2/(V \cdot s)$)	0.12	2.25	1.03
I_{on}/I_{off}	6.4×10^5	1.4×10^8	4.9×10^7
S (V/decade)	1.20	0.44	0.45

Various elements including organic remains of C and hydrogen (H) in IZO thin films were investigated by secondary ion-microprobe mass spectrometry (SIMS; Ion-Microprobe Atomika-6500) using a Cs ion beam, as shown in Fig. 3-6. As annealing temperature increased, concentrations of C and H ions decreased, which suggested that a high annealing temperature was effective to exclude organic remains. From the annealing temperature of 400 to 700 ^{o}C, no change of concentrations of In and Zn ions were found. However, the concentration of Zn decreased in the IZO-800 thin film. It suggested that the Zn could not endure high annealing temperature and volatilized from the thin film. Since no volatile of In and Zn was found in thin films which were annealed under 700 ^{o}C, the variation of TFTs' properties was considered to be mainly affected by the variation of C and H impurities. These impurities commonly act as traps or scattering centers to prevent the increase of the mobility.[8-9] On the other hand, although concentrations of C and H ions in the IZO-800 were lower than those in the IZO-700, the IZO-800 TFT showed lower μ_{FET} than that of the IZO-700 TFT. The deviation of the Zn was considered to affect the properties of IZO-800 TFT.[4]

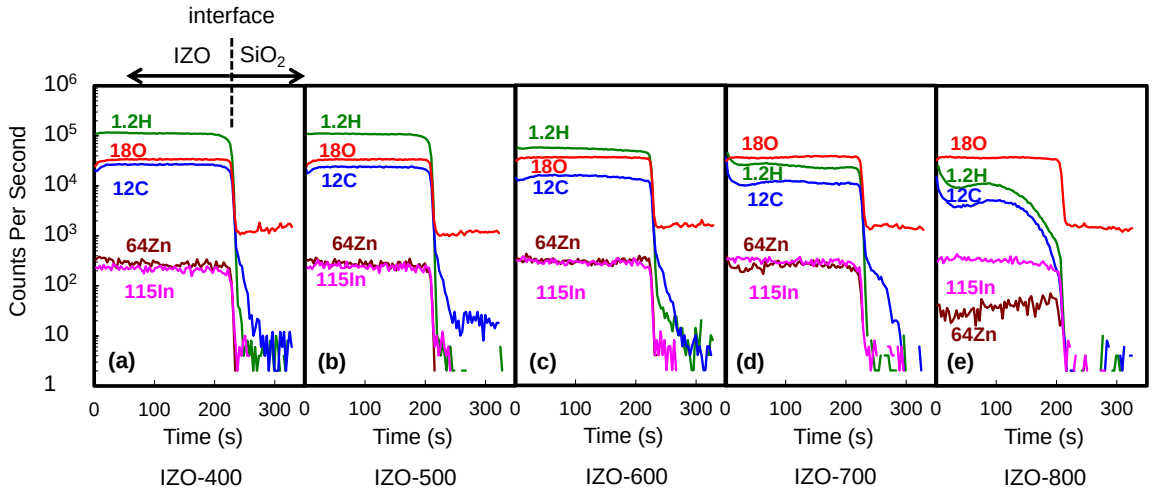


Fig. 3-6 Depth profiles of various elements in (a) IZO-400, (b) IZO-500, (c) IZO-600, (d) IZO-700, and (e) IZO-800 thin films.

According to the investigation on the temperature dependency of IZO TFTs, the appropriate annealing temperature of organic solution-derived IZO thin films was decided at 700 ^{o}C. The best properties were mainly due to the crystal growth, and low

concentrations of C and H impurities.

3.3 UV/O_3-assisted annealing of organic solution-derived IZO TFTs

For the fabrication of TFTs on glass and flexible substrates, the fabrication temperature should be lower than 500 and 300 ^{o}C (in general, 150 ^{o}C), respectively. In order to lower the fabrication temperature, Song *et al.* used microwave-assisted annealing to enhance the crystallization and subsequently obtained high-performance TFTs.[10] The UV/O_3-assisted annealing was proved to effective for improving leakage current properties of $SrTa_2O_6$ thin films which were fabricated at a lower temperature of 500 ^{o}C. Therefore, the UV/O_3-assisted annealing was also used to decrease the fabrication temperature of solution process-derived IZO thin films. IZO thin films were heated on the hotplate at 290 °C for 4 h under UV irradiation in the O_3 atmosphere after spin-coating. The fabricated thin film will be abbreviated as IZO-290UV/O_3.

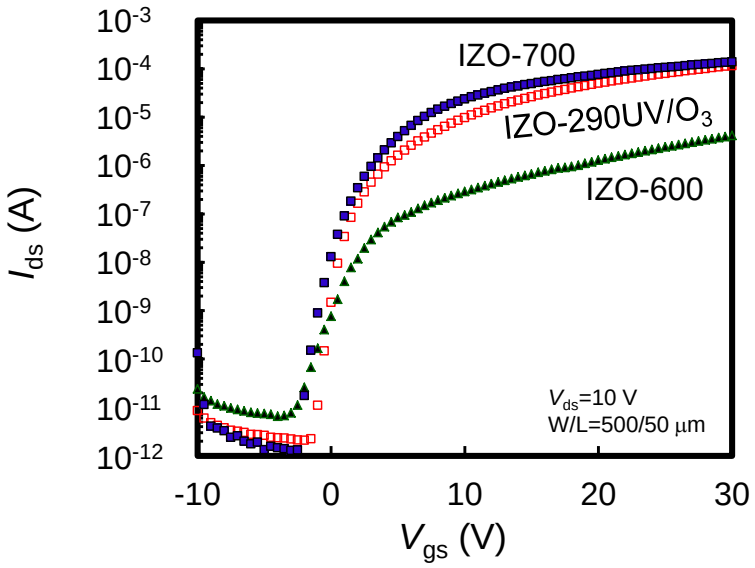


Fig. 3-7 Transfer characteristics of IZO-600, IZO-700, and IZO-290UV/O_3 TFTs.

In order to understand the UV/O_3-assisted annealing well, properties of IZO-600 and IZO-700 TFTs were compared. Figure 3-7 shows transfer characteristics of these TFTs at V_{ds} of 10 V. The IZO-290UV/O_3 TFT has characteristics, such as μ_{FET} of 2.19 $cm^2/(V\cdot s)$, threshold voltage (V_{th}) of 1.78 V, and S of 0.44 V/decade, much better

than those of the IZO-600 TFT and similar to those of the IZO-700 TFT. A high μ_{FET} of 2.19 $cm^2/(V\cdot s)$ was obtained although the annealing temperature of 290 °C was lower than the pyrolysis temperature of 348°C. This μ_{FET} was much higher than that (0.02 $cm^2/(V\cdot s)$) reported by Koo *et al.* for IZO TFTs prepared at 350 °C,[4] and almost the same as that for TFTs which were annealed at 300°C with microwave-assisted annealing (2.12 $cm^2/(V\cdot s)$).[10]

To understand the high mobility of the IZO-290UV/O_3 TFT, depthwise profiles of possible elements in these IZO thin films were investigated by SIMS, as shown in Fig. 3-8. Compared with the IZO-600 and IZO-700 thin films, IZO-290UV/O_3 had higher C and H ion concentrations. This suggested that the high μ_{FET} of the IZO-290UV/O_3 TFT was not primarily affected by the C and H. On the other hand, a higher concentration of Si ions was found in the IZO-290UV/O_3 thin film. Ishikawa *et al.* reported that the diffusion of the Si could be enhanced by UV irradiation at a low temperature.[11] Si was also detected from the surface on only the UV-irradiated thin film in a study of TaO_x thin films derived by various annealing processes.[12] Therefore, it was considered that the Si in the underlayer of the SiO_2 thin film might be induced by the UV irradiation and diffused into the IZO-290UV/O_3 thin film.

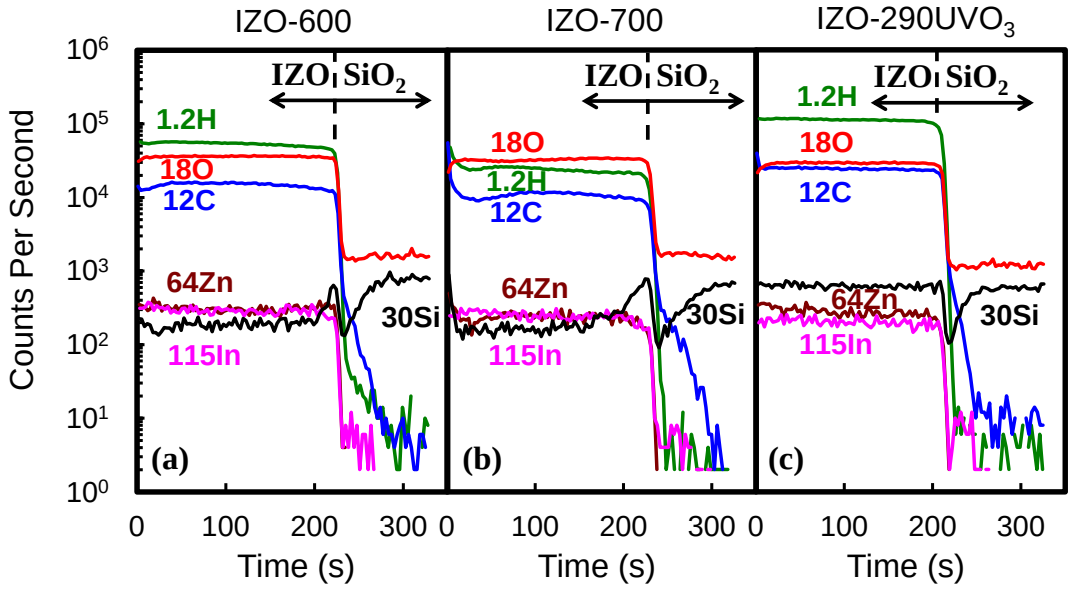


Fig. 3-8 Depthwise profiles of various elements in (a) IZO-600, (b) IZO-700, and (c) IZO-290UV/O_3.

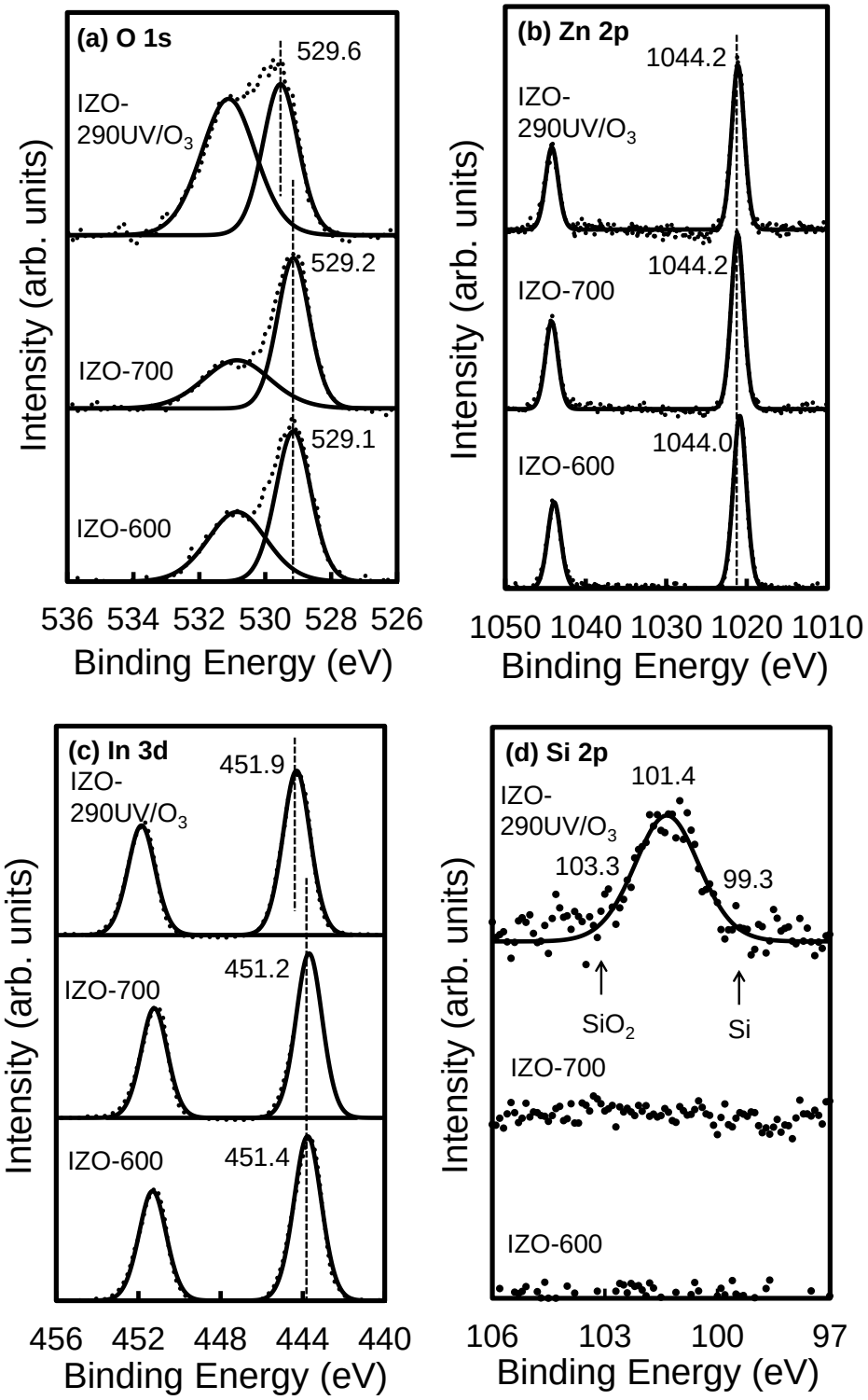


Fig. 3-9 Binding energy spectrums of (a) O 1s, (b) Zn 2p, (c) In 3d, and (d) Si 2p in IZO-600, IZO-700, and IZO-290UVO_3.

Binding energies of O 1s, Zn 2p, In 3d, and Si 2p in IZO-600, IZO-700, and IZO-290UVO$_3$ thin films were measured by X-ray photoelectron spectroscopy (XPS) using an mono-Al Kα radiation; they are shown in Fig. 3-9. The O 1s peaks were divided into two peaks that were determined by Gaussian fitting (Fig. 3-9(a)). The peak with a lower binding energy (O_L) represents stoichiometric oxidized bonds (O-M).[13-14] These peaks are centered at 529.1, 529.2, and 529.6 eV for IZO-600, IZO-700, and IZO-290UVO$_3$, respectively. Almost no difference in these positions was found in IZO-600 and IZO-700, but a small higher-energy shift was found in the IZO-290UVO$_3$. The peak with a higher binding energy (O_H) originated from oxygen in the oxygen-deficient (V_o) region in the IZO compound.[13-14] The ratios $O_H/(O_{H+}O_L)$, representing relative quantities of V_o, were 0.40, 0.44, and 0.58 for IZO-600, IZO-700, and IZO-290UVO$_3$, respectively. The IZO-700 showed a little higher V_o than IZO-600, however, V_o significantly increased in IZO-290UVO$_3$.

Binding energies of Zn $2p_{1/2}$ of IZO-600, IZO-700, and IZO-290UVO$_3$ were located at 1044.0, 1044.2, and 1044.2 eV. Almost no energy shift was found (Fig. 3-9(b)). The binding energies of In $3d_{3/2}$ in IZO-600, IZO-700, and IZO-290UVO$_3$ were located at 451.4, 451.2, and 451.9 eV (Fig. 3-9(c)). A higher-energy shift of ≥0.5 eV was found in IZO-290UVO$_3$. Meanwhile, the XPS peak of the Si 2p, which was located at 101.4 eV, was detected in IZO-290UVO$_3$ but not in IZO-600 and IZO-700 (Fig. 3-9(d)). These results were in accordance with the SIMS measurement results that the Si diffused into IZO-290UVO$_3$ thin film and reached its surface. In general, the Si 2p peak is located at 99.3 eV in Si but at 103.3 eV in SiO_2 because of the O-Si-O bonding.[15] However, the binding energy of the Si 2p in IZO-290UVO$_3$ did not follow this pattern. This suggested that the generated bonding was not Si-Si and O-Si-O, i.e., the diffused Si combined with other elements. Since no shift of binding energies of Zn 2p was found in the IZO-290UVO$_3$, it was thought that Zn kept its initial bonding with elements of O and In as Zn-O-In in the IZO matrix even though the Si diffused into the IZO thin film.

The first-principle density-functional calculation result of Lyons *et al.* showed that the substitution of Zn by Si (Si_{zn}^{2+}) had the lowest-energy configuration than other substitution pattern while there was an impurity of Si in ZnO.[16] On the other hand, Lyons *et al.* pointed out that the Si acted as a shallow donor in ZnO and could increase the conductivity of ZnO.[16] Zhang *et al.* also observed that Si existed as Si_{zn}^{2+} while Si was doped in the $In_2O_3(ZnO)_3$ nanobelt, and subsequently induced a low resistivity.[17] Since conductivity is proportional to the product of mobility and carrier concentration, the Si improved carrier concentration and mobility of ZnO and $In_2O_3(ZnO)_3$. In this research, the μ_{FET} of IZO-290UVO$_3$ TFT was much higher than that of the IZO-600 and very close to that of the IZO-700 although there were many

more C and H ions remaining in the IZO-290UVO_3, therefore it was considered that the Si atoms also entered the site of Zn ions in the IZO system of IZO-290UVO_3 according to the following defect equation,

$$\mathrm{Zn}_{Zn} \xrightarrow{Si} Si_{Zn}^{2+} + 2e. \quad (3\text{-}1)$$

These additional two more electrons acted as moving carriers and induced a higher μ_{FET} in the IZO-290UVO_3 TFT than in the IZO-600 TFT.

The electronegativity of the Si, O and Zn were 1.8, 3.5 and 1.6 respectively. The difference of the electronegativity of the Si (1.8) and the O (3.5) is smaller than that of the Zn (1.6) and the O(3.5), so the Si tended to combine with the O less strongly than the Zn combined with the O. The additive Si atoms allowed the escape of oxygen atoms, which led to the increase of the V_o.[14] It agreed the XPS results well that much higher concentration V_o existed in the IZO-290UVO_3. The higher energy shift of O 1s was commonly accompanied by the increase of V_o,[18] therefore, the observed higher binding energy shifts of O 1s and In 3d were also considered to be due to the formed Si-O-In bonding.

Under the UV/O_3-assisted annealing, the TFT with an IZO thin film fabricated at 290 °C showed a much higher μ_{FET} of 2.19 $cm^2/(V\cdot s)$, a higher on/off-current ratio of 10^7, and a lower *S* value of 0.44 V/decade compared to the corresponding values for the TFT fabricated at 600 °C although the fabrication temperature of 290 °C was lower than the pyrolysis temperature of the precursor solution. These values were almost the same as those for the TFT fabricated at 700 °C. However, high concentrations of C and H impurities still remained in the UV/O_3-assisted annealed IZO thin film (still higher than those in the IZO-600 and IZO-700). Therefore, the properties were still not high enough to compare with TFTs that were fabricated by vacuum-based processes. In order to solve this problem, less C and H included inorganic solution should be developed.

3.4 High performance IZO TFTs fabricated by aqueous solution

Recently, a high-performance IZO TFT fabricated under 250 ^oC using metal alkoxide precursors was reported.[8] However, fabrication steps requiring anhydrous conditions were very expensive and complicated. On the other hand, Jeon *et al.* obtained much higher mobility TFTs at low temperatures through the use of aqueous solution derived fluorine-doped zinc tin oxide (ZTO:F) thin films. In their reports, the

values of μ were 2.85 and 7.95 $cm^2/V\cdot s$ when the ZTO:F thin films were fabricated at temperatures of 250 °C for 12 h and 300 °C for 1 h, respectively.[19] Since the diffusion of generated V_o were effectively passivated by metal fluoride bonds at the ZTO:F channel/gated dielectric interface, high mobility was obtained.[19] However, IZO TFTs without any element doping and fabricated at 300 °C showing mobility value of over 10 $cm^2/V\cdot s$ were still rarely reported until now.

In this research, an aqueous precursor using water as solvent, nitrate-based inorganic salt as solute were also fabricated to deposit IZO thin films. A very small part of organic material was added in the aqueous precursor to improve the quality of the aqueous precursor. Composition ratio of In to Zn was also about 4 to 1. After spin-coating, IZO thin films were heated on hot plates at 100 °C for 5 min to evaporate the solvent and then annealed at 300 °C for 1 h on hotplates. Thicknesses of the fabricated IZO thin films were about 10 nm. These IZO thin films will be abbreviated as A-IZO300 thin films.

The TG-DTA result of the aqueous solution is shown in Fig. 3-10. The endothermic peak was found at a temperature of 80 °C with large weight loss because the solvent was water. The exothermic peak was found at a temperature of 203 °C. This temperature was about 130 °C lower than that of the MOD solution (337 °C). It indicates that the chemical reaction and the generation of IZO thin films could be completed at a much lower temperature by the use of this aqueous solution.

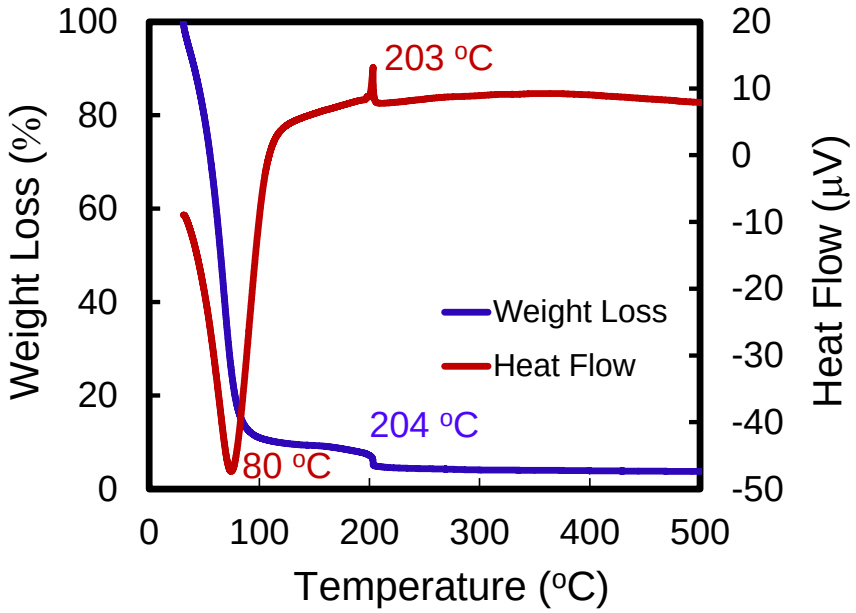


Fig. 3-10 TG-DTA result of the aqueous solution.

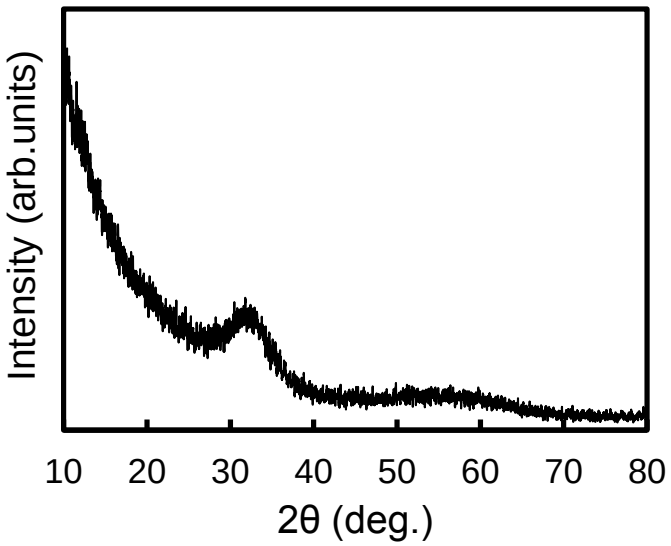


Fig. 3-11 The XRD pattern of the A-IZO300 thin film. A broad and weak peak was found.

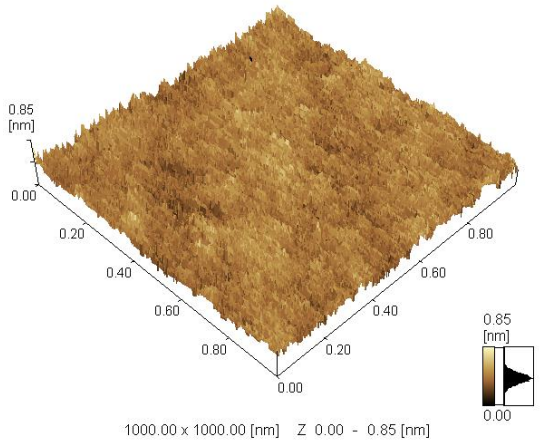


Fig. 3-12 The surface morphology of the A-IZO300 thin film. Very low arithmetic average roughness of 0.06 nm was obtained.

Crystalline structure of the A-IZO300 thin film is shown in Fig. 3-11. The diffraction peak which was found at around 32 ^{o} suggested that the A-IZO300 thin film was correctly fabricated. Since the peak was weak and broad, the thin film was considered as the mixture of nanocrystalline and amorphous. Surface morphology of the A-IZO300 thin film is shown in Fig. 3-12. A very low arithmetic average roughness of 0.06 nm was obtained. This low value suggested that the A-IZO300 thin film was well fabricated on the substrate with good uniformity. Good interfaces of A-IZO300/SiO_2 and A-IZO300/electrodes were also expected to be obtained.

Output and transfer characteristics of the A-IZO300 TFT are depicted in Fig. 3-13(a) and 3-13(b), respectively. Very clear pinch off state was obtained, as shown in the output diagram (Fig. 3-13(a)). The saturation state of the TFT was observed at the V_{ds} of lower than 5 V. It was much lower than many other solution process-derived IZO TFTs.[1-6)] Meanwhile, low off-currents of 10^{-13} A were obtained at V_{ds} of 0.1 (linear area) and 5 V (saturation area), as shown in transfer diagrams (Fig. 3-13(b)). These off-currents were also much lower than those of the organic solution-derived IZO TFTs in this work and many other solution process derived IZO TFTs.[13-14)] Various parameters were estimated at the V_{ds} of 5 V. The μ_{FET} was as high as 19.5 $cm^2/(V\cdot s)$. No higher values of μ_{FET} were reported until now at such low off current states for solution process-derived IZO TFTs. The I_{on}/I_{off} exceeded 10^9. Low S of 0.36 V/decade and V_{th} of -1.9 V were also obtained. These values indicated that a high performance TFT was fabricated at a low temperature of 300 ^{o}C.

No impurity of nitrogen was found in the aqueous solution-derived thin film although nitrate salts were used as metal sources (measured by SIMS). Since remaining C and H significantly affect the properties of fabricated TFTs, the C and H were investigated in the A-IZO300 thin film. As the reference, the SIMS profiles of organic solution-derived IZO thin films which were annealed at 700 ^{o}C (IZO-700) were compared in Fig. 3-14. No variation of In and Zn was found between them. However, the C in the A-IZO300 was much lower than that in the IZO-700 even though the annealing temperature was as low as 300 ^{o}C. It is reported that carbon-related impurities work as shallow acceptors in semiconductors.[20-21)] These defect states trap carriers in thin films. Thus, higher on-current were obtained when less carbon remained in the thin films. On the other hand, since the precursor was H_2O, the concentration of H in the A-IZO300 was higher than that in the IZO-700 and very close to that in the IZO-400. Mollwo, Baik *et al.*, and Kohiki *et al.* observed an increased conductivity in ZnO while they were annealed in hydrogen at temperatures above 200 °C.[22-24)] Kim *et al.* also reported that stable high conductive amorphous InGaZnO was obtained by hydrogenation using hot isostatic pressing.[25)] Walle explained the increase of conductivity using the first principle calculation.[25)] In this

research, the H in thin films might also contribute to the increase of conductivity of fabricated thin films. Therefore, very high mobility was obtained in the A-IZO300 TFT. It was the same that H might be the reason of no off-states in IZO-400 and IZO-500 TFTs.

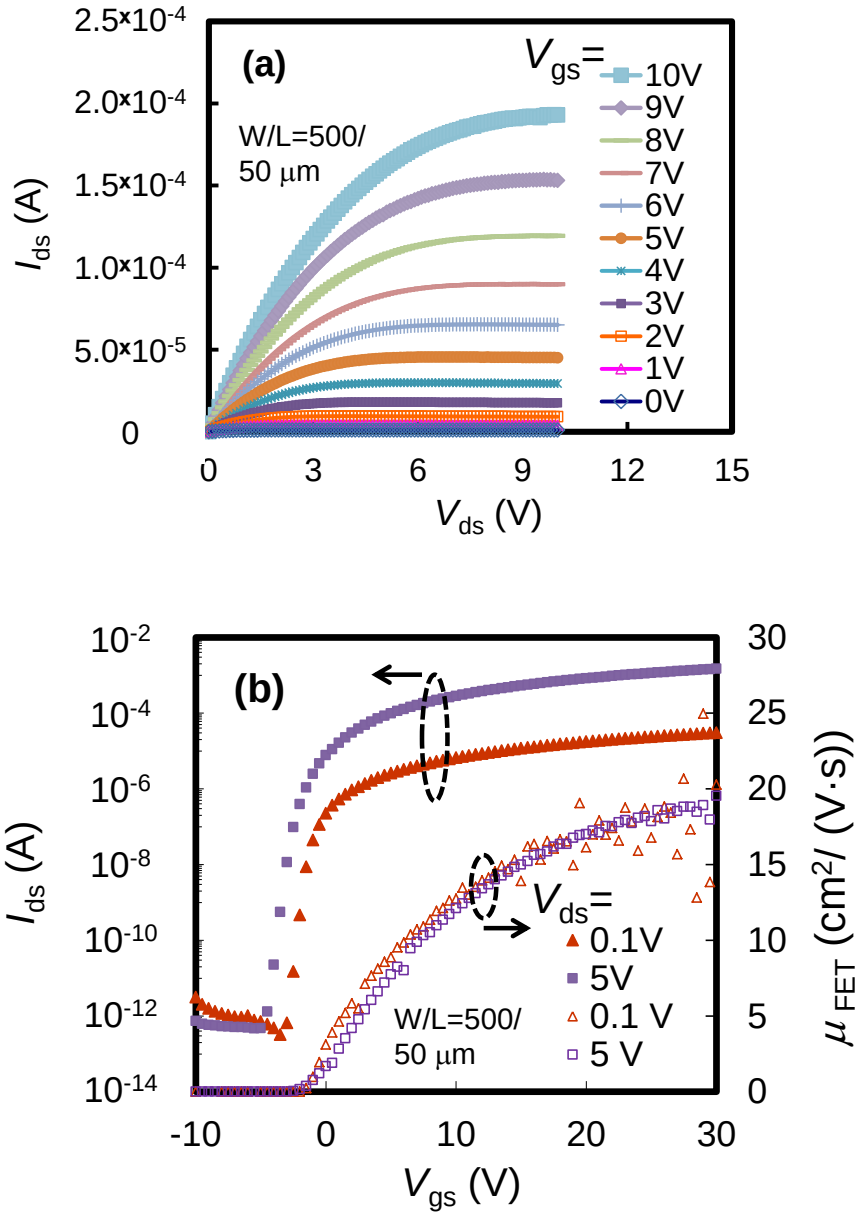


Fig. 3-13 (a) Output and (b) transfer characteristics of the A-IZO300 TFT.

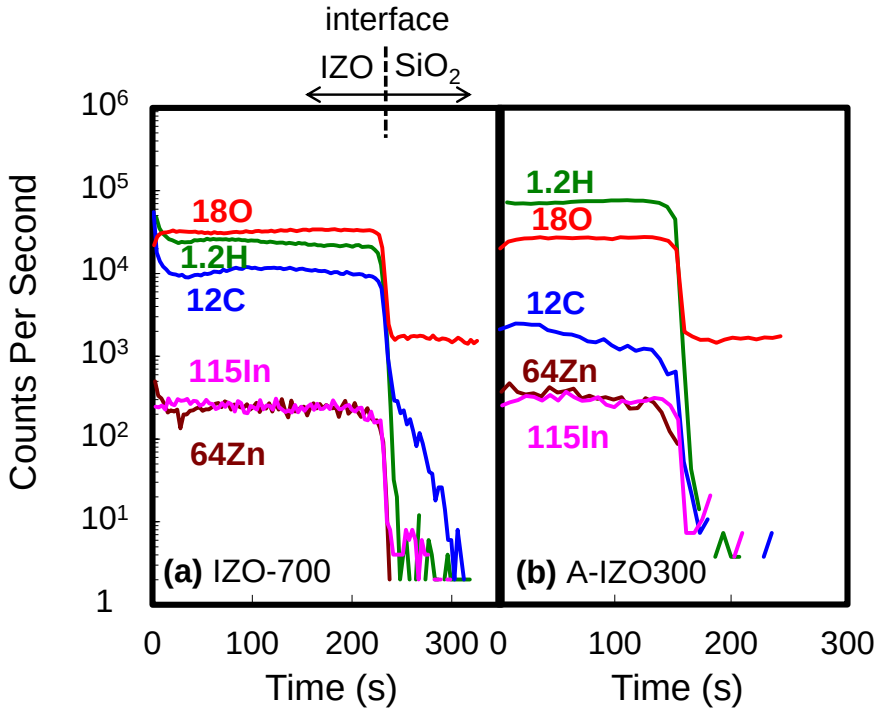


Fig. 3-14 Depth profiles of various elements in (a) IZO-700 and (b) A-IZO300. The C impurity significantly decreased in the A-IZO300 thin film.

By the use of the aqueous solution, high performance IZO TFTs with μ_{FET} of 19.5 $cm^2/(V\cdot s)$ and I_{on}/I_{off} of exceeding 10^9 were fabricated at a low temperature of 300 ^oC. These properties are comparable with those of vacuum process-derived TFTs. They are suitable for the application of transparent and flexible displays.

3.5 Conclusion

The annealing temperature effect of an organic solution–MOD solution derived IZO TFTs were investigated. Among TFTs with various temperature annealed IZO thin films as channel layers, the IZO-700 TFT showed the best properties. As the annealing temperature increased, crystallinity of IZO thin films improved. Meanwhile, the C and H impurities decreased. Therefore, TFTs' properties increased as the annealing temperature increased. However, at the 800 ^oC annealing, the Zn volatilized from the thin film and induced deteriorated properties of the IZO-800 TFT.

In order to obtain high properties at the temperature of lower than 300 ^oC for the application on flexible substrates, an UV/O_3-assisted annealing method was

adopted to decrease the annealing temperature of IZO thin films. Under the UV/O_3-assisted annealing, the TFT with the IZO thin film fabricated at 290 °C as the channel layer showed a much higher μ_{FET} of 2.19 $cm^2/(V\cdot s)$, a higher I_{on}/I_{off} of 10^7, and a lower S of 0.44 V/decade compared to the corresponding values of the IZO-600 TFT although the fabrication temperature of 290 °C was lower than the pyrolysis temperature of the solution. These values were almost the same as those of the IZO-700 TFT. Impurities of Si ions diffused into the IZO thin film under UV/O_3-assisted annealing and entered the Zn ions' sites in the IZO matrix. The weaker bonding of Si-O increased oxygen vacancies, subsequently more freely moving electrons were generated because of this substitution. Thus, a high mobility was obtained.

However, large amounts of C still remained in the IZO thin film after UV/O_3-assisted annealing, the μ_{FET} was not high enough. Therefore, a C-less aqueous solution was used for realizing low temperature fabrication. High-performance IZO TFTs such as the μ_{FET} as high as 19.5 $cm^2/(V\cdot s)$, the I_{on}/I_{off} exceeded 10^9, low off currents of 10^{-13} A, low S of 0.36 V/decade, and low V_{th} value of 1.7 V, were obtained at a low temperature of 300 ^oC using this aqueous solution. Reports of such a high μ_{FET} value by the use of the solution process were rare until now. The completion of chemical reaction of the aqueous precursor was about 130 ^oC lower than that of the organic solution. This low temperature supplied the possibility to fabricate a high quality IZO thin film at a low annealing temperature. The fabricated IZO thin film showed a very smooth surface. It suggested that IZO thin films were well fabricated on the substrates. Significant low concentration of C impurity was found in the fabricated IZO thin film. Meanwhile, high H concentration was also found in the IZO thin film. The less C and high concentration of H were considered to enhance the μ_{FET} of aqueous solution-derived IZO TFTs.

[References]

1) D.-H. Lee, Y.-J. Chang, G. S. Herman, and C.-H. Chang: Adv. Mater. **19** (2007) 843.

2) Y.-J. Chang, D.-H. Lee, G. S. Herman, and C.-H. Chang: Electrochem. Solid-State Lett. **10** (2007) H135.

3) C. G. Choi, S.-J. Seo, and B.-S. Bae: Electrochem. Solid-State Lett. **11** (2008) H7.

4) C. Y. Koo, K. Song, T. Jun, D. Kim, Y. Jeong, S.-H. Kim, J. Ha, and J. Moon: J. Electron. Soc. **157** (2010) J111.

5) S. Jeong, Y. Jeong, and J. Moon: J. Phys. Chem. **112** (2008) 11082.

6) K.-B. Park. J.-B. Seon, G. H. Kim, M. Yang, B. Koo, H. J. Kim, M.-K. Ryu, and S.-Y. Lee: IEEE Electron Device Lett. **31** (2010) 311.

7) B.-H. Hwang: J. Phys. D: Appl. Phys. **34** (2001) 2469

8) K. K. Banger, Y. Yamashita, K. Mori, R. L. Peterson, T. Leedham, J. Rickard, and H. Sirringhaus: Nat. Mater. **10** (2011) 45

9) Y. S. Rim, W. H. Jeong, D. L. Kim, H. S. Lim, K. M. Kim, and H. J. Kim: J. Mater. Chem. **22** (2012) 12491

10) K. Song, C. Y. Koo, T. Jun, D. Lee, Y. Jeong, and J. Moon: J. Cryst. Growth **326** (2011) 23.

11) Y. Ishikawa and T. Tamagawa: Electronics and Communications in Japan **79** (1996) 78.

12) M. Matsui, S. Oka, K. Yamagishi, K. Kuroiwa, and Y. Tarui: Jpn. J. Appl. Phys. **27** (1998) 506.

13) B. Kumar, H. Gong, and R. Akkipeddi: J. Appl. Phys. **97**(2005) 063706.

14) D. N. Kim, D. L. Kim, G. H. Kim, S. J. Kim, Y. S. Rim, W. H. Jeong, and H. J. Kim: Appl. Phys. Lett. **97** (2010) 192105.

15) Handbook of X-ray Photoelectron Spectroscopy (Physical Electronics, Minnesota, 1995) p. 56–57.

16) J. L. Lyons, A. Janotti, and C. G. Van de Walle: Physical Review B **80** (2009) 205113.

17) J. Y. Zhang, Y. Lang, Z. Q. Chu, X. Liu, L. L. Wu, and X. T. Zhang: Cryst. Eng. Comm. **13** (2011) 3569.

18) S.-Y. han, G. S. Herman, and C. Chang: J. Am. Chem. Soc. **133** (2011) 5166

19) J.-H. Jeon, Y. H. Hwang, J. H. Jin, and B.-S. Bae: MRS Communicaions **2** (2012) 17

20) S. P. Watkins and G. Haacke: Appl. Phys. Lett. **59** (1991)2263

21) D. J. As and U. K¨ohler: J. Phys.: Condens. Matter **13** (2001) 8923

22) E. Mollwo: Z. Phys. **138** (1954) 478
23) S. J. Baik, J. H. Jang, C. H. Lee, W. Y. Cho, and K. S. Lim: Appl. Phys. Lett. **70** (1997) 3516
24) S. Kohiki, M. Nishitani, T. Wada, and T. Hirao: Appl. Phys. Lett. **64** (1994) 2876
25) W.-K. Kim, S. Lee, Y. C. Cho, H. Koinuma, S.-Y. Jeong, J. M. Shin, C. R. Cho,
26) C. G. Van de Walle: Phys. Rev. Lett. **85** (2000) 1012

Chapter 4

Oxide thin film transistors using high-k gate dielectrics of solution process-derived $SrTa_2O_6$ thin films

The 700 ^oC-annealed $SrTa_2O_6$ (STA-700) thin film was firstly used as the gate dielectric for the thin film transistor (TFT) with a sputtered-InGaZnO (IGZO) thin film as the channel layer. Higher on-current was obtained at lower gate and drain voltages compared with the sputtered-IGZO TFT using a thermal oxidized SiO_2 thin film as the gate dielectric. Extremely low subthreshold swing (*S*) of 0.07 V/decade was obtained. The sputtered-IGZO TFT using a STA thin film which was annealed at 500 ^oC and assisted by UV/O_3-treatment (STA-500UVO_3) showed almost the same properties to those of the sputtered-IGZO TFT using the STA-700 thin film as the gate dielectric. Meanwhile, extremely high field effect mobility (μ_{FET}) of 173.4 and 237.4 $cm^2/(V \cdot s)$ were obtained by the use of STA-700 and STA-500UVO_3 as gate dielectrics, respectively.

However, the aqueous solution could not be well deposited on the STA thin film, thus no switching properties were found for the TFT fabricated by aqueous solution-derived InZnO (IZO) and STA thin films.

On the contrary, organic solution-derived IZO thin films could be well fabricated on STA thin films. The TFT with organic solution derived-IZO thin film which was annealed at 400 ^oC as the channel layer and the STA-700 thin film as the gate dielectric also showed higher on/off current ratio (I_{on}/I_{off}), μ_{FET} and lower *S* than those of the TFT using the thermal oxidized SiO_2 as the gate dielectric. In order to obtain low fabrication temperatures of TFTs, both IZO and STA thin films were treated by the UV/O_3-assisted annealing. However, during the fabrication of IZO thin film, additional UV/O_3 treatment deteriorated the leakage current properties of the STA thin film. Thus, higher off-current and gate leakage current were found comparing the TFT fabricated by UV/O_3-assisted IZO and STA-700 thin films. Further improvement of the UV/O_3 conditions should be carried out in the future.

4.1 Previous reports of TFTs using high-k gate dielectrics

High operating voltages are often required to achieve high mobility and high

I_{on}/I_{off} for oxide TFTs, which increases power consumption in electronic circuits.[1-5] In addition to using high-mobility semiconductors, operating voltages can be reduced by developing gate dielectric materials capable of large capacitance densities with low leakage currents that have good compatibility for the growth of the semiconductor channel, leading to low trap densities at the semiconductor-gate dielectric interface.[1-5]

J. B. Kim *et al.* used an atomic layer deposition (ALD)-derived Al_2O_3 as the gate dielectric.[5] The obtained transfer characteristics of fabricated TFTs are shown in Fig. 4-1. By the use of Al_2O_3, operating voltage of lower than 5 V, threshold voltage (V_{th}) close to 0 V, and S of around 0.1 V were obtained. Other materials, such as sputtered (Ba,Sr)TiO_3,[1] plasma enhanced ALD-derived TiO_x,[3] and electron beam evaporation derived Ta_2O_5 were also studied.[6]

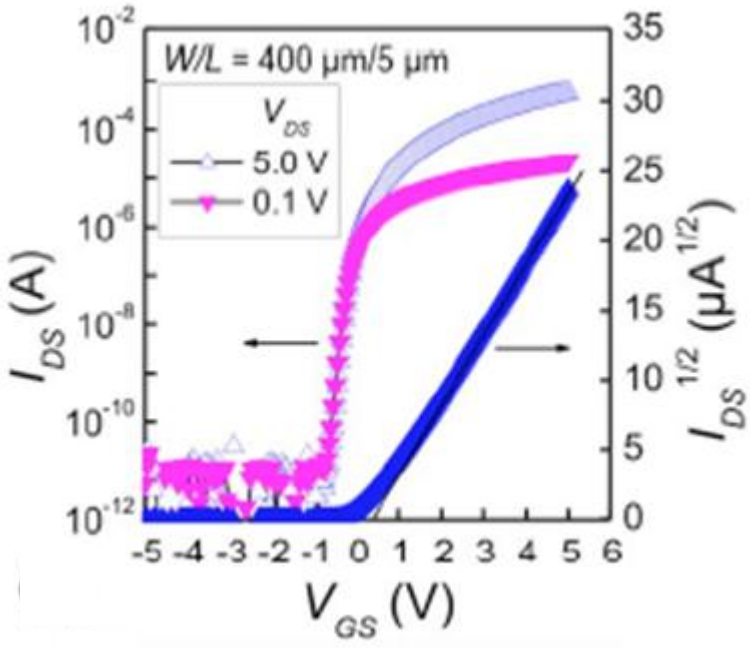


Fig. 4-1 Transfer characteristics of IGZO TFTs with the gate dielectric of ALD-derived Al_2O_3 thin film.[1]

4.2 Sputtered-IGZO TFTs using STA thin films as gate dielectrics

In chapter 2, the electrical properties of high-k materials of (Ba,Sr)Ta_2O_6 were

discussed. Among them, the STA thin film without Ba doping showed the highest dielectric constant (ε) and the lowest leakage current. Moreover, the STA-700 thin film showed the ε higher than many other high-k materials, better voltage stability and lower leakage current than other temperatures annealed STA thin films. Therefore, the STA-700 thin films were used as gate dielectrics of TFTs firstly.

However, the use of STA thin films as gate dielectrics of TFTs has not been reported until now. The compatibility of STA thin films with solution process derived IZO thin films is not clear. On the other hand, the research on sputtered-IGZO with other high-k materials has been researched a lot. Therefore, the effect of solution process-derived STA thin films as gate dielectrics was firstly investigated by sputtered-IGZO TFTs.

4.2.1 Characteristics of sputtered-IGZO TFT using the STA-700 thin film as the gate dielectric

On the low resistivity P^+-Si substrate, the STA thin film with thickness of about 100 nm was spin-coated and annealed at 700 ^oC for 1 h in O_2 atmosphere. Then, the amorphous IGZO (In : Ga : Zn=2 : 2 : 1 at. %) channel thin films were deposited on the STA thin film by radio frequency magnetron sputtering in a mixture atmosphere of Ar and O_2 (Ar:O_2= 19.1/0.9 sccm) at room temperature. Thicknesses of IGZO thin films were about 70 nm. In order to compare the properties, the thermally oxidized SiO_2 thin film was also used as the gate dielectric. The thickness of SiO_2 thin film was also about 100 nm. The channel width and length of fabricated TFTs were about 20 and 30 μm, respectively. Post-annealing at a temperature of 300 ^oC for 2 h in air atmosphere was carried out for fabricated TFTs.

Output characteristics of sputtered-IGZO TFTs with STA-700 and thermally oxidized SiO_2 thin films as gate dielectrics (sputtered-IGZO/STA-700 and sputtered-IGZO/SiO_2 TFTs, respectively), are shown in Fig. 4-2(a) and 4-2(b), respectively. Considering the practical device and the low-operating-voltage applications, the applied drain voltage (V_{ds}) was limited in a range of not higher than 5 V. The gate voltage (V_{gs}) was changed from 0 to 5 V to the sputtered-IGZO/STA-700 TFT. Good saturation and clear pinch off behaviors were found. Moreover, although the V_{gs} was as low as 5 V, the drain current (I_{ds}) was as high as 10^{-6} A at the V_{ds} of 5 V. Therefore, it was considered that the TFT with the STA-700 thin film as the gate dielectric was successfully fabricated. On the other hand, three orders lower I_{ds}, i.e. 10^{-9} A, was found while the applied V_{ds} and V_{gs} were 5 V for the sputtered-IGZO/SiO_2 TFT. Therefore, output curves were investigated until the applied V_{gs} reached 10 V, as shown in Fig. 4-2(b). However, the drain

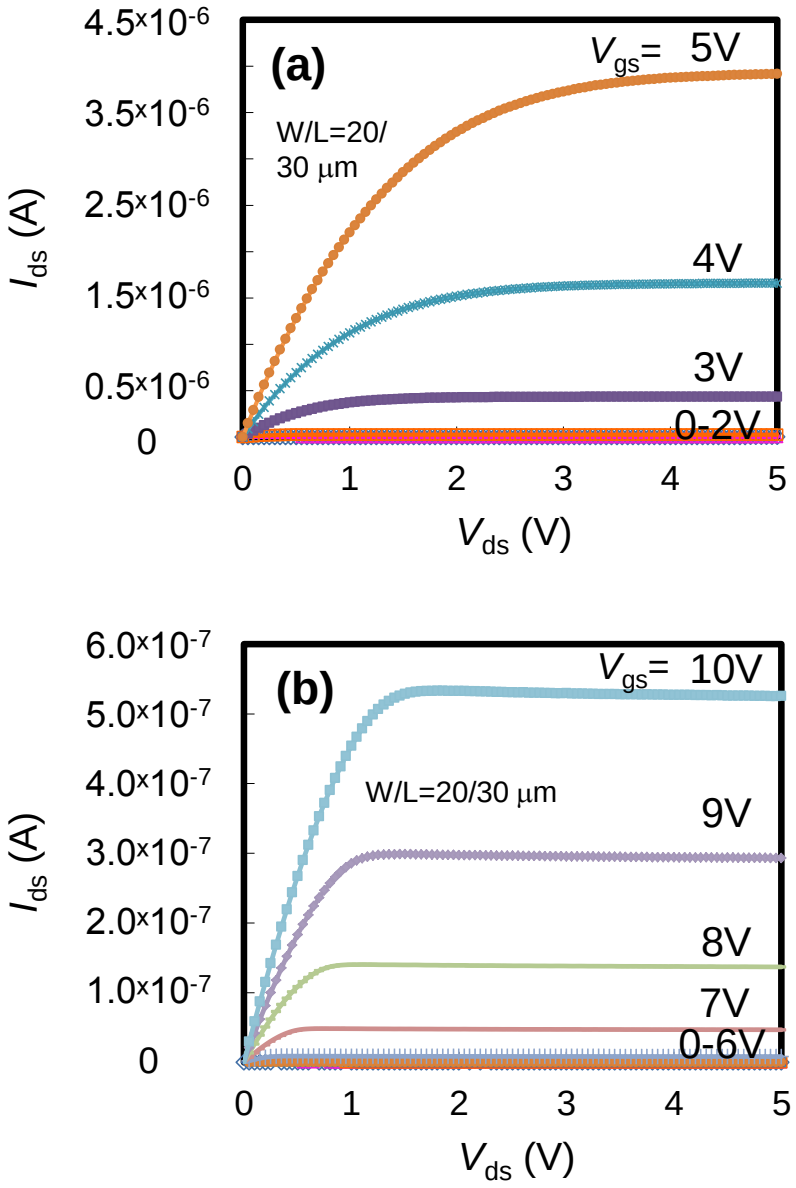


Fig. 4-2 Output characteristics of sputtered-IGZO TFTs with gate dielectrics of (a) STA-700 and (b) thermally oxidized SiO_2 thin films.

current still remained at a lower value of 10^{-7} A.

Transfer characteristics with the V_{ds} of 2 V are shown in Fig. 4-3 for sputtered-IGZO/STA-700 and sputtered-IGZO/SiO_2 TFTs. The V_{th} was 1.2 V and the I_{on}/I_{off} was 2.4×10^{7} at the V_{gs} of 5 V for the sputtered-IGZO/STA-700 TFT. A high μ_{FET} of about 4.8 $cm^2/(V\cdot s)$ was also obtained at the V_{gs} of 5 V. In particular, an extremely low S value of 0.07 V/decade was obtained. The value was very close to

the limit value of S for TFTs, 0.06 V/decade. However, for the sputtered-IGZO/SiO_2 TFT, no on-state was found at the V_{gs} of 5 V. The S value of 0.13 V/decade was also higher than that of the sputtered-IGZO/STA-700 TFT. The values of V_{th} and S of sputtered-IGZO/STA-700 were quite small relative to many other TFTs.[7-8] Thus, the STA-700 thin film was very effective for low-operating-voltage application of TFTs.

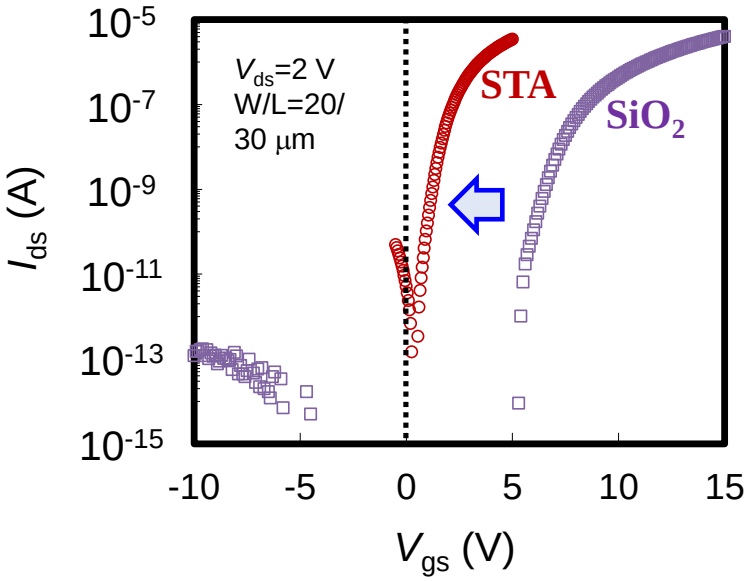


Fig. 4-3 Transfer characteristics at the applied V_{ds} of 2 V of sputtered-IGZO/STA-700 and sputtered-IGZO/SiO_2 TFTs.

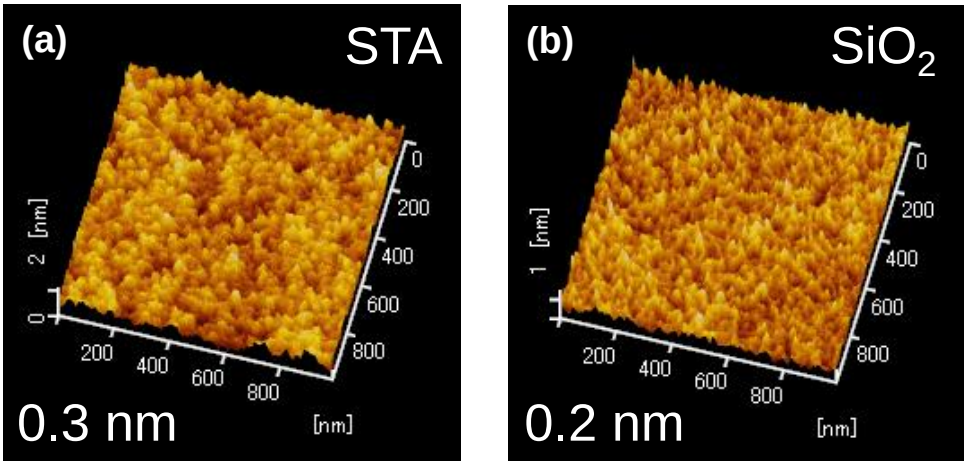


Fig. 4-4 Surface morphologies of (a) STA-700 and (b) thermally oxidized SiO_2 thin films.

In order to understand the extremely low *S* value, surface morphology of the STA-700 was investigated. Surface morphologies of STA and SiO_2 thin films are shown in Fig. 4-4(a) and 4-4(b), respectively. Since the STA-700 thin film was in amorphous state, it showed a low root mean square (RMS) surface roughness value of 0.3 nm. This value was almost the same to that of the thermally oxidized SiO_2 thin film, which was 0.2 nm. Therefore, a good interface characteristic of channel/gate dielectric was expected to be obtained in the sputtered-IGZO/STA-700 TFT.

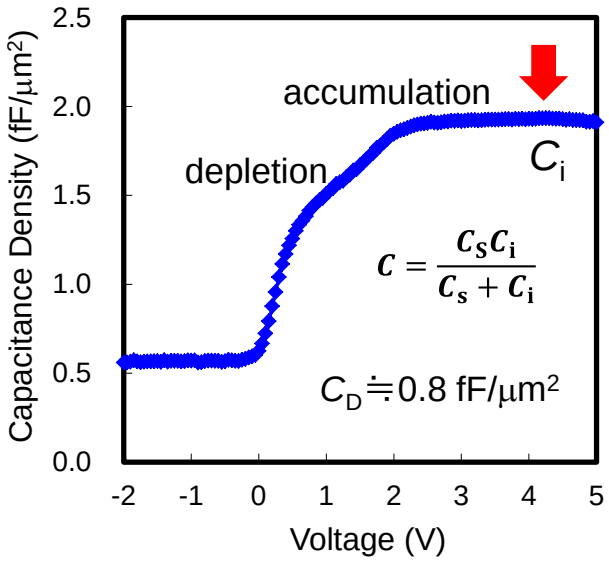


Fig. 4-5 *C-V* property of the Pt(10 nm)/Ti (90 nm)/IGZO/STA-700/Si capacitor. This structure was the same to that of the sputtered-IGZO/STA-700 TFT.

On the other hand, the *S* can also be approximately calculated using the following equation when there is no significant interface-trap density[9-10)]

$$S = \ln(10)\frac{kT}{q}\left(\frac{C_i + C_D}{C_i}\right), \tag{4-1}$$

where *k* is the Boltzmann's constant, *T* is the temperature, *q* is the electronic charge, C_i is the capacitance of the gate dielectric per unit area and C_D is the depletion-layer capacitance per unit area. In order to estimate the C_D, the capacitance-voltage (*C-V*) property of a capacitor with the same structure as the TFT, i.e., Pt(10 nm)/Ti (90 nm)/IGZO/STA-700/Si, was investigated. A high capacitance density of about 1.9

fF/μm^2 was obtained for the gate dielectric, as shown in Fig. 4-5. By using the equation of $C=(C_sC_i)/(C_s+C_i)$,[11] where C is the capacitance per unit area of the whole capacitor and C_s is the capacitance per unit area of the semiconductor, the C_D was estimated to be 0.8 fF/μm^2. According to the equation (4-1), the estimated S value was about 0.08 V/decade. It fitted well with the S value obtained from the transfer characteristic. Therefore, it was thought that the extremely low S value was resonable, and mainly resulted from the large capacitance density of the STA-700 thin film.[2, 10]

High μ_{FET} and I_{on}/I_{off} which were obtained at low gate and I_{ds} of 5 V, and the extremely low S of 0.07 V/decade suggested that the STA-700 was effective for the application of low-operating-voltage TFTs.

Since the leakage current property of a STA thin film which was annealed at 500 ^oC significantly improved by the UV/O_3 treatment (this was discussed in chapter 2, section 2.4), the application of STA-500UV/O_3 thin film as a gate dielectric of TFTs needed to be investigated for decreasing the fabrication temperature of TFTs.

4.2.2 Characteristics of sputtered-IGZO TFT using the STA-500UV/O_3 thin film as the gate dielectric

On the low resistivity P^+-Si substrate, STA-700 and STA-500UVO_3 thin films with thickness of about 150 nm were fabricated. Then, IGZO thin films with 70 nm were sputtered on these two thin films. The measured channel width and length of fabricated TFTs were about 500 and 50 μm, respectively. Transfer characteristics and gate leakage currents of these two TFTs which were measured at V_{ds} of 2 V are shown in Fig. 4-6. Almost same off-currents and on-currents were obtained. The S of the TFT using the STA-500UVO_3 thin film as the gate dielectric (sputtered-IGZO/STA-500UVO_3) was about 0.08 V/decade, which was a little larger than that of the sputtered-IGZO/STA-700 TFT. Since no obvious difference of RMS surface roughness was found for STA-700 and STA-500UVO_3 thin films, the slightly increased S might be due to the smaller ε of about 32 of the STA-500UVO_3 thin film. Although the value of 0.08 V/decade was a little larger than that of the sputtered-IGZO/STA-700 TFT, it was also extremely low. Moreover, extremely high μ_{FET} of about 173.4 and 237.4 cm^2/(V· s) were obtained through the improvement of fabrication process of sputtered-IGZO/STA-700 and sputtered-IGZO/STA-500UVO_3 TFTs, respectively. The sputtered-IGZO/STA-500UVO_3 TFT showed a higher μ_{FET}. This value was much higher than those of TFTs using other high-k materials as gate dielectrics.[12-15] These results suggested that the STA-500UVO_3 was also suitable for the application of low-operating-voltage TFTs, and the STA thin films have potential to provide high mobility through optimized processing.

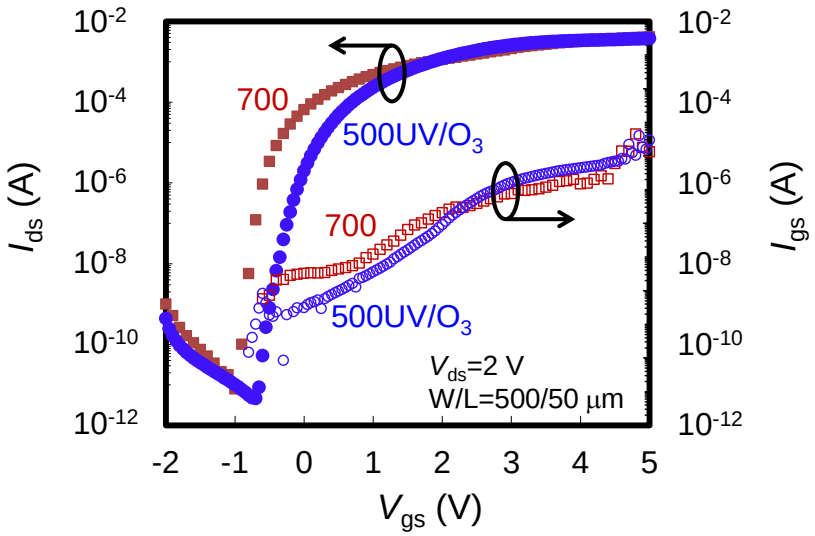


Fig. 4-6 Transfer characteristic of sputtered-IGZO TFTs using STA-700 and STA-500UVO$_3$ thin films as gate dielectrics.

The gate leakage current (I_{gs}) of the sputtered-IGZO/STA-500UVO$_3$ TFT was almost the same to that of the sputtered-IGZO/STA-700 TFT. In the on-region, I_{gs} did not contribute more than 0.1 % to the signal currents. These values were almost the same to that of the TFT using the sputtered amorphous $Ba_{0.5}Sr_{0.5}TiO_3$ thin film as the gate dielectric.[2)] These low leakage currents indicated that high quality STA thin films were fabricated and appropriate for the application of gate dielectrics.

STA thin films were proved to be effective for decreasing operating voltages of sputtered-IGZO TFTs. The UV/O_3-assisted annealing was also proved to be effective for decreasing the fabrication temperature. However, both channel layer and gate dielectric fabricated by solution process are rarely studied. Thus, the research on using solution-processed IZO and STA thin films were carried out.

4.3 Solution process-derived IZO TFTs using STA thin films as gate dielectrics

It was introduced in chapter 3 that high performance TFTs were fabricated using an aqueous solution derived-IZO thin films. Therefore, STA thin films were then used

as gate dielectrics for aqueous solution derived-IZO TFTs.

4.3.1 Aqueous solution-derived IZO TFTs using STA thin films as gate dielectrics

Firstly, the STA-700 thin film was used as the gate dielectric. On the STA-700 thin film deposited P^+-Si substrate, IZO aqueous solution was spin-coated and then annealed at 300 ^oC for 1 h on the hotplate (A-IZO300 thin film).

Obtained transfer characteristic of the A-IZO300/STA-700 TFT is shown in Fig. 4-7. The off-current was almost the same to the on-current. No switching characteristic was obtained. This characteristic was very similar to the leakage current property of a metal-insulator-metal capacitor. It suggested that A-IZO300 thin film was not well deposited on the STA-700 thin film. No switching characteristic of the A-IZO300/STA-500UVO$_3$ TFT was found, too. It was considered that the hydrophilicity of the STA thin film surface was not enough for the deposition of aqueous solution-derived thin film. Thus, organic solution-derived STA thin films were not suitable to be used as gate dielectrics of aqueous solution-derived IZO TFTs.

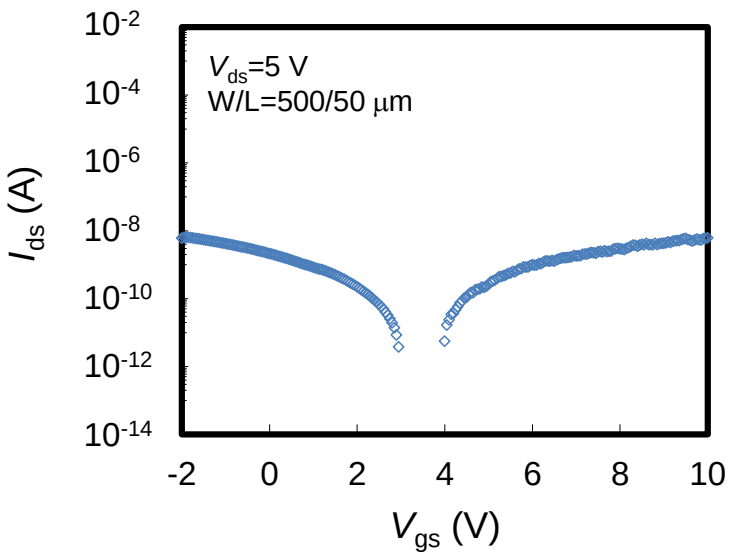


Fig. 4-7 The transfer characteristic of the A-IZO300/STA-700 TFT.

Although the aqueous solution was not easy to be deposited on organic solution-derived STA thin films, an organic solution was much easier to be deposited on them. Therefore, the application of STA thin films for the TFTs with organic solution-derived IZO thin films as channel layers needed to be investigated.

4.3.2 Organic solution-derived IZO TFT using the STA-700 thin film as the gate dielectric

It was introduced in chapter 3 that no off-state, i.e., intensively negatively shifted V_{th}, of the TFT with organic solution-derived IZO thin film which was annealed at 400 ^{o}C (IZO-400) as the channel layer and the thermally oxidized SiO_2 thin film as the gate dielectric was found. However, low fabrication temperature is necessary for the application of TFTs on glass and flexible substrates. Therefore, fabrication process of IZO-400 was improved. The annealing atmosphere was changed from normal air to dry air and the thickness was changed from 20 to 50 nm (IZO-400'). Switching characteristic was obtained through this improvement.

The output characteristic of the IZO-400'/SiO_2 TFT with the V_{gs} from 0 to 15 V were measured, as shown in Fig. 4-8(a). The width and length of measured TFTs were about 20 and 30 μm. Since a V_{ds} of about 10 V needed to saturate the TFT, the transfer characteristic in the saturation region with the V_{ds} of 10 V was measured, as shown in Fig. 4-8(b). The turn-on voltage (V_{on}) was found at -17 V and the I_{on}/I_{off} was 1×10^4 at the V_{gs} of 15 V. The calculated V_{th} was -5.8 V, S was 3.6 V/decade, and μ_{FET} was 0.02 $cm^2/(V\cdot s)$.

Then, the IZO-400' thin films were deposited on STA thin films. The STA-700 was also firstly used to investigate the effect of STA thin films. Output characteristic of the IZO-400'/STA-700 TFT is depicted in Fig. 4-9(a). The V_{gs} was changed from 0 to 5 V. Good saturation and clear pinch off behaviors were obtained, which suggests that the TFT using organic solution process-derived IZO and STA thin films was successfully fabricated. Compared with the IZO-400'/SiO_2 TFT, the IZO-400'/STA-700 TFT needs a lower V_{gs} to reach saturation. The transfer characteristic of the IZO-400'/STA-700 TFT with the V_{ds} of 2 V is shown in Fig. 4-9 (b). The V_{on} was -1.2 V and the I_{on}/I_{off} was 5×10^6 at the V_{gs} of 5 V. The I_{gs} versus V_{gs} property is shown in the insert figure of Fig. 4-9(b). Low leakage current (< 0.1% of the I_{on}) was also obtained, which suggested that the organic solution-derived IZO and STA thin films have good compatibility.

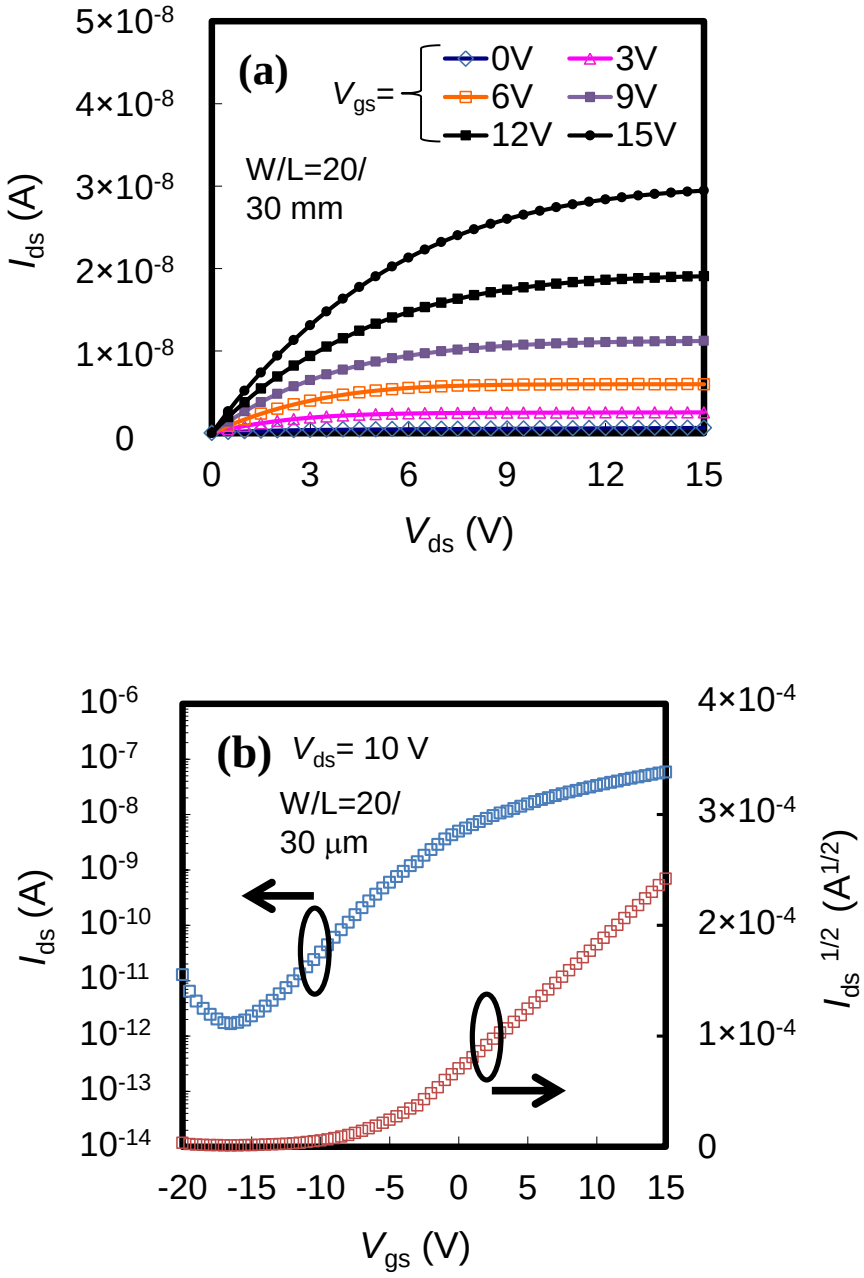


Fig. 4-8 (a) The output characteristic of the IZO-400'/SiO_2 TFT and (b) the transfer characteristic of the IZO-400'/SiO_2 TFT at the V_{ds} of 10 V.

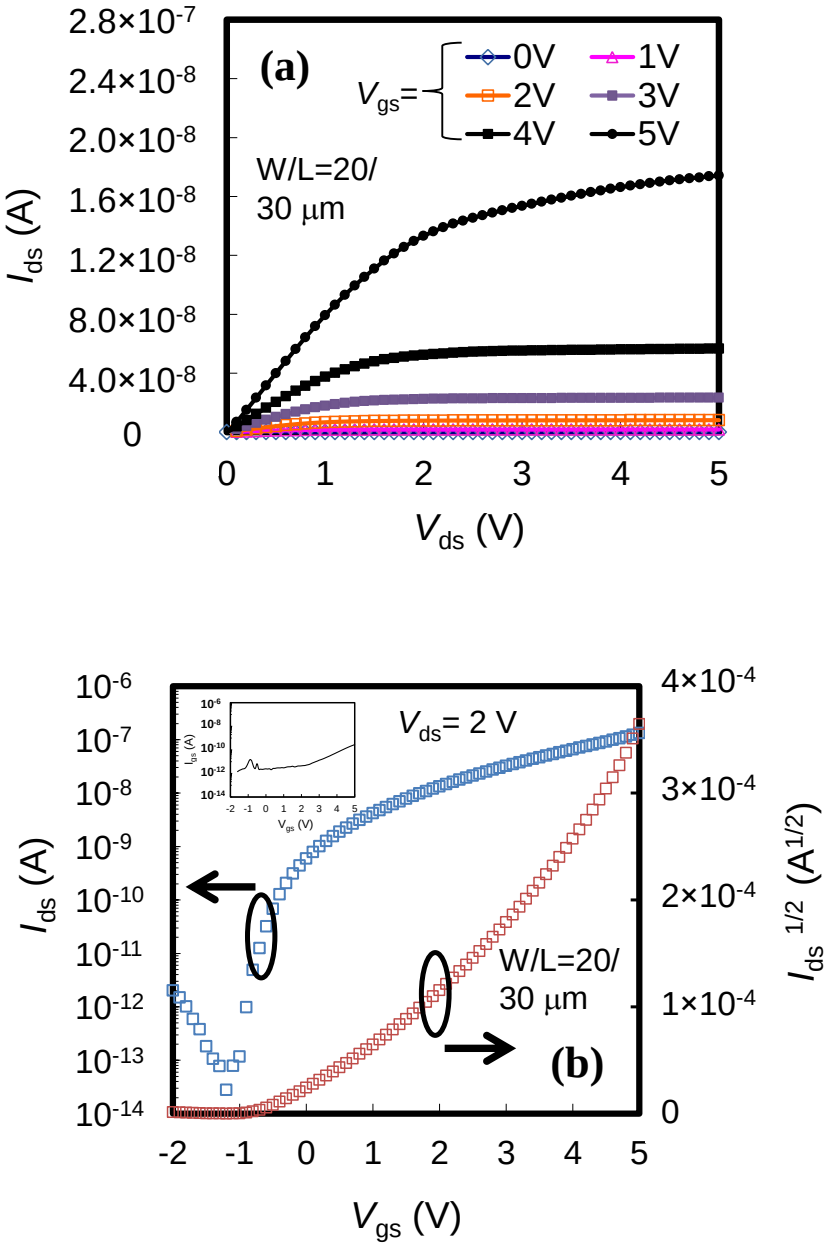


Fig. 4-9 (a) The output characteristic of the IZO-400'/STA-700 TFT and (b) the transfer characteristic of the IZO-400'/STA-700 TFT at the V_{ds} of 2 V.

The V_{th} and μ_{FET} of the IZO-400'/STA-700 TFT were 0.8 V and 0.24 $cm^2/(V\cdot s)$ at the V_{gs} of 5 V, respectively. The S was also about 0.08 V/decade. All of the parameters were improved by the use of the STA-700 as the gate dielectric. However, the μ_{FET} of 0.24 $cm^2/(V\cdot s)$ was smaller than that of the sputtered-IGZO/STA-700 TFT, and too small for the application of flat-panel display.[16] Even though the μ_{FET} of the IZO-400'/STA-700 was low, it still increased 10 times compared with that of the IZO-400'/SiO_2 TFT. Therefore, the main reason of these two low mobility was thought to be due to the poor quality of the IZO-400' thin film.

Same mobility value of the solution process-derived IZO/SiO_2 TFT with the same composition of In:Zn ratio was reported in ref. 17. They stated that in an In-rich composition, the charge carrier were abundant, causing scattering, which reduced the mobility. Therefore, in order to certify the scattering effect in the IZO-400' thin film, the mean free path (l) was evaluated using the following equation[18-21]

$$l = \frac{h}{2q}\left(\frac{3N}{\pi}\right)^{1/3}\mu_H \qquad (4\text{-}2)$$

where, h is the Plank's constant, q is the electron charge, N is the carrier concentration, and μ_H is the hall mobility. In the IZO-400' thin film, not only the carrier scattering, but also two other kinds of scattering should be considered. One was the grain boundary scattering,[18-23] because the XRD result showed the IZO-400' thin film crystallized. Another was the scattering of impurities, such as C and H. In solution process-derived thin films, the impurities of C and H which remain from the organic solution are hard to be completely eliminated, even though the annealing temperature is higher than the pyrolysis temperature.[24] These impurities could be the origin of the scattering or the traps which prevent the accumulating of carriers to form a sufficient conductive path, thus leading to low on-current and low mobility. This was also discussed in chapter 3. It is expected that the N and μ_H in the IZO-400' thin film were the same as reported in ref. 17. The calculated mean free paths was about 0.0015 nm, which was much smaller than the grain size of about 22 nm estimated from the XRD result using the Scherrer's equation[18, 21]: $t=K\lambda/\beta\cos\theta$, where t is the grain size, K is a shape factor with a typical value of 0.9, λ is the X-ray wavelength, θ is the diffraction angle, and β is the full width at half maximum intensity (FWHM) in radians. Thus, the grain boundary scattering effect could be ignored.[18-21] Meanwhile, it was thought that the N[17] of 6.7×10^{15} cm^{-3} was not high enough for scattering, because in many reports the carrier concentration of IZO thin films, derived from other fabrication methods showed much higher values of 10^{19}-10^{20} cm^{-3}, and the TFTs showed high mobility of larger than 30 $cm^2/V\cdot s$.[25-27]

Therefore, the main obstacle of the mobility might be the impurities of C and H.

Depthwise profiles of C and H in IZO-400'/SiO_2 and IZO-400'/STA-700 structures are compared in Fig. 4-10(a) and 4-10(b), respectively. Less C and H were found in the IZO-400' thin film with the gate dielectric of STA-700. As it was discussed above, the IZO-400'/STA TFT showed much higher mobility. Thus, these impurities were the main reason of the low mobility. Compared with the SiO_2 thin film, more oxygen ions existed in the STA-700 thin film and these oxygen ions diffused into the IZO-400' thin film through annealing. The C and H ions in the IZO-400' thin film combined with the diffused oxygen ions and escaped from the IZO-400' thin film to the atmosphere. Thus, the concentration of impurities decreased in the IZO-400' thin film when the gate insulator was STA and a higher mobility was obtained. This result suggests that an oxide high-k material like STA was effective for the performance improvement when the channel layer was fabricated by solution process. A higher mobility is expected to be achieved by optimizing the property of IZO thin film.

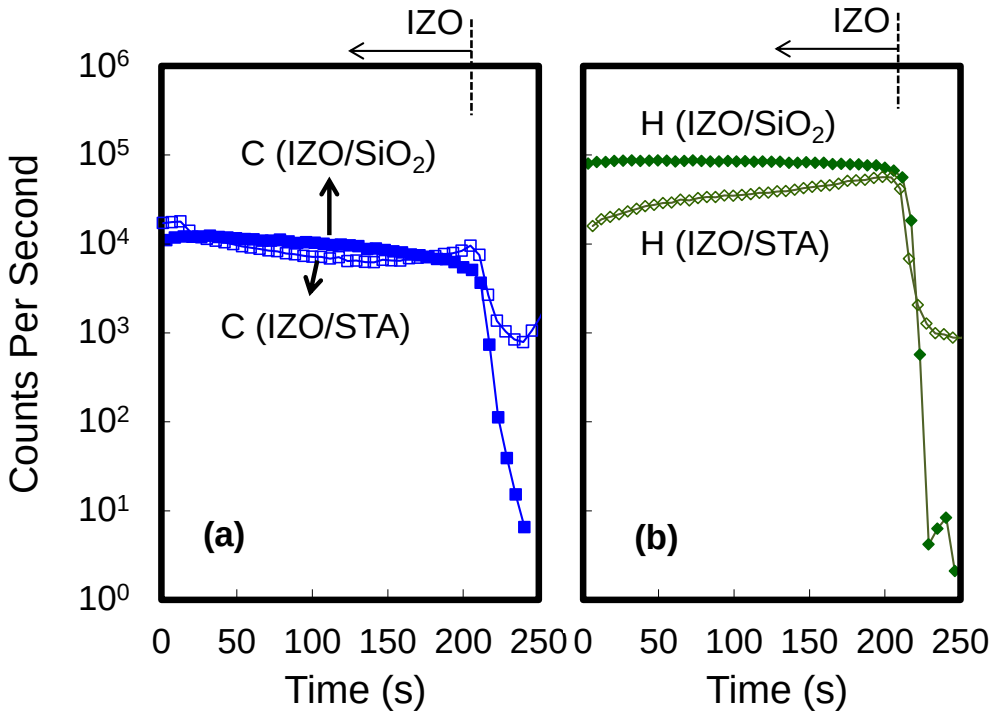


Fig. 4-10 SIMS profiles of (a) C and (b) H in IZO-400' thin films with gate dielectrics of SiO_2 and STA-700.

In chapter 3, it was introduced that the TFT using the IZO thin film fabricated at 290 ^{o}C with UV/O_3-assisted-annealing (IZO-290UVO_3) as the gate dielectric showed the same mobility to that of the TFT using the IZO thin film fabricated at 700 ^{o}C without UV/O_3-assisted-annealing as the gate dielectric. On the other hand, the sputtered-IGZO/STA-500UV/O_3 TFT showed almost same property to that of the sputtered-IGZO/STA-700 TFT. Therefore, TFTs using IZO-290UVO_3 thin films as channel layers, STA-700 and STA-500UV/O_3 as gate dielectrics were fabricated.

4.3.3 TFTs fabricated by UV/O_3-assisted-annealed IZO and STA thin films

The STA-700 and STA-500UV/O_3 thin films were fabricated on the P^+-Si substrates. Then, IZO-290UVO_3 thin films were fabricated on the STA thin films.

Transfer characteristics of these two TFTs are shown in Fig. 4-11. Both TFTs showed switching characteristics in the range of V_{gs} lower than 5 V. obtained μ_{FET} were both higher than 200 $cm^2/(V\cdot s)$. These results showed that the fabrication temperature of TFTs with solution process-derived IZO and STA thin films could be

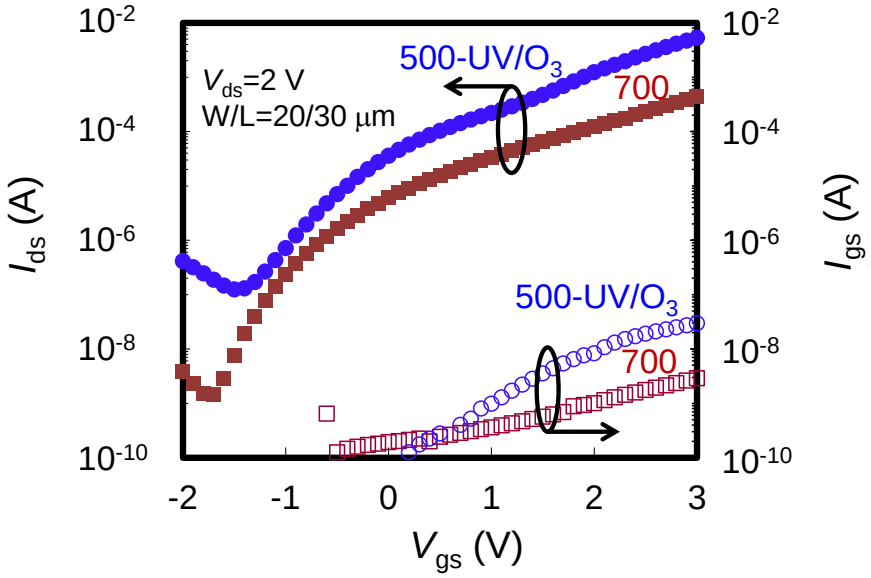


Fig. 4-11 Transfer characteristics and I_{gs} properties of IZO-290UVO_3/STA-700 and IZO-290UVO_3/STA-500UV/O_3 TFTs.

effectively decreased by UV/O_3-assisted-annealing. However, the IZO-290UVO_3/STA-700 TFT showed lower off-current and lower gate leakage current than those of the IZO-290UVO_3/STA-500UVO_3 TFT. This was not the same to that of the sputtered-IGZO/STA TFTs. It was considered that the UV/O_3-assisted annealing of IZO thin films damaged STA thin films, thus, a worse leakage current property was obtained.

4.4 Conclusion

The STA-700 thin film was used as the gate dielectric of the sputtered-IGZO TFT in order to understand the effect of STA thin films. A high μ_{FET} of 4.8 $cm^2/(V\cdot s)$ and I_{on}/I_{off} of 2.4×10^7 were obtained at low V_{ds} and V_{gs} of 5 V for the sputtered-IGZO/STA-700 TFT. Meanwhile, a low V_{th} of 1.7 V and an extremely low S of 0.07 V/decade were also obtained. The high ε and good surface morphology of the STA-700 thin film were considered to contribute to this extremely low S.

The sputtered-IGZO/STA-500UV/O_3 TFT showed almost same transfer characteristic and gate leakage current to those of the sputtered-IGZO/STA-700 TFT. Extremely high μ_{FET} of 173.4 and 237.4 $cm^2/(V\cdot s)$ were obtained by the use of STA-700 and STA-500UVO_3 as gate dielectrics, respectively, through the improvement of fabrication process. It suggested that the STA-500UV/O_3 was also suitable for the low-operating-voltage application. The fabrication temperature of TFTs was decreased by the UV/O_3-assisted annealing.

However, because of the incompatibility of the aqueous solution with the organic solution derived-STA thin film, no switching characteristic was found for A-IZO300/STA TFTs.

On the other hand, organic solution-derived IZO thin films were well fabricated on STA thin films. For the IZO-400'/STA-700 TFT, good pinch off characteristic and saturation state were obtained. This suggested that TFTs using solution process-derived semiconductor channel and gate dielectric layers were successfully fabricated. A low V_{on} of -1.2 V, a low V_{th} of 0.8 V, a very low S of 0.08 V/decade and a high I_{on}/I_{off} of 5×10^6 were also obtained at V_{ds} and V_{gs} of 5 V. However, a relatively low μ_{FET} of 0.24 $cm^2/(V\cdot s)$ was also obtained, it was much lower than that of the sputtered-IGZO/STA-700 TFT. High concentrations of organic impurities of C and H remained in the IZO-400' thin film, which induced low μ_{FET}.

In order to decrease the fabrication temperature of TFTs using organic solution-derived IZO and STA thin films. The UV/O_3-assisted annealing was carried out for both of these two thin films. However, the IZO-290UVO_3/STA-700 TFT showed lower I_{gs} than that of the IZO-290UVO_3/STA-500UV/O_3 TFT. The UV/O_3-assisted annealing of IZO thin films

deteriorated properties of the STA thin film, subsequently induced higher I_{gs}.

These results indicated that STA thin films were effective for low-operating-voltage applications of TFTs using both vacuum and solution processes-derived oxide semiconductor as channel layers. However, there still remained some problems should be solved: (1) improve the hydrophilicity of STA thin films for the deposition of aqueous solution-derived IZO thin films; (2) improve the quality of organic solution-derived IZO thin films, and (3) optimize the UV/O_3-annealing condition for the combination of IZO and STA thin films.

[References]

1) J. Siddiqui, E. Cagin, D. Chen, and J. D. Phillips: Appl. Phys. Lett. **88** (2006) 212903

2) J. B. Kim, C. F-Hernandez, and B. Kippelen: Appl. Phys. Lett. **93** (2008) 242111

3) J.-S. Park, J. K. Jeong, Y.-G. Mo, and S. Kim: Appl. Phys. Lett. **94** (2009) 042105

4) J.-M. Lee, I.-T. Cho, J.-H. Lee, W.-S. Cheong, C.-S. Hwang, and H.-I. Kwon: Appl. Phys. Lett. **94** (2009) 222112

5) J. B. Kim, C. F.-Hernandez, W. J. Potscavage, Jr., X.-H. Zhang, and B. Kippelen: Appl. Phys. Lett. **94** (2009) 142107

6) C. Bartic, H. Jansen, A. Campitelli, and S. Borghs: Organic Electronics **3** (2002) 65

7) C. G. Choi, S-J. Seo, and B-S. Bae: Electrochem. Solid-State Lett. **11** (2008) H7

8) S. J. Kim, G. H. Kim, D. L. Kim, D. N. Kim, and H. J. Kim: Phys. Status Solidi A **207** (2010) 1668

9) S. M. Sze and K. K. NG: Physics of Semiconductor Devices (3rd ed.) (John wiley & Sons, Inc., Hoboken, 2007) P. 315.

10) M. F. Chang, P.T. Lee, S. P. McAlister, and A. Chin, IEEE Electron Device Lett. **29** (2008) 215.

11) S. M. Sze and K. K. NG, Physics of Semiconductor Devices (3rd ed.), published by John wiley & Sons, Inc., Hoboken, 2007, P. 204.

12) N. C. Su, S. J. Wang, A. Chin: IEEE Electron Device Lett. **30** (2009) 1317

13) J. S. Lee, S. Chang, S.-M. Koo, S. Y. Lee: IEEE Electron Device Lett. **31** (2010) 225

14) C. J. Chiu, S. P. Chang, S. J. Chang: IEEE Electron Device Lett. **31** (2010) 1245

15) F. H. Chen, J. L. Her, Y. H. Shao, Y. H. Matsuda, T. M. Pan: Nanoscale Res. Lett. **8** (2013) 18

16) M.-C. Hung, H.-T. Hsiao, W.-T. Lin, C.-H. Tu, J.-J. Chang, and P.-L. Chen: Jpn. J. Appl. Phys. **50** (2011) 03CB07

17) C. Y. Koo, K. Song, T. Jun, D. Kim, Y. Jeong, S.-H. Kim, J. Ha, and J. Moon: J. Electron. Soc. **157** (2010) J111

18) G. Sanon, R. Rup, and A. Mansingh: Thin Solid Films **190** (1990) 287

19) A. K. Saxena, S. P. Singh, R. Thangaraj, and O. P. Agnihotri: Thin Solid Films **117** (1984) 95

20) J. J. Prince, S. Ramamurthy, B. Subramanian, C. Sanjeeviraja, and M. Jayachandran: J. Crys. Growth **240** (2002) 142

21) B. Kumar, H. Gong, N. N. Gosvami, R. Akkipeddi, and S. J. O'shea: Appl. Phys. Lett. **88** (2006) 093111

22) S. Jeong, Y. Jeong, and J. Moon: J. Phys. Chem. Lett. **112** (2008) 11082
23) Z. Yuan, X. Zhu, X. Wang, X. Cai, B. Zhang, D. Qiu, and H. Wu: Thin Solid Films **519** (2011) 3254
24) D. B. Haddow, P. F. James, and R. Vannoort: J. Mater. Sci. – Mater. Med. **7** (1996) 255
25) D. C. Paine, B. Yaglioglu, Z. Beiley, and S. Lee: Thin Solid Films **516** (2008) 5894
26) E. Fortunato, P. Barquinha, A. Pimentel, L. Pereira, G. Goncalves, and R. Martins: Phys. Stat. Sol. **1** (2007) R34
27) B. Yaglioglu, H. Y. Yeom, R. Beresford, and D. C. Paine: Appl. Phys. Lett. **89** (2006) 062103

Chapter 5

Gate voltage stress instability of aqueous solution-derived InZnO TFTs

It was introduced in chapter 3 that high performance thin film transistors (TFTs) using aqueous solution-derived InZnO (IZO) thin films which were annealed at a low temperature of 300 ^{o}C as channel layers and thermally oxidized SiO_2 thin films as gate dielectrics were fabricated. For practical applications, the stability under long term gate voltage (V_{gs}) stress should be guaranteed.[1-8] Therefore, the variations of transfer characteristics of these TFTs when gate voltage stress applied were investigated. The threshold voltage (V_{th}) moved to the positive V_{gs} direction, i.e., positively shifted, when a positive gate voltage stress applied. This positive shift was considered mainly due to the adsorption of O_2 from the ambient atmosphere at the back-channel region of the IZO TFT. In order to improve the gate voltage instability, TFTs were passivated by atomic layer deposition (ALD)-derived Al_2O_3 thin films. Less shift of V_{th} was found after the passivation.

5.1 Gate voltage stress instability and improvement

5.1.1 Mechanism of gate voltage stress instability

In the case of amorphous Si TFTs, the device instability under gate voltage stress has been attributed to two different mechanisms: charge trapping in the gate dielectric or the creation of metastable dangling-bond states in amorphous Si.[2-3] Based on these models, the V_{th} instabilities of oxide transistors have mainly been attributed solely to the charge trapping at or near the oxide channel layer and gate dielectric.[2-5] However, O_2 and H_2O in the ambient atmosphere are known to affect the oxide transistor properties, the voltage stress instability of oxide TFTs is also considered to be affected by the external molecules adsorption/desorption from the ambient atmosphere to oxide channel layer.[2-6] In particular, for an inverted staggered structure TFTs, i.e., bottom-gated TFTs which were used in this research, the effect of O_2 and H_2O onto the exposed back-channel region might play more important roles during gate voltage stress applied.

Song *et al.* reported that amorphous InGaZnO thin film transistors were sensitive to O_2 molecules.[1] For adsorption effect study, the controlled amount of O_2 was

introduced into the measurement chamber through mass flow controller and O_2 pressure was monitored by pressure gauges. They found that when O_2 was introduced into the chamber, the transfer curves systematically positively shifted, as shown in Fig. 5-1.

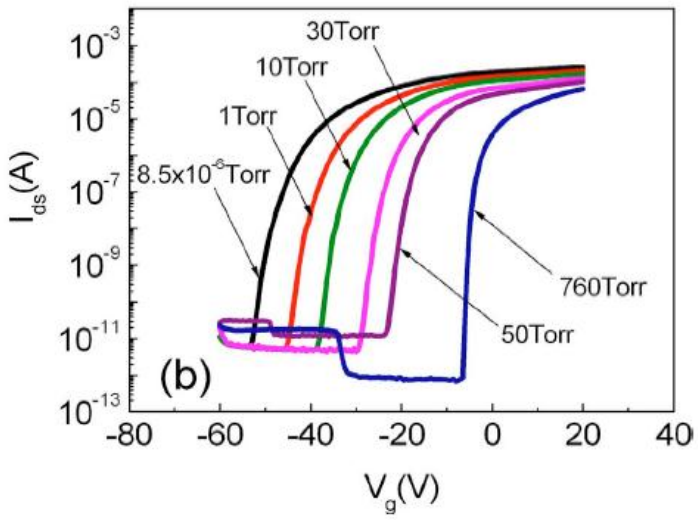


Fig. 5-1 Transfer curves when the O_2 increased from 8.5×10^{-6} to 70 Torr.[1)]

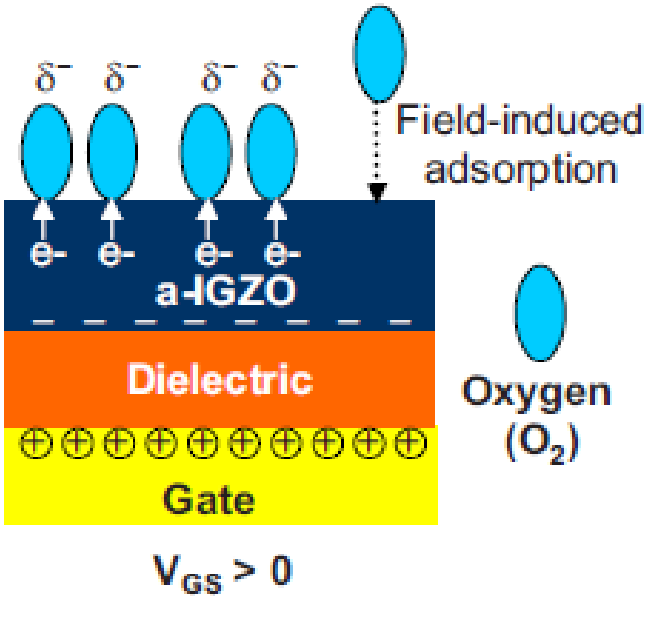


Fig. 5-2 Schematic showing the electric-field-induced adsorption of O_2 molecules from the ambient atmosphere under the application of positive gate voltage stress.[2)]

Jeong *et al.* also found that O_2 was adsorbed on the InGaZnO surface under the positive gate voltage stress and pointed out that it is largely responsible for the observed positive V_{th} shift. Owing to this, they suggested a model,[2)] which is schematically shown in Fig. 5-2, that the adsorbed oxygen can capture an electron (e) from the conduction band and that the resulting oxygen species can exist in various forms such as O^{2-} or O^{-}, as described by the following chemical reaction

$$O_2 \text{ (gas)} + e^{-} = 2O^{-} \text{ (solid)}. \qquad (5\text{-}1)$$

As a result of charge transfer, a depletion layer was formed beneath the InGaZnO thin film surface, leading to an positively shifted V_{th} of the TFT.

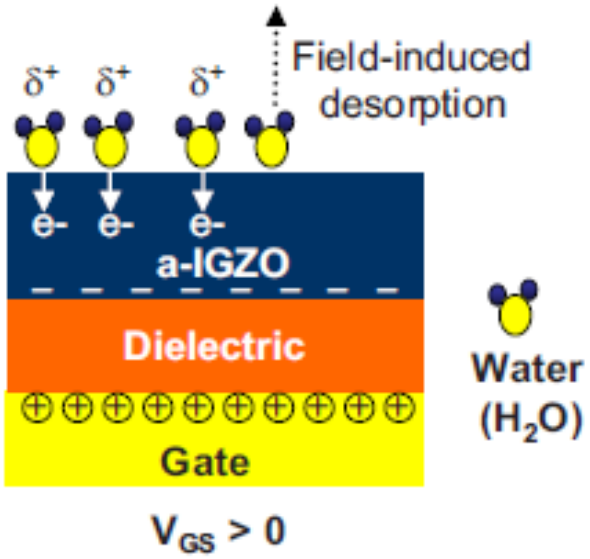


Fig. 5-3 Schematic showing the electric-field-induced desorption of water molecules into the ambient atmosphere under the application of positive gate voltage stress.[2-3)]

On the contrary, the adsorbed H_2O molecules induced a reverse behavior to the adsorbed O_2 molecules, i.e., the V_{th} moved to the negative V_{gs} direction, suggesting that the role of the adsorbed H_2O molecules seemed to form an accumulation layer below the semiconductor thin film surface, as shown in Fig. 5-3.[2-3)]

5.1.2 Improvement of gate voltage stress instability by passivation

It was reported by many researchers that the passivation of back-channel region is effective to improve the gate voltage stress instability.[2, 5-6)] As shown in Fig. 5-4,

the shift of V_{th} (ΔV_{th}) significantly decreased by the passivation of SiO_x and dense SiO_x thin films.[2] In particular, almost no ΔV_{th} was found by the passivation of the dense SiO_x thin film. However, the ΔV_{th} inversely increased after the passivation of an organic photoacryl (PA) thin film. These results suggested that an appropriate passivation thin film with high quality is very important to improve gate voltage stress instability.

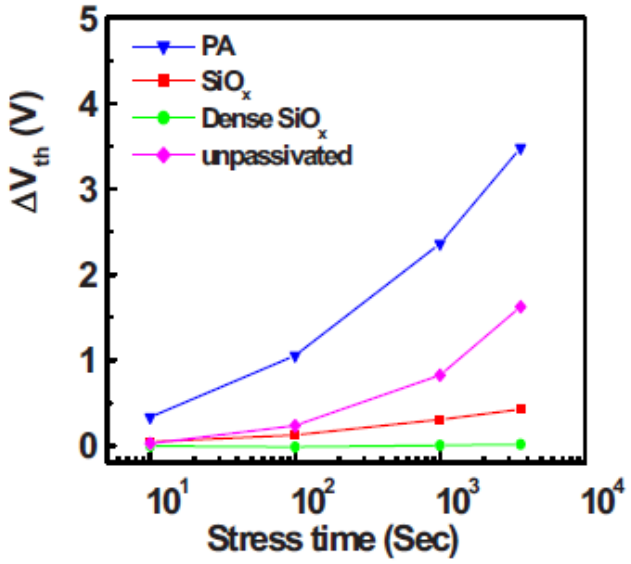


Fig. 5-4 Improvement of the V_{th} under positive gate voltage stress by the passivation of the back-channel region using various passivation materials.[2]

5.2 Gate voltage stress instability of aqueous solution-derived IZO TFTs

The instability evaluation under positive gate voltage and negative gate voltage ($-V_{gs}$) stresses of TFTs which were fabricated by the aqueous solution derived IZO thin films were firstly carried out. In this chapter, the gate dielectrics of TFTs were thermally oxidized SiO_2 thin films. The values of applied voltages were 20 V. They were continuous applied on TFTs for 1000 s. The drain voltages (V_{ds}) were kept at 5 V. The variations of transfer curves over time are shown in Fig. 5-5. A large positive shift of transfer curve was found when positive gate voltage stress applied on the TFT for 1000 s (Fig. 5-5(a)). The positively shifted ΔV_{th} value was 3.4 V after 1000 s. It was introduced in previous part that the adsorption of O_2 molecule generated positively shifted ΔV_{th} and the adsorption of H_2O molecule generated negatively shifted ΔV_{th}. Therefore, the positively shifted ΔV_{th} of aqueous solution derived IZO

TFTs might be mainly attributed to the adsorption of O_2 molecules.

Under the negative gate voltage stress, almost no shift was found after 1000 s (Fig. 5-5(b)). This result was the same to other vacuum process fabricated oxide TFTs. It was due to the depletion of carriers in the channel layer.[8)]

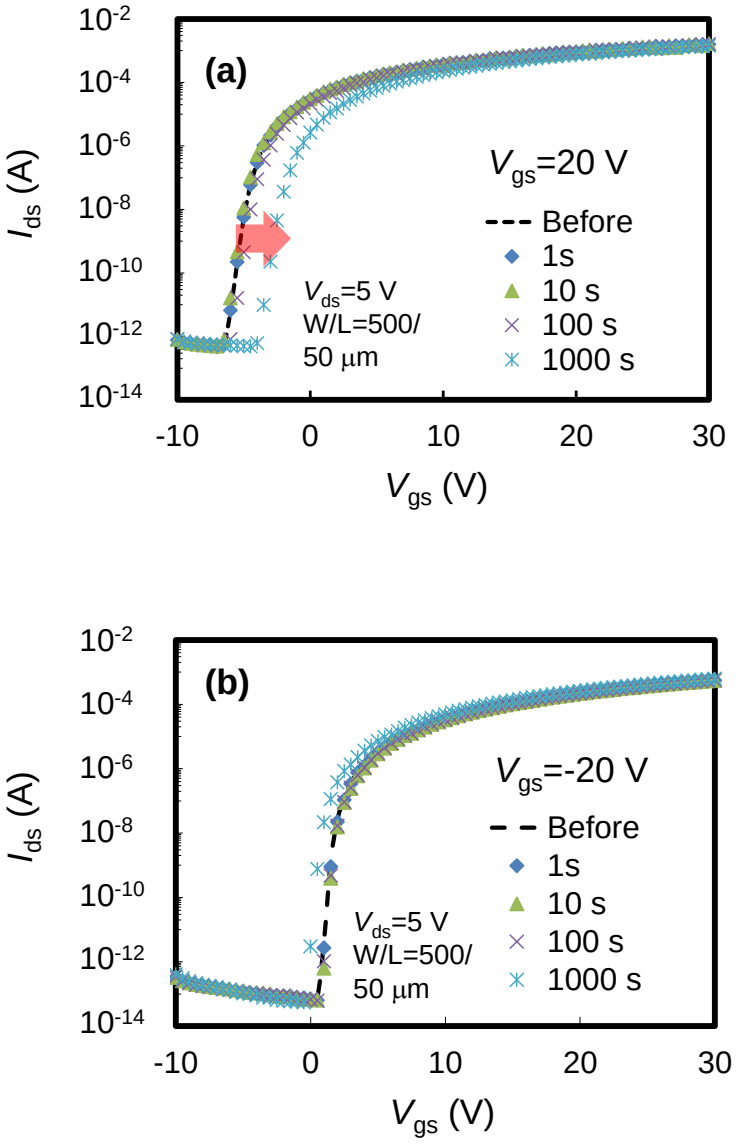


Fig. 5-5 Variation of transfer characteristics under (a) positive and (b) negative gate voltage stresses of 20 V for 1000 s.

In order to improve the positive gate voltage stress instability, a passivation layer was fabricated onto the back-channel region of IZO TFTs.

5.3 Improvement of gate voltage stress instability by the passivation of ALD-derived Al_2O_3 thin films

ALD is a self-limiting method that the amount of film material deposited in each reaction cycle is constant. Due to the characteristics of self-limiting and surface reactions, ALD film growth makes atomic scale deposition control possible. Fabricated films are extremely conformal and uniform in thickness.[10-12] High quality and dense thin films are expected to be fabricated. Therefore, ALD deposited Al_2O_3 thin films were used as the passivation layers in this research.

5.3.1 Fabrication of Al_2O_3 thin films by ALD method

Trimethyl-aluminium was used as the metal precursors to prepare Al_2O_3 thin films. Two kinds of oxidizer were used. One was a conventional O_3 gas (the fabricated Al_2O_3 thin film will be abbreviated as O_3-Al_2O_3 thin film), another one was oxygen radical (O*) which was generated from O_2 by a plasma-assisted treatment (the fabricated Al_2O_3 thin film will be abbreviated as PA-Al_2O_3 thin film). The growth of material layers by ALD consisted of repeating the following characteristic four steps (as shown in Fig. 5-6):

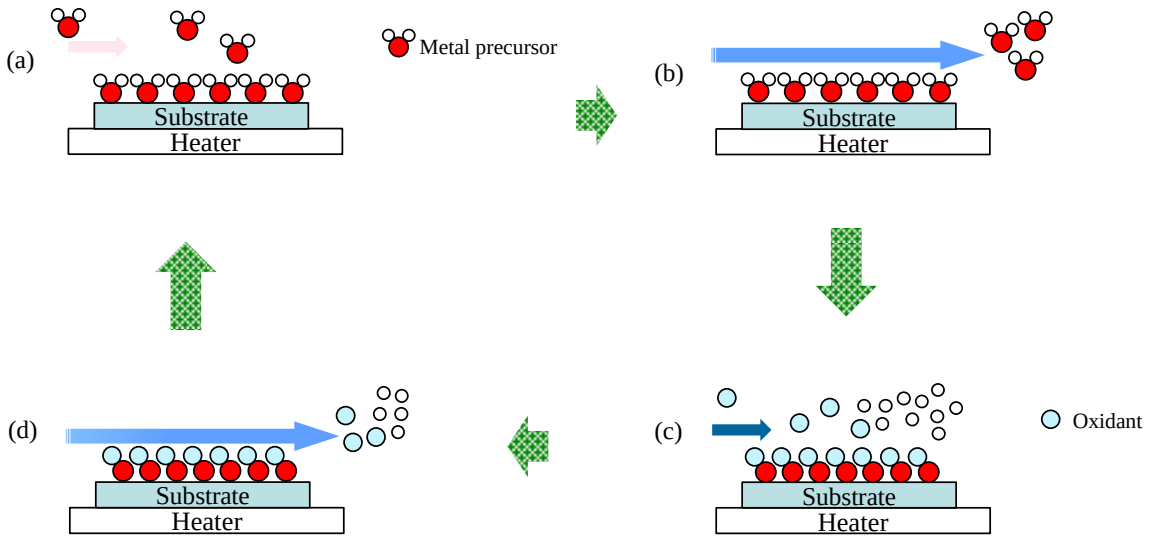


Fig. 5-6 Schematic diagram of ALD process.

a. Exposure of the precursor trimethyl-aluminium in the chamber.
b. Purge or evacuation of the reaction chamber to remove the non-reacted precursors and the gaseous reaction by-products.
c. Exposure of the oxidizers: O_3 gas or O_2 gas assisted by plasma (the O* was generated in the chamber).
d. Purge the reaction chamber.

Each reaction cycle added a given amount of material to the surface. During the growth of Al_2O_3 layer, the substrates, on which IZO TFTs were fabricated, were heated to an enough temperature to enhance chemical reaction on the surface. Reaction cycles were repeated as many as required for the desired film thickness. One cycle took time of a few seconds and deposited about 1 Å of film thickness.

5.3.2 Characteristics of TFTs passivated by O_3-Al_2O_3 and PA-Al_2O_3 thin films

Using an O_3 gas to fabricate thin films is very common for ALD deposition. However, it was reported in previous work that less impurities of carbon (C) and hydrogen (H) remained in the PA-Al_2O_3 thin films because the residual C and H were sufficiently oxidized even though at low fabrication temperatures by active O*.[10-11] High quality Al_2O_3 thin films were expected to be fabricated by a plasma-assisted ALD method.[10-11] Therefore, in this research, in addition to conventional O_3-Al_2O_3

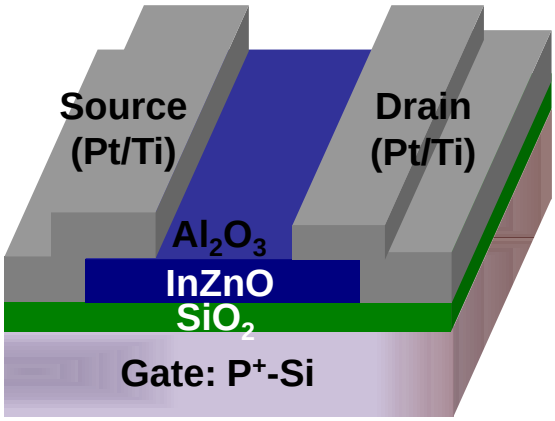


Fig. 5-7 Schematic diagram of Al_2O_3 thin film passivated TFTs.

thin films, PA-Al_2O_3 thin films were also deposited as passivation layers of IZO TFTs. Both of O_3-Al_2O_3 and PA-Al_2O_3, film thicknesses were about 50 nm. A low heating temperature of 100 ^oC was used to deposit these thin films. The schematic structure of passivated TFTs is shown in Fig. 5-7.

Transfer characteristics of TFTs which were unpassivated, passivated by O_3-Al_2O_3 and PA-Al_2O_3 thin films are shown in Fig. 5-8. No obvious change of transfer characteristic was found after the passivation of O_3-Al_2O_3 thin film except an order of magnitude decrease in off-current. In the PA-Al_2O_3 passivated TFTs, a decreased off-current was also found. However, the V_{th} significantly positively shifted.

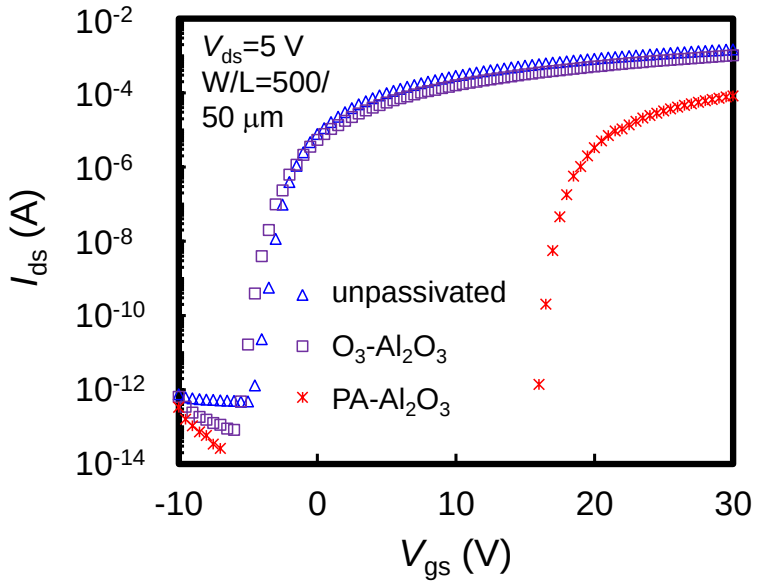


Fig. 5-8 Transfer characteristics of unpassivated, O_3-Al_2O_3 and PA-Al_2O_3 thin films passivated TFTs.

Output and transfer characteristics of the PA-Al_2O_3 passivated TFT are shown in Fig. 5-9(a), 5-9(b) (V_{ds}=0.1 V) and 5-9(c) (V_{ds}=5 V), respectively. Abnormal output characteristics were observed. All the output curves were divided into two parts: low V_{ds} region and high V_{ds} region. The drain currents (I_{ds}) firstly increased as V_{ds} increased until it reached a saturation state in the low V_{ds} region. And then, the increase and saturation phenomenon occurred again in the high V_{ds} region. Transfer characteristics with hysteresis behaviors which correspond to these two regions are

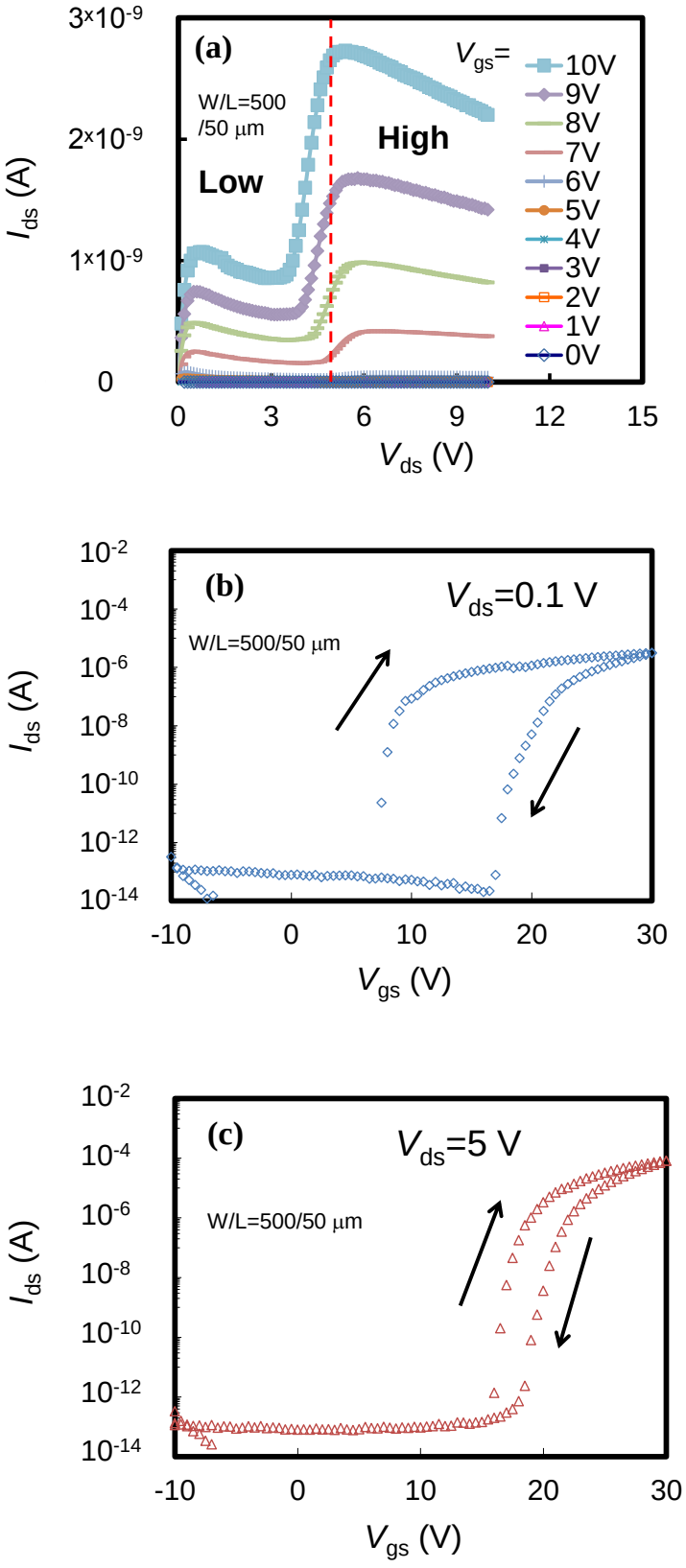


Fig. 5-9 (a) Output characteristic, and transfer characteristics at (b) V_{ds}=0.1 V and (c) V_{ds}=5 V of PA-Al_2O_3 passivated TFTs.

shown in Fig. 5-9(b) and 5-9(c), respectively. Transfer characteristics at V_{ds} of 0.1 and 5 V were investigated. Clockwise hysteresis characteristics were observed under sweeping V_{gs} between -10 and 30 V. Comparing the forward sweeping transfer curve, the reverse sweeping transfer curve intensively shifted to the positive direction (positive hysteresis window) at V_{ds}=0.1 V. The positively shifted V_{th} (ΔV_{th}') was about 11.5 V. At V_{ds}=5 V, a much smaller positive hysteresis window was found. The ΔV_{th}' was about 3.0 V.

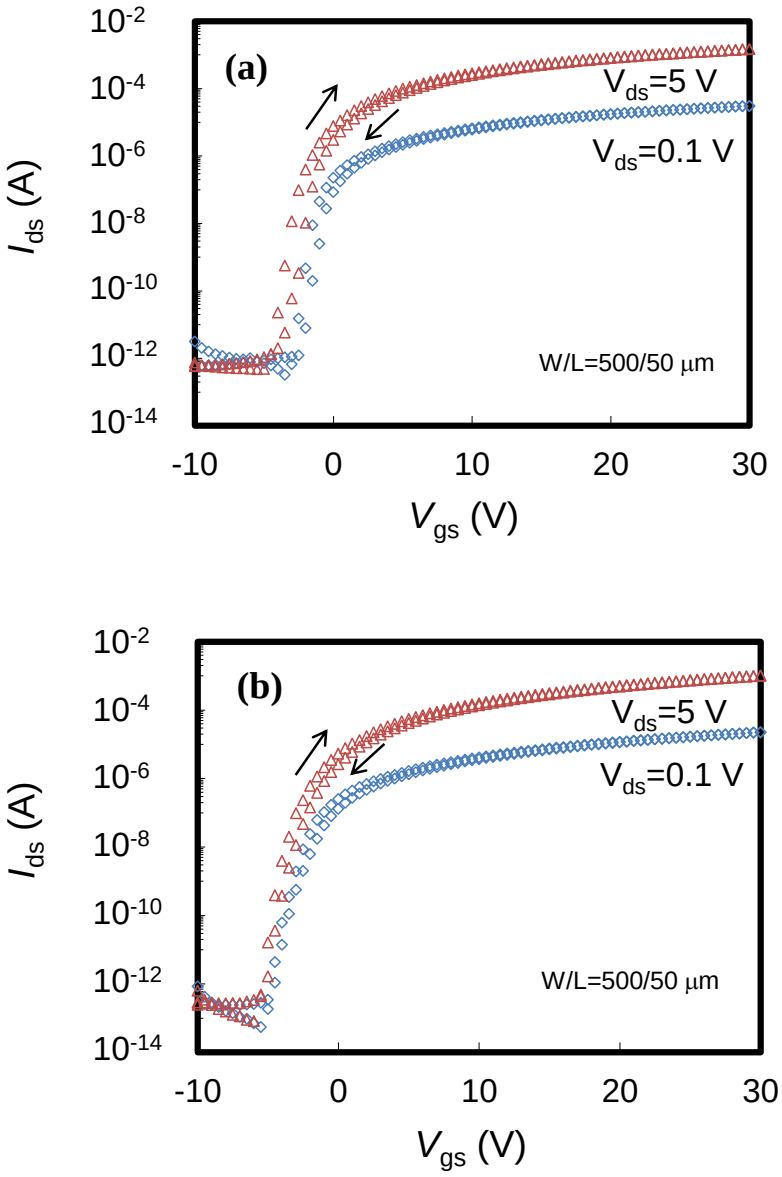


Fig. 5-10 Transfer characteristics with hysteresis behaviors of (a) unpassivated and (b) O_3-Al_2O_3 passivated TFTs.

In general, a clockwise hysteresis indicates that negative charge carriers trapped at the interface between the channel layer and the gate dielectric.[5, 13)] However, for these three TFTs, the interfaces of channel layer and gate dielectric must be the same. Therefore, the hysteresis behaviors of other two TFTs were also investigated, as shown in Fig. 5-10(a) and 5-10(b), respectively. Both of them showed very small positive hysteresis window. The 'ΔV_{th}' of the unpassivated and O_3-Al_2O_3 passivated TFTs were about 1.2 and 1.1 V, respectively. Therefore, the huge positive hysteresis window of PA-Al_2O_3 passivated TFT was not due to the negative charge carriers trapped at the interface between the IZO channel layer and the SiO_2 gate dielectric.

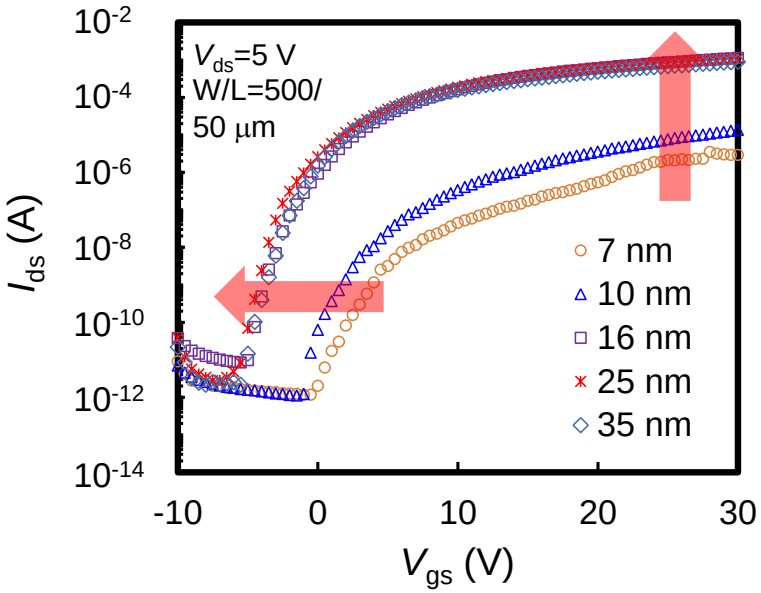


Fig. 5-11 Transfer characteristics of unpassivated TFTs with various thicknesses IZO thin films.

On the other hand, the dominance of the donor density and acceptor-like trap density depends on the active channel thickness in semiconductor.[4)] In order to understand the active channel thickness of IZO thin films in these three TFTs, the thickness dependency on the properties of unpassivated TFTs with various thicknesses IZO thin films was investigated. Transfer characteristics of TFTs with these IZO thin films are shown in Fig. 5-11. The thickness was changed by the change of rotation speed and spin-coating layer number. Except the thickness of 10 nm which was used for the evaluation of instability, other IZO thin films with thicknesses of 7,

16, 25, 35 nm were also fabricated. As the thickness increased from 7 to 16 nm, the transfer characteristic negatively shifted with the increase of on-current. However, no change of characteristic was found with further increase of IZO film thickness. It is known that as thicknesses increased, the carrier concentration in semiconductor increased.[14] Thus, transfer characteristic negatively shifted and on-current increased from 7 to 16 nm. From 16 to 25 nm, although the thickness increased and the carrier concentration increased, the increased carries seemed to have no contribution on the action of the TFTs. The active thickness (t_{act}) of the channel layer in these TFTs was considered to be in the range of 10 nm$<t_{act}<$ 16 nm. The thickness of IZO thin films in TFTs which were used for the instability investigation was 10 nm, it was thinner than the active thickness. Therefore, the characteristic of back-channel region significantly affected the transfer characteristics of the TFTs. The abnormal output characteristic and the huge positive hysteresis window were considered to due to the change of the back-channel region in the PA-Al_2O_3 thin film passivated TFT.

During the deposition of PA-Al_2O_3 thin film, large amounts of O* must be remained on the IZO surface. These O* trapped large amounts of electrons and induced significantly positively shifted $V_{th.}$ At the low V_{ds} region, the electric field between source and drain electrodes in the IZO thin film could not provide enough energy for releasing trapped electrons, as shown in Fig. 5-12(a). However, at the high V_{ds} region, more electrons could be released from trap sites (Fig. 5-12(b)). Thus, higher on-current and smaller positive hysteresis window were observed at the high V_{ds} region in the PA-Al_2O_3 thin film passivated TFT.

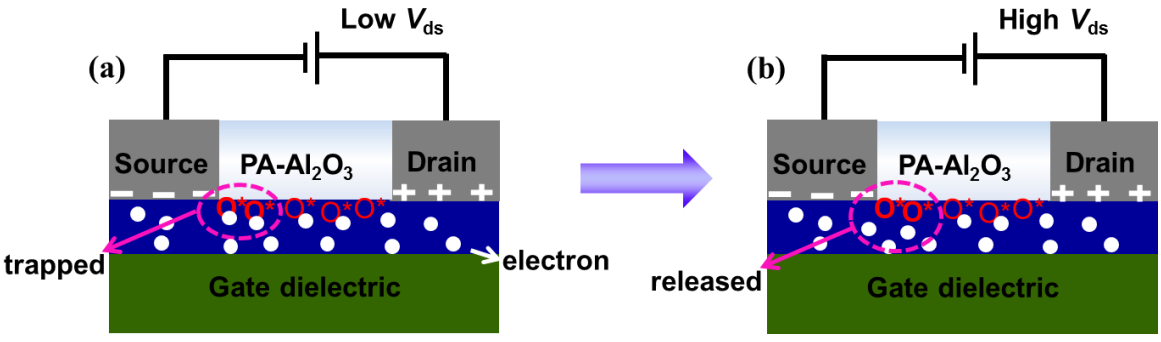


Fig. 5-12 Schematic diagram of the change on trapped electrons by O* at the back-channel of the PA-Al_2O_3 thin film passivated IZO TFT from the (a) low V_{ds} region to the (b) high V_{ds} region.

Hysteresis behaviors of the PA-Al_2O_3 passivated TFT were continuously measured twice, as shown in Fig. 5-13. Every time, the hysteresis behavior was firstly measured at the V_{ds} of 0.1 V, and then measured at the V_{ds} of 5 V. At the second time, the positive hysteresis window significantly decreased even though measured at a low V_{ds} of 0.1 V, which because after the first time sweeping at the high V_{ds} of 5 V, the electrons that trapped by the O* were released. Therefore, at the second time, the positive hysteresis window significantly decreased. It was explained well by the mechanism discussed above.

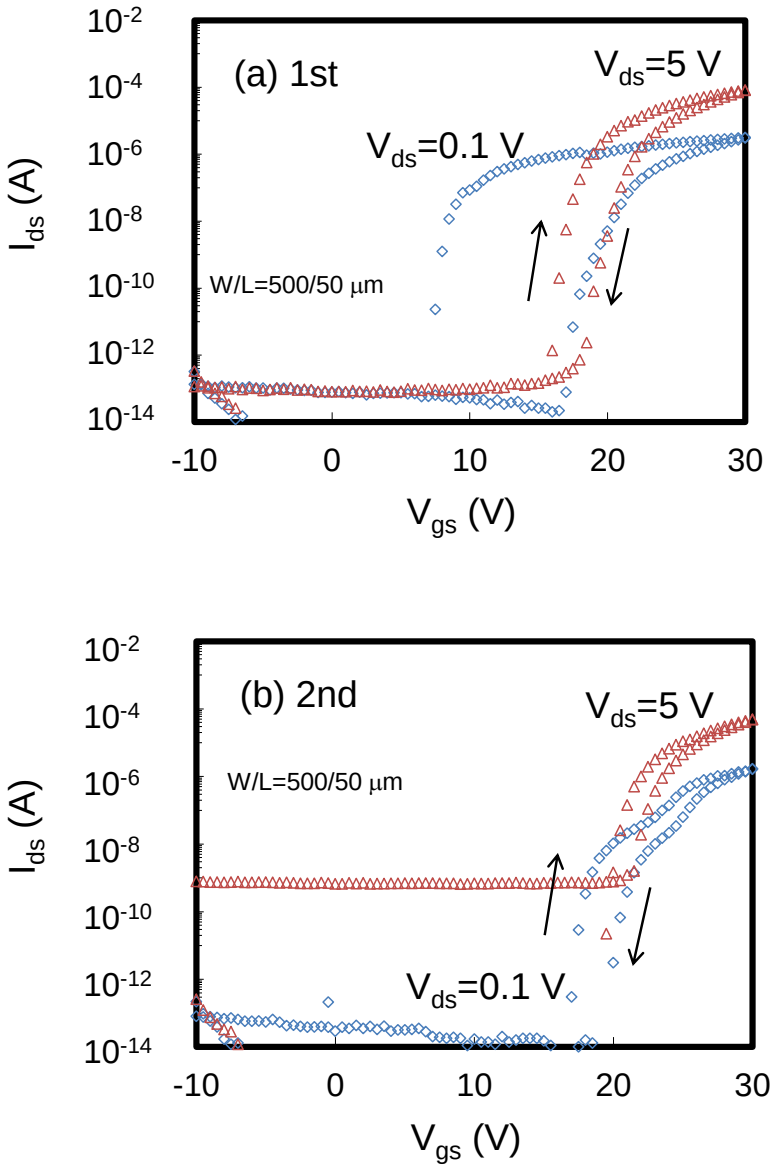


Fig. 5-13 Hysteresis behaviors of TFTs which were continuously measured at V_{ds} of 0.1 and 5 V for the (a) first and (b) second time.

These results suggested that the PA-Al_2O_3 thin film was not suitable for the passivation of aqueous solution-derived IZO TFTs fabricated in this research. The positive gate voltage stress instability of O_3-Al_2O_3 thin film passivated TFT was further investigated.

5.3.3 Improvement of the gate voltage stress instability by the passivation of the O_3-Al_2O_3 thin film

Figure 5-14(a) shows the variation of transfer characteristics as a function of the applied stress time for the O_3-Al_2O_3 thin film passivated TFT. The positive shift of transfer curves of the O_3-Al_2O_3 thin film passivated TFT significantly decreased comparing the unpassivated TFT (Fig. 5-5(a)). The ΔV_{th} as a function of stress time of unpassivated and O_3-Al_2O_3 thin film passivated TFTs is show in Fig. 5-14(b). The ΔV_{th} after the stress time of 1000 s under gate voltage applied decreased from 3.4 V of the unpassivated TFT to 1.9 V of the O_3-Al_2O_3 thin film passivated TFTs.

The positive shifted V_{th} of oxide TFTs under positive gate voltage stress has been attributed to two different mechanisms in detail: the parallel shift in V_{th} without significant change in the subthreshold swing (S) during stress time is attributed to simple charge trapping; the positive shift in V_{th} accompanying the change in S comes from the creation of defects within the oxide semiconductor channel material.[7, 15] Therefore, the changes of the S were also investigated for the unpassvated and O_3-Al_2O_3 thin film passivated TFTs. Almost no changes of S were found for both of them. This means that the V_{th} degradation were mainly caused by charge trapping rather than the creation of bulk trap states in the IZO thin film. The density of the trapped electrons could be estimated from the extent of the ΔV_{th} using $N=C_i\Delta V_{th}/q$, where C_i and q are the capacitance per unit area of the gate dielectric and the electronic charge, respectively. The density of the trapped electrons was 6.4×10^{11} cm^{-2}. By the passivation of O_3-Al_2O_3 thin films, the adsorption of O_2 from the ambient atmosphere was kinetically prevented, subsequently prevented the trapping of electrons, thus the gate voltage stress instability improved.

The interface of Al_2O_3 and IZO thin films were investigated by the transmission electron microscope (TEM; JEM-2100F) using an acceleration voltage of 200 kV. Energy dispersive X-ray spectrometry (EDS) profiles showed that the diffusion of Al and In occurred close the interface of IZO/Al_2O_3 thin films (Fig. 5-15 (a)). A mixed layer of 4 nm was found, as shown in Fig. 5-15(b). Therefore, it suggested that a thin AlInZnO interface layer was generated between the IZO and Al_2O_3 thin films, as shown in Fig. 5-15 (c). Since the Al has a higher chemical bonding energy with oxygen rather than In or Zn, provided less oxygen vacancies and therefore decreased

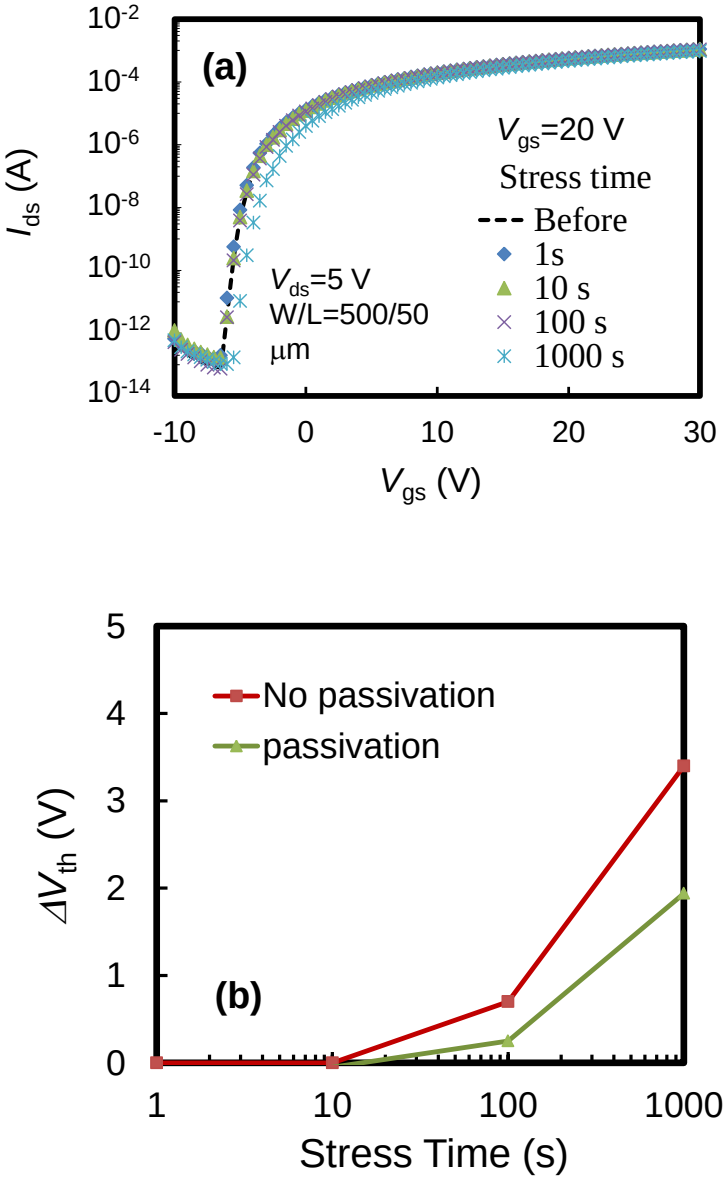


Fig. 5-14 (a) Variation of transfer characteristics of the O_3-Al_2O_3 thin film passivated TFTs as a function of the applied stress time. (b) Variation of the V_{th} shifts as a function of stress time for unpassivated and passivated TFTs.

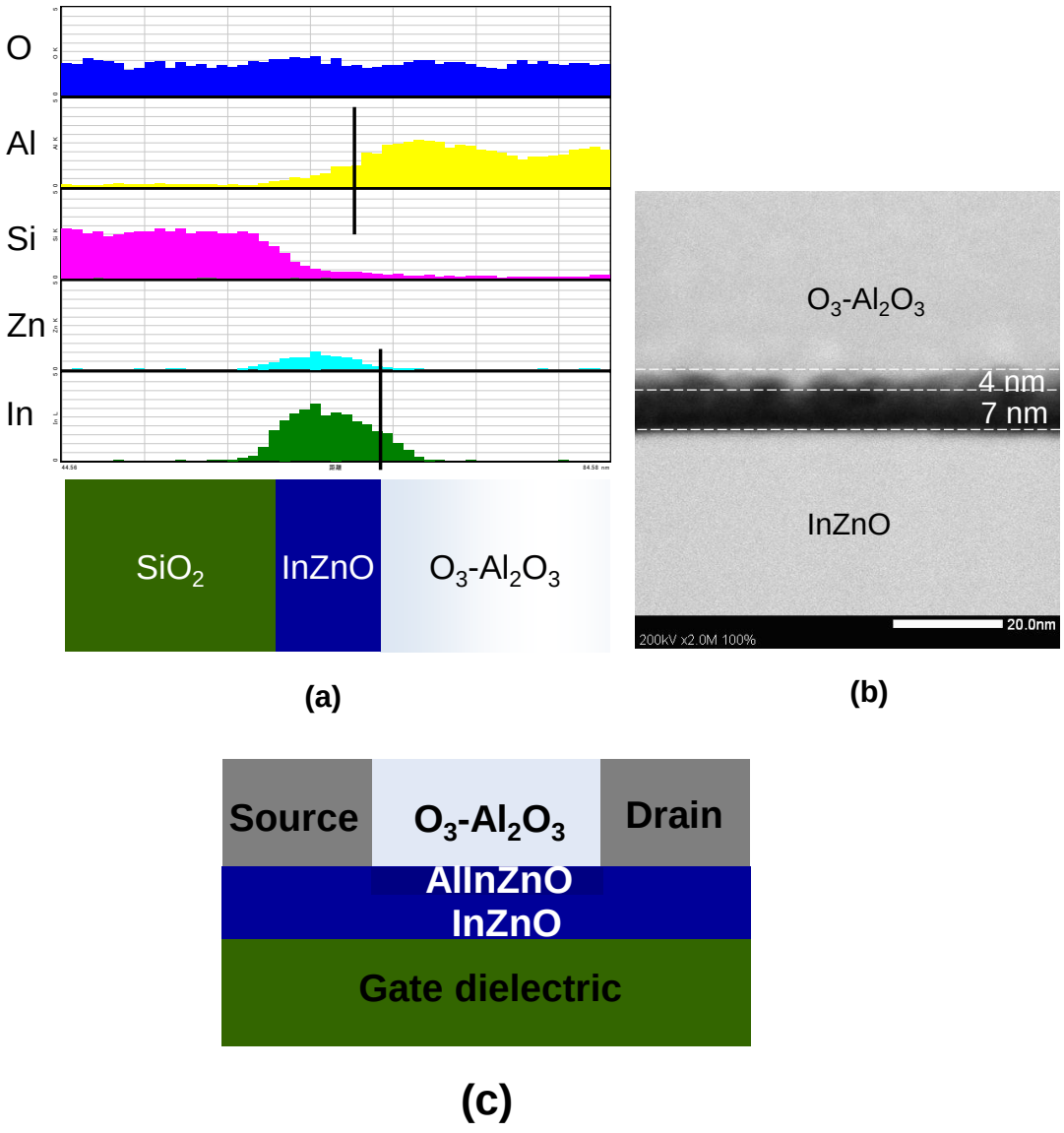


Fig. 5-15 (a) EDS profiles of various elements which were measured by TEM in the O_3-Al_2O_3 thin film passivated TFT, (b) TEM images of the interface of IZO and O_3-Al_2O_3 thin film, and (c) schematic diagram of the generated AlInZnO interface layer in the O_3-Al_2O_3 thin film passivated TFT.

the carrier concentration of the whole channel.[16] Therefore, lower off-currents were found in passivated TFTs.

5.3.4 TFTs passivated by various conditions fabricated O_3-Al_2O_3 thin films

Various thicknesses O_3-Al_2O_3 thin films were fabricated at various temperatures. All of these O_3-Al_2O_3 thin films were used to passivate aqueous solution-derived IZO TFTs. All of the passivated TFTs showed smaller ΔV_{th} than the unpassivated TFT, as shown in Fig. 5-16. It indicated that passivation of O_3-Al_2O_3 thin films were effective to improve gate voltage stress instability. Moreover, higher temperatures deposited thin films with thicker thickness were more effective.

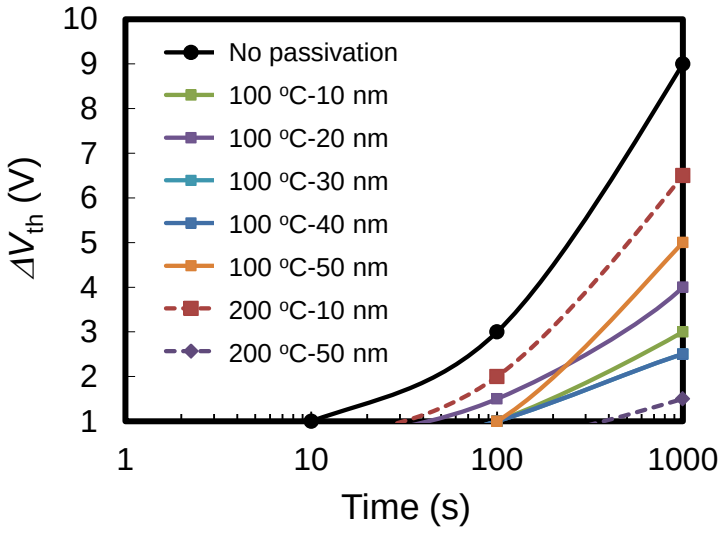


Fig. 5-16 ΔV_{th} of TFTs passivated by various conditions fabricated O_3-Al_2O_3 thin films.

5.4 Conclusion

Aqueous solution-derived IZO TFTs showed positively shifted V_{th} under a positive gate voltage stress. From the analysis of thickness dependency of IZO TFTs, the t_{act} of the IZO channel layer was decided in the range of 10 nm$<t_{act}<$16 nm. The characteristic of back-channel intensively affected properties of TFTs which were used for the instability investigation (the thicknesses of the IZO thin films were about 10 nm). Therefore, in order to improve this instability, ALD-derived Al_2O_3 thin films were used to passivate the back-channel region of the IZO TFTs.

After the passivation of the plasma-assisted ALD derived PA-Al_2O_3 thin film,

the transfer characteristic significantly positively shifted even though no gate voltage stress was applied. Large positive hysteresis window was also observed. Amounts of O* which were generated by plasma assistance were considered to remain on the IZO surface. Because of the adsorption of electrons by these active O*, a depletion layer was created under the IZO surface, therefore the V_{th} significantly positively shifted. Thus, the PA-Al_2O_3 thin film was not suitable for the passivation of aqueous solution derived IZO TFT.

By the passivation of conventional ALD derived O_3-Al_2O_3 thin film, the positively shifted V_{th} under a positive gate voltage stress improved. The adsorption of O_2 from the ambient atmosphere was kinetically prevented, thus the gate voltage stress instability improved. In addition, TFTs were passivated by various conditions fabricated O_3-Al_2O_3 thin films. All of them showed improved instability. Higher temperatures deposited O_3-Al_2O_3 thin films with thicker thickness were more effective to improve the positive gate voltage instability.

[References]

1) D. Kang, H. Lim, C. Kim, I. Song, J. Park, Y. Park, and J. Chung: Appl. Phys. Lett. **90** (2007) 192101

2) J. K. Jeong, H. W. Yang, J. H. Jeong, Y.-G. Mo, and H. D, Kim: Appl. Phys. Lett. **93** (2008) 123508

3) R. B. M. Cross, and M. M. D. Souza: Appl. Phys. Lett. **89** (2006) 263513

4) J.-S. Park, J. K. Jeong, H.-J. Chung, Y.-G. Mo, and H. D. Kim: Appl. Phys. Lett. **8** (2008) 072104

5) J. Lee, J.-S. Park, Y. S. Pyo, D. B. Lee, E. H. Kim, D. Stryakhilev, T. W. Kim, D. U. Jin, and Y.-G. Mo: Appl. Phys. Lett. **95** (2009) 123502

6) S.-J. Seo, S. C. Yang, J.-H. Ko, and B.-S. Bae: Electrochem. Solid-State Lett. **14** (2011) H375

7) S. Lee, K. Jeon, J.-H. Park, S. Kim, D. Kong, D. M. Kim, D. H. Kim, S. Kim, S. Kim, J. Hur, J. C. Park, I. Song, C. J. Kim, Y. Par, and U.-I. Jung: Appl. Phys. Lett. **95** (2009) 132101

8) J.-M. Lee, I.-T. Cho, J.-H. Lee, and H.-I. Kwon: Appl. Phys. Lett. **93** (2008) 093504

9) K. Nomura, T. Kamiya, M. Hirano, and H. Hosono: Appl. Phys. Lett. **95** (2009) 013502

10) Y. Kawamura, N. Hattori, N. Miyatake, M. Horita, and Y. Uraoka: Jpn. J. Appl. Phys. **50** (2011) 04DF05

11) Y. Kawamura, M. Tani, N. Hattori, N. Miyatake, M. Horita, Y. Ishikawa, and Y. Uraoka: Jpn. J. Appl. Phys. **51** (2012) 02BF04

12) M. D. Groner, S. M. George, R. S. McLean, and P. F. Carcia: Appl. Phys. Lett. **8** (2006) 051907

13) S. J. Kim, D. L. Kim, Y. S. Rim, W. H. Jeong, D. N. Kim, D. H. Yoon, and H. J. Kim: J. Cryst. Growth **326** (2011) 163

14) Y. Wang, X. W. Sun, G. K. L. Goh, H. V. Demir, and H. Y. Yu: IEEE Trans. Electron Devices **58** (2011) 480

15) S.-J. Kim, S.-Y. Lee, Y.-W. Lee, W.-G. Lee, K.-S. Yoon, J.-Y. Kwon, and M.-K. Han: Jpn. J. Appl. Phys. **50** (2011) 024104

16) K. M. Kim, W. H. Jeong, D. L. Kim, Y. S. Rim, Y. Choi, M.-K. Ryu, K.-B. Park, and H. J. Kim: IEEE Electron Device Lett. **32** (2011) 1242

Chapter 6

Conclusions and future works

High performance thin film transistors (TFTs) with aqueous solution process-derived InZnO (IZO) thin films as channel layer and thermally oxidized SiO_2 thin films as gate dielectrics were fabricated. On the other hand, TFTs with IZO and gate dielectrics of $SrTa_2O_6$ (STA) thin films which were both fabricated by solution process using organic solutions were successfully fabricated. Low-operating-voltage TFTs were obtained by the use of STA thin films.

6.1 Conclusions

Four main results were obtained in this research.

1) Dielectric and leakage current properties of solution process-derived high-k materials of $(Ba,Sr)Ta_2O_6$ (BSTA) were investigated for the first time. Among five compositions of crystalline BSTA thin films, the STA thin film showed the highest dielectric constant (ε) of about 140, the lowest loss tangent ($\tan\delta$) of about 0.6 %, and the lowest leakage current of about 10^{-7} A/cm^2, therefore, it was regarded as the most promising composition for application of TFTs.

Of various temperatures annealed STA thin films, the STA which were annealed at 700 ^oC exhibited the lowest leakage current. In order to decrease the leakage current of STA thin film which was annealed at a lower temperature of 500 ^oC, an additional UV/O_3-assisted annealing was proposed. Appropriate concentrations of Si and Ti impurities from the substrates diffused into Ta^{5+} sites in the STA thin film, decreased its leakage current.

2) IZO thin films were fabricated by two kinds of solutions: organic and aqueous solution. For the organic solution process-derived IZO TFTs, a high annealing temperature of 700 ^oC should be carried out to obtain a high performance. In order to decrease the fabrication temperature, an UV/O_3-assisted annealing with a temperature of 290 ^oC was carried out for the IZO thin film for the first time. Obtained TFTs showed the same field effect mobility (μ_{FET}) of about 2.19 cm^2/(V$\cdot$ s) as that of the 700 ^oC annealed-IZO TFTs. However, this mobility was still not enough for the application of displays. By the use of the aqueous solution, an extremely high μ_{FET} of 19.5 cm^2/(V$\cdot$ s) was obtained at a low temperature of 300 ^oC. No additional treatment needed to be added on the annealing process. The on/off current ratio

(I_{on}/I_{off}) exceeded 10^9. The less remained carbon impurity in the aqueous solution-derived IZO thin film was regarded as contributing these high performances. Higher mobility than that obtained in this work is rarely reported.

3) STA thin film which was annealed at 700 ^oC (STA-700) was used as the gate dielectric of the sputtered-IGZO TFT. A high μ_{FET} of 4.8 $cm^2/(V\cdot s)$ and I_{on}/I_{off} of 2.4 $\times 10^7$ were obtained at low gate and drain voltages of 5 V. On the other hand, an extremely low subthreshold swing (S) of 0.07 V/decade which was close to the limit value of S by theoretical calculations was also obtained. The high ε and good surface morphology of the STA-700 thin film were considered to contribute to this extremely low S. STA thin film which was annealed at 500 ^oC assisted by UV/O_3 treatment (STA-500UV/O_3) showed the same effect. On the other hand, through the improvement of fabrication process, extremely high mobility of 173.4 and 237.4 $cm^2/(V\cdot s)$ were obtained by the use of STA-700 and STA-500UV/O_3 as gate dielectric, respectively.

TFTs with semiconductor channel IZO and gate dielectric STA thin films which were both fabricated by the solution process using organic solutions were successfully fabricated. Moreover, the TFT using the high-k material of STA as the gate dielectric showed lower threshold voltage (V_{th}) of 0.8 V and lower S of 0.08 V/decade than the TFT using the SiO_2 as the gate dielectric. However, a relatively low μ_{FET} of 0.24 $cm^2/V\cdot s$ was obtained. It is expected to be increased by the improvement of the quality of IZO thin films.

4) Aqueous solution derived-IZO TFTs showed positively shifted V_{th} under a positive gate voltage stress. The adsorption of O_2 from the ambient air while gate voltage applied mainly affected the gated voltage stress instability. Therefore, in order to improve this instability, Al_2O_3 thin films which were fabricated by a conventional atomic layer deposition method were used to passivate the back-channel region of the IZO TFTs. After the passivation, the positively shifted V_{th} significantly improved.

6.2 Future works

There are some problems still need to be solved.

- STA thin films:

The fabrication temperature of STA thin films was still high. It is not suitable for the application on flexible substrates. A new solution with low chemical reaction

temperature is needed.

- IZO thin films fabricated by aqueous solution:

A good compatibility of IZO thin films with other thin films and substrates is needed.

The chemical reaction temperature was still higher than 200 ^{o}C. This temperature needs to be decreased to lower than 150 ^{o}C for the application on flexible substrates.

Although the positive gate voltage instability was improved by the passivation of atomic layer deposition-derived Al_2O_3 thin films, it was still worse than that of the vacuum process-derived IZO TFTs. Therefore, the positive gate voltage instability needs to be further improved through the improvement of the solution or the fabrication condition of IZO thin films.

- Organic solution-derived IZO/STA TFTs:

In order to lower the fabrication temperature, the UV/O_3 condition should be optimized for organic solution derived-IZO/STA bilayers.

- Fabrication process:

The fabrication of all materials including electrodes (gate, source and drain), semiconductor, gate dielectric and passivation layers needs the solution process.

Even though the fabrication process of thin films could be simplified by a solution process, the patterning of these materials was still complicated. Moreover, most of the materials were wasted during patterning. Therefore, advanced processes like ink-jet printing and gravure coating, which were introduced in the chapter 1, need to be developed.

Low energy consumption (low-operating-voltage) and high quality (high mobility, high stability, and so on) flexible displays are expected to be fabricated at low cost with high throughput (by solution process) after solving these problems.

Appendix 1

Thermally Stimulated Current Analysis of Defects in Solution Process-Derived $SrTa_2O_6$ Thin-Film Capacitors

1. Introduction

The solution process is a very simple method for fabricating dielectric and semiconductor thin films. However, solution process-derived thin films usually show weaker electrical properties than those of other vacuum process derived thin films. Impurities of carbon (C) and hydrogen (H) which originated from the organic precursor are often considered as one of the main reasons that leakage current properties deteriorate. For the solution process-derived $SrTa_2O_6$ (STA) thin films, the remaining C and H or other impurities, such as Ti, which was found in this work, were expected to play an important role for the leakage currents. In order to improve the electrical properties, the defect states in STA thin films need to be well understood. Since no detailed defect analysis in solution process derived STA thin films has been reported until now, we adopted a thermal simulated current (TSC) technique to investigate the defect states. TSC technique is a simple and nondestructive method for studying defect states in semiconductor and insulators.[1-3)]

2. Experimental Procedure

The STA sol-gel solution (Mitsubishi Material) used had a composition of Sr:Ta = 1:2 and a metal alkoxide concentration of 7 wt.%. The prepared precursor was spin-coated onto $Pt/TiO_2/SiO_2/Si$ substrates at 3000 rpm for 30 s. The TiO_2 layer was used to improve the adhesion between the electrode and the SiO_2/Si substrate.[4)] After spin coating, the deposited thin films were dried at 100 °C for 5 min and pyrolyzed at 450 °C for 4 min on hot plates in air. The coating and heat treatment procedures were performed several times until the thin films were about 150 nm thick. Then, the thin films were annealed in O_2 at 700 (STA-700) and 800 °C (STA-800) for 1 h.

Deposited film thicknesses were investigated by scanning electron microscopy (SEM; JEOL JSM-6301F). Depthwise distributions of elements were analyzed by secondary ion-microprobe mass spectrometry (SIMS; Ion-Microprobe

Atomika-6500) using Cs ion beam. Refractive index (n) of the fabricated STA thin films were measured by spectroscopic ellipsometry (HORIBA Jobin Yvon, UVISEL ER AGMS-NSD). Leakage currents were measured with a programmable electrometer (Keithley 617). Hold times of 20 s were set for each measuring point to eliminate the effect of relaxation processes.

The TSC of the capacitor with a Pt/STA/Pt structure was measured. Pt top electrodes of about 0.1 mm diameter were prepared with a shadow mask using rf-sputtering. In order to measure the TSC, the film capacitor was set on a heater stage and connected to a programmable electrometer (Keithley, 6517) by a Pt wire. The measurement atmosphere of vacuum with an atmospheric pressure of about 10 Pa and air were used. In order to observe clear TSC peaks, various poling voltages (V_p) and collecting voltages (V_c) were investigated. The V_p and V_c were finally set at ±0.3 and ±0.01 V for the STA-700, and ±0.1 and 0 V for the STA-800, respectively. The $+V_p$ expressed that a positive V_p was applied on the bottom Pt electrode. The measurement temperature was performed from room temperature (RT) to 300 ^oC with a heating rate of 2 ^oC/min. The measurement profile is shown in Fig. 1. Detailed measurement information was reported in ref. 2. In order to understand whether the electrical properties of thin films would deteriorate or not at higher measurement temperatures, the dielectric properties of all thin films were measured twice from RT to 300 ^oC. Since no deteriorations were found in both STA thin films, the TSC measurements were carried out.

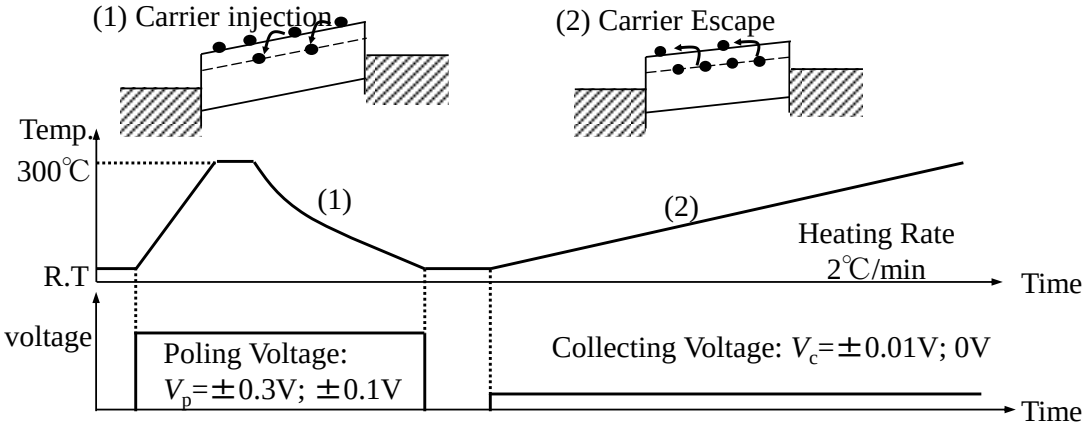


Fig. 1 The TSC measurement profile.

3. Results and Discussion

Figure 2(a) and 2(b) show the TSC profiles of the STA-700 and STA-800 which were measured in the air, respectively. In both of these two thin films, two TSC peaks were observed at lower temperatures of around 130-150 ^{o}C, and two TSC peaks were observed at higher temperatures of around 270-300 ^{o}C. It indicated that similar defect

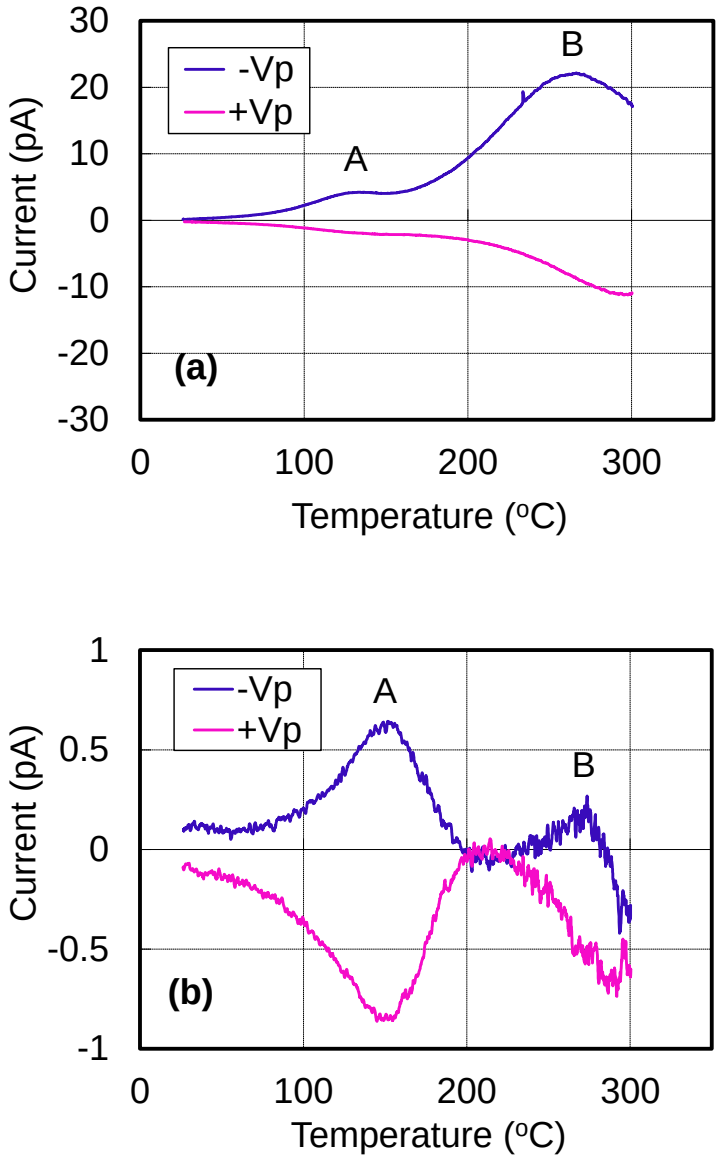


Fig. 2 TSC diagrams of the (a) STA-700 and (b) STA-800 which were measured in the air while $+V_p$ and $-V_p$ were applied.

states existed in these two thin films. The defect which caused the TSC peaks at lower temperatures will be called defect A, and the defect which caused the TSC peaks at higher temperatures will be called defect B. However, the peaks which were observed at the higher temperature were much stronger than the peaks which were observed at the lower temperature in the STA-700. On the contrary, stronger peaks were observed at the lower temperature in the STA-800. Trap density and activation energy were calculated by the curve fitting of the TSC using the following equation[2-3)]

$$I_{TSC} = I_0 \exp[-\frac{E_t}{kT} - \frac{\nu}{\beta}\int_{T_0}^{T} \exp(-\frac{E_t}{kT})dT], \quad (1)$$

where E_t is the activation energy, ν is the escape frequency factor, β is the heating rate. The calculated activation energies of defects A and B were about 0.3 and 0.5 eV, respectively. The trap densities of defect A in the STA-700 and STA-800 were about 0.2×10^{19} and 0.5×10^{19} cm^{-3}, respectively. Higher density of defect A was found in the STA-800. The trap density of defect B in the STA-700 was about 2.8×10^{19} cm^{-3}. It was much higher than densities of defect A in both thin films. Since the TSC peaks which were caused by defect B in the STA-800 were very weak or very close to the highest measurement temperature of 300 ^{o}C, the trap densities were hard calculated accurately. However, these peaks were much weaker than the peaks which were observed at the lower temperature. Therefore, the densities of defect B in the STA-800 should be lower than those in the STA-700. On the other hand, it was found that the TSC profiles were asymmetrical while the $+V_p$ and $-V_p$ were applied on the thin films.

In order to understand these defects, the impurities in the thin films were investigated using the SIMS. Depth profiles of various elements are shown in Fig. 3. Less concentration of C and H impurities were observed in the STA-800, compared with those in the STA-700. The impurity of Ti was detected in both thin films. These Ti was considered to diffuse from the TiO_2 layer under the bottom Pt electrode. In the STA-700, the detected Ti was in the area close to the bottom interface. In the STA-800, higher concentration Ti was observed and it was diffused into the whole thin film. It was readily apparent that the distributions of the Ti were ununiform in both thin films. Since a higher density of defect A was observed in the STA-800, we suggested that defect A might be a Ti related defect, and defect B might be related to the impurities of C and H. In our previous work, electron energy-loss spectroscopy mapping of transmission electron microscopy showed that the diffused Ti mainly existed at grain boundaries in crystalline $BaTa_2O_6$ thin films.[5)]Therefore, diffused Ti

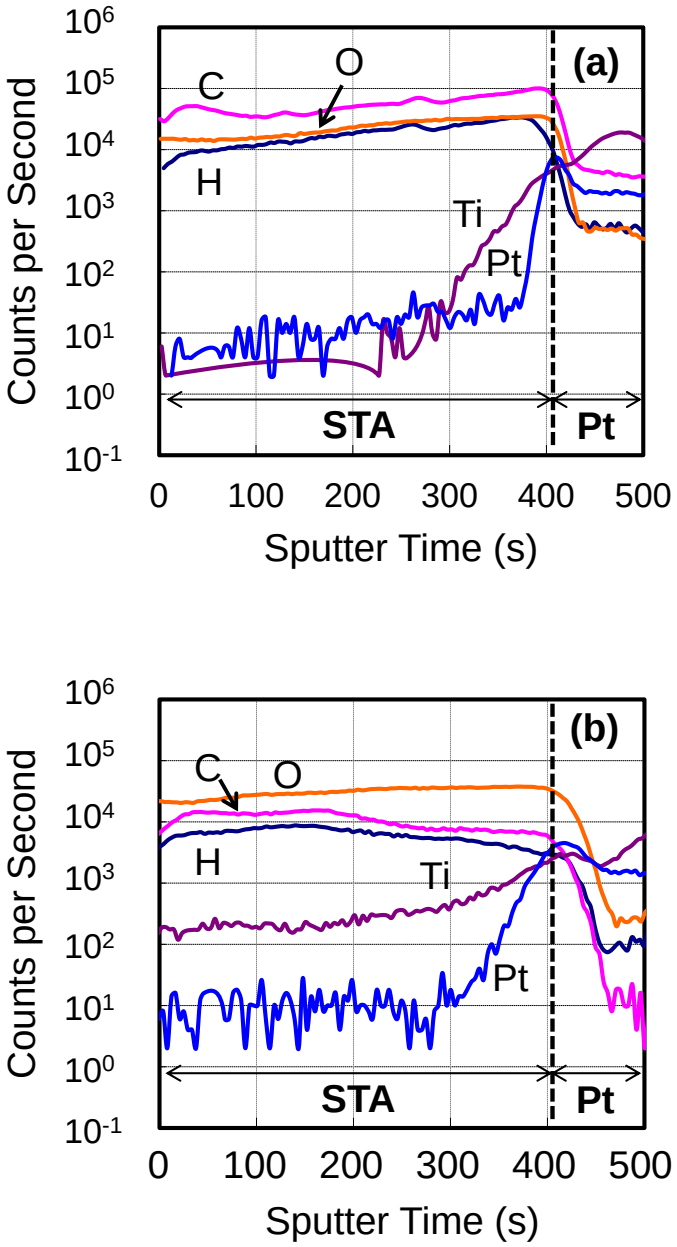


Fig. 3 Depthwise profiles of various elements in the (a) STA-700 and (b) STA-800.

defects might have also existed in the STA thin films as Ti^{4+}. On the other hand, some researchers reported that the Ta in Ta_2O_5 could be substituted by the Ti,[6] so a small part of diffused Ti might have also substituted the Ta in the STA matrix and generated Ti^{-} in our research. The asymmetry characteristics of the TSC peaks that were referred to above might be due to the different states of the top and bottom electrode/STA interfaces, because the impurity concentrations are different in the areas close to the two interfaces in the STA thin films. Continuous study should be carried out to clearly understand the state of Ti impurities, and the asymmetry through the change of electrode material, substrate and film thickness, etc.

The leakage current properties of these two thin films were investigated, as shown in Fig. 4(a). At lower electrical fields, the STA-800 showed a little larger leakage current than that of the STA-700. However, at higher electrical fields, the leakage current was much larger in the STA-800. To determine the dominant leakage current mechanism at the higher electrical fields in the STA-800, Poole-Frenkel (PF) analysis using the following equation was carried out[7-10]

$$J \propto E\exp\left[\frac{q\left(-\Phi_B+\sqrt{\frac{qE}{\pi\varepsilon_0\varepsilon_{op}}}\right)}{kT}\right], \quad (2)$$

where J denotes current density, T represents absolute temperature, k is Boltzmann constant, q denotes electronic charge, E represents electric field, Φ_B is barrier height of the trap, ε_o is the dielectric constant of the vacuum, and ε_{op} denotes dynamic dielectric constant of the insulator material. A good linear fit was obtained in the PF plot, as shown in Fig. 4(b). If the calculated n using $\varepsilon_{op}=n^2$ from the slope of the fitted line is the same as an experimental n, the leakage current can be determined by the PF mechanism limited.[8, 10-11] The calculated value of n was 1.5. This value agreed well with the value of (1.8–2.2) which was measured by the spectroscopic ellipsometry. Thus, the PF mechanism was considered to dominate in the STA-800 at higher electrical fields. It suggested that moving electrons were trapped in the thin film by defect states and the much larger leakage current occurred at higher electric fields. As we discussed above, a higher density of the defect A was found in the STA-800. Therefore, we suggested that the larger leakage current in the STA-800 was mainly caused by this higher density defect A; i. e., the impurity of Ti mainly caused the leakage current of STA thin films.

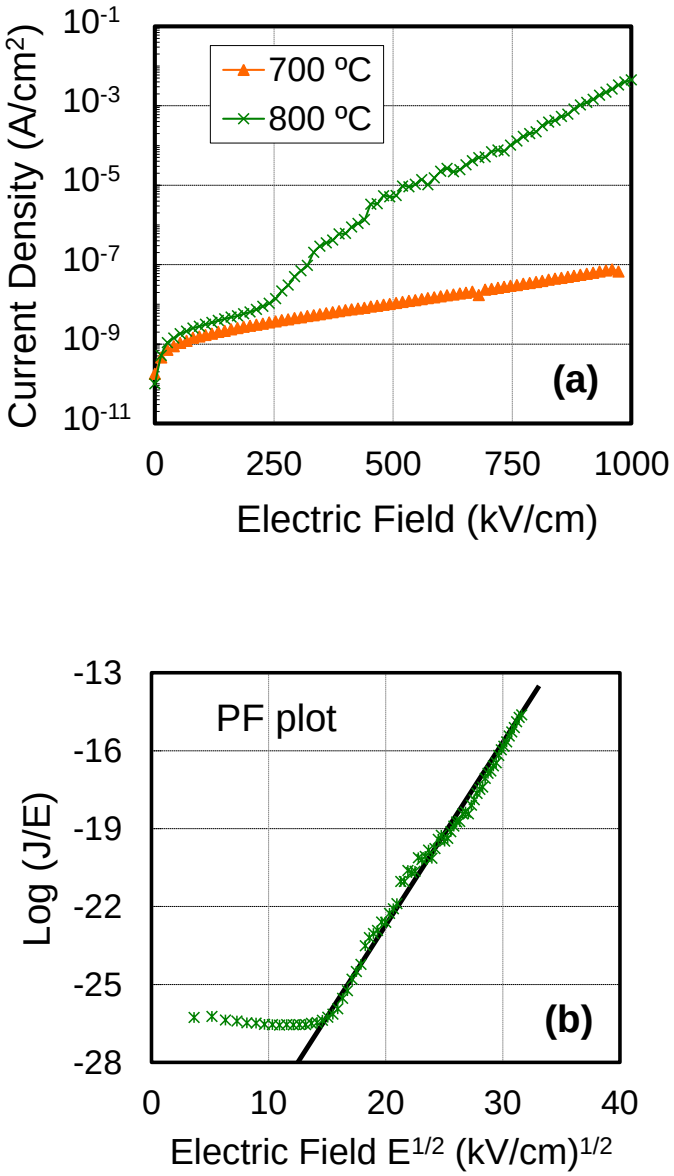


Fig. 4 (a) Leakage current properties of the STA-700 and STA-800. (b) Poole-Frenkel fitting plot of the STA-800.

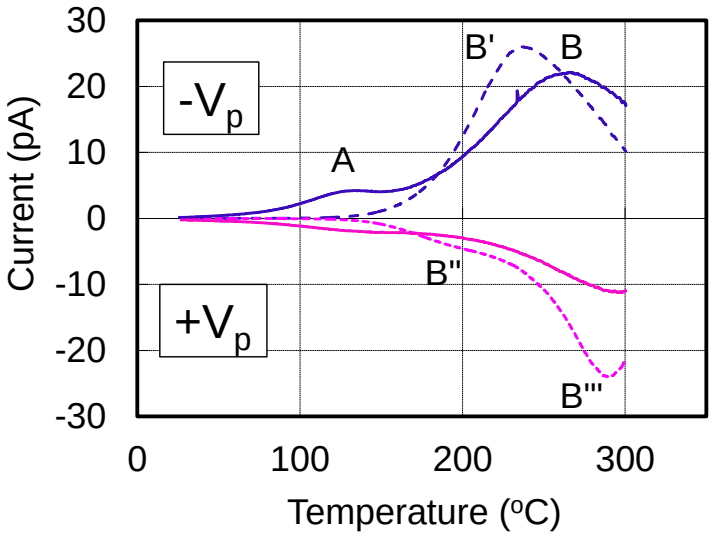


Fig. 5 TSC diagrams of the STA-700 when it was measured in air (solid lines) and vacuum (dashed lines).

It is well known that the oxygen vacancy played an important role in oxide thin films.[12] In many reports, oxygen vacancies in oxide materials could be generated while annealing in the vacuum.[13-14] Therefore, the STA-700 was also measured in the vacuum for further investigation. In consideration of the low pressure measurement atmosphere of TSC and the increase of measurement temperature (the measurement temperature over 250 ^{o}C was about 1 h), more oxygen vacancies were expected to be generated and oxygen vacancy related defects were expected to be easily observed. The TSC profiles, which were measured in air and vacuum are compared in Fig. 5. Different peaks were observed when the thin film was measured in vacuum. A TSC peak was found at a temperature lower than 270 ^{o}C while the $-V_p$ was applied. The defect which caused this peak will be called B'. Two other peaks were clearly observed at around 200 and 290 ^{o}C while $+V_p$ was applied. The defects which caused these two peaks will be called B" and B"', respectively. The calculated activation energy of defect B"' was about 0.8 eV. This value was the same as the energy of the first ionization of oxygen vacancy deep double donor reported by Lau et al. and Sawada et al..[12, 15] Moreover, this peak was observed in an environment that oxygen vacancies were easily generated. Thus, we thought that defect B"' was an oxygen vacancy related defect. Lau et al. also pointed out the oxygen vacancy double donors could be single and doubly ionized to V_o^+ or V_o^{++}. The V_o^+ could attract the ionized

C^- and H^- to generate relatively shallow single donors C^--V_o^+ and H^--V_o^+.[6-8] In their reports, the activation energies of the generated C^--V_o^+ and H^--V_o^+ shallow donors were about 0.49-0.57 eV. These values were close to the activation energies of defects B' and B"(0.5-0.6 eV). Therefore, we thought that the same phenomenon might has occurred in our thin film, and defects B' and B" originated from the combination of C and H impurities with the oxygen vacancies. These results also reinforced the hypothesis that the defect B was related to the impurities of C and H. Although the oxygen vacancy related defects could not be clearly observed by the TSC measurement in the air, it was clearly observed in the vacuum. It is suggested that most of the defects in the STA thin film could be easily observed through the further improvement of the TSC measurement condition.

It was also found that the TSC peaks which were caused by defect A disappeared when the thin film was measured in vacuum. While the thin film was measured in air, some H_2O or other impurities from the air could be adsorbed in the thin film when voltage was applied.[16] On the other hand, when the thin film was measured in vacuum, more oxygen vacancies were expected to be generated in the thin film. Therefore, the disappearing of the peaks might be affected by the environment or the oxygen vacancies. Further research will be done for understanding this problem.

4. Conclusions

In this research, we demonstrated that defect states in solution process-derived STA thin films can be detected by a TSC technique. We also tentatively explained leakage current properties using these defect states. Similar defect states were found in the STA-700 and STA-800 thin films through the TSC investigation. It was suggested that the TSC peaks which were observed at lower temperatures might be caused by the impurity of Ti, and the TSC peaks which were observed at higher temperatures might be caused by the impurities of C and H. The Ti related defects were likely to mainly contribute leakage currents of STA thin films. Thus, larger leakage current was found in the STA-800 which more Ti impurities were contained. Oxygen vacancy related defects were also clearly observed when the STA thin films were measured in a vacuum. It was expected that most of the defects in the STA thin films could be easily observed through the improvement of measurement conditions. Continuous research, such as the change of the electrode material, substrate, film thickness and measurement atmosphere, need to be done for more understanding.

[References]

1) Y. H. Lee, T. W. Kang, and T. W. Kim: J. Appl. Phys. **71** (1992) 5419.

2) T. Nishida, M. Matsuoka, S. Okamura and T. Shiosaki: Jpn. J. Appl. Phys. **42** (2003) 5947.

3) R. R. Haering and E. N. Adams: Phys. Rev. **117** (1960) 451.

4) T. P.-C. Juan, S.-M. Chen, and J. Y.-M. Lee: J. Appl. Phys. **95** (2004) 3120.

5) L. Lu, T. Nishida, M. Echizen, K. Uchiyama, and Y. Uraoka: Jpn. J. Appl. Phys., **49**, (2010) 09MA14.

6) W. S. Lau, T. S. Tan, P. Babu, and N. P. Sandler: Appl. Phys. Lett. **90** (2007) 12903.

7) L. Lu, T. Nishida, M. Echizen, K. Uchiyama, and Y. Uraoka: Thin Solid Films, **520**, (2012) 3620.

8) B. Miao, R. Mahapatra, N. Wright, and A. Horsfall: J. Appl. Phys. **104** (2008) 054510.

9) T. Nozaka, Y. Mizutani, B. Gun, M. Echizen, T. Nishida, H. Takeda, K, Uchiyama, and T. Shiosaki: Jpn. J. Appl. Phys. **47** (2008) 7494.

10) F.-C. Chiu, J.-J. Wang, J. Y. Lee, and S. C. Wu: J. Appl. Phys. **81** (1997) 6911.

11) K.-H. Cho, C.-H. Choi, J.-Y. Choi, T.-G. Seong, S. Nahm, C.-Y. Kang, S.-J. Yoon, J.-H. Kim: J. Eur. Ceram. Soc. **30** (2010) 513.

12) H. Sawada, and K. Kawakami: J. Appl. Phys. **86** (1999) 959.

13) N. Zhong, S. Okamura, K. Uchiyama, and T. Shiosaki: Appl. Phys. Lett. **87** (2005) 252901.

14) S.-J. Seo, Y. H. Hwang, and B.-S. Bae: Electrochem. Solid-State Lett. **13** (2010) H357

15) W. S. Lau, L. L. Leong, T. Han, and N. P. Sandler: Appl. Phys. Lett. **83** (2003) 2835.

16) J.-S. Park, J. K. Jeong, H.-J. Chung, Y.-G. Mo, and H. D. Kim: Appl. Phys. Lett. **92** (2008) 072104.

Acknowledgements

The research could not have been accomplished without the collaboration of many other people, to whom I wish to express my greatest gratitude.

First of all, I sincerely thank my academic supervisor Prof. Yukiharu Uraoka, Nara Institute of Science and Technology, for his extensive, guidance, patience, encouragement and support during the whole work. Thanks him for his kindness and help in all aspects of my life.

I would like to thank Assoc. Prof. Yasuaki Ishikawa, Nara Institute of Science and Technology and Assoc. Prof. Takashi Nishida, Fukuoka University, for their professional advice, technical help, valuable guidance in the experiment and the analysis of experimental datum.

I would like to offer sincere thanks to Prof. Takashi Fuyuki and Assoc. Prof. Takashi Matsuo, Nara Institute of Science and Technology, for their valuable and insightful comments and discussion.

I would like to thank Assist. Prof. Masahiro Horida and Assist. Prof. Mutsunori Uenuma, Nara Institute of Science and Technology, for their help in my research. I would like to thank Assoc. Prof. Kiyoshi Uchiyama, Tsuruoka National College of Technology, for his professional advice. I would also like to thank Prof. Tadashi Shiosaki and Dr. Masahiro Echizen for their discussion of this research.

I would like to thank Yuta Miura (graduated) and Yukihiro Osada who worked with me in these two years. I would like to thank Dr. Mami Fujii (graduated) and Yoshihiro Ueoka for the fabrication of InGaZnO thin films. I would like to thank Yumi Kawamura for the fabrication of Al_2O_3 thin films. I would also like to express my gratitude to all the students in the Information Device Science Laboratory and the students who have graduated from this laboratory in the last four years. It has been pleasant and fruitful experience for me to work with them, and thanks for making a good and friendly research environment.

I would like to thank Leigh Mcdowell for his help of my English. I would also like to thank all the technicians in Graduate School of Materials Science for their technical help.

I would like to thank Mr. Maeda, Mr. Akimoto and Mr. Hamada, Nissan Chemical Industries, Ltd., for the preparation of InZnO aqueous solution and valuable discussion.

I would like to thank for the financial support of Japan Society for the Promotion of Science and Heiwa Nakajima Foundation. I would also like to thank for the support of Foundation for Nara Institute of Science and Technology.

At last, I would like to thank my beloved family for their support and all my friends for their kindness help.

Research Results

1. Publications

1. Li Lu, Takashi Nishida, Masahiro Echizen, Yasuaki Ishikawa, Kiyoshi Uchiyama and Yukiharu Uraoka, "Effects of Si and Ti impurities on electrical properties of sol-gel-derived amorphous $SrTa_2O_6$ thin films by UV/O_3 treatment", Appl. Phys. A, (published online)
2. Li Lu, Takashi Nishida, Masahiro Echizen, Yasuaki Ishikawa, Kiyoshi Uchiyama, Tadashi Shiosaki and Yukiharu Uraoka, "Thermally Stimulated Current Analysis of Defects in Sol–Gel Derived $SrTa_2O_6$ Thin-Film Capacitors", Jpn. J. Appl. Phys., **51**, 09LA18 (2012)
3. Li Lu, Masahiro Echizen, Takashi Nishida, Kiyoshi Uchiyama, Yasuaki Ishikawa, and Yukiharu Uraoka, "Low-temperature fabrication of solution-processed InZnO thin-film transistors with Si impurities by UV/O_3-assisted annealing", AIP Advances, **2**, 032111 (2012)
4. Li Lu, Yuta Miura, Takashi Nishida, Masahiro Echizen, Yasuaki Ishikawa, Kiyoshi Uchiyama and Yukiharu Uraoka, "Low-Operating-Voltage Solution-processed InZnO Thin Film Transistors Using High-k $SrTa_2O_6$", Jpn. J. Appl. Phys., **51**, 03CB05 (2012)
5. Li Lu, Takashi Nishida, Masahiro Echizen, Kiyoshi Uchiyama and Yukiharu Uraoka, "Capacitance-voltage and leakage-current characteristics of sol-gel-derived crystalline and amorphous $SrTa_2O_6$ thin films", Thin Solid Films, **520**, 3620 (2012)
6. Li Lu, Takashi Nishida, Masahiro Echizen, Kiyoshi Uchiyama and Yukiharu Uraoka, "Voltage Linearity and Leakage Currents of Crystalline and Amorphous $SrTa_2O_6$ Thin Films Fabricated by Sol-Gel Method", Ferroelectrics, **421**, 82, (2011)
7. Li Lu, Takashi Nishida, Masahiro Echizen, Kiyoshi Uchiyama and Yukiharu Uraoka, "Thickness Dependence of Electrical Properties for High-k $SrTa_2O_6$ Thin Films Fabricated by Sol-Gel Method", Jpn. J. Appl. Phys., **50**, 03CA05, (2011)
8. Li Lu, Takashi Nishida, Masahiro Echizen, Kiyoshi Uchiyama and Yukiharu Uraoka, "Annealing and Composition Effects of $(Ba_xSr_{1-x})Ta_2O_6$ Thin Films Fabricated by Sol-Gel Method", Jpn. J. Appl. Phys., **49**, 09MA14, (2010)
9. Li Lu, Masahiro Echizen, Takashi Nishida, Kiyoshi Uchiyama and Yukiharu Uraoka, "Electrical Properties of $Ba_{0.5}Sr_{0.5}Ta_2O_6$ Thin Film Fabricated by Sol-Gel Method", IEICE Trans. Electron., **E93-C**, 1511, (2010)
10. Li Lu, Masahiro Echizen, Takashi Nishida, Kiyoshi Uchiyama and Yukiharu Uraoka, "Electrical Properties of $(Ba_x,Sr_{1-x})Ta_2O_6$ Thin Films Using Sol-Gel Method",

Trans. Mater. Res. Soc. Jpn., **35**, 177, (2010)

In submission

1. Li Lu, Masahiro Echizen, Takashi Nishida, Kiyoshi Uchiyama and Yukiharu Uraoka, "Low-operating-voltage InGaZnO thin film transistors with high-k $SrTa_2O_6$ as gate dielectric". (Thin Solid Films)

2. Proceedings (peer reviewed)

1. Li Lu, Masahiro Echizen, Takashi Nishida, Kiyoshi Uchiyama and Yukiharu Uraoka, "Fabrication and Evaluation of $SrTa_2O_6$ Thin Films Using Chemical Solution Deposition Method", Proceedings of 6th Thin Film Materials & Devices Meeting, 100228043, (2009)

3. Conferences

3.1 International conferences

1. Li Lu, Yukihiro Osada, Yumi Kawamura, Takashi Nishida, Yasuaki Ishikawa and Yukiharu Uraoka, "High Performance Indium Zinc Oxide Thin-Film Transistors Fabricated by Solution-Process at Low Temperature", *The 19th International Display Workshops in conjuction with Asia Display 2012*, Japan, December, (2012)
2. Li Lu, Masahiro Echizen, Takashi Nishida, Yasuaki Ishikawa, Kiyoshi Uchiyama and Yukiharu Uraoka, "Low-Operating-Voltage ZnO-based Thin Film Transistors Using High-k $SrTa_2O_6$", *TCM 2012 4th International Symposium on Transparent Conductive Materials (former TCOs)*, Greece, October, (2012)
3. Li Lu, Masahiro Echizen,Takashi Nishida, Yasuaki Ishikawa, Kiyoshi Uchiyama and Yukiharu Uraoka, "Low Temperature Fabrication of Wet-processed ZnO-based Thin Film Transistors", *The 2012 International Conference on Flexible and Printed Electronics*, Japan, September, (2012)
4. Li Lu, Takashi Nishida, Masahiro Echizen, Yasuaki Ishikawa, Kiyoshi Uchiyama and Yukiharu Uraoka, "Temperature Effect of Solution-Processed InZnO Thin Film Transistors", *8th International Thin-Film Transistor Conference*, Portugal, January, (2012)
5. Li Lu, Takashi Nishida, Masahiro Echizen, Yasuaki Ishikawa, Kiyoshi Uchiyama and Yukiharu Uraoka, "Interface Effect of High-K $SrTa_2O_6$/ Gate Electrode on the Characteristics of Solution Processed Thin-Film Transistors", *The 20th IEEE*

International Symposium on Applications of Ferroelectrics International Symposium on Piezoresponse Force Microscopy & Nanoscale Phenomena in Polar Materials, Canada, July, (2011)

6. Li Lu, Takashi Nishida, Masahiro Echizen, Yasuaki Ishikawa, Kiyoshi Uchiyama and Yukiharu Uraoka, "Interface Effect of High-k $SrTa_2O_6$/Gate Electrode on the Characteristics of Solution Processed $InZn_4O_x$ Thin-Film Transistors", *2011 The Eighteen International Workshop on Active-Matrix Flatpanel Displays and Devices*, Japan, July, (2011)

7. Li Lu, Takashi Nishida, Masahiro Echizen, Yasuaki Ishikawa, Kiyoshi Uchiyama and Yukiharu Uraoka, "Characteristics of Solution-processed TFTs with $In_4ZnO_x/SrTa_2O_6$ Thin Films", *The 2011 International Meeting for Future of Electron Devices, Kansai*, Japan, May, (2011)

8. Li Lu, Takashi Nishida, Kiyoshi Uchiyama, and Yukiharu Uraoka, "Voltage linearity and leakage currents of amorphous and crystalline $SrTa_2O_6$ thin films", *The joint meeting of the 2010 International Symposium on the Applications of Ferroelectrics and the European Conference on the Applications of Ferroelectrics*, UK, August, (2010)

9. Li Lu, Masahiro Echizen, Takashi Nishida, Kiyoshi Uchiyama, and Yukiharu Uraoka, "Dielectric Properties of Sol-gel Derived $BaTa_2O_6$ Thin Films", *2010 The Seventeenth International Workshop on Active-Matrix Flatpanel Displays and Devices-TFT Technology and FPD Materials*, Japan, July, (2010)

10. Li Lu, Takashi Nishida, Kiyoshi Uchiyama, and Yukiharu Uraoka, "Electrical Properties of $SrTa_2O_6$ Thin Films Fabricated by Sol-Gel Method", *The 2010 International Meeting for Future of Electron Devices, Kansai*, Japan, May, (2010)

11. Li Lu, Masahiro Echizen, Takashi Nishida, Kiyoshi Uchiyama, and Yukiharu Uraoka, "Fabrication and Characterization of $(Ba_x, Sr_{1-x})Ta_2O_6$ Thin Films Using Sol-Gel Method", *International Thin-Film Transistor Conference 2010*, Japan, January, (2010)

12. Li Lu, Masahiro Echizen, Takashi Nishida, Kiyoshi Uchiyama, and Yukiharu Uraoka, "Fabrication and Evaluation of $(Ba_x,Sr_{1-x})Ta_2O_6$ Thin Films Using Sol-Gel Method", *19th MRS-J Symposium (International Session)*, Japan, December, (2009)

3.2 Domestic conferences

1. 呂 莉, 西田 貴司, 越前 正洋, 石河 泰明, 内山 潔, 塩崎 忠, 浦岡 行治, ″熱刺激電流法による $SrTa_2O_6$ 薄膜キャパシタの欠陥分析″, 第 29 回強誘電体応用会議, コープイン京都, 5 月, (2012)

2. 呂 莉, 三浦 祐太, 西田 貴司, 越前 正洋, 石河 泰明, 内山 潔, 浦岡

行治，″High-k 材料を用いた InZnO 薄膜トランジスタの電気特性におけるゲート電極材料の影響″，第 59 回応用物理学会学術講演会，早稲田大学，3 月，(2012)
3. 呂 莉，三浦 祐太，西田 貴司，越前正洋，石河 泰明，内山 潔，浦岡行治，″High-k 材料 $SrTa_2O_6$ を用いた InZnO 薄膜トランジスタの電気特性におけるゲート電極材料の影響″，薄膜材料デバイス研究会・第 8 回，龍谷大学，11 月，(2011)
4. 呂 莉，西田 貴司，三浦 佑太，石河 泰明，内山 潔，浦岡 行治，″$(Ba_xSr_{1-x}Ta_2O_6)$高誘電薄膜の低温作製と電気的特性″，第 72 回応用物理学会学術講演会，山形大学，8 月，(2011)
5. 呂 莉，西田 貴司，越前 正洋，石河 泰明，内山 潔，塩崎 忠，浦岡 行治，″溶液法で作製した $In_4ZnO_x/SrTa_2O_6$ 薄膜トランジスタの特性″，第 28 回強誘電体応用会議，コープイン京都，5 月，(2011)
6. 呂 莉，西田 貴司，石河 泰明，内山 潔，浦岡 行治，″アモルファス $(Ba_xSr_{1-x}Ta_2O_6)$薄膜の低温作製と評価″，第 71 回応用物理学会学術講演会，長崎大学，9 月，(2010)
7. 呂 莉，西田 貴司，内山 潔，浦岡 行治，″ゾルゲル法で作製した $(Ba,Sr)Ta_2O_6$ 薄膜の電気特性の組成依存性″，第 27 回強誘電体応用会議，コープイン京都，5 月，(2010)
8. 呂 莉，越前 正洋，西田 貴司，内山 潔，浦岡 行治，″酸素雰囲気でアニールした $BaTa_2O_6$ 薄膜の電気特性″，第 57 回応用物理学会学術講演会，東海大学，3 月，(2010)
9. 呂 莉，越前 正洋，西田 貴司，内山 潔，浦岡 行治，″ゾルゲル法による $SrTa_2O_6$ 薄膜キャパシターの作製と電気特性評価″，ゲートスタック研究会 ―材料・プロセス・評価の物理―，東レ総合研修センター，1 月，(2010)
10. 呂 莉，越前 正洋，西田 貴司，内山 潔，浦岡 行治，″CSD 法による $SrTa_2O_6$ 薄膜の作製と評価″，薄膜材料デバイス研究会・第６回，龍谷大学，11 月，(2009)
11. 呂 莉，越前 正洋，西田 貴司，内山 潔，浦岡 行治，″化学溶液堆積(CSD)法による MIM 構造 $SrTa_2O_6$ 薄膜キャパシターの作製と電気特性″，2009 セラミック協会・秋季シンポジウム，愛媛大学，9 月，(2009)
12. 呂 莉，越前 正洋，西田 貴司，内山 潔，浦岡 行治，″Sol-Gel 法による $(Ba_x,Sr_{1-x})Ta_2O_6$ 薄膜の作製とその電気的特性″，第 70 回応用物理学会学術講演会，富山大学，9 月，(2009)
13. 呂 莉，越前 正洋，内山 潔，塩崎 忠，″MOD 法によるアモルファス $(Ba_x,Sr_{1-x})Ta_2O_6$ 薄膜の作製とその電気的特性″，第 56 回応用物理学会学術講演会，筑波大学，3 月，(2009)