Fabrication of High-Performance Polycrystalline Silicon Thin Film Transistors at Super Low-Temperature and Its New Electrical Characterization Method

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Abstract

For the application of system on flexible display using high-quality polycrystalline silicon (poly-Si) thin films formed at super low-temperature, the new laser annealing method utilizing flowing water has been demonstrated. Effects on grain growth, the crystallinity, and electrical characteristics of the poly-Si films are investigated. Moreover, super low-temperature crystallization of amorphous silicon (a-Si) thin films on polyethylene terephthalate (PET) and polyethylene naphthalate (PEN) substrates without thermal damage of the substrates have been demonstrated. In addition, new electrical characterization methods with the purpose of the understanding of the local electrical properties of the poly-Si thin films have been studied. The main conclusions obtained in the present study are summarized as follows.

In chapter 2, local electrical characterization with the purpose of the realization to distinguish grain boundary from grain in the poly-Si have been studied. Behavior of the electrons at defect sites in the poly-Si films and the change in conductivity by area or hydrogenation process are determined using conductive atomic force microscopy (C-AFM) and Kelvin force microscopy (KFM) measurements. By the forming of the junction between the cantilever and poly-Si surface, probe current flows from the cantilever to electrical defects by the electron emission. In the grain, the probe current reduced due to the emission of

electron from defect sites inducing the charging of defect sites. In grain boundary, the probe current shows little changing since there are denser defect sites. Hydrogen termination at 300°C reduces the change in probe current drastically, meaning that electrical defects are almost inactivated. In addition, current-voltage (*I-V*) curves of grain and grain boundary changed from symmetric rising to asymmetric rising indicating that the conduction mechanism becomes similar to ideal semiconductor conduction mechanism. On the other hand, high-temperature treatment over 400°C promotes dehydrogenation rather than hydrogenation, resulting in increasing of electrical defects. In the case of hydrogenation at 400°C, *I-V* curves of the poly-Si showed as symmetric rising as metallic conductive mechanism behavior.

In chapter 3, the underwater laser annealing (WLA) as super low-temperature laser annealing technique for poly-Si formation has been demonstrated. The crystallization of a-Si thin films on glass or plastic substrates has been achieved by WLA. It is determined that WLA promotes giant and uniform grain growth by the decreasing surface temperature of substrate and homogenization of temperature distribution within the Si films. In the microwave photo conductivity decay (μ-PCD) measurements, the peak reflectivity of microwave, which is proportional to the excess carrier lifetime, from WLA poly-Si is larger than that of LA poly-Si although both poly-Si films have the same average grain size. Moreover, the crystallinity of WLA poly-Si films on plastic substrates is comparable to that on glass substrates.

Furthermore, WLA poly-Si films contain more hydrogen than LA poly-Si films, and indicates smaller probe current attributed to fewer electrical defects. Hydrogen in water vapor generated by WLA inactivates electrical defects, and WLA poly-Si indicates much better electrical properties than LA poly-Si films. Hydrogen concentration of WLA poly-Si films was the same level as the poly-Si films with a forming gas annealing (FGA) which used for conventional hydrogenation process. Although short processing time and low-substrate temperature as compared to the case of FGA, WLA succeeded in the hydrogen diffusion to the poly-Si layer and improvement of its electrical properties.

In chapter 4, WLA techniques have been applied to other fabrication processes for low-temperature poly-Si (LTPS) TFT. The dopant activation treatment by WLA has been demonstrated. WLA successfully conducted activation annealing more effectively than conventional laser annealing (LA). Carrier concentration of WLA samples is almost the same as that of furnace annealed samples, although annealing time in WLA is much shorter. Next, the inactivation of electrical defects in LTPS TFTs has been accomplished by WLA. It is demonstrated that WLA has more inactivation ability as compared to the LA. The mobility was increased 30% after WLA while that of LA was 5%. WLA also improved other TFT factors such as subthreshold swing, on/off ratio, and threshold voltage. Hydrogen concentration in the WLA poly-Si and gate-SiO_2 films was much higher than that of non-annealed poly-Si and LA poly-Si films, although those of oxygen and hydroxyl were the

same level. It is thought that hydrogen which is diffused from water vapor generated by WLA inactivates electrical defects in gate-SiO_2 and/or poly-Si film, and improves TFT characteristics.

In chapter 5, top-gate type n-channel LTPS TFTs using the poly-Si thin films formed by WLA are fabricated, and their device performance has been investigated. LTPS TFTs using WLA poly-Si films show clearly switching operation. It is demonstrated that WLA poly-Si films are applicable to the active layer for the electrical devices. The mobility of the LTPS TFTs using WLA poly-Si was equal or higher than general LTPS TFTs (> 50cm^2/Vsec), and other TFT factors such as subthreshold swing were also the same level or higher. Therefore, WLA poly-Si thin film has excellent electrical characteristics attributed to high-crystallinity and/or lower dense defects.

In chapter 6, a summary of the present study is given, together with the remaining issues to be solved and suggestions for future work.

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Contents

Chapter 1
Introduction

1.1 Background

A flat panel display (FPD) is infinitely familiar electronic device to us today. FPDs are everywhere: on TV, mobile phone, tablet, personal computer and so on. Since the 14-inch liquid crystal display (LCD) for TV was introduced from Sharp Corp. in 1988 [1], the FPD market has been growing up remarkably due to its advantage over ordinary cathode-ray tube (CRT) display: thin, light, and size-free. Today there are three typical FPDs: the plasma display panel (PDP), the organic light emitting diode (OLED) display, and the LCD as shown in **Fig. 1.1**. In particular, the LCD had rapidly become popular in the past several decades by the application for notebook computer, TV, cellphone, and others. Thus, its market size became over 10 trillion yen industry as of 2010. New application of FPDs to electronic devices which make our daily life more convenient is behind the popularity of the FPDs. TV became thinner and larger over 40-inch size which bring in TV watching with high-definition and powerful vision. Personal computers changed from heavy and bulky type to light and/or portable type by using the LCD for their display. We can work a more effective anywhere by using high-resolution display at large size and using multiple displays in some cases. Phone

not only became portable, but also provides many useful functions such as e-mail and web search.

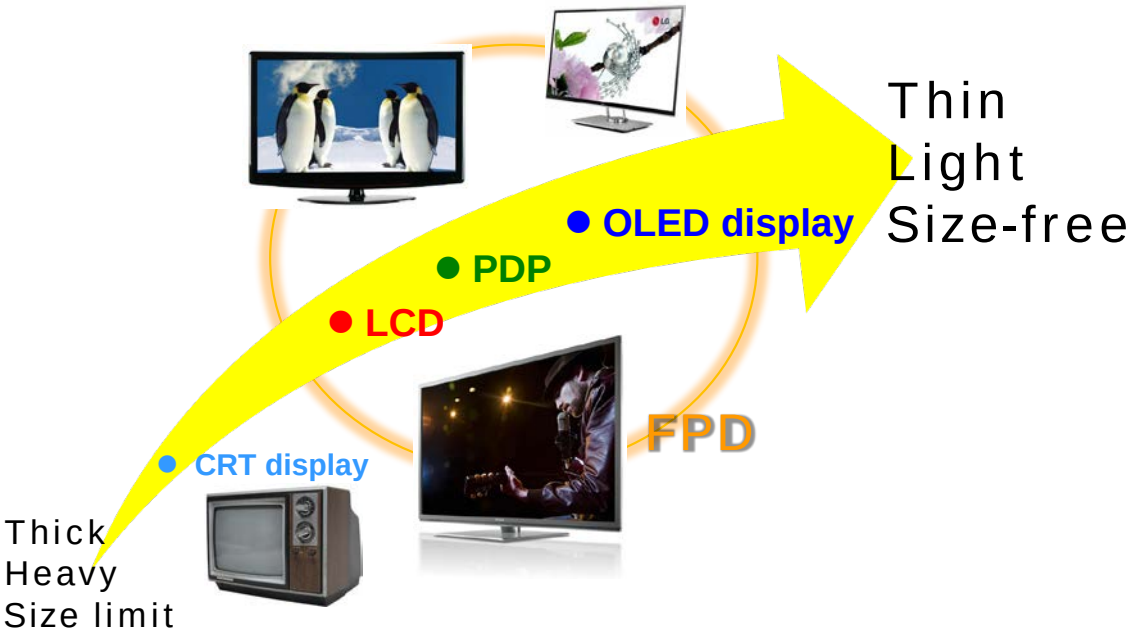

Figure 1.1: Development trend of display from ordinary CRT display to FPDs.

In recent years, studies in order to elevate FPDs more user friendly than before by addition of not only visual display but also input and operation are under active investigation in addition to tendency of getting larger, thinner, and lighter. A system-on-panel (SOP) [2] is a typical case: it integrates functional circuits such as CPU, memory, sensor and others into the display. By doing so, thickness and total weight of the electronic device are greatly reduced. In addition, studies in an effort to make with a whole new electrical device such as a flexible display and transparent display have done actively in recent years. The flexible display can be

realized by the replacement conventional glass substrate for the FPD by flexible substrate. Transparent display can be realized by using transparent materials for all components or layout changing of a backlight in the case of the LCD. These next-generation displays will create a new application field and market.

1.2 Thin Film Transistor

Transistor is categorized as bipolar transistor or field-effect transistor (FET). Thin film transistor (TFT) is a kind of a metal-oxide-semiconductor (MOS) FET and generally used for pixel switching devices of active matrix-FPDs such as LCD and OLED displays. **Figure 1.2** shows the LCD used for cellphone and schematic design of typical structure of top-gate type TFT for pixel switching of the LCD. In the LCD, the transmission or blocking of backlight at each pixel controlled by switching of TFT makes image. When TFT becomes on-state, the backlight transmits through color filter on LC layer and pixel substrate. The on/off control by each TFT on numerous pixels describes image.

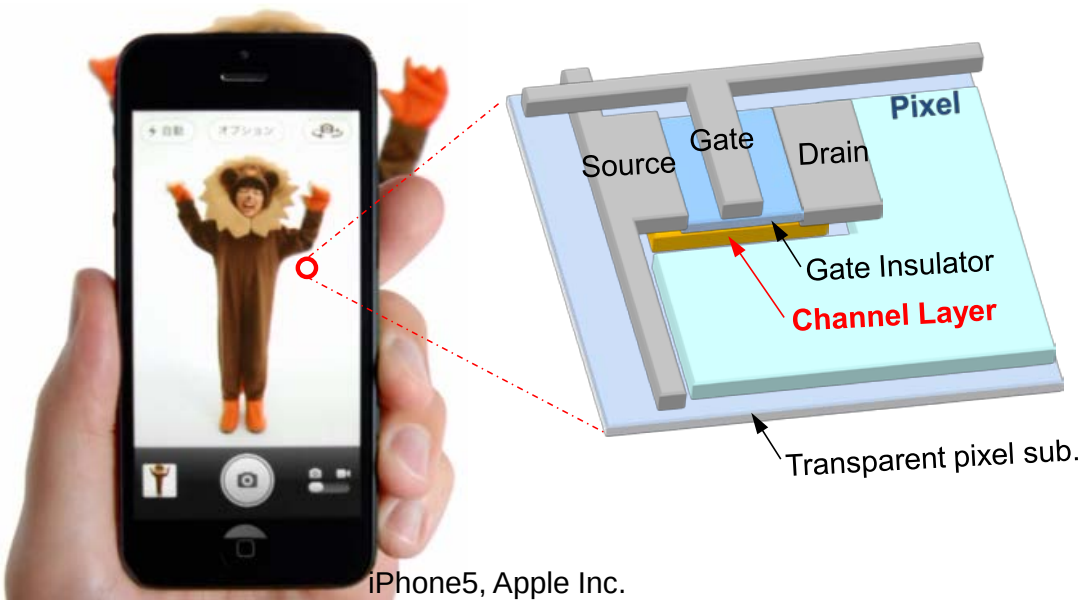

Figure 1.2: LCD used for cellphone and schematic of top-gate type TFT on pixel substrate.

The world's first investigation about TFT was proposed by Lilienfeld from Leipzig Univ. in 1930 as a patent [3] for the purpose of a replacement of expensive vacuum tubes for the control of electric current. The structure which he suggested was functional thin film materials and three electrodes on glass substrate. In 1934, Heil in Germany had a patent application on three-terminal amplifying element [4]. His device has semiconductor material and gate insulator which are basic component of today's TFT. However, either device did not show device operation. In 1947, Bardeen and Brattain from Bell Laboratories developed a point-contact transistor. Next year, Shockley from Bell Laboratories reported a theory related to the bipolar transistor. Thereafter studies about transistors had been investigated actively. In 1960, the basic MOSFET structure using the first device-quality Si-SiO_2 system was proposed by Atalla. Subsequently, the first MOSFET was reported by Kahng and Atalla in 1960.

The first practical TFT was reported by Weimer from RCA Laboratories in 1961 [5]. His TFT composed of microcrystalline cadmium sulfide (CdS) semiconductor layer, gate dielectric layer, and three gold (Au) electrodes, and all films were deposited by evaporation on the glass substrate. Although TFT using II-VI chalcogenide compound semiconductor materials are under investigated actively, these materials have several problems about controllability of film quality, difficulty in fabrication of n-type TFT, and their toxicities.

In 1975, Spear *et. al.* from Dundee Univ. investigated a hydrogenated a-Si (a-Si: H) thin film formed by a glow discharge method [6, 7], and they reported the TFT with good switching performance using the a-Si: H film as channel material in 1979 [8]. These reports provide significant turning point in the TFT development, because their a-Si: H thin films formed by glow discharge method had many superior features complies with semiconductor processes: scalability, large-area uniformity, reproducibility, stability, and safety. Furthermore, the a-Si: H film can be formed at low-temperature (<300°C) which makes available inexpensive and transparent glass substrate. From these reasons, the a-Si: H TFT had been generally used for the pixel switching of LCD for a long time. In 1971, Lechner from RCA Laboratories proposed TFT-driven display device using liquid crystal; active-matrix LCD [9]. After that, development race of TFT-driven LCD has continued in worldwide.

1.3 Low-Temperature Polycrystalline Silicon Thin Film Transistor

1.3.1 Potential of low-temperature polycrystalline silicon thin film transistor

It is well known that the device performance of TFT is significantly affected by electrical characteristics of its channel material. **Table 1.1** shows characteristics comparison of various channel materials of already commercialized TFT. Although the a-Si: H thin film had been a major channel materials for TFT for long times due to its good uniformity and scalability, its application to higher-definition and shorter response time display is difficult because of its poor mobility less than 1 cm^2/Vsec [10]. Oxide semiconductors represented by amorphous indium-gallium-zinc-oxygen (a-IGZO) investigated by Nomura *et. al.* in 2003 [11] are one of candidates for post-a-Si: H. Electronic manufacturer such as Sharp Corp. began commercial production of LCD panels using oxide TFT from 2012. On the other hand, the oxide TFT has issues of poor stability in film quality against processes, an insufficient of mobility for driving OLED (~50 cm^2/Vsec), and the difficulty of miniaturization and fabrication of p-channel type TFT.

The polycrystalline silicon (poly-Si) thin film has been used in semiconductor

devices such as active layer and electrode, because of great electrical characteristics and controllability of valence-electron density by an ion doping. Poly-Si TFT has big advantage on a device miniaturization because the poly-Si TFT can be fabricated by using self-aligned process. Furthermore, the p-channel type TFT can be fabricated by using the poly-Si films because of its high hole mobility. In the TFT field, the poly-Si is categorized as high-temperature poly-Si (HTPS) or low-temperature polycrystalline silicon (LTPS) by the difference in process temperature. The HTPS TFT and HTPS TFT display were available earlier than LTPS TFT [12, 13], because the HTPS TFTs can be formed by utilizing Si large-scale integration (LSI) technology. Since the HTPS TFTs are fabricated at 800-1000°C by furnace annealing, quartz glass is generally used for TFT substrate. Therefore, the mobility of HTPS TFT is usually higher than that of other TFTs. On the other hand, process cost of HTPS TFT is much higher than that of other TFTs. The LTPS is generally formed by laser annealing around several hundred degrees Celsius, and LTPS TFTs have greater field-effect mobility (>50 cm^2/Vsec) [14-17] than other channel materials. Because the maximum processing temperature of LTPS TFT fabrication is less than 600°C, LTPS TFT can be fabricated on inexpensive and low heat resistance glass substrates such as non-alkali glass. Consequently, the LTPS TFT has the applicability to not only high-performance pixel switching devices but also driver circuit or memory, that is, the system-on-panel display can be realized.

Table 1.1: Feature comparison of various channel materials of commercialized TFT.

	a-Si: H	LTPS	Oxide
Mobility [cm^2/Vsec]	<1	**50-300**	5-30
Processing temperature	~300°C	500-600°C	~350°C
Uniformity	○	△	○
Stability	×	◎	△
Scalability	○	△	○
Miniaturization	△	◎	△
Transistor	n-type	**n-type and p-type**	n-type

In recent years, several studies have been conducted in order to achieve further low-temperature fabrication of LTPS TFTs for the use of flexible plastic substrates [18-20]. Fabrication of LTPS TFTs at super low-temperature achieves high-definition display, multiple function display, or system on panel using flexible plastic films. However, there are some high-temperature annealing processes in the LTPS TFT fabrication as shown in **Table 1.2**. Process temperature of these annealing exceeds 200°C and it is too high to use typical plastic substrates. Therefore, super low-temperature annealing technique are required for the realization of LTPS TFTs on the plastic substrates. In the **Table 1.2**, the gate-SiO_2 deposition is also categorized as high-temperature process over 200°C, because the tetra-ethyl-ortho-silicate chemical vapor deposition (TEOS CVD) method is generally used in industrial method. High-temperature around 300°C is needed to form CVD SiO_2 films which have good interfacial characteristics. On the other hand, Serikawa *et. al.* report that sputtered SiO_2 films formed below 200°C can be applied for gate-SiO_2 of the LTPS TFT [21-23].

Kobayashi *et. al.* report that SiO_2 films formed by the nitric acid oxidation of Si (NAOS) method below 120°C also can be used for gate-SiO_2 of the LTPS TFT [24-26]. Therefore, temperature reduction of the crystallization, the activation of dopant ion, and the inactivation of electrical defects has been demonstrated in this study.

Table 1.2: General fabrication process of self-aligned LTPS TFT.

	Process	Method	Temperature
1	Crystallization to poly-Si	laser annealing	300-400°C
2	Channel patterning	Dry etching	RT
3	Gate-SiO_2 deposition	CVD	~300°C
4	Gate-electrode formation	Vacuum evaporation or sputtering	RT
5	Source/drain region formation	Ion doping	RT
6	Activation of dopant ion	Furnace annealing	500-600°C
7	Formation of contact hole	Wet etching or dry etching	RT
8	Source/drain electrodes formation	Vacuum evaporation or sputtering	RT
9	Inactivation of electrical defects	Furnace annealing	~400°C

High-temperature process definitely over 200°C is typed in red.

1.3.2 Electrical characterization of polycrystalline silicon

The poly-Si is composed of many single-crystalline silicon grains which have different crystal orientation and grain size of several hundred nanometers. It is reported that the poly-Si film has many electrical defects at grain boundaries [27]. These electrical defects hinder carrier

transport from the source to the drain by the increasing of the Coulomb scattering, and cause a marked reduction in field-effect mobility. In recent years, the channel size of LTPS TFT has been decreasing owing to the device miniaturization. In addition, local high-defect and low-defect density regions coexist in the channel layer. It is very important to investigate the location of electrical defects and evaluation of its electrical properties for improving the electrical performance of LTPS TFTs. On the other hand, device characterization only provides averaged data with grain and grain boundary in channel region. Moreover, device properties are also affected by electrical defects at the interface between channel and gate-oxide layers. Furthermore, a long time and many processes are needed for the fabrication of device structure as shown in **Table 1.2**.

1.4 Outline of This Thesis

In this thesis, new laser annealing method toward the super low-temperature fabrication of high-performance LTPS TFT has been studied. The annealing method is applied to some high-temperature annealing processes intended to fabricate the TFT at super low-temperature, which make transparent flexible plastic film usable for the TFT substrate. In addition, new electrical characterization method with the purpose of the understanding of the local electrical property of the poly-Si films has been proposed. Electrical characterization, which is able to

distinguish electrical property of grain from that of grain boundary, is demonstrated.

In chapter 2, local electrical characterization using atomic force microscopy (AFM) technologies has been proposed in order to evaluate electrical properties of grain and grain boundary of the poly-Si in sub-micrometer scale. Behavior of carriers at defect sites in the poly-Si film and the change in probe current by repeating scan is determined using AFM measurements. In addition, effects of hydrogen termination on local electrical properties of the poly-Si have been determined.

In chapter 3, an underwater laser annealing (WLA) as a laser annealing technique for super low-temperature fabrication of LTPS TFTs is proposed. The crystallization of a-Si thin films on glass and plastic substrates has been performed by WLA and conventional laser annealing technique. Impact of WLA on grain growth, temperature reduction, and electrical properties of poly-Si thin films has been investigated.

In chapter 4, WLA techniques have been applied to other high-temperature processes for LTPS TFT fabrication with the purpose of the realization of electrical devices on flexible plastic films. The dopant activation and inactivation annealing treatments by WLA has been studied. From device characterization, the possibility of the application of WLA to dopant activation and inactivation treatments has been discussed.

In chapter 5, LTPS TFTs using the poly-Si thin film formed by WLA as the channel layer are fabricated and characterized. LTPS TFTs using LA poly-Si films are also fabricated.

Comparison of the TFT characteristics comparison between WLA and LA poly-Si films are discussed.

In chapter 6, conclusions and suggestions for future work are presented.

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Chapter 2

Observation of Local Electrical Properties of Polycrystalline Silicon Thin Films by Atomic Force Microscopy

2.1 Introduction

Figure 2.1 shows schematic illustrations of **(a)** cross-sectional device structure and **(b)** diagram of carrier transport on the poly-Si surface in the case of TFT characterization for LTPS TFT. The poly-Si is composed of many single-crystalline silicon grains which have different crystal orientation. It is reported that there are many electrical defects at the SiO_2/poly-Si interface and grain boundaries in poly-Si film [1-3]. These electrical defects hinder carrier transport from the source to the drain, and cause a marked reduction in field-effect mobility or change in threshold voltage [4, 5]. Furthermore, in the case of poly-Si film has small grain size around several dozen nanometers, carrier transport is also inhibited in grain. Recently, the channel length of TFTs has been decreasing owing to the miniaturization of device technology. In addition, local high-defect and low-defect density regions coexist in the channel layer of TFTs. Consequently, the investigation of the location of electrical defects in the poly-Si film and evaluation of its electrical properties are very

important in order to improve the electrical performance of LTPS TFTs. However, device characterization only provides average data with grain and grain boundary in channel region. Moreover, device properties are also affected by electrical defects at the interface between channel and gate-oxide layers. Many fabrication processes and complicated-device structure make it difficult to understand electrical properties of the poly-Si film.

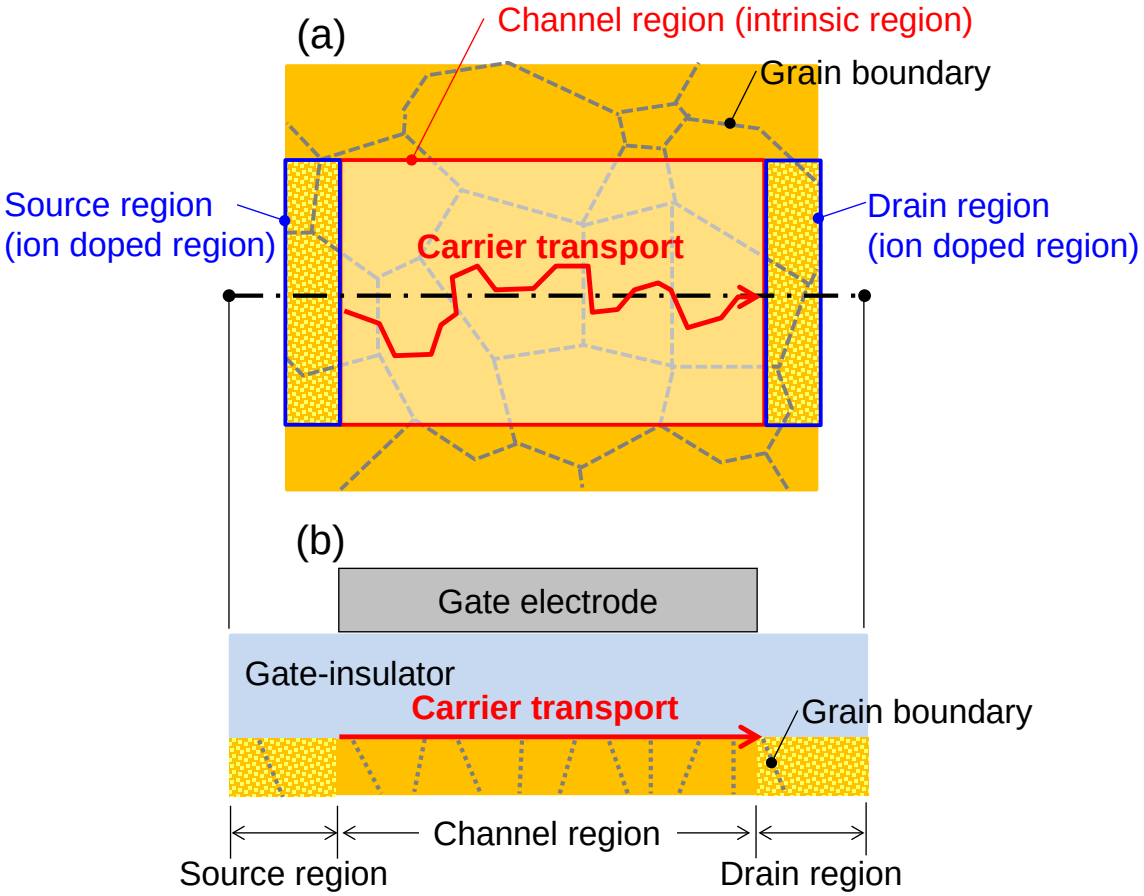


Figure 2.1: Schematic illustration of (a) diagram of carrier transport on poly-Si surface and (b) cross-sectional device structure in the case of TFT characterization. Gray dashed lines indicate grain boundary of the poly-Si. Grain size of the poly-Si for LTPS TFT is typically several hundred nanometers, and the channel length and channel width are several micrometers.

In this chapter, local electrical properties of the poly-Si films are observed by using conductive atomic force microscopy (C-AFM) and Kelvin probe microscopy (KFM), which are a powerful tool for measuring nanometer-scale electrical characteristics. The surface topography and current or surface potential images of the poly-Si films are simultaneously obtained by C-AFM or KFM. From these measurements, conduction mechanism of grain and grain boundary has been studied. In addition hydrogenation effects on local electrical properties of the poly-Si films are investigated. C-AFM measurements of the poly-Si were performed before and after inactivation treatment by the hot-wire method.

2.2 Electrical Properties of Polycrystalline Silicon Thin Films after Device Fabrication

2.2.1 MOSFET mobility

The location of the carriers near the oxide-semiconductor interface introduces additional scattering mechanisms like Coulomb scattering from oxide charges and interface states, as well as surface roughness scattering, reducing the MOSFET mobility below the bulk mobility [6] such as the conductivity, Hall, and magnetoresistance mobility.

Effective mobility

When considering an n-channel MOSFET of gate length L and width W, the drain current I_D is a combination drift and diffusion currents

$$I_D = \frac{W\mu_{eff} Q_n V_{DS}}{L} - W\mu_{eff} \frac{kT}{q} \frac{dQ_n}{dx} \tag{2.1}$$

where Q_n is the mobile channel charge density [C/cm^2], and μ_{eff} the effective mobility, usually measured at drain voltages of typically 50-100 mV. Lower source-drain voltage V_{DS} is better, because then the channel charge is more uniform from source to drain, allowing the diffusive second term in Eq. (2.1) to be dropped. Solving for the effective mobility μ_{eff} gives

$$\boxed{\mu_{eff} = \frac{g_d L}{W Q_n}} \tag{2.2}$$

where the drain conductance g_d is defined as

$$g_d = \left. \frac{\partial I_D}{\partial V_{DS}} \right|_{V_{GS}=const.} \tag{2.3}$$

Two approaches in order to determine Q_n are commonly used. In the first, the mobile channel charge density is approximated by

$$Q_n = C_{ox}\left(V_{GS} - V_{th}\right) \tag{2.4}$$

Although channel charge exists in the sub-threshold region below threshold voltage V_{th}, the expression V_{GS}-V_{th} ensures the device operation in the above-threshold, drift-limited regime Nevertheless, this approach has some deficiencies. The first is that the channel charge density is not exactly given by Eq. (2.4). Second, the threshold voltage is not necessarily well known and C_{ox} is not strictly the oxide capacitance/unit area. It is an effective oxide capacitance

taking into account poly-Si gate depletion and the fact that the inversion layer resides slightly below the SiO_2/Si interface. Both effects introduce additional series capacitances.

Field-effect mobility

The field-effect mobility is determined from the transconductance, defined by

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=const.} \tag{2.5}$$

The drift component of the drain current with $Q_n = C_{ox}(V_{GS} - V_{th})$ is

$$I_D = \frac{W}{L}\mu_{FE} C_{ox}(V_{GS} - V_{th})V_{DS} \tag{2.6}$$

When the field-effect mobility is determined, the g_m is usually taken to be

$$g_m = \frac{W}{L}\mu_{FE} C_{ox} V_{DS} \tag{2.7}$$

When this expression is solved for the mobility, it is known as the field-effect mobility

$$\boxed{\mu_{FE} = \frac{L g_m}{W C_{ox} V_{DS}}} \tag{2.8}$$

The μ_{FE} is generally lower than the effective mobility [7]. This is rather disturbing, since it is the same device measured under identical bias conditions. This discrepancy between μ_{eff} and μ_{FE} is due to the neglect of the electric field dependence of the mobility in the derivation of Eq. (2.8) [8, 9]. Considering the μ_{eff} dependence on gate voltage, gives the transconductance

$$g_m = \frac{W}{L}\mu_{eff}C_{ox}V_{DS}\left(1+\frac{(V_{GS}-V_{th})}{\mu_{eff}}\frac{d\mu_{eff}}{dV_{GS}}\right) \tag{2.9}$$

and the field-effect mobility becomes

$$\mu_{FE} = \frac{Lg_m}{WC_{ox}V_{DS}\left(1+\frac{(V_{GS}-V_{th})}{\mu_{eff}}\frac{d\mu_{eff}}{dV_{GS}}\right)} \tag{2.10}$$

Since $d\mu_{eff}/dV_{GS} < 0$, it is obvious that Eq. (2.10) gives a higher than Eq. (2.8).

2.2.2 Discussion

These electrical characterization methods described previously are performed after device fabrication using multiple steps. These processes complicate the understanding of electrical property of target material. For example, processes of deposition of gate-insulator layer on target channel layer, ion doping to contact region, formation of electrodes, and post-metalization annealing are necessarily for the MOSFET mobility measurements. However, these processes create new electrical defects or might change initial property of target material. Moreover, it is very difficult to determine sub-micrometer-scale characterization, which is important for the understanding of poly-Si's characteristics by using device characteristics. New local and simple electrical characterization is required for realization to distinguish grain boundary from grain in the poly-Si and better understanding.

2.3 Electrical Properties of Polycrystalline Silicon Thin Films as Crystallized

For the discussion of the energy band diagram, symbol shown in **Table 2.1** was used.

Table 2.1: List of symbols

Description	Symbol	Value
Vacuum level	E_{VAC}	0 eV
Elementary charge	q	1.6×10^{-19} C
Work function of PtIr	$q\phi_m$	5.7 eV [14]
Fermi energy level of PtIr	E_{VAC}-E_{Fm}	5.7 eV
Work function of Si	$q\phi_{Si}$	4.7 eV
Electron affinity of Si	$q\chi_{Si}$	4.1 eV
Conduction band minimum of Si	E_{VAC}-E_{CSi}	4.1 eV
Valence band maximum of Si	E_{VAC}-E_{VSi}	5.3 eV
Energy band gap of Si	E_{gSi}	1.1 eV

2.3.1 Scanning probe microscopy

Since development of a scanning tunneling microscopy (STM) by G. Binning and H. Rohre at IBM Zürich in 1982 [10, 11], various scanning probe microscopy (SPM) methods have been created with the concept of “observation of atomic arrangement and/or electronic states by an approximation of tiny probe to sample surface”. I would like to describe about C-AFM and KFM used in this experimental.

Figure 2.2 shows a schematic illustration of conventional SPM measurement system. Local variation of physical quantity is detected by the approximation of tiny probe to sample surface. The measured quantity is maintained constant by feedback control of elasticized piezoelectric device in a vertical direction (*z* direction). The SPM image on sample surface can be obtained by scanning with applying a scanning voltage to piezoelectric devices of in-place direction (*x*, *y* direction) at the same time. Especial measuring system and methods are necessary for the acquisition of measuring physical quantity such as tunneling current, atomic force, and so on.

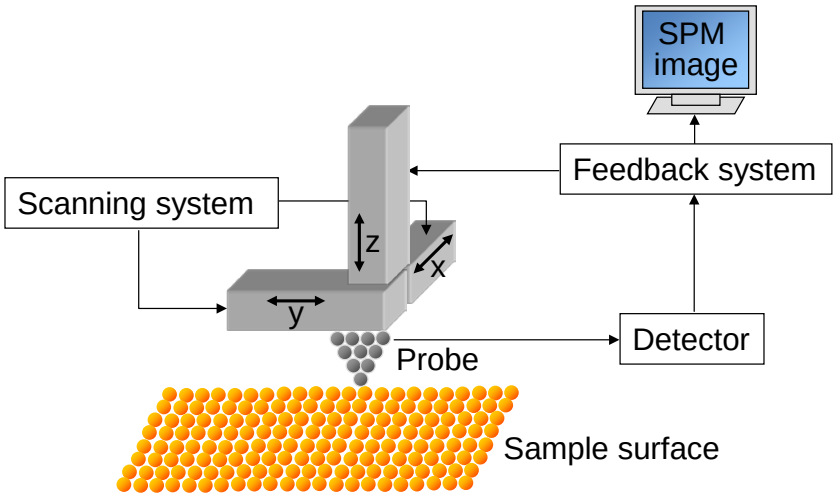


Fig. 2.2: Schematic illustration of general measuring system for SPM.

STM observes physical quantity such as atomic arrangement or electronic state of sample surface by approach of acuminated conductive probe in atomic scale called “cantilever”. Because STM observes the tunneling current between cantilever and sample,

STM is only available for conductive sample. On the other hand, AFM is available for conductive and non-conductive samples, because AFM observes atomic force between the cantilever and sample. In the AFM, surface topography images can be obtained by calculation vertical displacement of the cantilever during scanning of the cantilever on sample surface in contact or maintain a constant spacing. Typical measuring methods of surface topography in AFM are as follows.

Contact mode

In a contact mode, scanning of the cantilever is performed in contact with sample surface. The vertical displacement of the cantilever is detected as reflected laser beam from tabular part of the cantilever by a photo diode. If the cantilever approaches sample surface, the cantilever contacts on surface atomic layer of sample by atomic force with distortion of the cantilever and then, an angle of reflected laser changes resulting that a difference in photovoltaic power. Surface topography can be obtained by feedback control which cancel out the difference in photovoltaic power, that maintains a constant displacement of the cantilever.

Dynamic mode

In a dynamic mode, non-contact scanning of the cantilever is performed with vibrating of the cantilever at resonant frequency. The dynamic mode is available for breakable sample such as

biological sample, weakly-absorbed matter, and so on. In addition, the dynamic mode can be carried out in liquid.

Non-contact mode

A non-contact mode is a sort of the dynamic mode. In this mode, the tip of the cantilever does not contact the sample surface. The cantilever gets close up to sample surface in several nanometers with the vibrating of self-induced vibration cantilever at resonant frequency. The difference in resonant frequency of the cantilever, which is induced by an interatomic interaction between the cantilever and sample, is detected, and the scanning of the cantilever is performed with canceling out the difference in resonant frequency by a frequency modulation.

Tapping mode

This mode is also a kind of dynamic mode. The scanning of the cantilever is performed with forced vibrating at fixed value around resonant frequency. In this mode, the tip of the cantilever contacts the sample surface in a part of vibration period of the cantilever which is caused a repulsive interaction. Detected difference in vibration amplitude generated due to the repulsive interaction is controlled by an amplitude modulation.

2.3.2 Conductive-atomic force microscopy

AFM has two typical advantages below,

- Available for non-conductive sample
- Various forces such as electrostatic force, frictional force, magnetic force, etc. can be measured

However, AFM has disadvantage below,

- Information on conductivity of sample surface is not available

For these reasons, new measuring method, which provides surface topography and STM current images simultaneously at the same observation area, is desired. C-AFM is developed according to this request by combination STM and AFM. In the C-AFM, a bias voltage is applied to sample during contact of the conductive cantilever with the sample surface as shown in **Fig. 2.3**. In this time, a probe current which flows between the tip of the cantilever and the sample is observed by the current-voltage amplifier circuit. Thus, C-AFM can be observed current-voltage characteristic or two dimensional current distribution images with surface topography at the same area simultaneously.

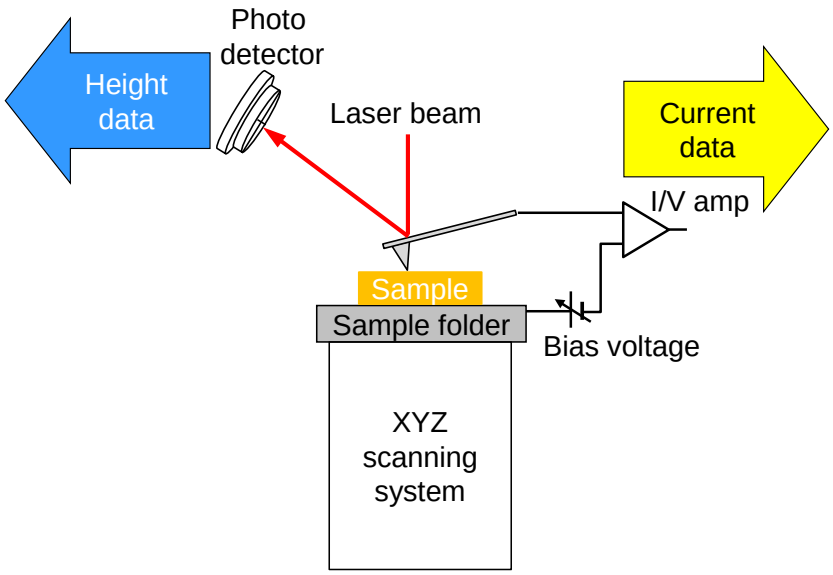


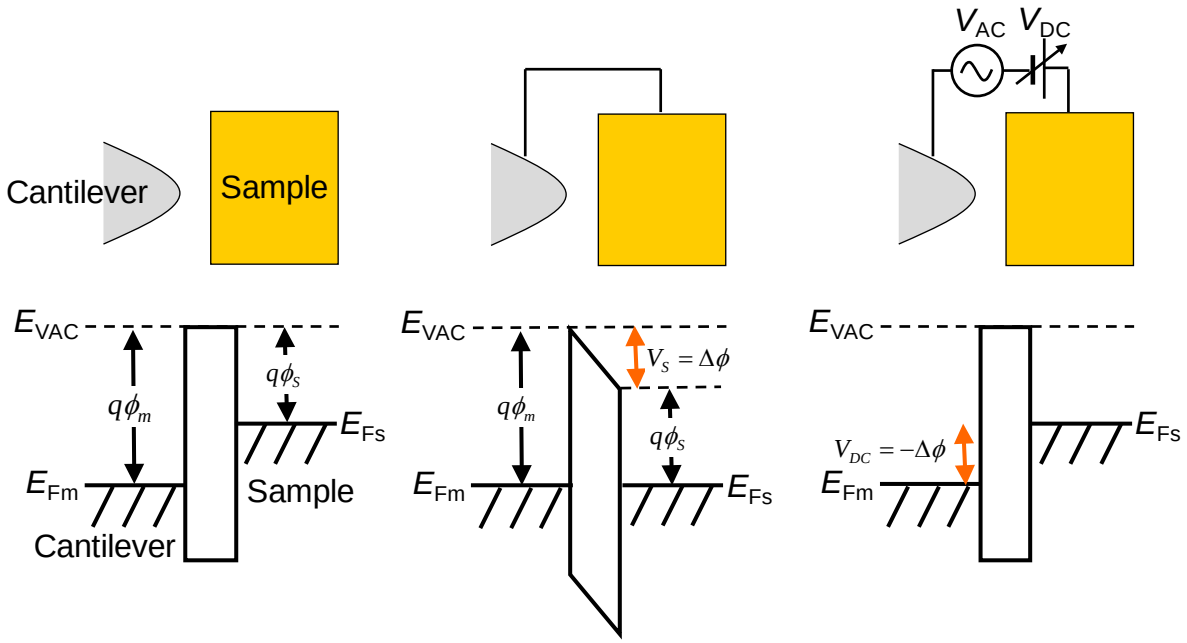
Figure 2.3: Schematic illustration of measuring system for C-AFM.

2.3.3 Kelvin force microscopy

KFM was invented by M. Nonnenmacher *et. al.*, in 1991 [12]. With KFM, surface topography and surface potential images can be observed at atomic or molecular scale by detecting electrostatic force between the cantilever and the sample surface. Surface potential is defined as the energy required for pull out an electron from Fermi level and put it in vacuum level. Surface potential is depend on material and its surface conditions.

Figure 2.4 shows an energy band diagram between the cantilever and sample for KFM measurements. Before the junction of the cantilever and the sample surface as shown in **Fig. 2.4 (a)**, each surface potential ϕ_m and ϕ_S is represented as $q\phi_m = |E_{VAC} - E_{Fm}|$ and $q\phi_S = |E_{VAC} - E_{FS}|$.. After the junction of the cantilever and the sample surface as shown in **Fig. 2.4**

(b), the cantilever has Fermi level equal to the sample. Therefore, the difference in surface potential $V_S = q|\phi_m - \phi_S|$ is generated by surface charge induced on the cantilever and the sample surface.



(a) Before junction (b) After junction (c) V_{AC} & V_{DC} application

Figure 2.4: Energy band diagram between the cantilever and sample for KFM measurements.

Next, the cantilever is forcibly vibrated by applying the alternating current voltage V_{AC} to the cantilever at the resonant frequency ω_r as shown in **Fig. 2.4 (c)**. The ω_r changes due to the difference in potential of the sample surface, and this change is canceled out by feedback to direct-current voltage V_{DC}. In the applying V_{DC} and V_{AC} at ω_m as shown in **Fig. 2.4 (c)**, the electrostatic force F is defined by the equation (2.12) as follows,

$$F = -\frac{1}{2}\frac{\partial C}{\partial Z}\left(V_S + V_{DC} + V_{AC}\cos\omega_m t\right)^2 \quad (a)$$
$$= -\frac{1}{2}\frac{\partial C}{\partial Z}\left\{\left(V_S + V_{DC}\right)^2 + 2\left(V_S + V_{DC}\right)V_{AC}\cos\omega_m t + {V_{AC}}^2\cos^2\omega_m t\right\} \quad (b) \qquad (2.12)$$
$$= -\frac{1}{2}\frac{\partial C}{\partial Z}\left\{\left(V_S + V_{DC}\right)^2 + 2\left(V_S + V_{DC}\right)V_{AC}\cos\omega_m t + {V_{AC}}^2\frac{\cos 2\omega_m t + 1}{2}\right\} \quad (c)$$

C: capacitance between the cantilever and the sample

Z: distance between the cantilever and the sample

In the equation (2.12-c), first member, second member, and third member indicates an static attraction force between the cantilever and sample, force from alternating electric field induced by surface charges, and electrostatic force between the cantilever and sample generated by V_{AC}, respectively. By feedback controlling of V_{DC} for cancelling out V_S; $V_S + V_{DC} = 0$, the difference in surface potential between the cantilever and the sample surface is calculated as $V_S = -V_{DC}$. In the KFM measurements, the cantilever does not contact to the sample surface at all times, because *F* does not become 0 if $V_S + V_{DC} = 0$.

2.4 Experimental

In this experimental, poly-Si films on glass substrates formed by conventional XeCl excimer laser annealing (wavelength = 308 nm) was used for C-AFM and KFM measurements. The sample structure of the poly-Si is poly-Si (50 nm)/buffer layers (100 nm-thick SiO_2 on 50

nm-thick SiN_x)/non-alkali glass substrate. **Figure 2.5** shows **(a)** SEM image and **(b)** cross-sectional TEM image, and **(c)** surface topography of the poly-Si film used for experiments. Before SEM observation, the poly-Si sample was etched by Secco-etching [13] and 10 nm-thick Pt film was deposited on Secco-etched poly-Si surface. The average grain size of crystallized poly-Si films was approximately 300 nm, and the root mean square (rms) of the surface roughness of the films was 11 nm. As shown in **Fig.2.5 (b, c)**, a prominent ridge at grain boundary was clearly observed. Thus, grain boundaries can be determined.

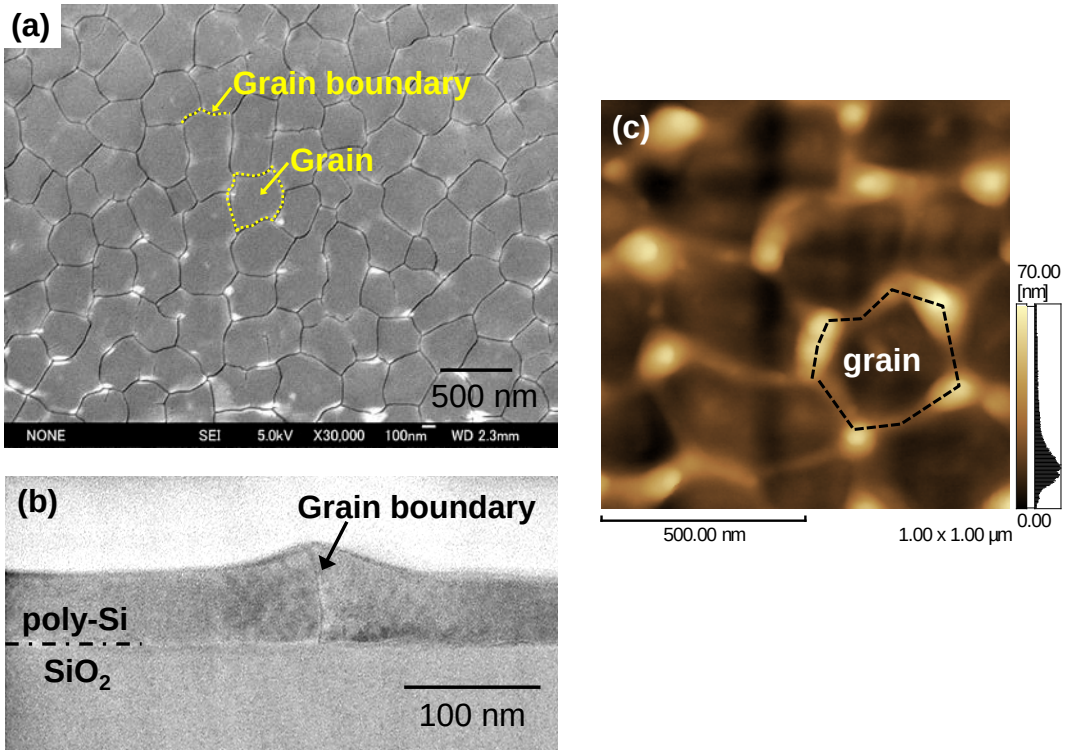


Figure 2.5: (a) SEM image, (b) cross-sectional TEM image, and (c) surface morphology image obtained by AFM of ELA poly-Si film. Selective etching of grain boundaries was carried out by using Secco-etching for SEM measurements.

Figure 2.6 shows a schematic illustration of experimental setup for C-AFM and

KFM measurements. C-AFM measurements were performed using Shimadzu SPM-9600 with a platinum-iridium (PtIr)-coated Si cantilever (NanoWorld, CONTPt) at a constant sample voltage (V_{sub}) of -1.0 V or -2.0 V. Before C-AFM measurements, native oxide and/or thermally oxidized SiO_2 film on the poly-Si films was removed using a buffered hydrogen fluoride (BHF) solution. Surface topography and corresponding current images were simultaneously obtained by C-AFM at room temperature in air ambient. The sample holder, to which the sample voltage was applied, was electrically connected to the poly-Si films by a conductive paste. Thus, the V_{sub} was applied between the cantilever and the poly-Si. KFM measurements were performed before and after C-AFM measurements at the same area of samples in order to observe the change in surface potential due to C-AFM measurements. KFM measurements were also performed using Shimadzu SPM-9600 with the PtIr-coated Si cantilever (NanoWorld, EFM) at a sample voltage (V_{AC}) of 1.5 V. A resonance frequency of the cantilever was 75 kHz. Surface topography and corresponding surface potential images were simultaneously obtained by KFM at room temperature in air ambient.

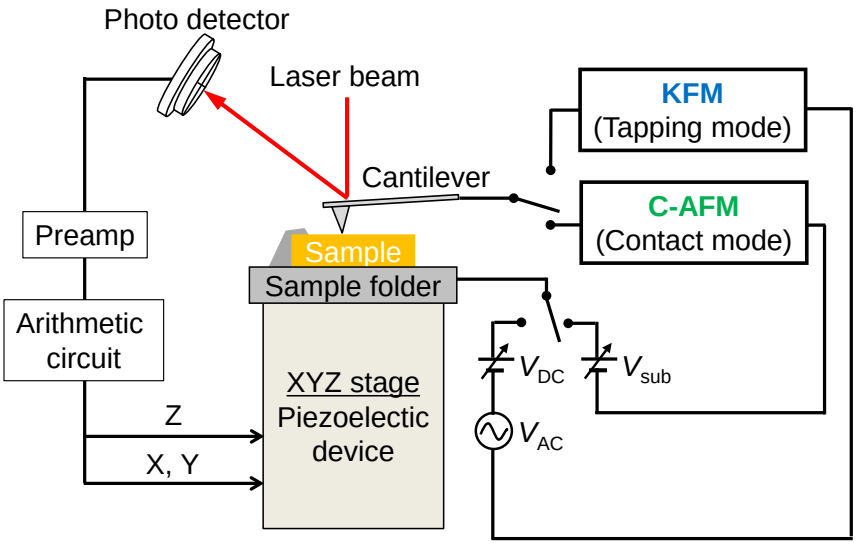


Figure 2.6: Schematic illustration of experimental setup for C-AFM and KFM measurements.

For evaluation of change in conductivity due to termination of electrical defects within the poly-Si samples, hydrogenation was carried out. **Figure 2.7** shows a schematic illustration of experimental setup for hydrogen termination of poly-Si samples. The hydrogen termination of the poly-Si films was performed for 5 min, 10 min (5 min×2), 20 min (5 min×4) by a hot-wire method [15]. Atomic hydrogen was generated by the thermal separation of H_2 gas due to contact with a high-temperature tungsten filament in a vacuum chamber. The poly-Si film surface was exposed to the atomic hydrogen in a vacuum chamber to terminate the poly-Si surface. The base pressure of the chamber was 3.0×10^{-5} Pa, and the H_2 gas pressure was 1.0×10^{-1} Pa. The substrate temperature of the poly-Si films was changed from 200°C to 400°C. Before and after hydrogen termination, native oxide on the films was removed using a BHF solution.

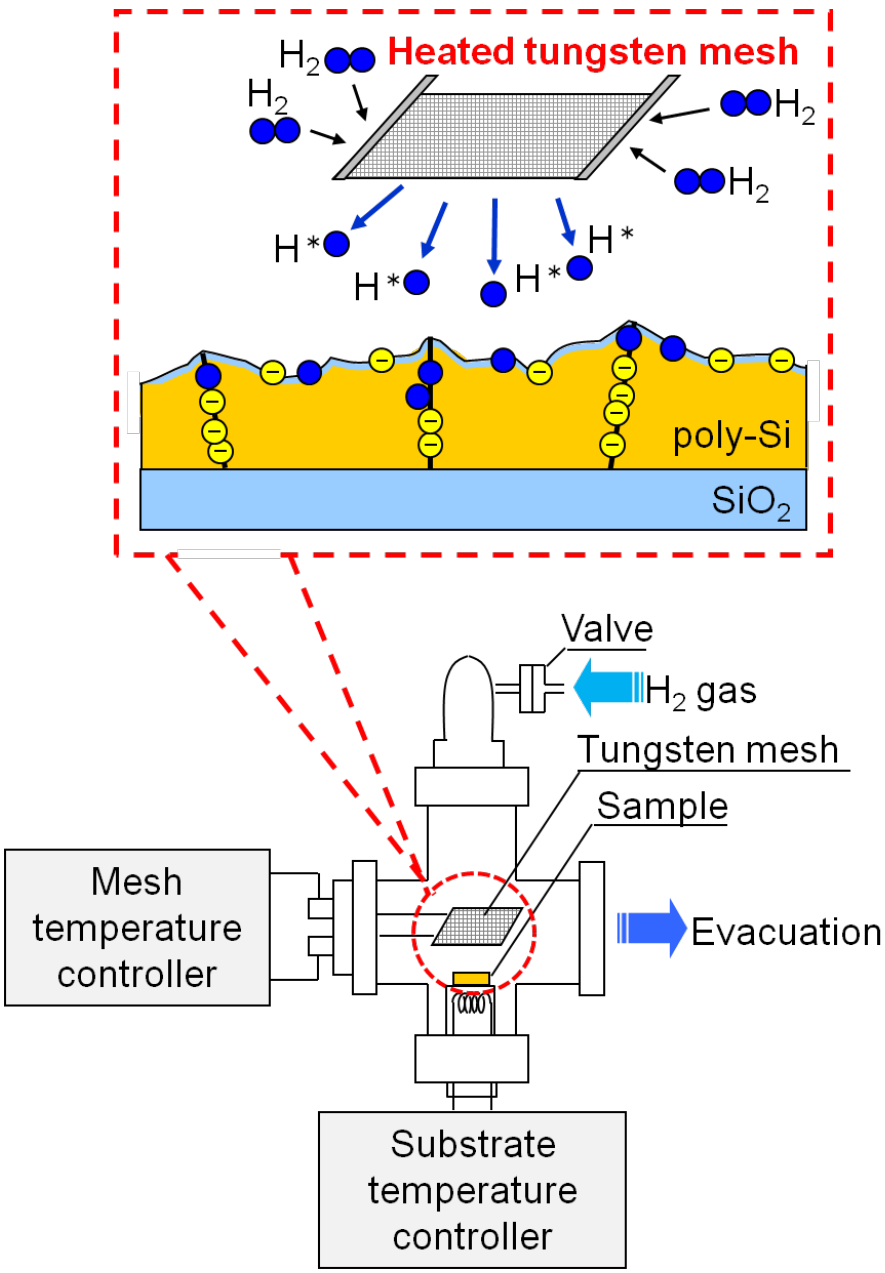


Figure 2.7: Schematic illustration of experimental setup for hydrogen termination by hot-wire method.

2.5 Behavior of Electron at Electrical Defects within Polycrystalline Silicon Thin Films

2.5.1 Conduction mechanism of grain and grain boundary

Figure 2.8 shows the surface topography, first and fourth scanning current images of the poly-Si thin film before hydrogen termination taken at the V_{sub} of **(a)** -1.0 V or **(b)** -2.0 V. The white dotted lines in surface topography show grain boundaries. Surface topography and current images were simultaneously obtained at the same scanning area. In the case of the V_{sub} of -1.0 V, current flows only at grain boundary, and change in probe current in grain and grain boundary is very small. In contrast, in the case of V_{sub} of -2.0 V, the probe current flows not only at grain boundary but also at grain in the first current image shown in **Fig. 2.8 (b_2, b_3)**. The change in probe current of grain is larger than that in the case of V_{sub} of -1.0 V. In this experiment, the V_{sub} was set to -2.0 V in order to observe the change in probe current in grain as well as that of grain boundary.

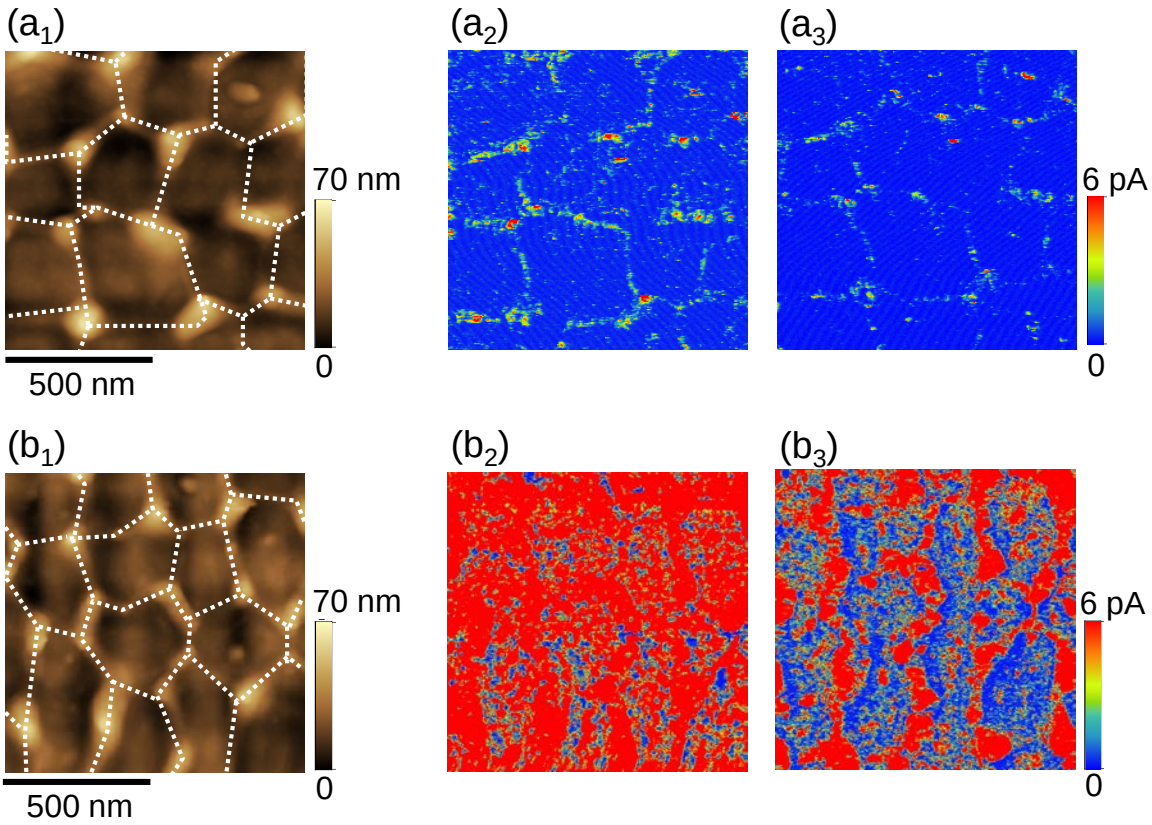


Figure 2.8: C-AFM images: (a_1, b_1) Surface topography and current images of (a_2, b_2) first and (a_3, b_3) fourth scanning of non-hydrogenated poly-Si thin films. The V_{sub} was (a) -1.0 V and (b) -2.0 V. The white dotted lines on surface topography show grain boundaries of the poly-Si surface.

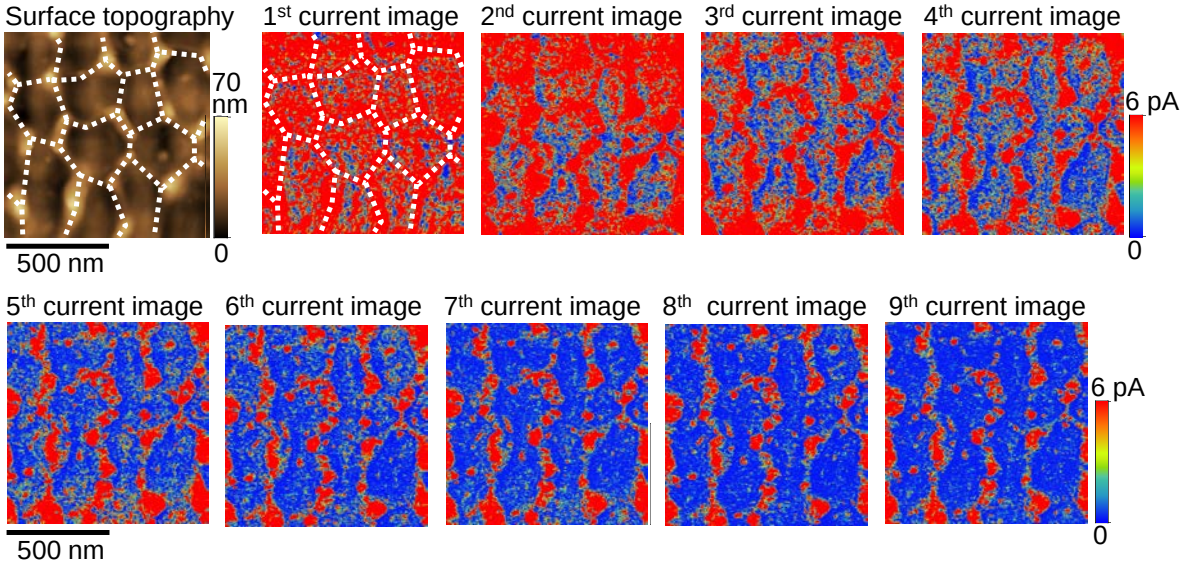


Figure 2.9: C-AFM images: Surface topography and current images of non-hydrogenated poly-Si thin film at the V_{sub} of -2.0 V. White dotted lines show grain boundaries of the poly-Si.

Figure 2.9 shows the surface topography and current images of the poly-Si thin film before hydrogen termination taken at the V_{sub} of -2.0 V. In the current image of first scanning, conductive regions covered the entire surface of the poly-Si film. Conductive regions in grain significantly decreased in area with an increase in the number of scans to 4th repeated scan, and conductive regions in grain boundary almost unchanged. It is expected that the conduction mechanism of grain differ from that of grain boundary. After changing the measuring area in order to obtain a new first scanning image, new conductive regions were successfully observed, similar to those shown in **Fig. 2.9**. Thus, we concluded that the area of the conductive regions is not reduced by the degradation of the cantilever, but rather based on the change of conductivity of the poly-Si film. It is well known that there are many electrical defects such as a dangling bond in grain boundary [16-18]. These suggest that many conductive regions which are low-resistance regions correspond to electrical defects in the poly-Si films.

Focusing on the C-AFM measurements of 1st to 4th scan shown in **Fig. 2.9**, the average probe current of grain drastically decreased from 21 to 3 pA despite of that of grain boundary remained approximately 25 pA. Emitted electrons from grain or grain boundary to the cantilever during 4th repeated C-AFM observation were estimated. As the estimation, emitted electrons from grain boundary at first and fourth scanning were 9.9×10^{17} /cm^2 and 9.7×10^{17} /cm^2, respectively, and total emitted electrons were 3.7×10^{18} /cm^2. These results

indicate that emitted electrons from defects sites at grain boundary during repeating C-AFM observation is much larger than Si atom concentration at 50 nm thickness of 2.5×10^{17} /cm^2. From these results, it is thought that probe current flow continuously due to hopping conduction through many defect sites produced in grain boundary as shown in **Fig. 2.10 (a)**. In contrast, emitted electrons from grain at first and fourth scanning were 8.4×10^{17} /cm^2 and 0.7×10^{17} /cm^2, respectively. Thus, it is thought that almost electrons, which were emitted from grain to the cantilever at first scanning, also flow continuously without emission from defect sites. If there are defect sites in grain, these defect sites should charge positively based on the electron emission from defect sites to the cantilever as shown in **Fig. 2.10 (b)**.

Next, the rise in surface potential due to repeating C-AFM measurements was observed by KFM measurements. **Figure 2.11** shows KFM images measured **(a)** before and **(b)** after 4th repeated C-AFM measurements on non-hydrogenated poly-Si film. Dotted lines show grain boundaries on the poly-Si surface. Measured rise in surface potential of grain and grain boundary was 45 mV and 17 mV, respectively. Consequently, it is concluded that conductive regions in grain decrease with the positive charging of defect sites due to the electron emission as shown in **Fig. 2.10 (b)**.

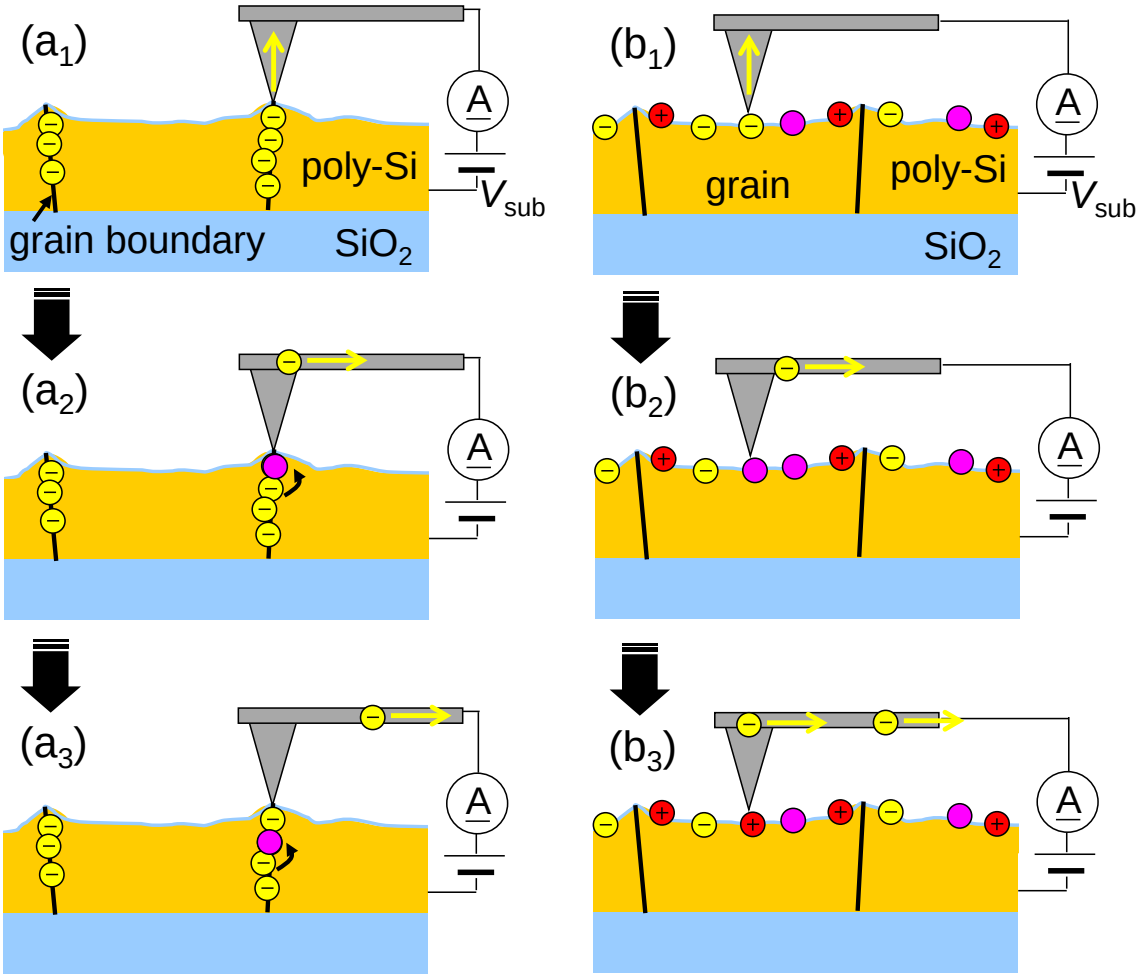


Figure 2.10: Schematic diagram of behavior of electron from the poly-Si to the cantilever during C-AFM measurements at (a_1-a_3) grain boundary and (b_1-b_3) grain.

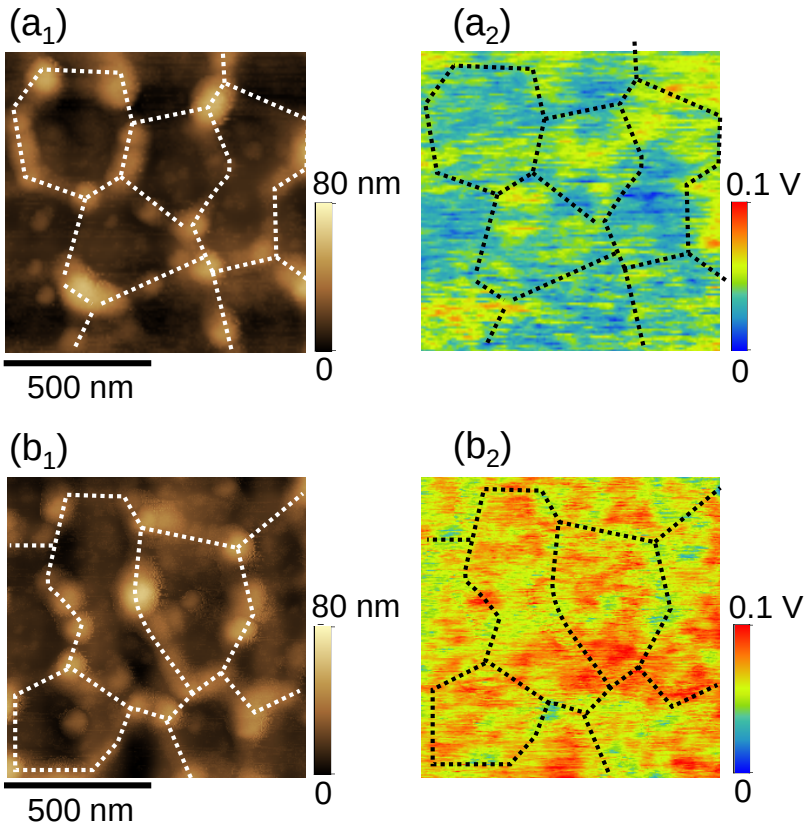


Figure 2.11: KFM images: Surface topography and surface potential images of (a) before and (b) after 4 times C-AFM scan. The dotted lines show grain boundaries of the poly-Si films.

2.5.2 Behavior of electron at electrical defect sites

Focusing on the 7^{th}-9^{th} scanning C-AFM images scan shown in **Fig. 2.9**, the probe current of both grain and grain boundary did not change. However, there are some current spots indicating characteristic behavior in grain as shown in **Fig. 2.12** which is magnified image of **Fig 2.9**. Current spots A_1 and A_2 disappear with the repeating scan as the case of **Fig. 2.11 (b)** discussed above. Disappearance of these current spots might be induced by the positive charging of electrical defect sites. Current spot B remained despite repeating C-AFM scan

indicating that there is a locally high-dense defect region exists in grain. In addition, there are current spots C which repeat disappearance and appearance during C-AFM scan. Behavior of current spots C could be caused by trapping of electron at charged defect sites or detrapping of it as shown in **Fig. 2.13**. The diameter of the current spots, which repeat disappearance and appearance, was estimated. As shown in **Fig. 2.14**, estimated diameter was 5.8±1.8 nm. It is reported that the change in potential due to formation of a single charge in non-dope Si is approximately 6 nm in diameter [19, 20]. It is considered that the disappearance and appearance of current spots at the same grain area is occurred by the trapping and emission of the electron at the electrical defect sites.

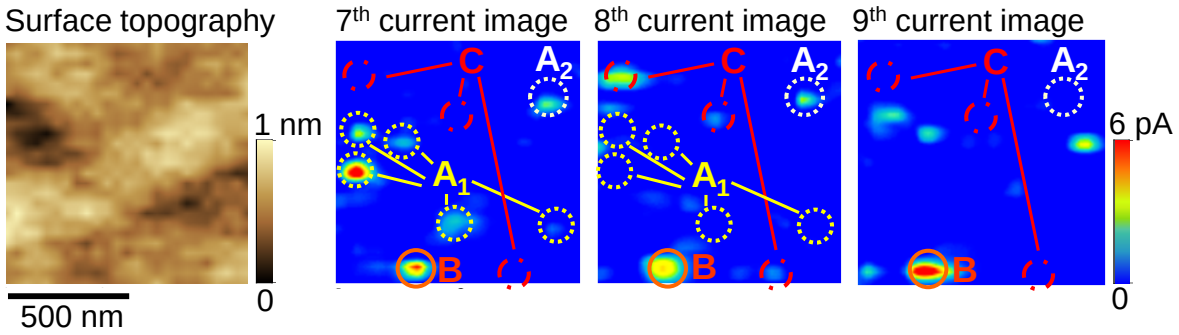


Figure 2.12: C-AFM images: Surface topography and current images of grain in non-hydrogenated poly-Si thin film at the V_{sub} of -2.0 V. White dotted lines show grain boundaries of the poly-Si. A_1, A_2: decreasing current spots, B: remained current spots, and C: current spots repeat disappearance and appearance due to repeating scan.

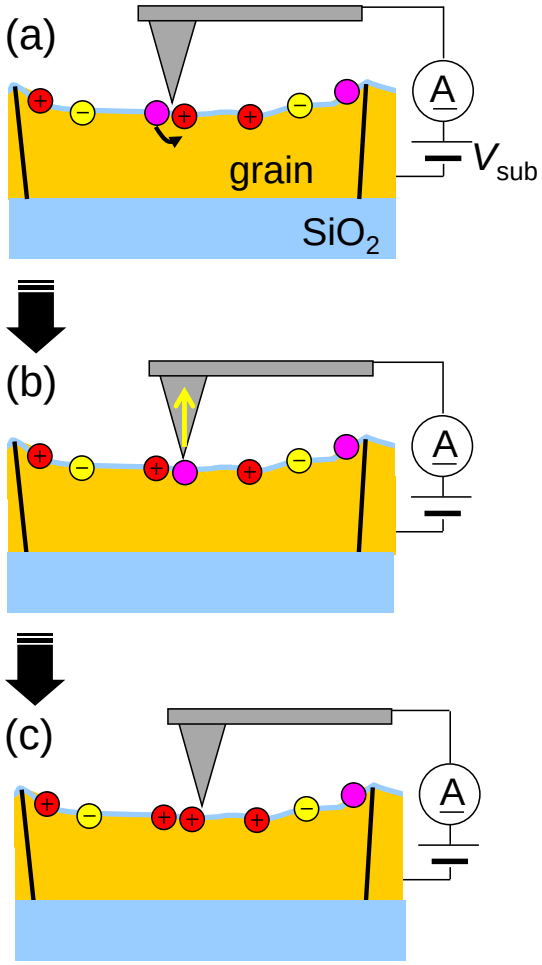


Figure 2.13: Schematic diagram of behavior of electron at grain. (a) Trapping of electron at positively charged defect sites. (b) Current flow due to the electron emission from defect sites to the cantilever. (c) Positively charging of defect sites after electron emission.

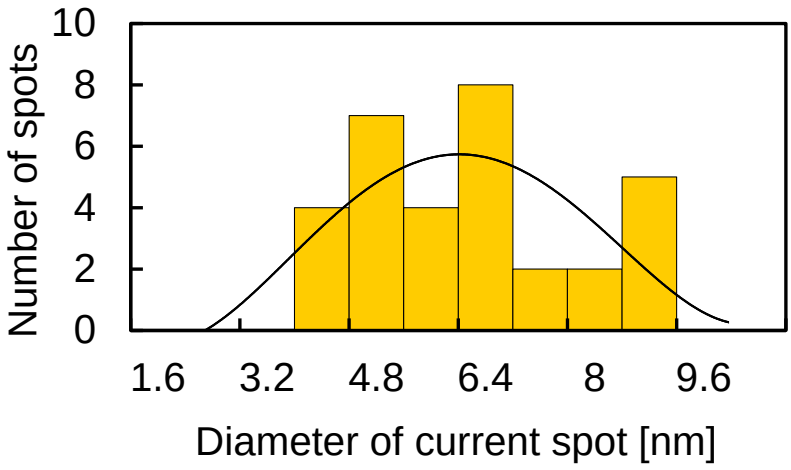


Figure 2.14: Diameter of current spots repeat disappearance and appearance by repeated C-AFM measurements.

2.5.3 Change in local current images by inactivation annealing

Figure 2.15 shows the current images of the poly-Si film **(a)** before and **(b-d)** after 300°C hydrogen termination taken at the V_{sub} of -2.0 V. During this hydrogenation treatment, the hydrogenation time was changed from 5 min to 20 min. The white dotted lines show grain boundaries on the poly-Si surface. In the non-hydrogenated poly-Si films, current flow entire poly-Si surface. On the other hand, after the hydrogenation at 300°C for 5 min, the average current at grain and grain boundary decreased as compared to before hydrogenation. Average current of poly-Si more decreased with the increasing hydrogenation time. Decreasing of average current is the largest at the hydrogenation temperature of 300°C for 20 min as shown in **Fig. 2.15 (d)**. Moreover, conductivity of grain unchanged in spite of the increasing of the number of scans, indicating that defect sites are not charged by the electron emission. It is striking that there is locally non-hydrogenated region (circled region by a black dotted line in **Fig. 2.15 (b)**) near grain boundaries in the case of short hydrogenation time. In the poly-Si films crystallized by conventional ELA, a prominent ridge was formed at a grain boundary owing to the stress concentration [21]. Thus, it is expected that crystal strain is easily caused near grain boundaries. Therefore, it is concluded that hydrogen termination does not randomly progress, but there are regions which cannot be easily inactivated near grain boundaries.

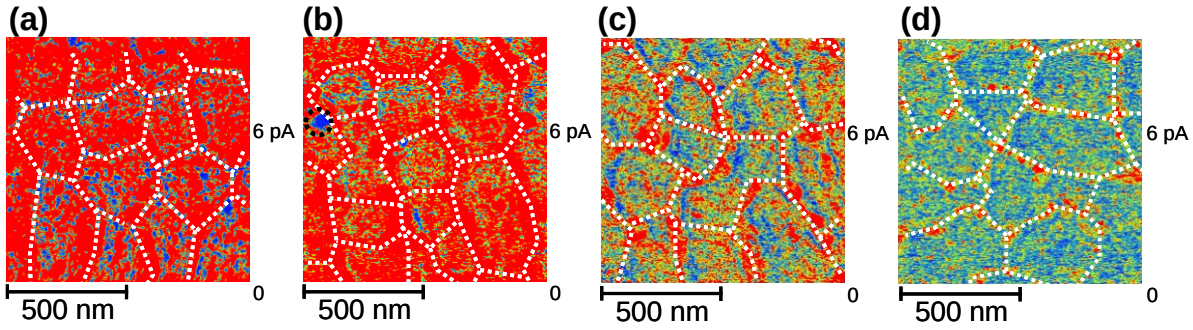


Figure 2.15: Current images of (a) non-hydrogenated and hydrogenated poly-Si surface for (b) 5 min, (c) 10 min, and (d) 20 min at 300°C. The V_{sub} was -2.0 V. White dotted lines show grain boundaries of the poly-Si films.

Figure 2.16 shows the current images of the poly-Si film **(a)** before and **(b-d)** after 20 min hydrogen termination taken at the V_{sub} of -2.0 V. During this hydrogenation treatment, the substrate temperature was changed from 200°C to 400°C with temperature step of 100°C. After the hydrogenation at 200°C for 20 min, the average current at grain and grain boundary decreased as compared to before hydrogenation. Average current of the poly-Si decreased as the increasing hydrogenation temperature to 300°C. On the other hand, the average current of the poly-S increased as compared to the case of hydrogenation at 300°C as shown in **Fig. 2.16 (c, d)**. It is well known that hydrogen is easily eliminated from Si at high-temperature annealing over 400°C. It is thought that high-temperature annealing induces the dehydrogenation of electrical defects rather than hydrogenation, resulting that the increasing of electrical defects.

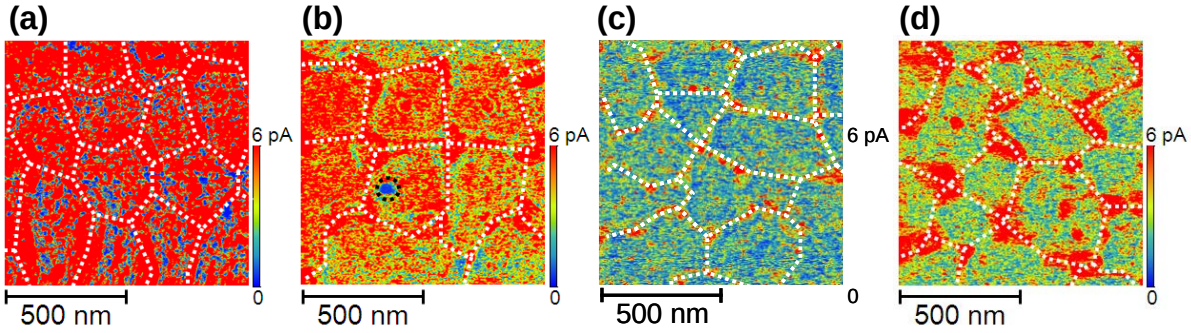


Figure 2.16: Current images of (a) non-hydrogenated and hydrogenated poly-Si surface at (b) 200°C, (c) 300°C, and (d) 400°C for 20 min. The V_{sub} was -2.0 V. White dotted lines show grain boundaries of the poly-Si films.

2.5.4 Change in current-voltage curves by inactivation annealing

Figure 2.17 shows current-voltage (*I-V*) curves at **(a)** grain and **(b)** grain boundaries before and after hydrogenation at 200°C, 300°C, or 400°C. Hydrogenation time was set to 20 min. For the use the poly-Si as channel layer of TFT, it is preferable that *I-V* curve shows asymmetric rising as shown in **Fig. 2.18 (a)**. Before hydrogen termination, *I-V* characteristics of grain showed symmetric rising. Moreover, *I-V* curves were much affected by change in observation area, and the current edge was very unstable and current did not flow until the application of a high voltage. As shown in **Fig. 2.17 (b)**, *I-V* curve of non-hydrogenated grain boundary also shows symmetric rising. It is expected that the conduction mechanism of grain boundaries is similar to metallic conductive mechanism behavior.

After 20 min-hydrogenation, the *I-V* curves of grain and grain boundary became

asymmetric rising and a very stable edge after hydrogenation at 200°C and 300°C. Probe current at inverse direction region decreases with the increasing of hydrogenation temperature. It is thought that the conduction mechanism of poly-Si films becomes similar to ideal semiconductor conduction mechanism behavior due to the inactivation of electrical defects in the poly-Si films. In the case of hydrogenation at 400°C, *I-V* curves of the poly-Si showed as symmetric rising as non-hydrogenated poly-Si. These results indicate that high-temperature annealing induces the dehydrogenation from electrical defects rather than hydrogenation, resulting in increasing of electrical defects.

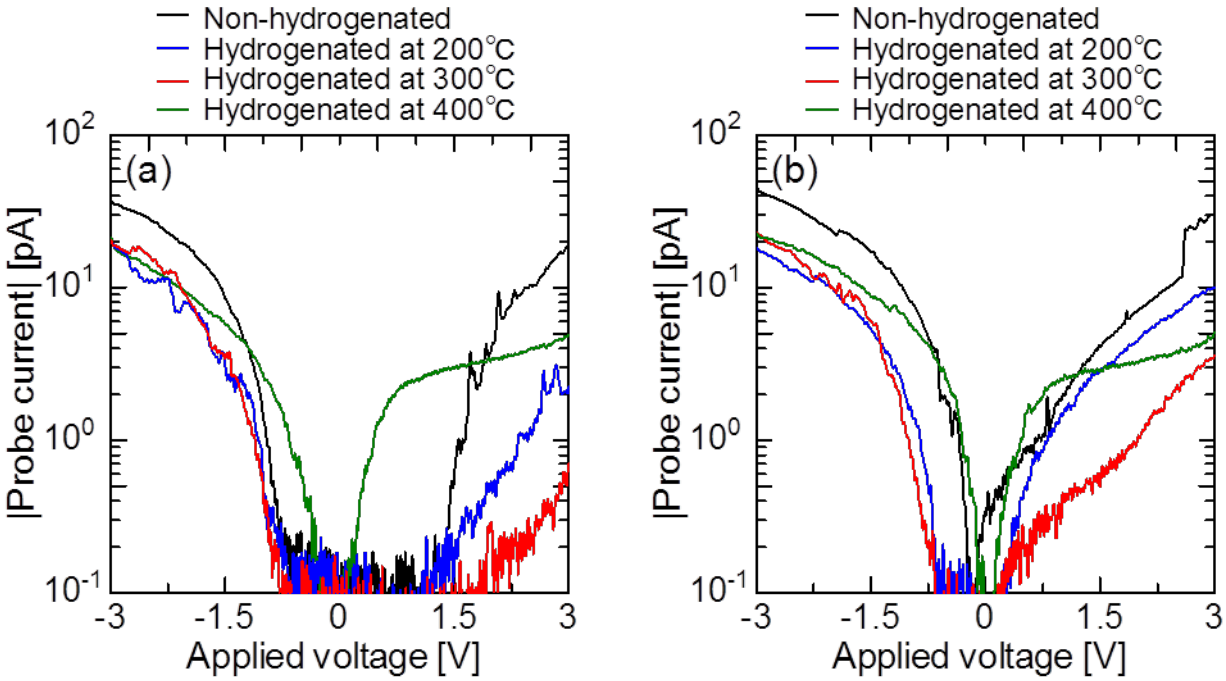


Figure 2.17: *I-V* curves of (a) grain and (b) grain boundary before and after hydrogen termination at 200°C, 300°C, or 400°C for 20 min.

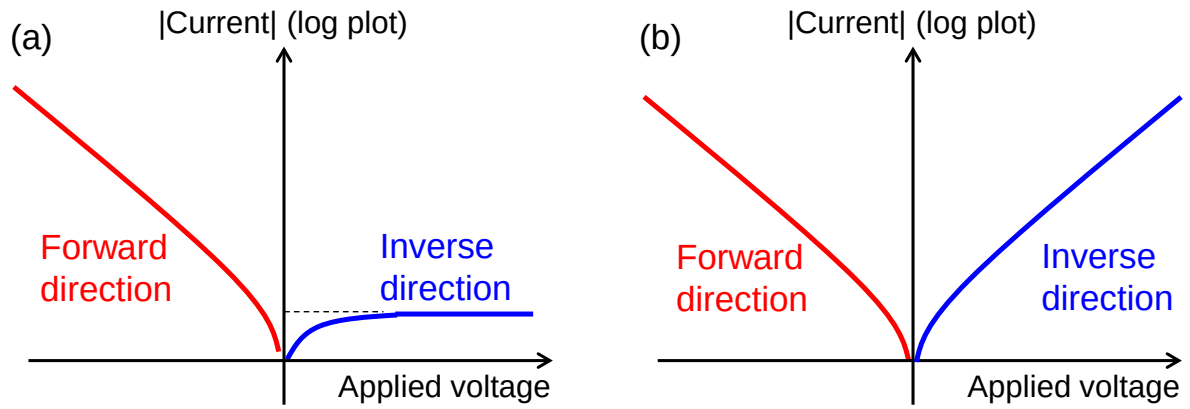


Figure 2.18: Single logarithmic plots of *I-V* curves of (a) ideal semiconductor and (b) ohmic properties.

2.6 Discussion

Figure 2.19 shows energy band diagram of **(a)** before and **(b, c)** after the junction of the cantilever (PtIr) and grain (Si). **Figure 2.19 (b)** shows non-hydrogenated grain and **Figure 2.19 (c)** indicates hydrogenated grain. Because the poly-Si film usually shows an intrinsic n-type nature [22], the E_{Fm} exists near E_{CSi}. Before hydrogen termination, it is expected that there are many electrical defects at the poly-Si surface. The electron move from defect sites to the cantilever because $\phi_m > \phi_{Si}$, and space-charge layer is formed after moving of electron. Thus, the band bending is caused at the junction interface due to the charging of electrical defects as shown in **Fig. 2.19 (b)**. The distance of depleted layer is expected to thin enough for the tunneling of electron in grain. Since the increasing of carrier, which contributes probe current, the conductivity of grain becomes higher. After hydrogen termination at 300°C for 20 min, electrical defects at the interface are inactivated. Thus, the electron become difficult to

move and the band bending describes gently slope as shown in **Fig. 2.19 (c)**, resulting in decreasing of carrier which contributes probe current. Therefore, probe current is much smaller than that of before hydrogen termination. After hydrogenation at 400°C, it is speculated that electrical defects are newly created by the dehydrogenation by high-temperature annealing. The energy band diagram in the case of hydrogenation at 400°C is close to the case of non-hydrogenated poly-Si as shown in **Fig. 2.19 (b)**, and thus, probe current increased owing to the increasing of carrier contributing probe current.

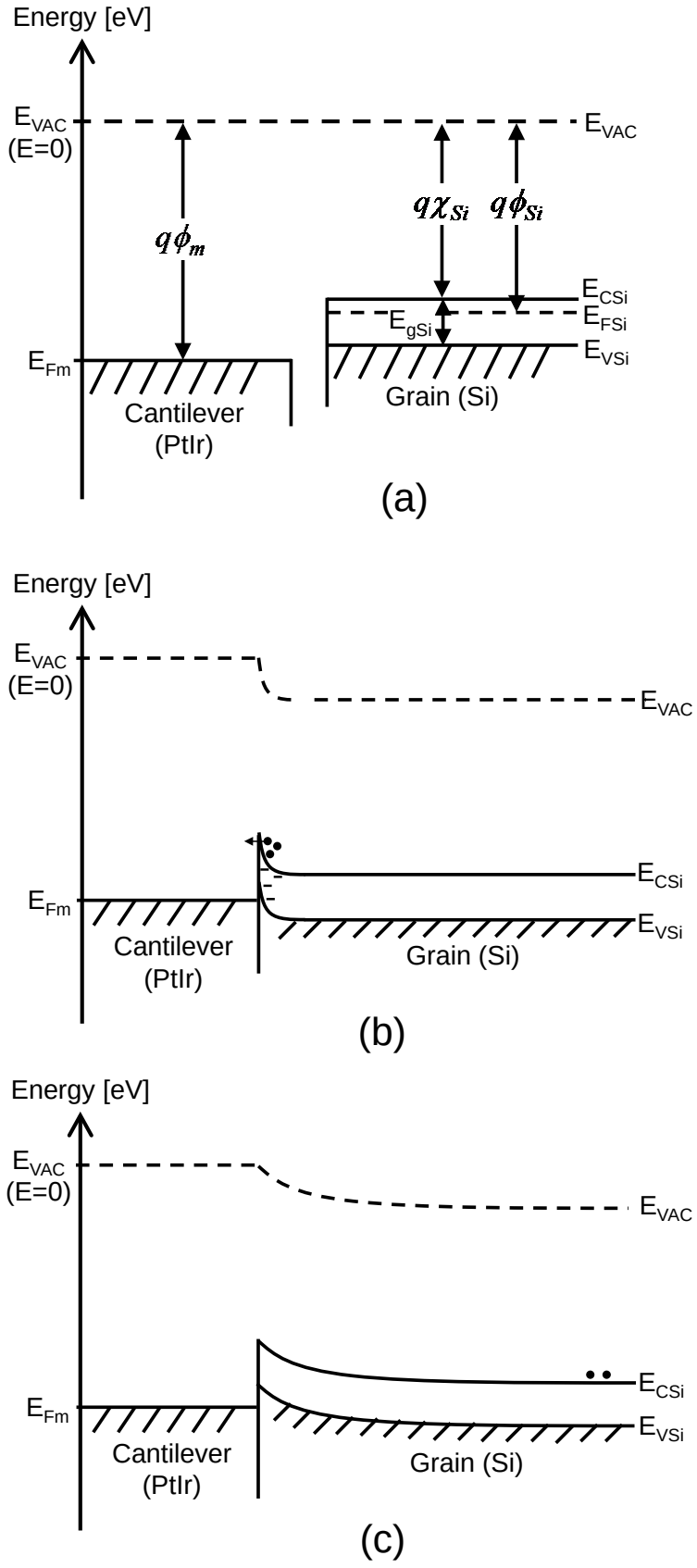


Figure 2.19: Energy band diagram between the cantilever and grain (Si). (a) Before junction and after junction of (b) non-hydrogenated grain and (c) hydrogenated grain. V_{sub} = 0 V.

2.7 Summary

Local electrical properties of poly-Si thin films formed by XeCl ELA were analyzed by utilizing C-AFM and KFM. The surface topography and current images of the poly-Si films were simultaneously obtained by C-AFM, and the probe current of the poly-Si were determined before and after hydrogen termination. Before hydrogen termination, conductive regions in grain disappeared with the repeated scanning of the cantilever, suggesting that defect sites in grains were charged positively by the electron emission from defect sites to the cantilever. In contrast, conductive regions in grain boundary almost unchanged. It is considered that probe current flowed continuously through electrical defects in grain boundaries, and this suggests that hopping conduction is a major conduction mechanism of grain boundaries. After 20 min hydrogen termination at 300°C, electrical defects were almost inactivated. Probe current in grain and grain boundary decreased as compared to non-hydrogenated poly-Si, and *I-V* curves of grain and grain boundary became similar to semiconductor conduction mechanism behavior. In addition, it is suggested that hydrogen termination does not randomly progress, and there are regions which cannot be easily inactivated near grain boundaries. After 20 min hydrogen termination at 400°C, probe current in grain and grain boundary increased as compared to the case of hydrogen termination at 200-300°C. Moreover, *I-V* curves of the poly-Si showed as symmetric rising as

non-hydrogenated poly-Si. High-temperature annealing promotes the emission of electrical defects rather than hydrogenation, resulting in the increasing of electrical defects.

From C-AFM and KFM measurements, it is demonstrated that grain and grain boundary have different conduction mechanism. Conduction mechanism of grain and grain boundary changed after hydrogenation treatment, indicating that electrical defects within the poly-Si films are inactivated. SPM measurements can be realized local electrical characterization for the poly-Si thin films and we believe that C-AFM and KFM measurements are very promising method for electrical characterization of the poly-Si thin film.

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Chapter 3

Crystallization to Polycrystalline Silicon by Underwater Laser Annealing

3.1 Introduction

3.1.1 Conventional laser annealing method and its weak point

Poly-Si thin films as the channel material for TFT are generally formed by an excimer laser annealing (ELA) using a-Si films on the glass substrate as a starting material. Sameshima *et. al.* proposed the ELA as crystallization method for poly-Si thin films in 1986, and they demonstrated poly-Si formation by low-temperature process under 270°C [1]. The excimer laser has high-power and short wavelength ultra violet laser capable of the crystallizing a-Si thin film. The absorption coefficient of the excimer laser beam into a-Si is 10^6-10^7 cm^{-1}, and thus, the penetration length into the a-Si is around 10 nm [2]. After laser pulse irradiation, melted Si layer is cooled rapidly with the crystallization in several hundred nanoseconds. The substrate temperature remains lower enough for the use of inexpensive glass substrates such as non-alkali glass. Poly-Si thin films formed by ELA have grain size around several hundred nanometers, and LTPS TFTs using the ELA poly-Si as channel achieve extremely high

field-effect mobility over 50 cm^2/Vsec [1, 3-5]. Therefore, ELA has been a strong candidate for formation of high quality poly-Si thin films.

On the other hand, crystallization temperature is still high for the use of flexible plastic films. **Table 3.1** shows the characteristic comparison of transparent flexible plastic films which are already used for LTPS TFT substrates [6-11] and conventional glass substrate. In order to fabricate high-performance LTPS TFTs on flexible plastic substrates, the crystallization temperature must become lower than the glass transition temperature, T_g (< 200°C). Moreover, high-temperature annealing process over 400°C is definitely needed after laser crystallization in conventional LTPS TFT fabrication process. It is well known that laser crystallized poly-Si films still contain a huge amount of electrical defects and these electrical defects degrade the device performance [12, 13]. Inactivation treatment of electrical defects such as hydrogenation by forming gas annealing (FGA) is usually conducted after crystallization, but this process needs substrate temperature around 400°C [14] and this is too high to use typical transparent plastic substrates shown in **Table 3.1**. Therefore, further low-temperature annealing technique for the crystallization and the inactivation treatment is required to realize high-performance LTPS TFT fabrication on the plastic substrates.

Table 3.1: Properties comparison of various transparent flexible plastic substrates

	PET [6]	PEN [7]	PC [8]	PES [9, 10]	PAR [11]	Glass
T_g [°C]	70	155	145	185	193	-
CTE [ppm/K]	15	13	70	60	61	3.2
Visible light transmission [%]	87	87	89	88	87	93

T_g: Glass transition temperature, CTE: Coefficient of thermal expansion
PET: polyethylene terephthalate, PEN: polyethylene naphthalate,
PC: polycarbonate, PES: polyethersulfone, PAR: polyacrylate

3.1.2 Underwater laser annealing

Here an underwater laser annealing (WLA): a laser annealing technique is proposed for super low-temperature fabrication of LTPS TFTs on transparent flexible plastic substrates. In the WLA, local heating of Si using ultra violet laser and a cooling effect of sample by flowing water can achieve low-temperature annealing. In addition, it is expected that the WLA has a capability for inactivation treatment of electrical defects at the same time as crystallization. It is reported that a furnace annealing with water vapor ambient is very effective in order to improve the electrical properties of LTPS TFTs by the inactivation of electrical defects with active species within water vapor. [15-17] Water vapor contains some active species such as hydrogen, oxygen and hydroxyl-radical, and these active species inactivate electrical defects in gate-insulator and/or poly-Si thin films.

WLA process is one of the strong candidate for super low-temperature inactivation

technique, but I must note that the timing of WLA while the TFT fabrication process is very important for effective inactivation of electrical defects within the channel layer. Inactivation treatment is generally performed at the end of TFT fabrication process. Although active species have to diffuse into gate-electrode and gate-insulator to reach channel layer, a heating time of the pulse laser is much shorter than that of FGA. Therefore, it is very important for inactivation of electrical defects within the poly-Si film at the same time as crystallization.

In this chapter, the crystallization of a-Si films on glass or plastic substrates has been demonstrated by WLA. Firstly, the crystallization to poly-Si films on glass substrates is performed, and their crystallinity, impurity within the poly-Si films, and electrical properties are investigated. From these experiments, the impact of WLA on grain growth is clarified and simultaneous inactivation of electrical defects while crystallization is demonstrated. Secondary, the crystallization to poly-Si films on plastic substrates is demonstrated by WLA. Cooling effect of Si surface by water and the crystallinity of the poly-Si films have been investigated. In this study, two kinds of plastic films, PET and PEN are used for substrates. The difference in crystallinity between PET and PEN is discussed.

3.2 Experimental

3.2.1 Preparation of precursor amorphous silicon substrates

Figure 3.1 (a) shows a sample structure of a-Si on glass substrate used for crystallization. Fifty nanometers thick-a-Si films were deposited on quartz glass substrates by low-pressure chemical vapor deposition (LPCVD) at 550°C. Before the laser irradiation, a-Si substrates were cleaned by the RCA cleaning [18] which is a standard set of wafer cleaning processes. Subsequently, the crystallization to poly-Si was carried out with KrF excimer laser.

For the crystallization on plastic substrates, 50-nm thick a-Si thin films were deposited on buffer layers (SiO_2/ SiN_x)/ plastic substrates by RF magnetron sputtering under the conditions of base pressure under 2×10^{-4} Pa, power density at 2.5 W/cm^2, Ar gas working pressure at 0.2 Pa, and room temperature. Buffer SiO_2 and SiN_x films were also deposited by RF magnetron sputtering at room temperature. In this experiment, two kinds of plastic substrates were used; PEN and PET. The T_g of PEN and PET was 155°C and 70°C, respectively. A-Si films on plastic substrates were bonded with a UV light curing adhesive on quartz glass to diminish the curling of plastic films as shown in **Fig. 3.1 (b)**.

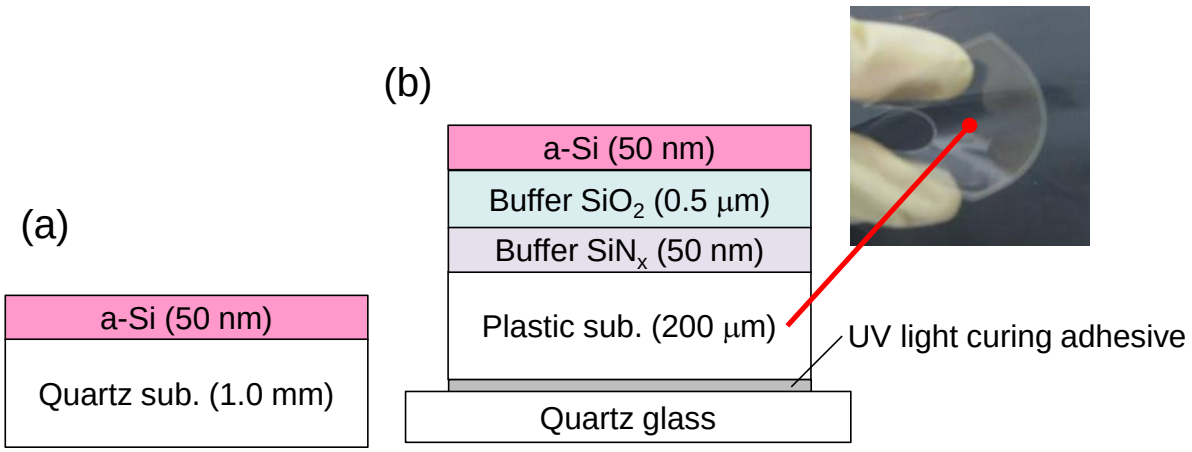

Figure 3.1: Sample structure of precursor a-Si and/or buffer layers on (a) quartz glass or (b) plastic substrates for the laser crystallization.

3.2.2 Laser annealing system

Figure 3.2 shows a schematic illustration of laser annealing system for laser crystallization. The laser beam has the wavelength of 248 nm, the pulse duration around 55 nsec, and the repetition rate of 100 Hz. The laser energy density and the number of laser beam shots were changed to 200-800 mJ/cm^2 and 5-100 shots/location, respectively. The beam size on the substrate surface was 360 μm×830 μm. In the WLA, the laser beam was irradiated to the substrate surface through the quartz window, which prevents a ruffle, and the flowing deionized-water (DI-water) layer. The thickness of quartz window is 1 mm and the distance between quartz window and substrate surface is about 3 mm. Conventional laser annealing in air (LA) is also performed for the comparison of irradiation medium. In the LA, the laser beam was irradiated in the laser annealing system without flowing water. Sample surface

during laser irradiation can be observed by CCD camera.

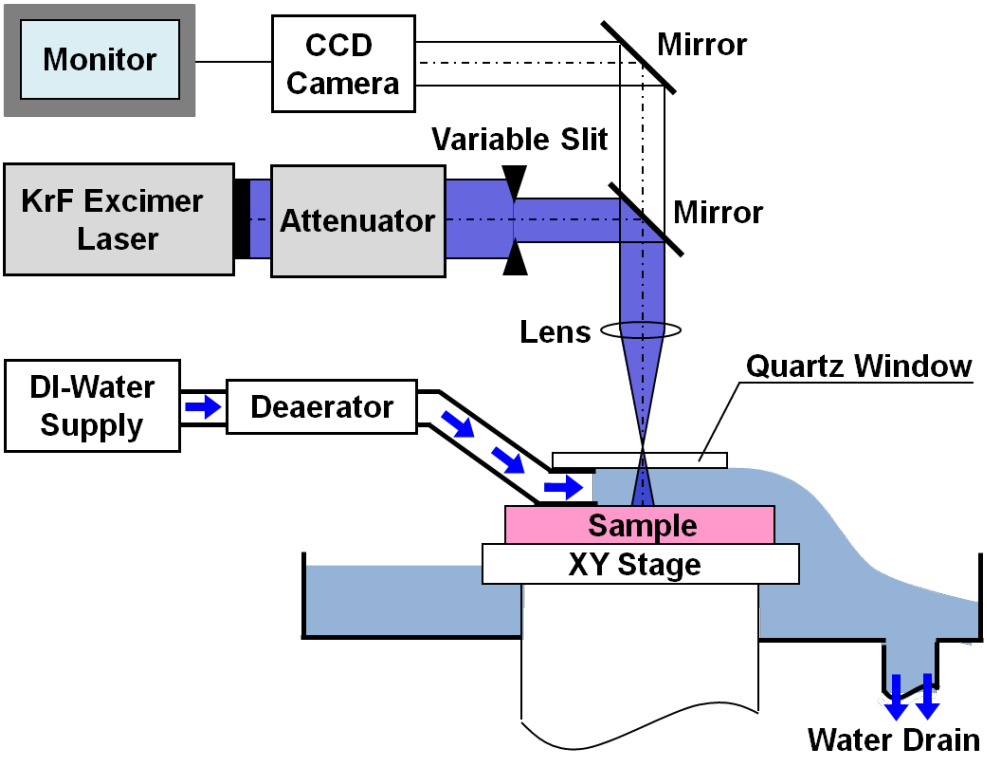

Figure 3.2: Laser annealing system for crystallization in the case of WLA.

In the WLA, DI-water was deaerated by using a vacuum deaerator to prevent the scattering of laser light by cavitation bubbles. **Figure 3.3** shows optical microscope images and SEM images of sample surface annealed by WLA. Before using the deaerator, laser light was scattered by cavitation bubbles as shown in **Fig. 3.3 (a)**. It is thought that dissolved oxygen and/or carbon dioxide are vaporized by heating from annealed substrate. Reflection of laser light at the interface between water and vapor deteriorates grain size uniformity. Moreover, in the **Fig. 3.3 (a)**, there are partially non-annealed region on laser irradiated area. After the deaeration of dissolved gases, there is no circle-shaped irradiation mark and grain

size and its uniformity improved as shown in **Fig. 3.3 (b)**.

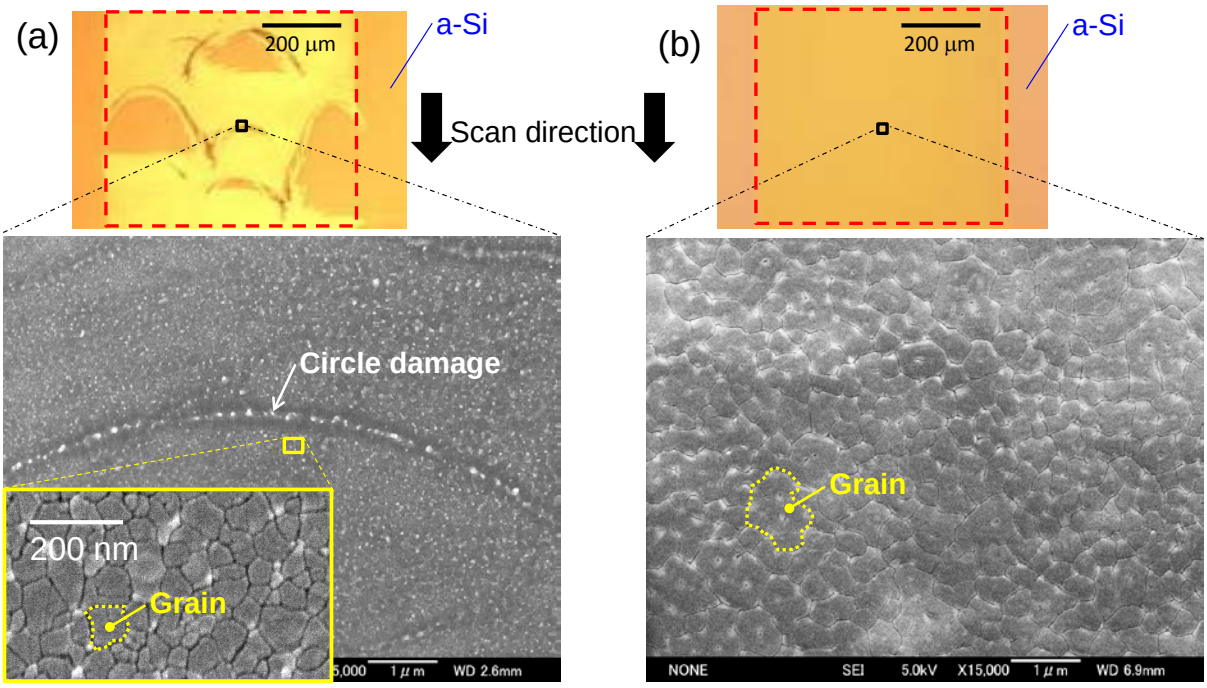

Figure 3.3: Optical microscope images and SEM images of laser annealed poly-Si surface (a) without and (b) with deaeration in WLA system. Circled area by red dashed line in optical microscope images indicates laser annealed region on sample surface.

3.2.3 Characterization

The grain size of poly-Si films was estimated by scanning electron microscopy (SEM; JEOL, JSM-7400F) measurements of the poly-Si film surface. After performing selective etching of grain boundaries by Secco-etching solution [19] and deposition of 10-nm thick platinum (Pt) to prevent electrically-charge of poly-Si surface, SEM observations were carried out.

The crystallinity was evaluated by Raman spectroscopy (JASCO, NRS-2100). Obtained

Raman spectra of crystallized samples were associated with the transverse optical (TO) phonon peak of single-crystalline Si (520 cm^{-1}), microcrystalline Si (510 cm^{-1}) and a-Si (470 cm^{-1}). Crystallinity of annealed poly-Si films were evaluated by the crystalline fraction and the full width at half maximum (FWHM) of Raman peak. Estimation of these values was performed after the fitting of measured Raman spectra were fitted using simulation soft (AISN Software Inc., PeakFIT) as shown in **Fig. 3.4**.

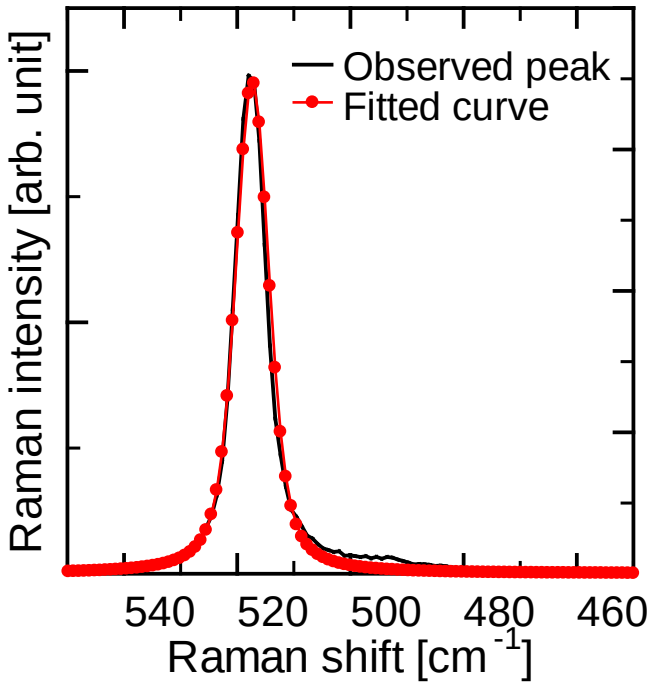

Figure 3.4: Raman spectra of poly-Si films formed by WLA. The number of shots was 10 shots/location and the laser energy density was 600 mJ/cm^2. Black and red lines indicate measured Raman peak and fitted curve using PeakFIT, respectively. Peak fitting was carried out using the Voigt amp function.

Impurity such as hydrogen and oxygen within the poly-Si films was measured by secondary ion mass spectroscopy (SIMS; ULVAC-PHI ADEPT-1010) using the Cs^+ primary

ion. In the measurements of oxygen, the depth profile of ^{18}O was measured as oxygen owing to too high detector responses of SIMS against ^{16}O.

Defect passivation effect of WLA was evaluated by the microwave photo conductivity decay (μ-PCD) measurements [20] and C-AFM (Shimadzu SPM-9600) measurements. We obtained the peak reflectivity of microwave instead of the excess carrier lifetime, because the lifetime of poly-Si thin film is around several hundred picosecond, which is too short for precise evaluation. The C-AFM measurements were performed with a PtIr-coated cantilever at a constant sample voltage (V_{sub}) of -2.0 V. Before C-AFM measurements, native oxide and/or thermally oxidized SiO_2 films on the poly-Si films was removed using a BHF solution for 10 sec to eliminate the influence of oxide layer on the conductivity. Surface morphology and corresponding current images were simultaneously obtained by C-AFM at room temperature in air ambient. The sample holder, to which the V_{sub} was applied, was electrically connected to the poly-Si film by a conductive paste. Thus, the V_{sub} was applied between the cantilever and the poly-Si films surface.

3.3 Physical Property Before and After Crystallization

3.3.1 Grain size

Figure 3.5 shows the relationship between laser energy density and the average grain size of crystallized poly-Si films by WLA. In all number of shots, grain size increases with the increasing in laser energy density from 500 to 600 mJ/cm^2, and the average grain size became largest at the laser energy density of 600 mJ/cm^2. The grain growth of poly-Si films was most promoted at number of shots of 10 shots/location. Next, maximum and average grain sizes of poly-Si films formed by WLA and LA were compared.

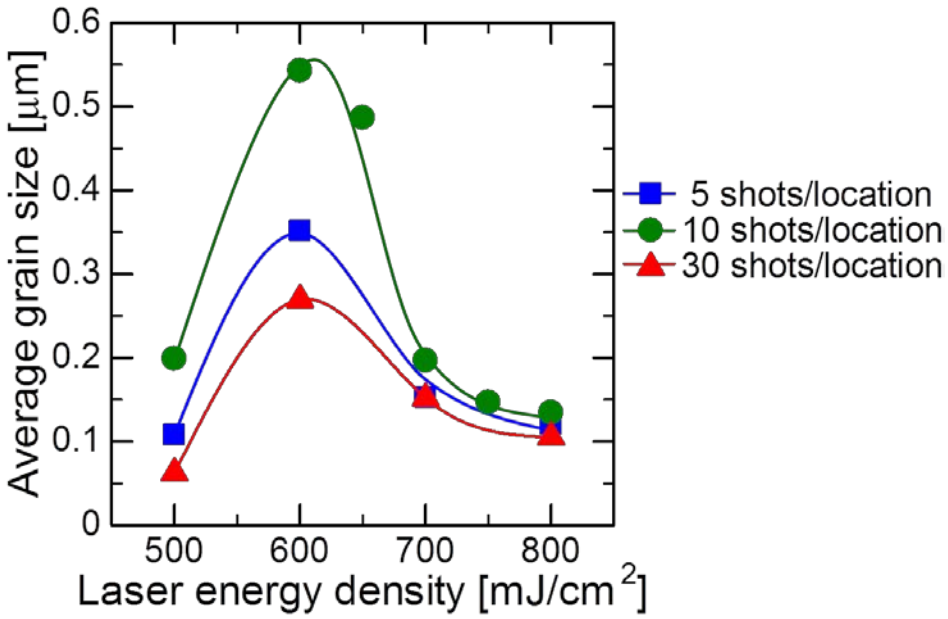

Figure 3.5: Relationship between laser energy density and the average grain size of poly-Si films formed by WLA. The number of shots was changed to 5 to 30 shots/location.

Figure 3.6 shows the relationship between laser energy density and grain size, and **Figure 3.7** shows SEM images of crystallized poly-Si films by LA or WLA. The maximum and average grain sizes of WLA poly-Si were larger than those of LA poly-Si in all conditions of irradiation energy. In the LA, the average grain size remained at small value less than 200

nm despite the maximum grain size enlarging with the increasing of laser energy densities. As shown in **Fig. 3.7 (a)**, there are many small grains whose size is around 100 nm in the LA poly-Si film even though the maximum grain size reached 0.9 μm. Moreover, there are partially removed region of Si layer after Secco-etching because nano-crystalline Si is easily etched by Secco-etching solution as compared to micro-crystalline Si and poly-Si. In the WLA, the average grain size increased as well as the maximum grain size with the increasing of laser energy densities from 500 to 650 mJ/cm^2. The maximum values of maximum and average grain size of WLA poly-Si films were 1.6 and 2.8 times larger than that of LA poly-Si films, that is, WLA achieves giant and uniform grain growth as shown in **Fig. 3.7 (b)**. These results indicate that irradiation medium of laser annealing is very important to promote grain growth. It is speculated that the difference of irradiation medium changes the temperature distribution within the Si films. In order to evaluate the difference of temperature distribution between WLA and LA poly-Si films, we observed surface morphology of the poly-Si films which suffers considerable damage due to high-energy laser irradiation in air or water.

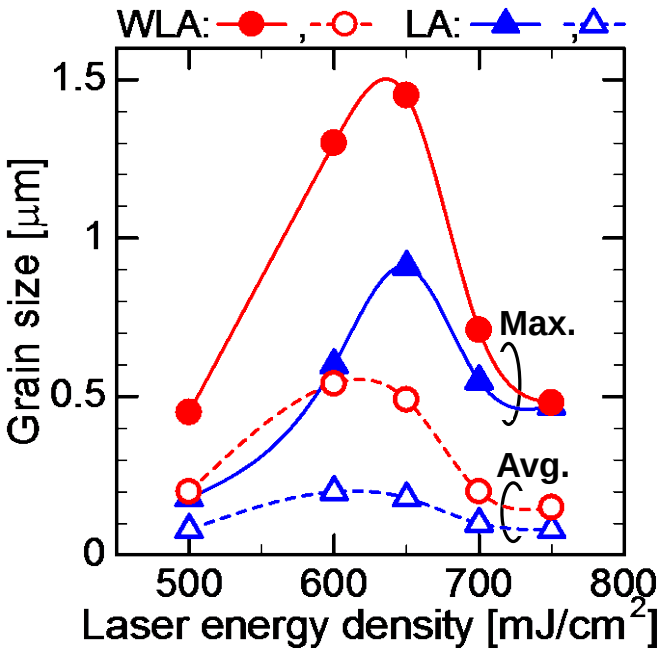

Figure 3.6: Grain size dependence of poly-Si films formed by LA or WLA on the laser energy densities. The solid line in graph shows the fitted curve of average grain size plots of LA poly-Si and the dashed lines show that of WLA poly-Si films. The average grain sizes were calculated from 100 grains of each film.

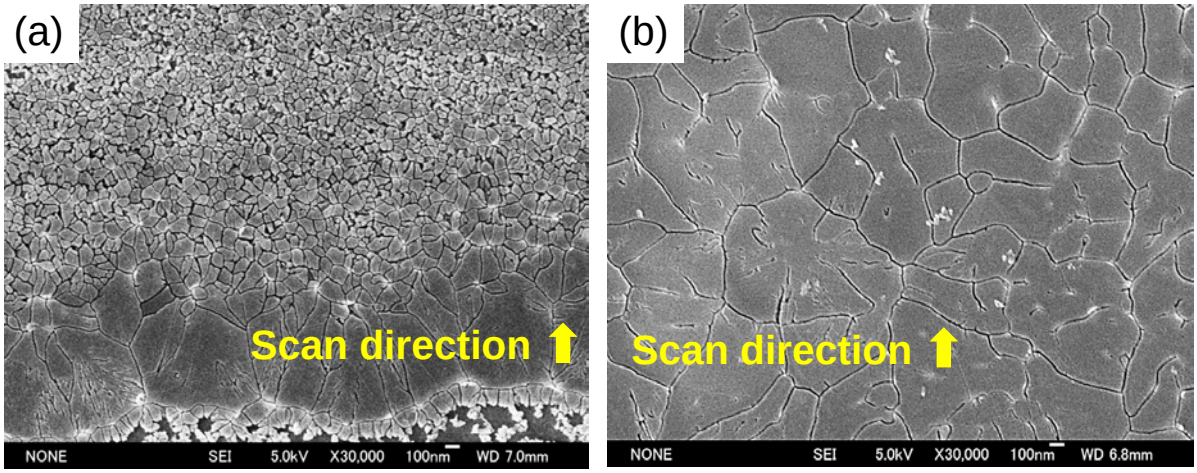

Figure 3.7: SEM images of (a) LA and (b) WLA poly-Si films formed at the number of shots of 10 shots/location and the laser energy density of 650 mJ/cm^2.

3.3.2 Temperature distribution within poly-Si films

Figures 3.8 (a) and **(d)** show SEM images of LA and WLA sample surfaces which have thermal damage by high-energy laser irradiation. While both samples suffered from considerable irradiation damage such as partially removing or thinning of Si layer by vaporization of molten Si, damage formation mechanism was absolutely different. The absorption coefficient of the laser beam (wavelength = 248 nm) for LPCVD a-Si is ~10^6 cm^{-1}, and thus the penetration length into the a-Si is approximately 7 nm [2]. In the LA, the highest point of temperature locates at the Si film surface. Therefore, the high-energy laser irradiation causes the vaporization of molten Si from surface side, and the vaporized Si atoms exert a reaction force, which cause agglomeration of molten Si, as shown in **Fig. 3.8 (b, c)**. On the other hand, the SEM image of WLA samples showed the evidence of vaporization from inside film. In the WLA, surface temperature is reduced due to the presence of flowing water, and irradiation energy diffuses from the Si surface into the water in addition to the thermal diffusion into the SiO_2 film. Therefore, high-energy laser irradiation in water causes vaporization from the inside film as shown in **Fig. 3.8 (e, f)**. From these results, it is considered that the temperature distribution within the Si film is homogenized by the presence of flowing water on the Si films, resulting in decreasing of nucleation density because a nucleation starts from the minimum point of temperature such as Si/buffer SiO_2 interface.

Decreasing of nucleation density brings in an enhancement of grain growth. Consequently, it is concluded that the temperature distribution within the Si film is homogenized in the case of WLA, and this effect leads to giant and uniform grain growth.

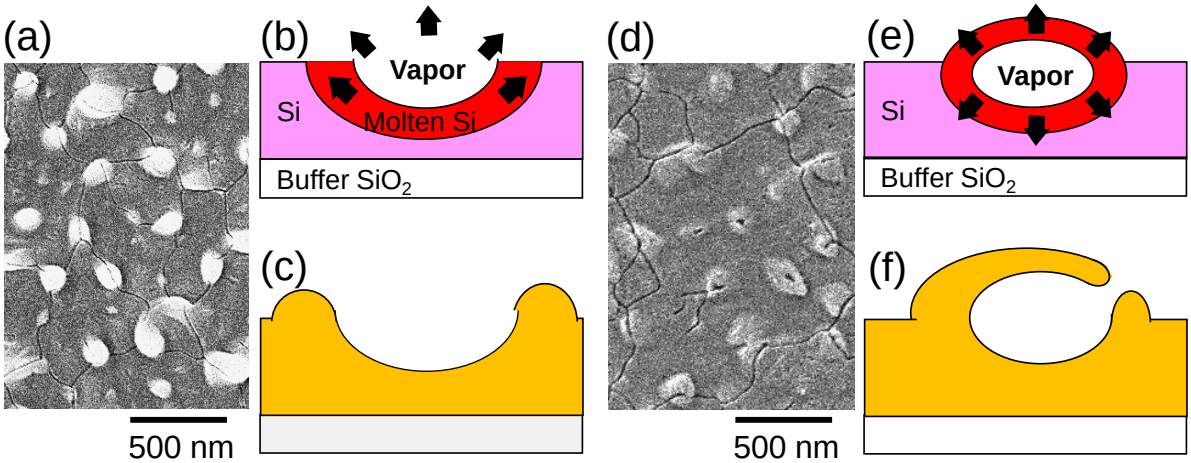

Figure 3.8: (a, d) SEM images of annealed Si film surface after high-energy laser irradiation in (a) air or (d) water. The laser irradiation conditions are the number of shots of 100 shots/location, the laser energy density of 600 mJ/cm^2. (b, c) and (e, f) show schematic illustration of formation mechanism of considerable damage such as agglomeration of molten Si.

3.3.3 Crystallinity

Figure 3.9 shows **(a)** the FWHM and **(b)** the crystalline fraction calculated from TO phonon peaks. The FWHM of Raman spectra of WLA poly-Si films are smaller than that of LA poly-Si films in all conditions of irradiation energy. Moreover, the crystalline fraction of WLA poly-Si films is higher than that of LA poly-Si films. From these results, the

crystallinity of WLA poly-Si films is better than that of LA poly-Si films. Furthermore, the FWHM of WLA poly-Si crystallized at the laser irradiation energy of 500-600 mJ/cm^2 is smaller than that of convention ELA poly-Si. The crystalline fraction of WLA poly-Si crystallized at the laser irradiation energy of 600 mJ/cm^2 is 100%. It is indicated that the crystallinity of WLA poly-Si is higher than LA poly-Si and conventional ELA poly-Si.

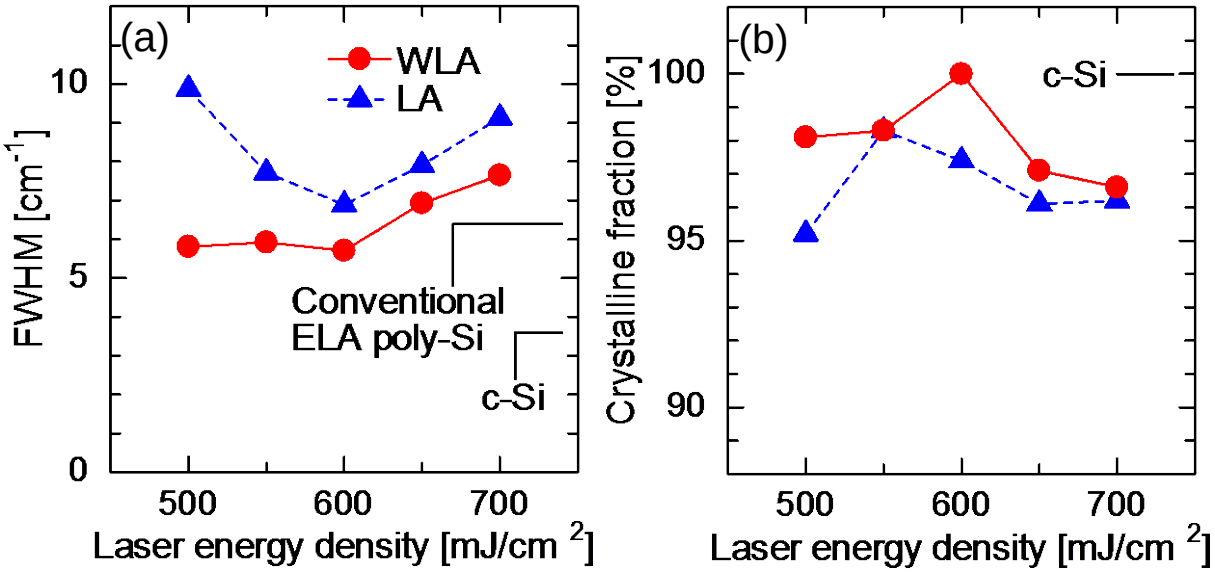

Figure 3.9: (a) FWHM of Raman peak and (b) crystalline fraction of poly-Si films formed by WLA or LA. The number of shots was 10 shots/location.

3.3.4 Depth profile of impurity

Next, we focused on the impurity of hydrogen and oxygen within the Si layer. **Figure 3.10** shows the depth profiles of **(a)** ^{18}O and **(b)** ^{1}H within the precursor a-Si film and crystallized poly-Si films (we measured ^{18}O as oxygen owing to too high detector responses of SIMS

against ^{16}O). Detected counts of oxygen from a-Si, WLA, and LA poly-Si layers were the same level. On the other hands, counts of hydrogen from the WLA poly-Si layer were much larger than those from the LA poly-Si and precursor a-Si layers. Estimated hydrogen concentration of WLA poly-Si at the surface and 20 nm deep were 3×10^{20} and 2×10^{20} atoms/cm^2, respectively, and these values are almost the same level as poly-Si films after FGA (H_2 gas concentration: 10%, substrate temperature: 400°C, processing time: 1h). These results indicate that hydrogen in water vapor generated by WLA diffuses into the Si films as well as FGA although short heating time and low-substrate temperature as compared to FGA. It is thought that this hydrogen will inactivate electrical defects such as dangling bonds in the poly-Si films, and WLA poly-Si films have better electrical characteristics than LA poly-Si films. Next, local electrical properties of crystallized poly-Si films are observed to discuss the effect of electrical characteristics by hydrogen within the poly-Si films.

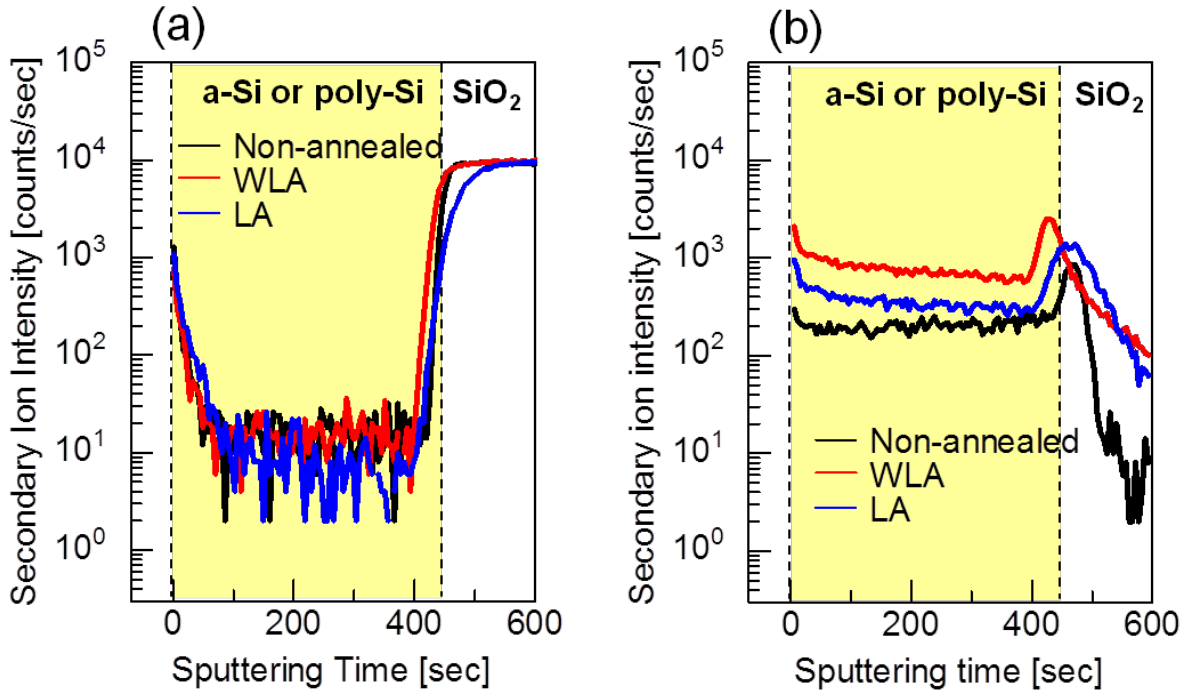

Figure 3.10: Depth profiles of (a) ^{18}O and (b) ^{1}H within the precursor a-Si, WLA poly-Si, and LA poly-Si. The average grain sizes of both WLA and LA poly-Si films were 197 nm, the number of shots was 10 shots/location, and the laser energy density of measured LA and WLA poly-Si samples were 600 mJ/cm^2 and 700 mJ/cm^2, respectively.

3.4 Electrical Properties of Crystallized Polycrystalline Silicon Thin Films

3.4.1 Microwave photo conductivity decay measurements for free-carrier life time observation

The μ-PCD measurement, which observes defect density or dangling-bond state, is valuable for electrical characterization of the poly-Si thin films [20]. The μ-PCD measurements of WLA and LA poly-Si films which were used for C-AFM measurements were performed to

evaluate defects within poly-Si films. The μ-PCD measurements estimate excess carrier lifetime of samples from time variation of reflectivity of microwave irradiated to the same area where pulse laser is irradiated for excess carrier generation. The peak reflectivity of micro wave reflectance is obtained because excess carrier life time of poly-Si thin films is too short for precise estimation.

Figure 3.11 shows **(a)** the grain size dependence of poly-Si films formed by LA or WLA on the laser energy densities, **(b)** peak reflectivity of microwave of LA and WLA poly-Si films. The number of shots for WLA and LA was set to 10 shots/location. Firstly, the peak reflectivity signals of microwave from crystallized poly-Si films which have the maximum value of average grain size (LA 600: 197 nm, WLA 600: 533 nm) are compared. As shown in **Fig. 3.11 (b)**, the peak reflectivity signal of WLA 600 is much larger than that of LA 600. The microwave reflectivity is proportional to the excess carrier lifetime, that is, higher peak reflectivity confirms fewer electrical defects within WLA poly-Si. Therefore, it is considered that WLA 600 has fewer electrical defects due to high crystallinity as compared to LA 600. Next, the peak reflectivity signals of poly-Si films, which have the same average grain size of 197 nm, that is, LA600 and WLA700, are compared. As shown in **Fig. 3.11 (b)**, the peak reflectivity of microwave from WLA poly-Si was 15% larger than that of LA poly-Si although these poly-Si films have the same average grain size. These results indicate that WLA forms poly-Si films which have not only high crystallinity but also good electrical

property by reducing defects. Consequently, it is concluded that WLA forms poly-Si films which have not only much better crystallinity but also fewer electrical defects as compared to LA.

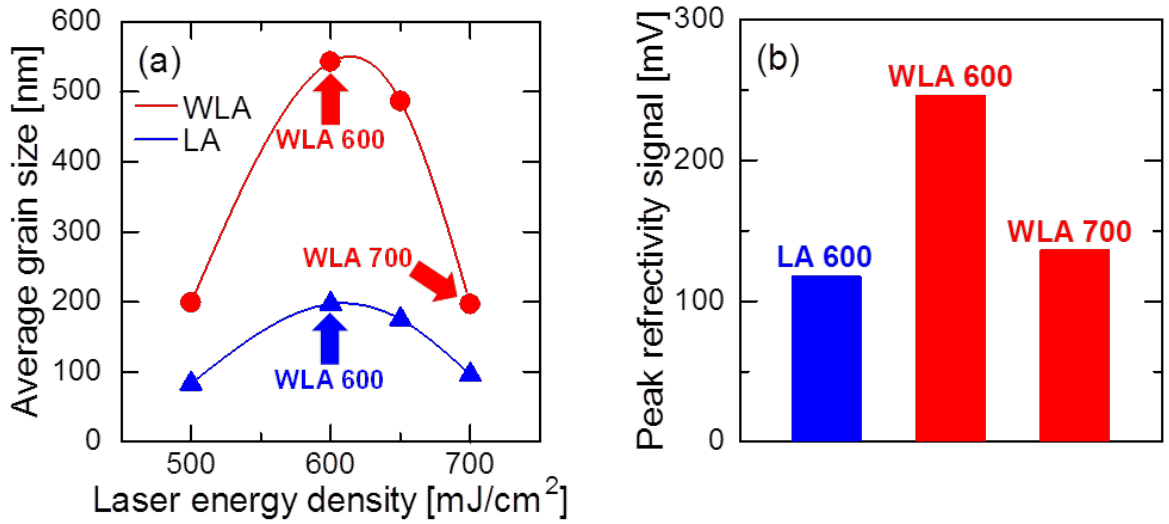

Figure 3.11: (a) The grain size dependence of poly-Si films formed by LA or WLA on the laser energy densities, (b) peak reflectivity of microwave of LA and WLA poly-Si films. The number of shots was 10 shots/location.

3.4.1 Local electrical properties measured by conductive-atomic force microscopy

C-AFM measurement of poly-Si films, which were formed by WLA or LA, was carried out in order to evaluate electrical properties. Before the C-AFM measurements, the SiO_2 layer on the poly-Si surfaces is removed by BHF solution. Therefore, even if the oxidation occurs during laser annealing, the oxide layer does not affect the C-AFM measurements. Since the

applying negative bias voltage to poly-Si substrates, the current flows from the cantilever to poly-Si surface by electron emission.

Figure 3.12 shows **(a)** surface topography and **(b-c)** current images of LA poly-Si film during four times C-AFM scanning in the same area. **Figure 3.13** shows those of WLA poly-Si films. The average grain size of poly-Si films formed by WLA and LA for C-AFM measurements was the same. At the first scan, current flowed in the entire area of LA poly-Si surface includes grain and grain boundary as shown in **Fig. 3.12 (b)**, and probe current reduced gradually as increasing number of scan as shown in **Fig. 3.12 (c)**. In the case of LA, it is expected that there are many electrical defects at not only at grain boundaries but also inside of grains, and current flows through the cantilever to these defect sites due to the electron emission. With increasing number of scan, defect sites charge positively and amount of current reduces gradually. On the other hand, the probe current of the WLA poly-Si was smaller than that of the LA poly-Si sample, and current mainly flowed at grain boundaries as shown in **Fig. 3.13 (b, c)**. It is considered that electrical defects in the poly-Si films are inactivated by hydrogen supplied from water vapor, and the probe current became smaller as compared to LA.

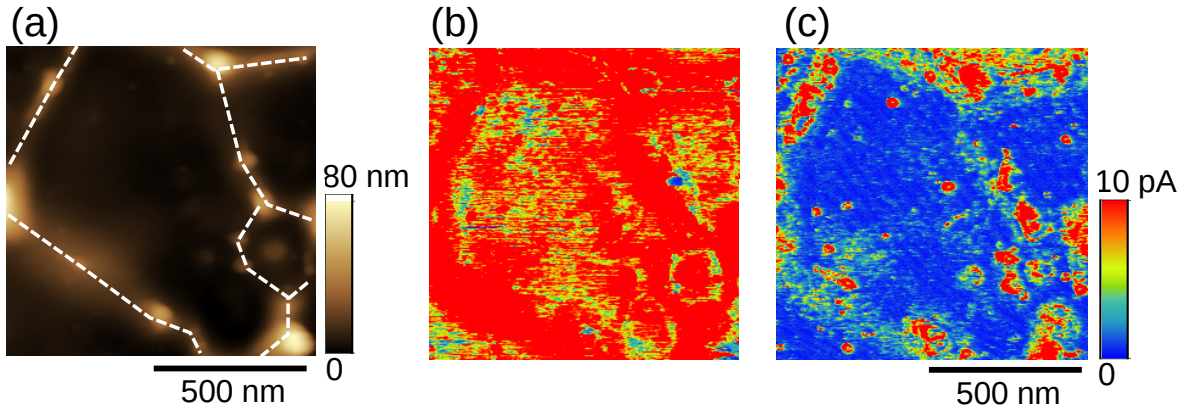

Figure 3.12: (a) Surface topography and (b) first and (c) forth current images of LA poly-Si films during four times scanning at the V_{sub} of -2.0 V. White dotted line in surface topography image shows grain boundaries of poly-Si film surface. The average grain size of LA poly-Si was 197 nm. The number of shots was 10 shots/location and the laser energy density was 600 mJ/cm^2.

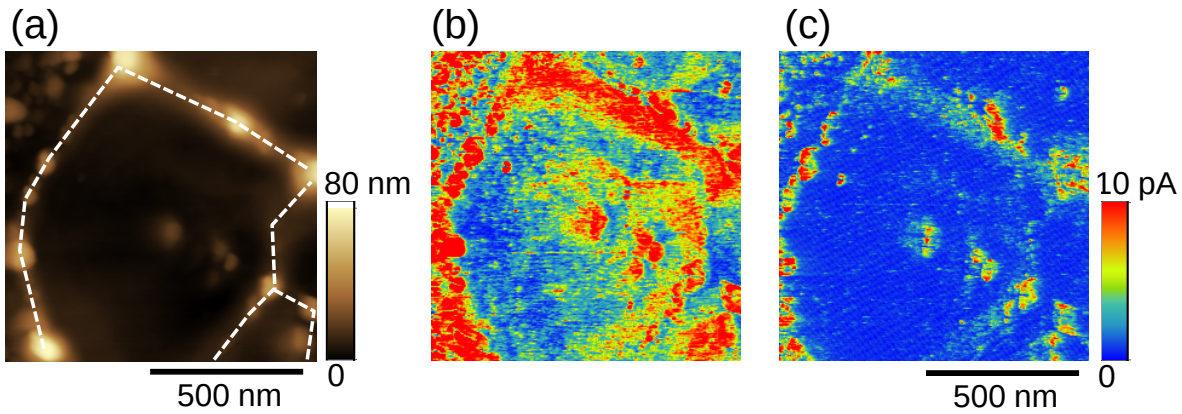

Figure 3.13: (a) Surface topography and (b) first and (c) forth current images of WLA poly-Si films during four times scanning at the V_{sub} of -2.0 V. White dotted line in surface topography image shows grain boundaries of poly-Si film surface. The average grain size of WLA poly-Si was 197 nm. The number of shots was 10 shots/location and the laser energy density was 700 mJ/cm^2.

3.5 Crystallization on Plastic Substrates

3.5.1 Cooling effect of film surface by WLA

Prior to crystallinity measurements, the observation of sample surface which laser annealed at various irradiation energies were performed. **Figure 3.14** and **Figure 3.15** show optical microscope images of annealed Si film surface on **Fig. 3.14** PET and **Fig. 3.15** PEN substrates after **(a)** LA or **(b)** WLA. The number of laser beam shots was set to 10 shots/location. Enclosed areas by red dashed line show laser irradiation area on sample surface. In the both irradiation media, a-Si films on PET substrates started to crystallize by laser annealing from the same laser energy density (200 mJ/cm^2). There was no noticeable damage such as peeling of Si films or severe shrinkage of plastic substrates below 260 mJ/cm^2 in the LA or 300 mJ/cm^2 in the WLA. On the other hand, LA easily caused thermal damage such as a removal of Si layer by the ablation in the whole or part of the irradiated area with the energy lower than that of WLA. The energy margin for the crystallization without thermal damage in WLA was 1.7 times larger than that in LA. These tendencies became much more pronounced with the increasing of the number of shots, and the energy margin for the crystallization in WLA at 100 shots/location was 2 times larger than that in LA. In the case of PEN substrates, the energy margin for the crystallization without thermal damage in WLA was 3 times larger than

that in LA. It is thought that cooling effect against substrate surface by flowing water suppress the rise in substrate temperature during crystallization. This effect offers a big advantage for super low-temperature annealing of thin films on plastic substrates.

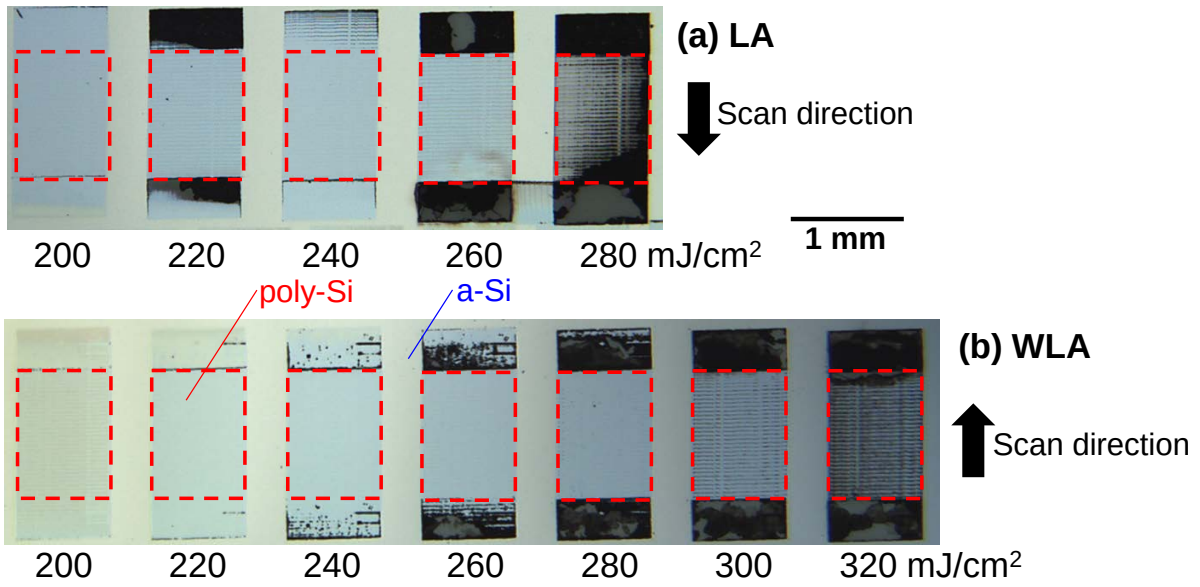

Figure 3.14: Optical microscope images of annealed Si surface on PET substrates crystallized by (a) LA or (b) WLA. The number of shots was 10 shots/location. Enclosed area by red dashed line indicates annealed area.

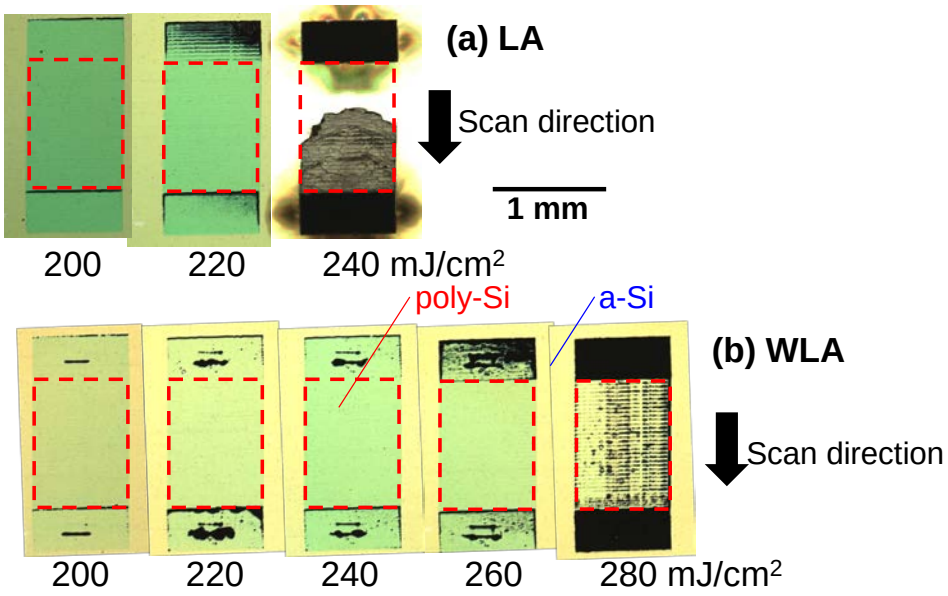

Figure 3.15: Optical microscope images of annealed Si surface on PEN substrates crystallized by (a) LA or (b) WLA. The number of shots was 10 shots/location. Enclosed area by red dashed line indicates annealed area.

3.5.2 Crystallinity of annealed Si films

Next, Raman spectroscopy measurements of laser annealed samples shown in **Fig. 3.14** were carried out. **Figure 3.16** shows Raman spectra of annealed samples by **(a)** LA or **(b)** WLA under the irradiation energy of 200-300 mJ/cm^2 and the number of shots of 10 shots/location. Raman spectroscopy observation was performed against laser annealed sample without the irradiation damage on sample surface. For the samples before the laser annealing or annealed at less than 200 mJ/cm^2 in both irradiation media, a broad peak around 480 cm^{-1} derived from a-Si was observed. The TO phonon peaks of crystallized Si were clearly observed around 510 cm^{-1} from annealed Si film at the irradiation energy of 200-260 mJ/cm^2 in the LA and 200-300 mJ/cm^2 in the WLA. In the use of PEN substrates, the peaks of crystallized Si were also observed. Obtained Raman peaks slightly shifted toward higher wave number direction and the FWHM of peaks decreases with the increasing of laser irradiation energy. Moreover, an amorphous constituent of the peaks also decreases, indicating that the crystallinity of poly-Si films on plastic substrates was improved by the increasing of laser energy density.

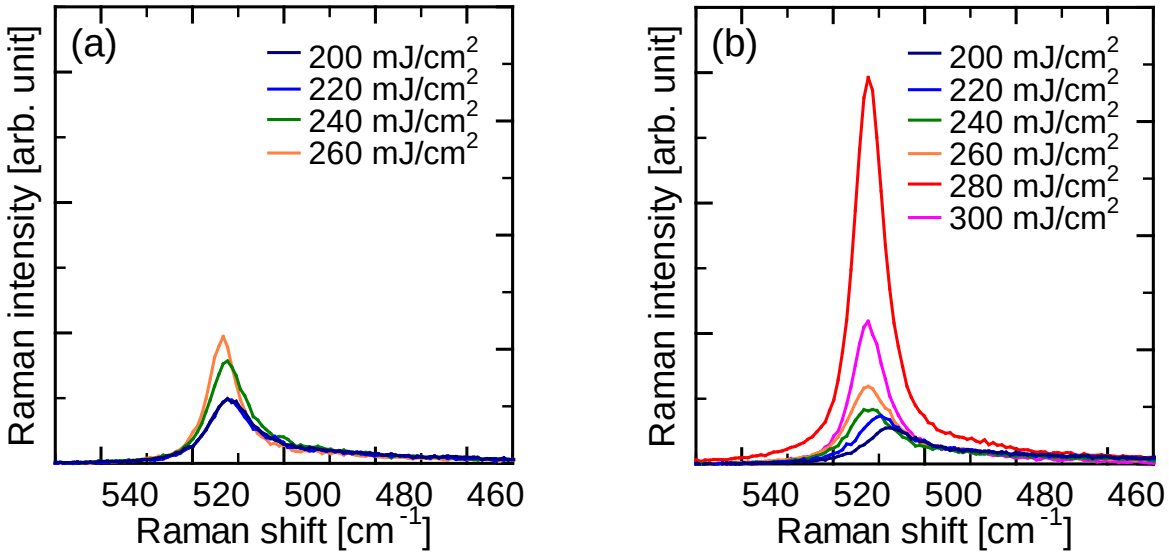

Figure 3.16: Raman spectra of annealed Si films by (a) LA or (b) WLA on PET substrates. The number of shots was 10 shots/location.

Figure 3.17 indicates the crystallinity of annealed Si samples by LA or WLA at various laser energy densities. The number of shots was 10 shots/location. It is striking that the FWHM and the amorphous constituent of the peak from WLA samples are much smaller than those from LA samples. WLA achieves the formation of high-crystallinity poly-Si films on plastic substrates without thermal damages. The maximum crystalline fraction and the minimum FWHM of WLA poly-Si on PET substrates are comparable to those values on glass substrates (as compared to **Fig. 3.9**). It is demonstrated that poly-Si films with good crystallinity can be formed on PET substrates by WLA as the same as the crystallization on glass substrates. Promotion of grain growth and suppress of thermal damage are due to the presence of flowing water on the Si films. Consequently, it is concluded that the super low-temperature crystallization to high-quality poly-Si films without thermal damage against

plastic substrates can be achieved by WLA. **Figure 3.18** shows the crystallinity of WLA poly-Si under various number of laser shots. As well as the case of laser crystallization on glass substrates, the crystallinity was highest at the number of shots of 10 shots/location as the same as the case of glass substrates.

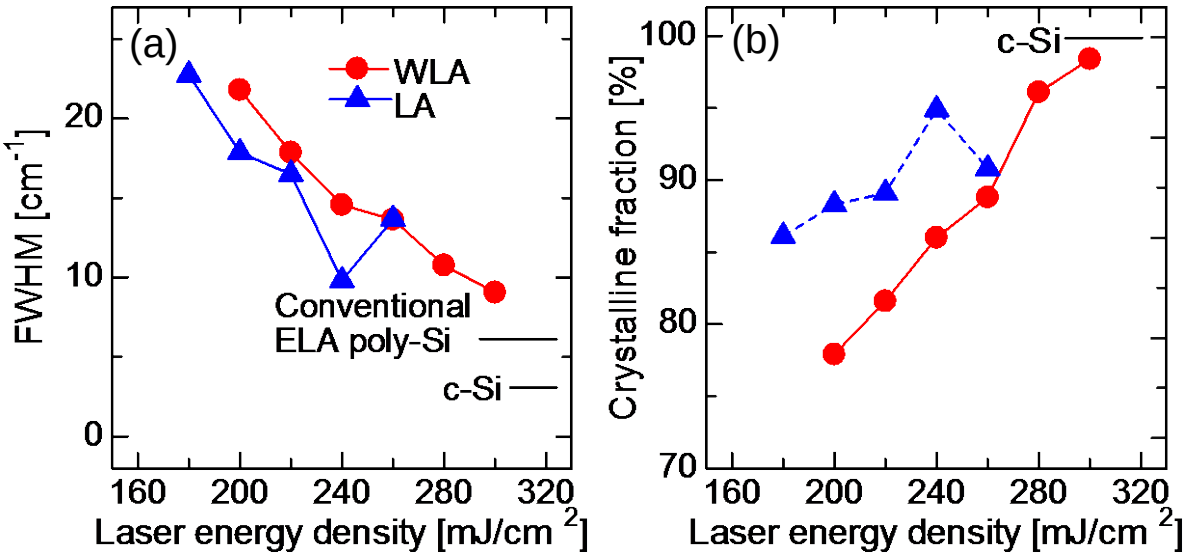

Figure 3.17: (a) FWHM of Raman peak and (b) crystalline fraction of poly-Si films formed by WLA or LA. The number of shots was 10 shots/location.

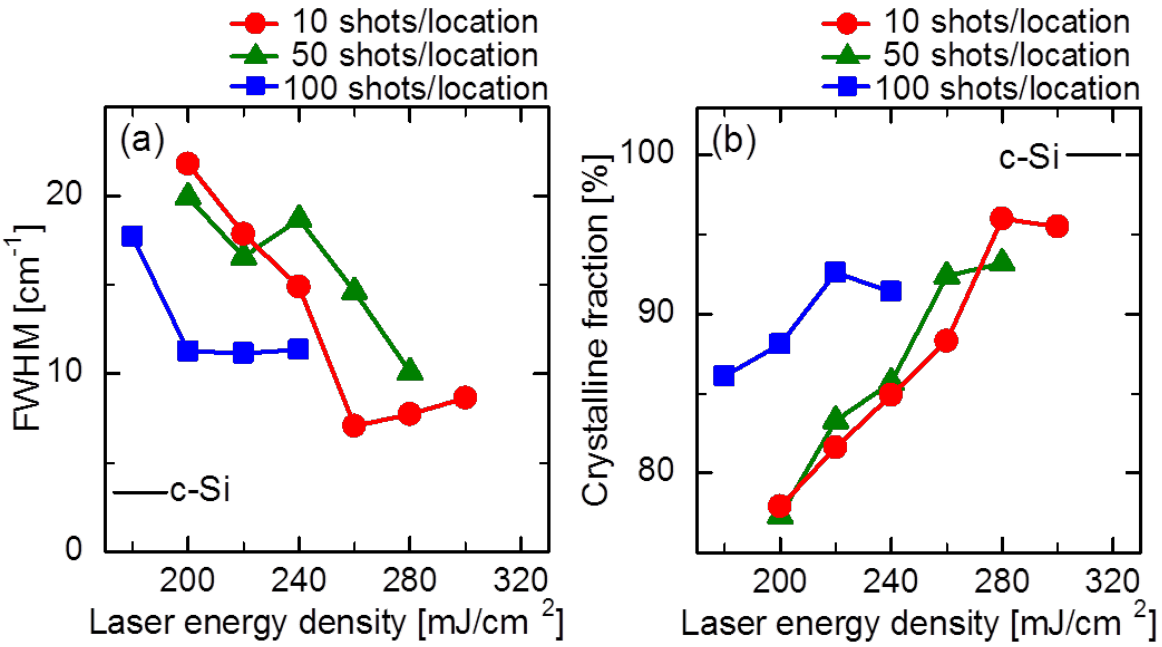

Figure 3.18: Relationship between the laser energy density and (a) FWHM of Raman peak and (b) crystalline fraction of poly-Si samples crystallized by WLA. The number of shots was changed to 10 to 100 shots/location.

3.5.3 Difference in crystallinity of PEN and PET

Figure 3.19 indicates the crystallinity of annealed Si on PEN or PET substrates by WLA. The number of shots was set to 10 shots/location. The crystalline fraction of WLA poly-Si on PET substrate is much higher than that on PEN substrate, and the FWHM of WLA poly-Si on PET substrate is much lower than that on PEN substrate in all the laser energy densities. These results indicate that the crystallinity of WLA poly-Si films on PET is better than that on PEN.

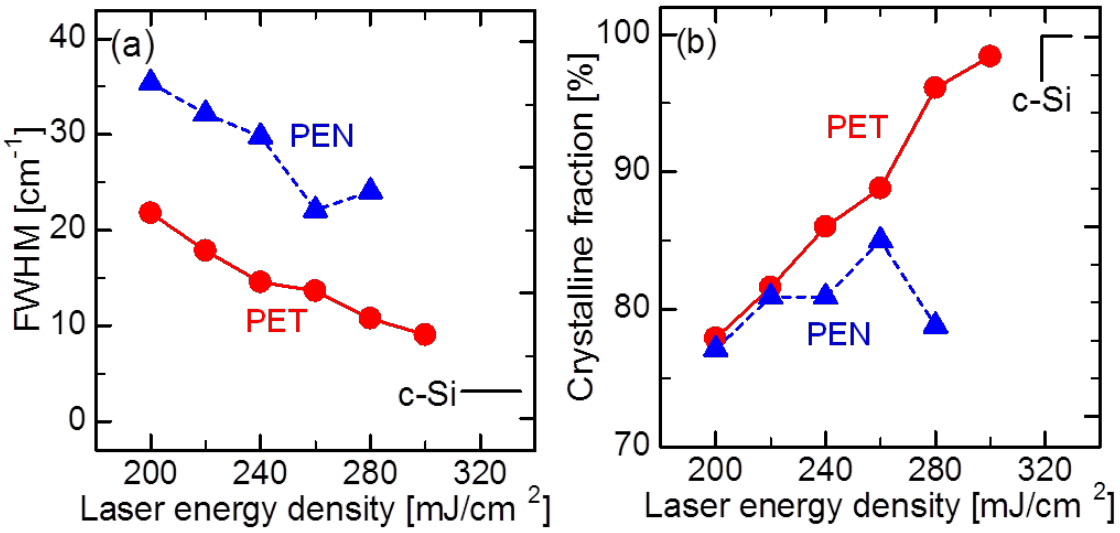

Figure 3.19: Relationship between the laser energy density and (a) FWHM of Raman peak and (b) crystalline fraction of WLA poly-Si on plastic substrates. The number of shots was 10 shots/location.

Figure 3.20 shows surface morphology images of **(a)** PEN substrates and **(b)** buffer SiO_2/SiN_x on the PEN substrates. **Figure 3.21** shows surface morphology images of **(a)** PET substrates and **(b)** buffer SiO_2/SiN_x on the PET substrates. The CTE of PEN (13 ppm/K) is comparable to that of PET (15 ppm/K), and the T_g of PEN is larger than that of PET. On the other hand, the rms of surface roughness of buffer layers on PEN substrate is higher than that of PET substrate as shown in **Fig. 3.20** and **Fig. 3.21**, although the deposition conditions of buffer layers and precursor a-Si is absolutely the same. There are many bumps on buffer layer surface on PEN substrate as compared to PET substrate. It is well known that grain growth starts near the interface between Si and buffer SiO_2 layers because the temperature of molten Si is easily reduces from that interface due to thermal diffusion to SiO_2 [21].

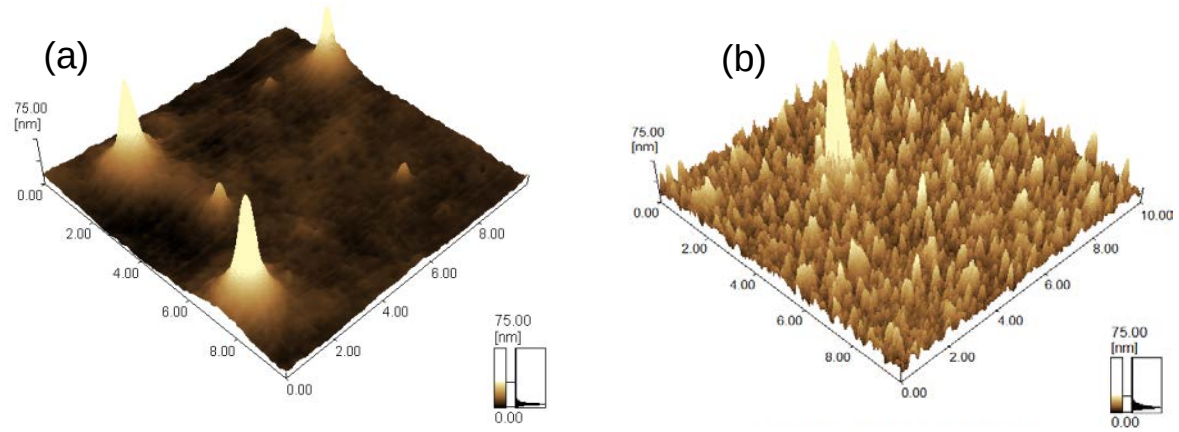

Figure 3.20: Surface topography images of (a) PEN substrate and (b) buffer SiO_2/SiNx on PEN substrates. The rms of surface roughness of (a) and (b) are 13.2 nm and 14.1 nm, respectively.

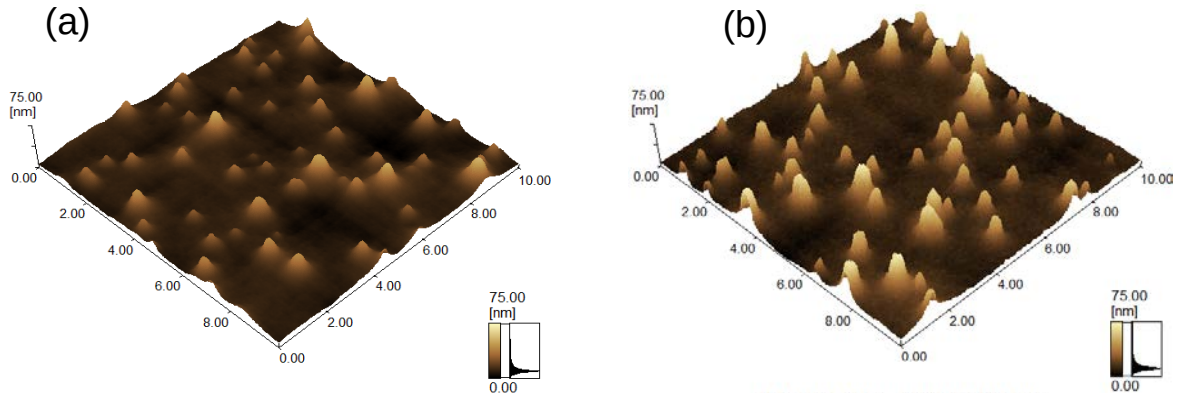

Figure 3.21: Surface topography images of (a) PET substrate and (b) buffer SiO_2/SiNx on PET substrates. The rms of surface roughness of buffer layers on (a) and (b) are 6.2 nm and 9.8 nm, respectively.

It is expected that molten Si at the valley of bumps shown in **Fig. 3.20** and **Fig. 3.21** is easily cooled because the efficiency of thermal storage is smaller as compared to peak of bump. **Figure 3.22** shows the schematic diagram of grain growth from the interface between Si and buffer SiO_2 layers during WLA in the case of **(a)** PEN and **(b)** PET substrates. In the case of PEN substrate shown in **Fig. 3.22 (a)**, many bumps at the Si/SiO_2 interface will

increase the crystal nucleus. Thus, it is speculated that grain growth is limited by the crystal nucleus. In contrast, the density of bumps at Si/SiO_2 interface is much lower in the case of PET substrate shown in **Fig. 3.22 (b)**. This could promote grain growth in the case of PET substrates. It is considered that surface morphology at the interface is very important to enhance the crystallinity of the poly-Si.

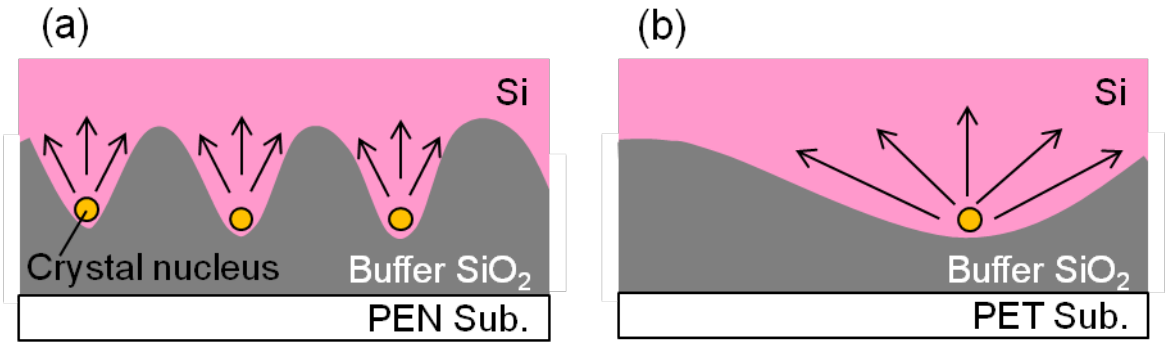

Figure 3.22: Schematic diagram of grain growth from the interface between Si and buffer SiO_2 layers during WLA in the case of (a) PEN and (b) PET substrates.

3.6 Summary

The super low-temperature crystallization of a-Si thin films on glass and plastic substrates was demonstrated by WLA. The a-Si films are also crystallized by conventional LA and their grain size, impurity, and electrical properties are determined. As the results, it is demonstrated that the crystallization to high-quality poly-Si films can be achieved by WLA as compared to LA. The maximum value of maximum grain size of WLA samples was 1.5 μm, and that of the

average grain size was about 3 times larger than that of LA samples. The crystalline fraction of WLA poly-Si is better than that of LA poly-Si and are comparable to the poly-Si films crystallized conventional ELA process. It is considered that WLA promotes giant and uniform grain growth by decreasing surface temperature and homogenization of temperature distribution of Si films.

In the SIMS measurements, it is determined that WLA poly-Si films contain more hydrogen than LA poly-Si films. In contrast, oxygen within the WLA poly-Si film is comparable to that of LA poly-Si and precursor a-Si films. In the μ-PCD measurements, the peak reflectivity of microwave which is proportional to the excess carrier lifetime from WLA poly-Si was larger than that of LA poly-Si although both poly-Si have the same average grain size. WLA realized the formation of poly-Si films which have not only higher crystallinity but also better electrical properties attributed to fewer electrical defects. Hydrogen in water vapor generated by WLA inactivates electrical defects, and WLA poly-Si indicated much better electrical properties than LA poly-Si films. Hydrogen concentration of WLA poly-Si films was the same level as FGA poly-Si films. Although short processing time and low-substrate temperature as compared to the case of FGA, we succeeded in the diffusion of hydrogen to poly-Si layer and improvement of its electrical properties. WLA is very promising technique for low-temperature fabrication technique of LTPS TFTs, and electrical devices using WLA poly-Si films as active layers must have excellent electrical properties.

The poly-Si films were successfully formed by WLA on PEN (T_g = 155°C) and PET (T_g = 70°C) substrates as well as on glass substrates. The energy margin and the crystallinity of the poly-Si films crystallized by WLA or LA were evaluated. As the results, it is demonstrated that WLA enhances the energy margin to crystallize without thermal damage to substrates or Si films. The energy margin in WLA was 1.6-2 times larger than that in LA. Moreover, the crystallinity of WLA poly-Si was much better than that of LA poly-Si. It is considered that WLA promotes grain growth by decreasing surface temperature and homogenization of temperature distribution. The crystallinity of WLA poly-Si on PET substrate is much higher than that on PEN substrate, although the CTE and deposition conditions are the same. Fewer bumps at the Si/SiO_2 interface in the case of PET substrate promote grain growth, resulting that higher crystallinity is achieved. It is suggested that surface morphology at the interface is very important to enhance the crystallinity of the poly-Si.

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Chapter 4

Activation of Dopant Ion and Inactivation of Electrical Defects by Underwater Laser Annealing

4.1 Introduction

For the use of LTPS TFT for the switching devices of next-generation displays such as SOP [1] using flexible plastic films, the processing temperature should be lower than 200°C: the T_g of typical plastic substrate. In chapter 3, crystallization of a-Si films on plastic substrates were demonstrated. Beside the crystallization to poly-Si thin films, there are two high-temperature annealing processes exceeds 200°C in the LTPS TFT fabrication process. The first process is an activation annealing of dopant ion [2]. The activation annealing of dopant ion has been generally performed by the furnace annealing in N_2 ambient at 500-600°C for several hours. Meanwhile, the dopant activation by using the ultra violet laser is proposed in recent years [3-6]. In this chapter, impact of WLA on dopant activation annealing has been studied. The second one is the inactivation treatment of electrical defects such as hydrogenation [7-11]. Low-temperature hydrogenation technique is very important and attractive technique for not only LTPS TFTs but also nanocrystalline or microcrystalline Si devices [12], because there are many electrical defects such as dangling bonds at grain boundary which deteriorate device

performance.

In this chapter, the activation annealing of dopant ion and the inactivation annealing of electrical defects after metalization are performed by WLA. The capability of dopant activation by WLA is clarified by the measurements of contact resistance and sheet resistance of the poly-Si in section 4.2. That of inactivation treatment after metalization is determined by device performance of TFTs in section 4.3.

4.2 Application of Underwater Laser Annealing to Activation of Dopant Ion

4.2.1 Measurement method of contact resistance and sheet resistance

Murrmann and Widmann used a simple transmission line model (TLM) considering both sheet resistance and the contact resistance [13]. They also described a structure to determine the contact resistance using linear and concentric contacts [14].

Figure 4.1 describes current transfer from semiconductor to metal represented by the arrows. When current flows from the semiconductor to the metal, it encounters the specific contact resistance ρ_c and sheet resistance R_{sh}, choosing the path of least resistance. The

potential distribution under the contact is determined by both ρ_c and R_{sh} according to [15, 16]

$$V(x) = \frac{I\sqrt{R_{sh}\rho_c}}{Z} \frac{\cosh\left(L - x \big/ L_T\right)}{\sinh\left(L \big/ L_T\right)} \tag{4.1}$$

where L is the contact length, Z the contact width, and the current I flowing into the contact. The voltage is highest near the contact edge x = 0 and drops nearly exponentially with distance. The "1/e" distance of the voltage curve is defined as the transfer length

$$L_T = \sqrt{\frac{\rho_c}{R_{sh}}} \tag{4.2}$$

The L_T can be thought of as that distance over which most of the current transfers from the semiconductor into the metal or from the metal into the semiconductor. Typical specific contact resistivity are $\rho_c \leq 10^{-6}\ \Omega\text{cm}^2$ for good contacts. The transfer length is on the order of 1 μm or less for such contacts. Contacts for constant resistance measurements are often longer than 1 μm. For such contacts, some of the contact is inactive during current transfer.

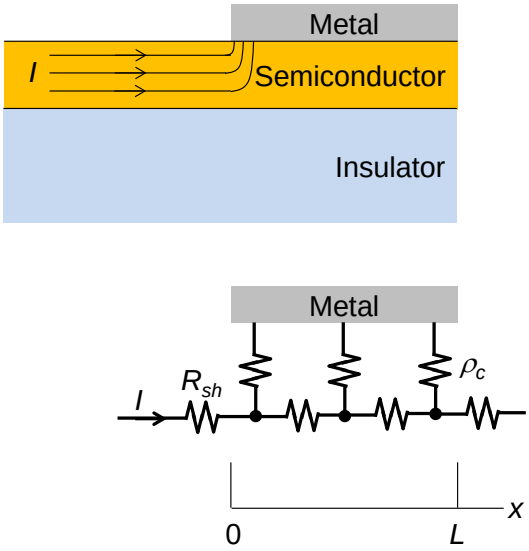

Figure 4.1: Current transfer from semiconductor to metal represented by the arrows. The semiconductor/metal contact is represented by the ρ_c - R_{sh} equivalent circuit with the current choosing the path of least resistance.

The total resistance, R_T is measured for various contact spacing and plotted versus d as illustrated in **Fig. 4.2**. For the TLM measurement of thin film samples, Z is generally made smaller than the diffusion width, W to prevent the sneak current from sample surface to back surface. Three parameters can be extracted from such a plot. The slope $\Delta R_T / \Delta d = R_{sh} / Z$ leads to the R_{sh} with the contact width Z independently measured. The intercept at $d = 0$ is $R_T = 2R_c$ giving the contact resistance. The intercept at $d = 0$ gives $-d = 2L_T$, which leads to the ρ_c with R_{sh} known from the slope of the plot. The transfer length method gives a complete characterization of the contact by providing the R_{sh}, the R_c, and the ρ_c.

With V measured between contact pair at $x = 0$, Eq. (4.1) and (4.2) give the contact front resistance as

$$R_{cf} = \frac{V}{I} = \frac{\sqrt{R_{sh}\rho_c}}{Z}\frac{\cosh\left(L - x/L_T\right)}{\sinh\left(L/L_T\right)} = \frac{\rho_c}{L_T Z}\frac{1}{\tanh(L/L_T)} = \frac{\rho_c}{L_T Z}\coth(L/L_T) \quad (4.3)$$

The expression R_{cf} is usually referred to simply as the contact resistance R_c. Two cases lead to simplification of Eq. (4.3). Provided $L \leq 0.5L_T$, $\coth\left(L/L_T\right) \approx L_T/L$ and

$$\boxed{R_c \approx \frac{\rho_c}{LZ}} \quad (4.4)$$

For $L \geq 1.5L_T$, $\coth\left(L/L_T\right) \approx 1$ and

$$\boxed{R_c \approx \frac{\rho_c}{L_T Z}} \quad (4.5)$$

The effective contact area $A_{c,\,eff}$ is the actual contact area $A_{c,\,eff} = A_c = LZ$ for the first case. However, in the second case the $A_{c,\,eff} = L_T Z$.

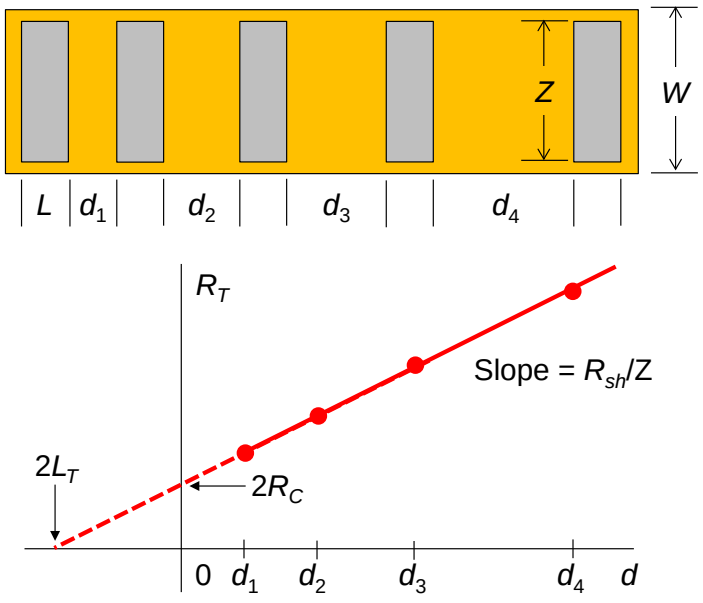

Figure 4.2: The test structure of transmission line model and a plot of R_T as a function of the interelectrode distance, d.

4.2.2 Experimental procedure

Test element group (TEG) for the TLM measurements was fabricated by processes as shown in **Table 4.1** and **Fig. 4.3**. In this experimental, poly-Si thin films on glass substrates were crystallized by conventional XeCl excimer laser annealing (wavelength = 308 nm) was used. The sample structure of the poly-Si substrate is poly-Si (50 nm)/buffer layers (100 nm-thick SiO_2 on 50 nm-thick SiN_x)/non-alkali glass substrate. The average grain size of crystallized poly-Si films was approximately 300 nm, and the rms of the surface roughness of the films was 11 nm. Firstly, patterning of the poly-Si film was performed by the inductive coupled plasma-reactive ion etching (ICP-RIE) using carbon tetrafluoride (CF_4) and O_2 gases for etching gas. A 100-nm thick SiO_2 was deposited by TEOS CVD at 300°C. In the TLM devices, gate-SiO_2 layer is not required. However, the SiO_2 layer is deposited for formation of uniform P doped layer within the poly-Si as shown in **Fig. 4.4** in this experiment. Next, phosphorous implantation was performed with the energy of 90 keV at a dose of 1.2×10^{15} cm^{-2}. Implanted P ion density within 50-nm thick poly-Si layer was estimated about 1×10^{20} cm^{-3} as shown in **Fig. 4.4**. Simulation of P ion implantation into the SiO_2/poly-Si/buffer layer structure was carried out by utilizing a SRIM. Subsequently, electrodes (Mo) were formed by RF magnetron sputtering deposition and a lift-off process after opening contact holes.

After TLM device fabrication, an activation annealing was performed by WLA, LA,

or FA. In the activation process by WLA and LA, a Q-switch Nd: YAG THG laser (wavelength = 355 nm) was used. **Figure 4.5** shows **(a)** schematic illustration of laser annealing system for WLA, **(b)** optical microscope image and **(c)** cross-sectional diagram of TEG for TLM measurements. Red dotted line in **Fig. 4.5 (b)** indicates laser irradiation area on the TLM device surface. The pulse duration time was around 4 nsec, and a repetition rate was 10 Hz. The beam size on the sample surface was 35 μm×300 μm. the number of shots was 200 shots/location. The irradiation energy for WLA and LA were 343 mJ/cm^2 and 345 mJ/cm^2, respectively. FA as conventional dopant activation was performed at 600°C for 5 h in N_2 ambient. For the TLM measurement, *Z* is usually made smaller than *W* to prevent the sneak current from sample surface to back surface. But the TEG devices, which are used in this experiment, are fully-isolated from back surface as shown in **Fig. 4.5 (c)**. Therefore it is no problem that *Z* is equal to *W*.

Table 4.1: Experimental procedure of TEG devices for TLM measurements

	Process	Method
0	Preparation of poly-Si	XeCl excimer laser crystallization
1	Patterining of poly-Si	ICP-RIE
2	Deposion of gate-SiO_2	TEOS CVD
3	Impurity doping	P ion implantation
4	**Activaton of dopant ion**	**Furnace annealing, FA**
		or **WLA**
		or **LA**
5	Formation of contact hole	Wet etching using BHF
6	Electrode formation	RF sputtering
7	Inactivation annealing	FA

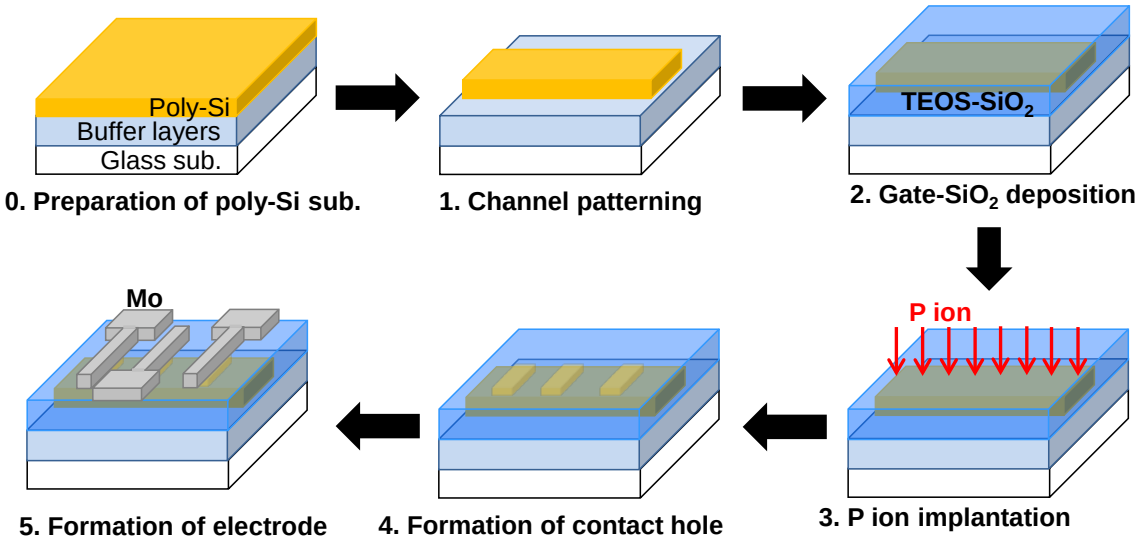

Figure 4.3: Schematic illustration of fabrication procedure of the device for TLM measurements.

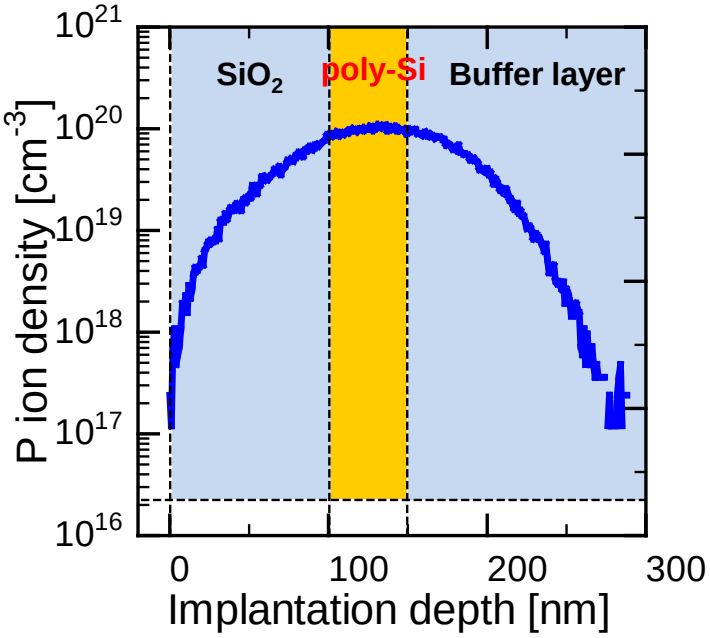

Figure 4.4: Simulation results of P ion profile during the ion implantation by utilizing SRIM. The energy for P implantation was 90 keV and the dose of 1.2×10^{15} cm^{-2}.

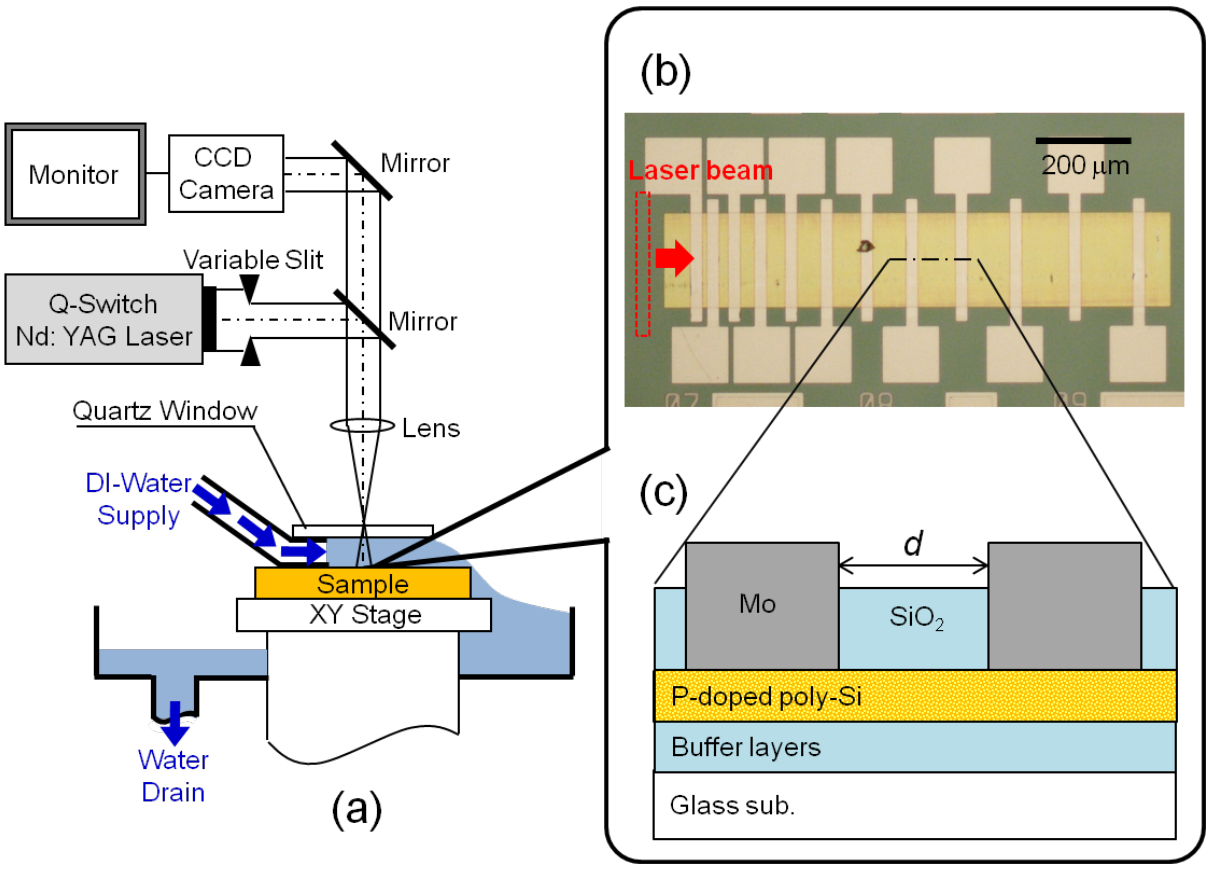

Figure 4.5: (a) Illustration of laser annealing system for WLA. (b) Optical microscope image of TLM device surface. Red dotted line indicates laser irradiation area on the TLM device surface. (c) Cross-sectional diagram of the TLM device.

4.2.3 Evaluation of activation

Figure 4.6 shows plots of R_T as a function of d of annealed TLM devices. **Table 4.2** shows the comparison of extracted TLM parameters. As shown in **Table 4.2**, the L_T estimated from WLA, LA, and FA samples are 0.3, 1.2, and 4.7 μm, respectively, and these TLM samples provides $L \geq 1.5L_T$. Therefore, the ρ_c is calculated by using Eq. (4.5). Next, the activation efficiency of each process was evaluated from obtaining of carrier concentration.

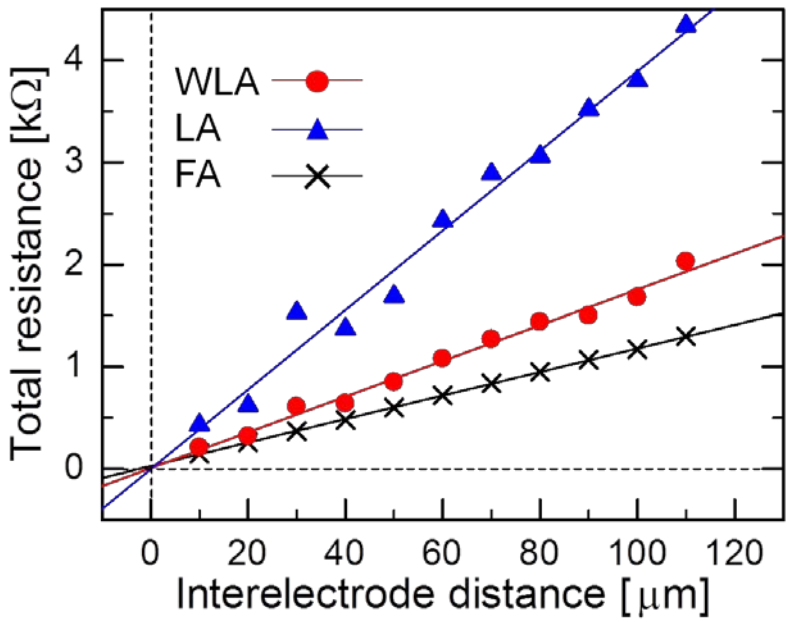

Figure 4.6: Plots of R_T as a function of d. Black, red, and blue lines show the fitted lines of R_T after conventional WLA, LA, and FA. The number of shots was 200 shots/location, and the irradiation energy for WLA and LA were 343 mJ/cm^2 and 345 mJ/cm^2, respectivery.

Table 4.2: Comparison of extracted TLM parameters

	L_T [μm]	R_c [Ω]	ρ_c [Ωcm^2]	R_{sh} [kΩ/sq.]
WLA	0.3	5	3×10^{-6}	5×10^{5}
LA	4.7	183	2×10^{-3}	9×10^{4}
FA	1.2	14	3×10^{-6}	8×10^{4}

Figure 4.7 shows **(a)** contact resistance and **(b)** carrier concentration of TEG samples calculated from TLM results shown in **Fig. 4.6**. Carrier concentration of TEG annealed by WLA was comparable to that by FA, although annealing time of WLA is much shorter than furnace annealing. It is demonstrated that dopant activation of LTPS TFTs can be performed by using WLA and LA. Activation efficiency of WLA is higher than that of LA although laser irradiation conditions were the same.

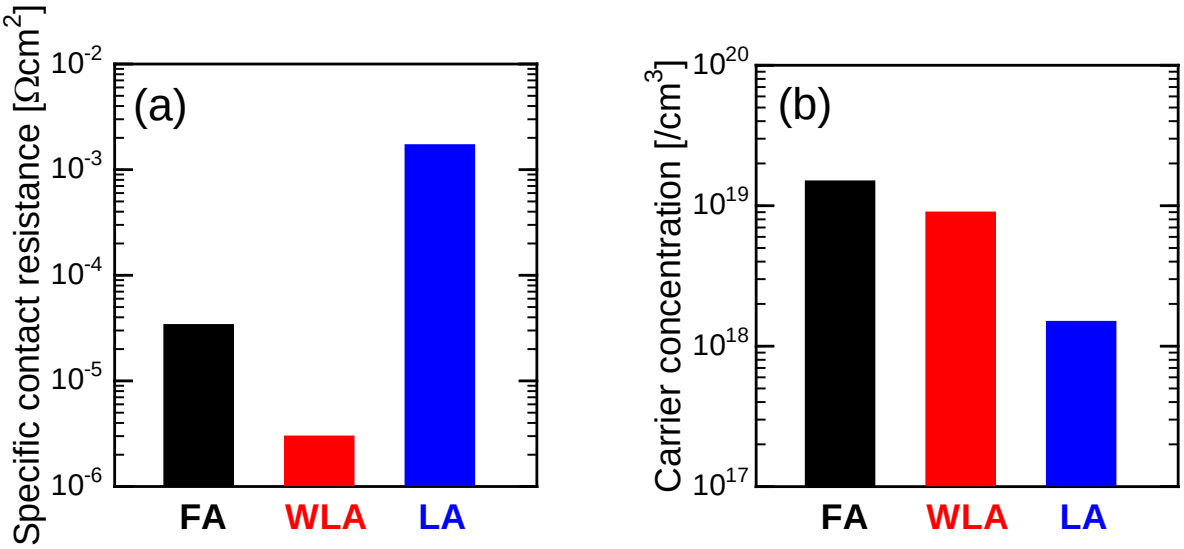

Figure 4.7: (a) Specific contact resistance ρ_c and (b) carrier concentration of TEG samples. The number of shots was 200 shots/location, and the irradiation energy for WLA and LA were 343 mJ/cm^2 and 345 mJ/cm^2, respectivery.

4.2.4 Discussion

Activation efficiency of WLA is higher than that of LA although laser irradiation conditions were the same. In the WLA, temperature distribution in poly-Si films was homogenized due to the presence of water layer on the sample surface. This effect might induce activation efficiency better as compared to LA. The contact resistance of WLA sample is lower than that of FA sample, however, this results include measurement uncertainty. It is very difficult to determine a precise amount of the contact resistance in the use of this device, because the contact resistance is negligible smaller than the sheet resistance as shown in **Table 4.2**. Although redesign of new TLM device which has shorter distance of electrodes pair is required for further refined analysis for contact resistance measurements, obtained contact resistance in thin experiments is small enough for TFT fabrication. TLM samples annealed by WLA or LA have large variation as compared to FA sample. In this experiment, YAG laser beam has Gaussian profile and interference pattern on irradiation area. Thus, it is speculated that the variation in input energy on annealed area in the case of WLA and LA becomes larger than in the case of FA. Homogenization of laser beam profile will be also needed for precise measurement of the R_{sh} and the R_c.

4.3 Application of Underwater Laser Annealing to Inactivation of Electrical Defects

4.3.1 Experimental procedure

Top-gate type n-channel LTPS TFTs were fabricated by using a conventional process. **Table 4.3** and **Figure 4.8** show a fabrication procedure for the LTPS TFT. The poly-Si thin films on glass substrates, which are crystallized by conventional XeCl excimer laser annealing (wavelength = 308 nm), was used for TFT channel. The sample structure of the poly-Si substrate is poly-Si (50 nm)/buffer layers (100 nm-thick SiO_2 on 50 nm-thick SiN_x)/non-alkali glass substrate. The average grain size of crystallized poly-Si film was approximately 300 nm, and the rms of the surface roughness of the films was 11 nm. Firstly, patterning of the poly-Si film in the channel layer was performed. A 100-nm thick gate-SiO_2 was deposited by TEOS CVD at 300°C and gate-electrodes (Ti) were formed by electron beam gun evaporation and a lift-off process. Next, phosphorous implantation was performed to the self-aligned source/drain region with the energy of 90 keV at a dose of 1.2×10^{15} cm^{-2}. Subsequently, an activation annealing at 600°C for 5 h in N_2 ambient was performed. Finally, source and drain-electrodes (Ti) were formed by the same process of the gate-electrode formation after opening contact holes. TFTs with the gate width of 5 μm and the length of 10 μm were used

for the measurement of TFT characteristics.

After fabrication of the LTPS TFTs, the TFTs were irradiated by a Q-switch Nd: YAG THG laser. As shown in **Fig. 4.9 (a)**, the laser beam irradiated to the TFT surface through a quartz window and flowing deionized (DI)-water. The quartz window assumes a role for avoiding the laser beam scattering from ruffle. We also carried out LA to the LTPS TFTs for comparison of electrical characteristics due to the difference in irradiation ambient. The pulse duration time was around 4 nsec, and a repetition rate was 10 Hz. The beam size on the sample surface was 100 μm×100 μm as shown in **Fig. 4.7 (b)**. The irradiation conditions were the irradiation energy density of 60 mJ/cm^2 and the number of shots of 100-500 shots/location. In this experimental, TFT characteristics were obtained using the selfsame LTPS TFT before and after WLA or LA, and valued electrical performance at the average of their properties from 3 TFTs. The μ_{FE} was extracted from the peak of the g_m from the Eq. (2.8).

Table 4.3: Experimental procedure of TFT fabrication

	Process	**Method**
0	Preparation of poly-Si	XeCl excimer laser crystallization
1	Channel patterning	ICP-RIE
2	Gate SiO_2 deposition	TEOS CVD
3	Gate-electrode formation	Vacuum evaporation and lift-off process
4	Source/drain region formation	Ion implantation
5	Activation of dopant ion	FA
6	Formation of contact hole	Wet etching using BHF
7	Source/drain electrodes formation	Vacuum evaporation and lift-off process
8	**Inactivation of electrical defects**	**FA**
		or **WLA**
		or **LA**

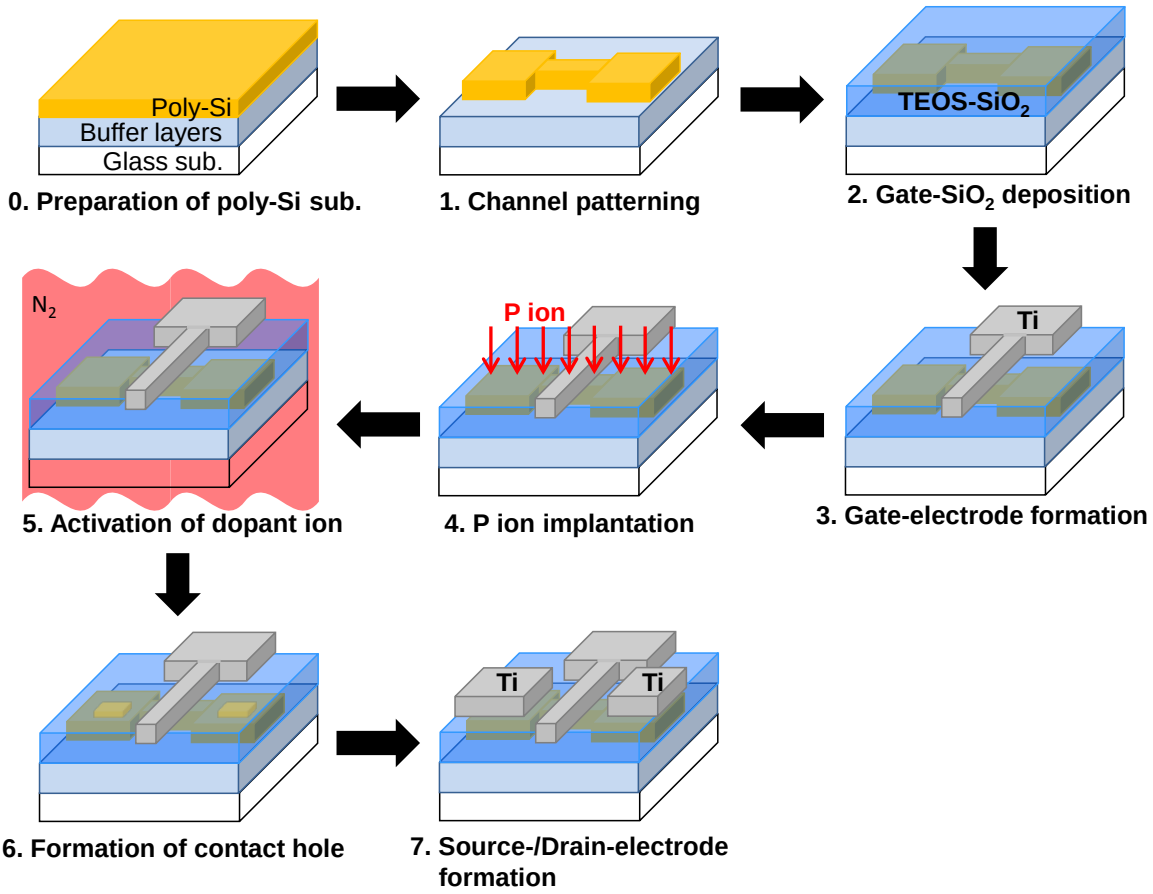

Figure 4.8: Schematic illustration of fabrication procedure of top-gate type n-channel LTPS TFT.

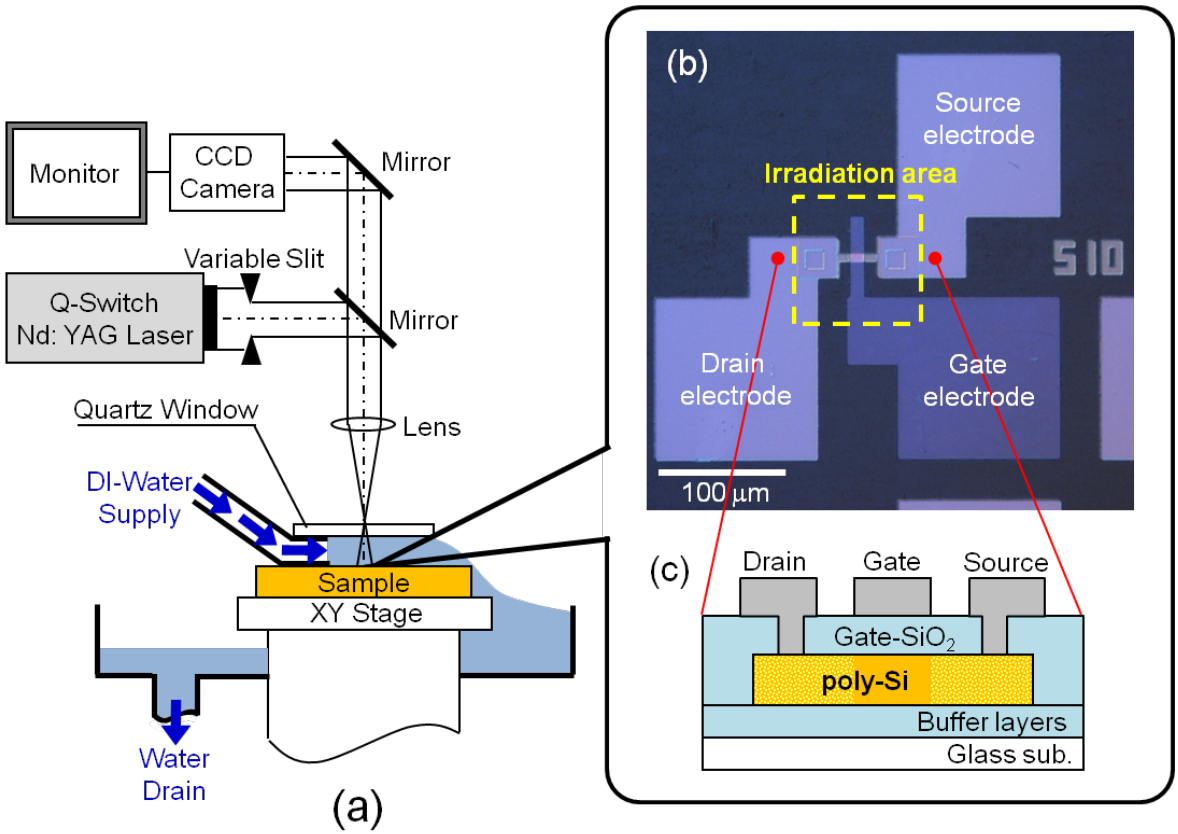

Figure 4.9: (a) Illustration of laser annealing system for WLA. (b) Optical microscope image of LTPS TFT surface. Yellow dotted-line indicates laser irradiation area on the TFT surface. (c) Cross-sectional diagram of the TFT.

Impurity of hydrogen, oxygen, and hydroxyl within the poly-Si films before and after WLA and LA was measured by SIMS using the Cs^+ primary ion. We prepared two kinds of samples for impurity evaluation. The structure of the first sample was 50 nm-poly-Si/buffer layers (SiO_2 and SiN_x)/non-alkali glass substrate. That of the second sample was 100 nm-SiO_2 films on the first sample. The formation conditions of the poly-Si substrates were the same as TFT fabrication processes, and 100 nm-SiO_2 films were deposited by TEOS CVD method under the same condition of gate-SiO_2 deposition process.

TFT characteristics were measured by using a semiconductor parameter analyzer (Agilent, Precision Semiconductor Parameter Analyzer 4156C). The field-effect mobility μ_{FE} consisting of linear regime mobility μ_{lin}, subthreshold swing (*S.S.*) and threshold voltage (V_{th}) of the LTPS TFTs were calculated by following equations [1]

$$\mu_{lin} = \frac{L}{WC_{ox}} \frac{1}{V_{DS}} g_m \tag{4.6}$$

$$S.S. = \frac{\partial V_{GS}}{\partial \{\log_{10}(I_d)\}} \tag{4.7}$$

$$I_{on} / I_{off} = \frac{I_{d\max}}{I_{d\min}} \tag{4.8}$$

The V_{th} was defined as the gate voltage (V_{GS}) where normalized drain current $I_{d'} = \frac{L}{W} I_d$ exceeds 1 nA.

4.3.2 Evaluation of inactivation by transistor property

Figure 4.8 shows the typical transfer curves in the linear region (drain-source voltage, V_{DS}) = 0.1 V) before and after **(a)** LA and **(b)** WLA. The irradiation conditions of LA and WLA were the irradiation energy density of 60 mJ/cm^2 and the number of shots of 500 shots/location. **Table 4.4** shows the comparison of extracted TFT parameters.

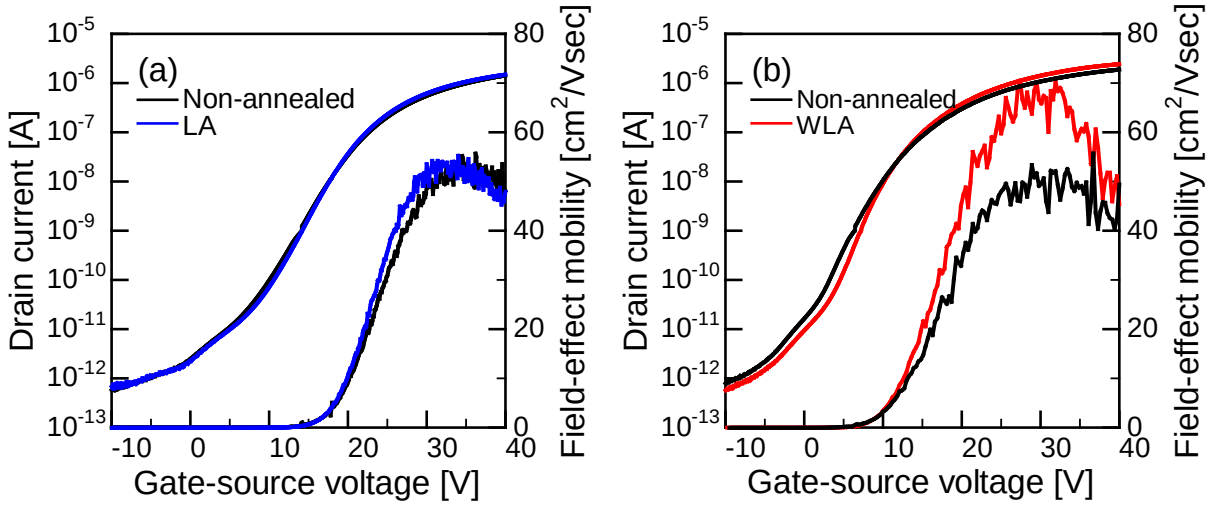

Figure 4.10: Transfer characteristics of the LTPS TFTs before and after (a) LA or (b) WLA. The number of shots was 500 shots/location, and laser energy density was 60 mJ/cm^2. V_{DS} = 0.1 V.

Table 4.4: Comparison of extracted LTPS TFT parameters

	LA sample		**WLA sample**	
	Before LA	**After LA**	**Before WLA**	**After WLA**
μ_{FE} [cm^2/Vsec]	53	56	52	72
I_{on}/I_{off} [-]	2×10^6	2×10^6	2×10^6	4×10^6
S.S. [V/dec]	3.41	3.20	2.60	2.16
V_{th} [V]	12.8	13.2	5.3	6.4

As shown in **Table 4.4**, TFT characteristics after LA showed little change of the μ_{FE} from 53 to 56 cm^2/Vsec. The I_{on}/I_{off} remained 2×10^6 and the sub-threshold slope (S.S.) was slightly decreased to 3.20 V/dec. In contrast, the transfer characteristics were remarkably improved after WLA. The I_{on}/I_{off} was enhanced to 4×10^6 and the S.S. was decreased to 2.16 V/dec. The μ_{FE} was increased from 52 to 72 cm^2/Vsec. Output characteristics were also improved. The inactivation of electrical defects in LTPS TFTs can be achieved successfully by

WLA.

Figure 4.11 shows **(a)** μ_{FE} change and **(b)** the threshold voltage (V_{th}) change between before and after laser irradiation. The solid red lines show the average change in the μ_{FE} ($\Delta\mu_{FE}$) for WLA TFTs, and the dotted blue lines show that for LA ones. In the initial properties, the V_{th} of the TFT showed positive value as shown in **Fig. 4.11**. Therefore, we defined positive shift of the V_{th} after laser irradiation means deterioration of TFT characteristics, and negative shift of the V_{th} implies improvement. The μ_{FE} of LA deteriorated with increasing number of shots. In addition, the ΔV_{th} also deteriorated and the dispersion of TFT properties is large. In contrast, the μ_{FE} of WLA increased at almost all of the irradiation conditions, and positive shift of the V_{th} and characteristic dispersion are much smaller. These results indicate that WLA has greater ability to improve electrical characteristics of LTPS TFTs. From these results, we speculated that water vapor generated by WLA plays important role to improve the TFT characteristics. Water vapor contains some active species such as hydrogen, oxygen, and hydroxyl. We thought that these active species inactivate electrical defects such as dangling bonds in the poly-Si resulting in WLA poly-Si films have better electrical characteristics than LA poly-Si films. Next, we focused on the impurity profiles of hydrogen, oxygen, and hydroxyl within the poly-Si films before and after WLA or LA.

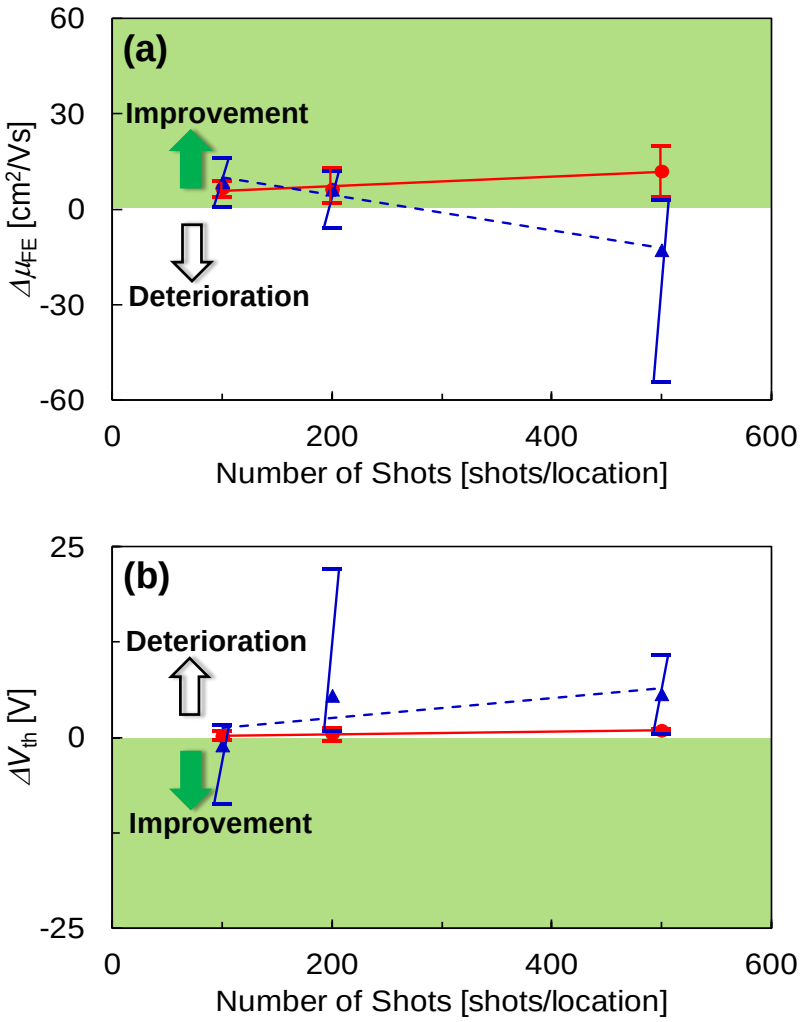

Figure 4.11: Dependence of change in the TFT properties on the number of shots: (a) field-effect mobility and (b) threshold voltage shift. The number of shots was 100-500 shots/location and the laser energy density was 60 mJ/cm^2.

Figure 4.12 shows the depth profiles of **(a)** ^{1}H, **(b)** ^{18}O, and **(c)** ^{18}O+^{1}H within the non-annealed, WLA, or LA poly-Si films (^{18}O was measured as oxygen owing to too high detector responses of SIMS against ^{16}O, and not to confuse ^{17}O with ^{16}O+^{1}H). Detected counts of oxygen and hydroxyl within the poly-Si films increased after WLA and LA, and those were the same level between WLA and LA samples. On the other hands, counts of hydrogen from the WLA poly-Si layer were larger than those from the LA and non-annealed poly-Si layers.

Estimated hydrogen concentrations of WLA and LA poly-Si films at the 25 nm deep were 1×10^{20} cm^{-3} and 5×10^{19} cm^{-3}, respectively. That value of non-annealed poly-Si film was 1×10^{19} cm^{-3}.

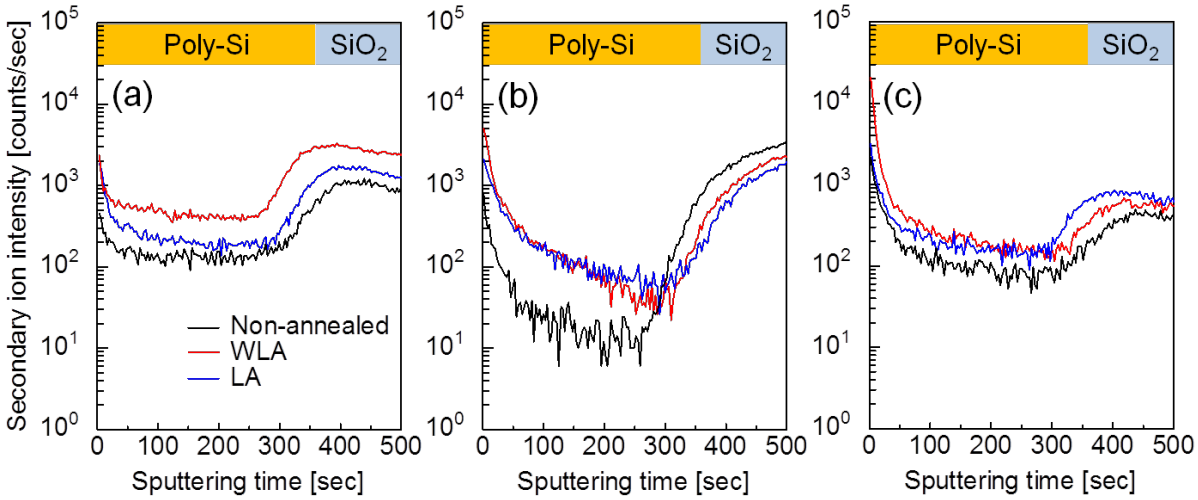

Figure 4.12: Depth profiles of (a) ^{1}H, (b) ^{18}O, and (c) $^{18}O+^{1}H$ within the WLA, LA, and non-annealed poly-Si films. WLA and LA were performed under the conditions of number of shots was 500 shots/location and laser energy density was 60 mJ/cm^2. Sample structure was 50 nm-poly-Si/buffer layers/non-alkali glass substrates.

Next, the impurity profile of the poly-Si films with gate-SiO_2 layers was measured. **Figure 4.13** shows the depth profiles of ^{1}H within the WLA poly-Si films annealed by various number of laser beam shots. Hydrogen diffuses into gate-SiO_2 and poly-Si films as shown in **Fig. 4.13**. It is striking that hydrogen concentration within the films in the case of 500 shots/location is the largest, and those values in the case of 100 and 200 shots/location are the same level. Concentration of oxygen and hydroxyl did not changed with increasing number of shots. These results indicate only hydrogen content grows with the increase of number of laser

beam shots in WLA. In addition, the increment of hydrogen content is well accorded with the dependence of change in the mobility on the number of shots as shown in **Fig. 4.11(a)**. From these results, we consider that diffused hydrogen into gate-SiO_2 and poly-Si layers inactivates electrical defects, and improves TFT characteristics. In the WLA, heating time by laser irradiation is much shorter than conventional inactivation annealing process such as FGA. Therefore, large number of shots is more efficient to improve the TFT properties, but even so, hydrogen diffuses into the poly-Si films through gate-SiO_2 layer, that is, WLA has ability of inactivation of electrical defects as well as FGA.

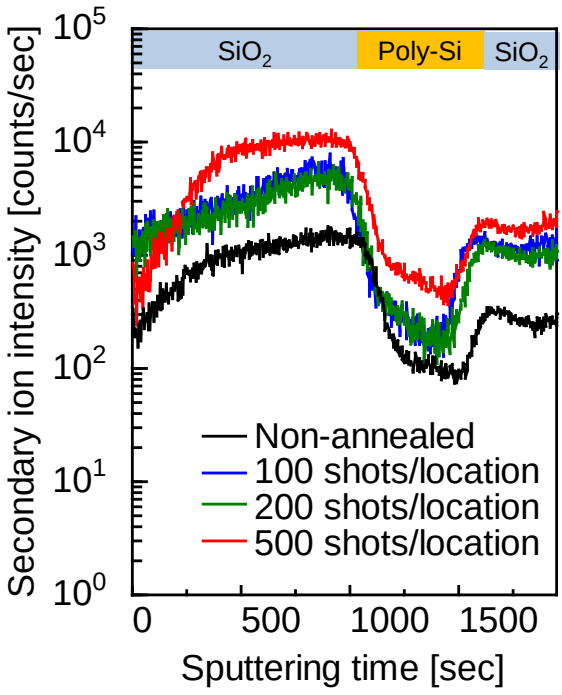

Figure 4.13: Depth profile of ^1H within the SiO_2 and Poly-Si films after WLA. The laser energy density was 60 mJ/cm^2. Sample structure was 100 nm-SiO_2/50 nm-poly-Si/buffer layers/glass substrate.

4.3.3 Discussion

The WLA results in vaporization of water on the TFT substrate surface, and thus the TFT surface is exposed to water vapor. Water vapor involves active species and they inactivate electrical defects such as dangling bonds in gate-SiO_2 and grain boundary of the poly-Si film [10, 11]. From the results of SIMS measurement as shown in **Fig. 4.12** and **Fig. 4.13**, hydrogen content within the WLA poly-Si and gate-SiO_2 films were higher than that of LA and non-annealed poly-Si films, although contents of oxygen and hydroxyl were the same level. It is considered that water vapor generated by laser irradiation contains larger amount of active hydrogen as compared to air. Hydrogen inactivates electrical defects such as dangling bonds in gate-SiO_2 or interface between SiO_2 and poly-Si in the WLA. In addition, WLA can reduce the substrate temperature due to the presence of flowing water, that is low-temperature inactivation treatment can be achieved. In the case of LA, the dispersion in mobility was very large and the V_{th} of TFTs widely shifted to the positive direction. It is thought that thermal damage caused by the rise in surface temperature creates newly electrical defects in the TFTs. Therefore, it is very import to form the water vapor on the TFT surface for effective inactivation of electrical defects at low-temperature.

Finally, we focused on the difference in the efficiency of TFT characteristics improvement between WLA and FGA. **Table 4.5** shows the comparison of extracted TFT

parameters. The measurement of TFT characteristics was performed by using the selfsame LTPS TFT. The annealing conditions of FGA were the H_2 concentration of 10%, annealing temperature of 200°C or 400°C, and annealing time of 1 h. FGA at 200°C was carried out after WLA and then, FGA at 400°C was performed.

Table 4.5: Comparison of extracted LTPS TFT parameters

	Non-annealed	**WLA**	**FGA at 200˚C**	**FGA at 400˚C**
μ_{FE} **[cm^2/Vsec]**	52	72	64	114
I_{on}/I_{off} **[-]**	2×10^6	4×10^6	1×10^7	7×10^7
S.S. [V/dec]	2.60	2.16	2.00	0.62
V_{th} **[V]**	5.3	6.4	4.5	2.2

Although FGA at 400°C greatly improved the TFT properties, this process is inapplicable to TFT fabrication process which uses plastic substrates due to low-T_g of typical transparent plastic film. In the case of FGA at 200°C which is the limitation for use of high-temperature-resistant transparent plastic substrates such as PAR, the μ_{FE} is smaller than that of WLA. Efficiency of TFT characteristics improvement by WLA is the same or higher than that by FGA at 200°C, although WLA has a disadvantage of shorter heating time resulting from the use of nanosecond pulse laser. In addition, we are convinced that we can overcome this disadvantage by changing the process order of WLA for inactivation after metalization or adding the processes of WLA for inactivation after metalization. For example,

if the crystallization to poly-Si films was performed by WLA, the inactivation of electrical defects at grain boundaries would be achieved. Likewise, WLA after gate-SiO_2 formation will inactivate electrical defects at the SiO_2/poly-Si interface. We would like to try to this approach in order to even improve TFT properties better at super low-temperature which is acceptable for the use of plastic substrates. We are sure of WLA's ability for super low-temperature fabrication of high-performance LTPS TFT.

4.4 Summary

Dopant activation and inactivation of electrical defects in LTPS TFTs after metalization were accomplished by WLA for temperature reduction of LTPS TFT fabrication. The devices using poly-Si films such as TLM devices and TFTs were irradiated by Nd: YAG THG laser in flowing DI-water. We also performed LA or FA in order to compare the difference in irradiation medium, annealing temperature, or annealing time.

Firstly, the dopant activation annealing by WLA has been performed. Dopant activation efficiency was determined by utilizing the TLM method. WLA successfully conducted activation annealing more effectively than conventional LA. In the WLA, temperature distribution in poly-Si films was homogenized due to the presence of water layer on the sample surface. It is speculated that this homogenization effect of temperature

distribution might increase activation efficiency better as compared to LA. R_c and R_{sh} of WLA samples are comparable to those of FA samples. It is concluded that the dopant activation by WLA is acceptable for LTPS TFT fabrication.

Secondary, the inactivation of electrical defects in LTPS TFTs has been accomplished by WLA. After TFT fabrication, WLA was performed. As the results, we investigated that WLA has more inactivation ability as compared to the LA. The mobility was increased from 52 to 72 cm^2/Vsec after WLA while that of LA was from 53 to 56 cm^2/Vsec. WLA also improved the I_{on}/I_{off} and the S.S. more than LA. In addition, we investigated hydrogen concentration within the WLA poly-Si and gate-SiO_2 films were much higher than that of non-annealed and LA poly-Si films, although those of oxygen and hydroxyl were the same level. Hydrogen content within the gate-SiO_2 and poly-Si films and the increment of mobility enlarged with the increasing number of laser beam shots in WLA. It is thought that hydrogen which is diffused from water vapor generated by WLA inactivates electrical defects in gate-SiO_2 and/or poly-Si film, and improves TFT characteristics. Moreover, the irradiation energy of WLA for inactivation annealing is much lower than that of WLA for crystallization on plastic films. Efficiency of TFT characteristics improvement by WLA is the same or higher than that by FGA at 200°C which is the limitation for use of high-temperature-resistant transparent plastic substrates, although WLA has a disadvantage of shorter heating time resulting from the use of nanosecond pulse laser. Consequently, we are sure of WLA's ability

for super low-temperature fabrication of high-performance LTPS TFT.

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Chapter 5
Fabrication of Thin Film Transistors using Polycrystalline Silicon Films Crystallized by Underwater Laser Annealing

5.1 Introduction

For the application of the poly-Si films formed by WLA to electrical devices, the LTPS TFT fabrication is conducted. Top-gate type n-channel LTPS TFTs are fabricated using WLA poly-Si as their channel layer, and their device performance are investigated by obtaining of output and transfer characteristics.

5.2 Fabrication Process of Thin Film Transistor

Top-gate type n-channel LTPS TFTs were fabricated by using a conventional process shown in **Table 5.1**. Poly-Si films crystallized by WLA or LA using the KrF excimer laser (wavelength = 248 nm) was used for TFT channel. The sample structure of the poly-Si substrate is poly-Si (50 nm)/quartz glass substrate. The number of laser shots was set to 10 shots/location, and the laser energy density was varied from 600 to 700 mJ/cm^2. Firstly,

patterning of the WLA poly-Si film in the channel layer was performed by dry etching process using the ICP-RIE. Subsequently, a 100-nm thick gate-SiO_2 film was deposited by TEOS CVD at 300°C and gate-electrodes (Ti) were formed by the electron beam gun evaporation and a lift-off process. Next, phosphorous implantation was performed to the self-aligned source/drain region with the energy of 90 keV at a dose of 1.2×10^{15} cm^{-2}. Subsequently, an activation annealing at 600°C for 5 h in N_2 ambient was performed. Finally, source and drain-electrodes (Ti) were formed by the same process of the gate-electrode formation after opening contact holes by wet etching process.

Table 5.1: Experimental procedure of TFT fabrication

	Process	**Method**
1	**Crystallization to poly-Si**	**WLA**
		LA
2	Channel patterning	ICP-RIE
3	Gate SiO_2 deposition	TEOS CVD
4	Gate-electrode formation	Vacuum evaporation and lift-off process
5	Source/drain region formation	Ion implantation
6	Activation of dopant ion	FA
7	Formation of contact hole	Wet etching using BHF
8	Source/drain electrodes formation	Vacuum evaporation and lift-off process
9	Inactivation of electrical defects	FA

5.3 Characterization of Thin Film Transistor

TFT characteristics were measured by using a semiconductor parameter analyzer (Agilent, Precision Semiconductor Parameter Analyzer 4156C). The field-effect mobility μ_{FE} consisting of linear regime mobility μ_{lin} and saturation regime mobility μ_{sat}, subthreshold swing (*S.S.*) and threshold voltage (V_{th}) of the LTPS TFTs were calculated by following equations [1]

$$\mu_{lin} = \frac{L}{WC_{ox}} \frac{1}{V_{DS}} g_m \tag{5.1}$$

$$\mu_{sat} = \frac{L}{WC_{ox}} \frac{1}{2I_d} g_m{}^2 \tag{5.2}$$

$$S.S. = \frac{\partial V_{GS}}{\partial \{\log_{10}(I_d)\}} \tag{5.3}$$

$$I_{on} \Big/ I_{off} = \frac{I_{d\max}}{I_{d\min}} \tag{5.4}$$

The V_{th} was defined as the gate voltage (V_{GS}) where normalized drain current $I_{d'} = \frac{L}{W} I_d$ exceeds 1 nA.

5.4 Performance of Thin Film Transistor

5.4.1 Output characteristics

Figure 5.1 and **Figure 5.2** show typical output characteristics of the LTPS TFTs using the

poly-Si films formed by **Fig. 5.1** LA and **Fig. 5.2** WLA. *W* and *L* of the TFTs was 10 μm and 20 μm, respectively. The output characteristics were obtained for various V_{GS} between 2 and 10 V. In both WLA and LA poly-Si samples, the I_d is modulated by the V_{GS} and shows good switching characteristics as well as conventional LTPS TFTs. The output curves show good saturation feature at the V_{DS} of 5.0 V. Thus, the linear and the saturation region were defined at the V_{DS} of 0.1 V and 5.0 V, respectively for transfer characteristic measurements.

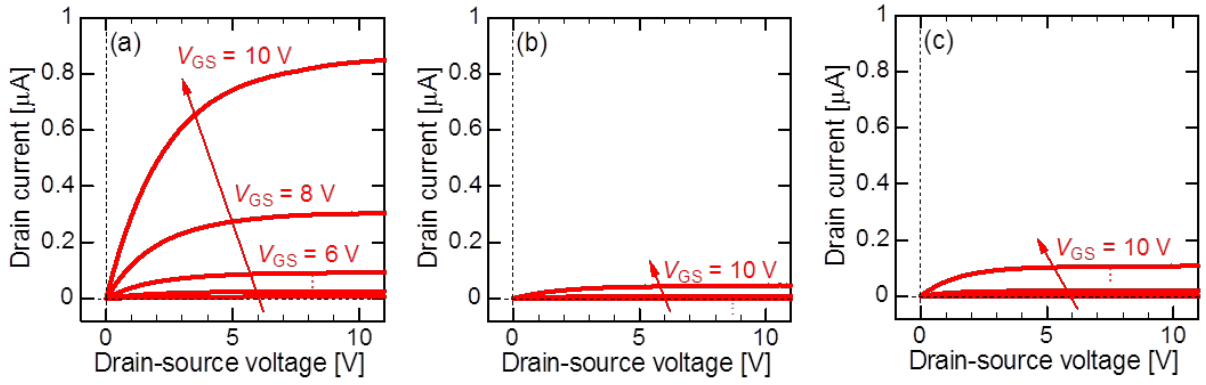


Figure 5.1: Typical output characteristics of TFTs using LA poly-Si as the channel layer. *W*/*L* = 10 μm/20 μm. V_{GS} = 2 to 10 V (2 V step). The average grain sizes of (a) 600 mJ/cm^2, (b) 650 mJ/cm^2, and (c) 700 mJ/cm^2 were 197 nm, 175 nm, and 96 nm, respectively.

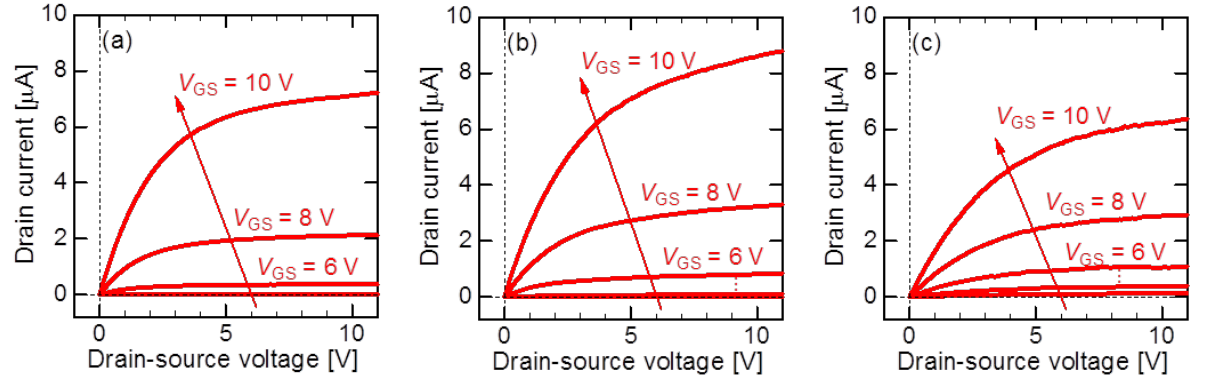


Figure 5.2: Typical output characteristics of TFTs using WLA poly-Si as the channel layer. *W*/*L* = 10 μm/20 μm. V_{GS} = 2 to 10 V (2 V step). The average grain sizes of (a) 600 mJ/cm^2, (b) 650 mJ/cm^2, and (c) 700 mJ/cm^2 were 543 nm, 487 nm, and 197 nm, respectively.

5.4.2 Transfer characteristics

Figure 5.3 and **Figure 5.4** shows typical transfer characteristics of the LTPS TFTs using the poly-Si films formed by **Fig. 5.3** LA and **Fig. 5.4** WLA. *W* and *L* of the TFTs were 10 μm and 20 μm, respectively. The transfer characteristics were measured for V_{DS} = 0.1 and 5.0 V. In both WLA and LA poly-Si samples, the I_d significantly increased with the increasing of the V_{GS} and the I_d-V_{GS} curves showed good switching operation. The μ_{FE} of the WLA poly-Si TFT was almost equal or higher than general LTPS TFTs (>50 cm^2/Vsec). The μ_{FE} of the TFT decreased and the switching characteristics deteriorated with the decreasing of the grain size of crystallized poly-Si films.

Table 5.2 indicates the comparison of extracted LTPS TFT parameters at linear region (V_{DS} = 0.1 V). In the same laser energy density of 600 mJ/cm^2, the μ_{lin} of LA and WLA were 17 and 101 cm^2/Vsec, respectively, and these values were the highest in all laser energy densities. These results are well accorded with the relationship between the average grain size and the laser energy density. It is thought that the decreasing of the number of the grain boundaries in channel region encourages carrier transport, resulting that the increasing of the field-effect mobility. The μ_{lin} of TFTs using WLA poly-Si is about 3-6 times larger than that using LA poly-Si, and the *S.S.* of TFTs using WLA is also better than that using LA poly-Si in all laser irradiation conditions. Moreover, the μ_{lin} of WLA poly-Si TFT is 3 times larger than

that of LA poly-Si TFT in the same average grain size comparison at 197 nm (LA; 600 mJ/cm^2, WLA; 700 mJ/cm^2). Other TFT characteristics of WLA poly-Si TFT are also better than LA poly-Si TFT. It is speculated that WLA poly-Si have better electrical properties owing to fewer electrical defects within the poly-Si as compared to LA poly-Si, because WLA has the ability of the inactivation effect during the crystallization. Consequently, it is concluded that the LTPS TFTs using WLA poly-Si as the channel layer show higher TFT performance due to higher-crystallinity and better electrical characteristics than LA poly-Si.

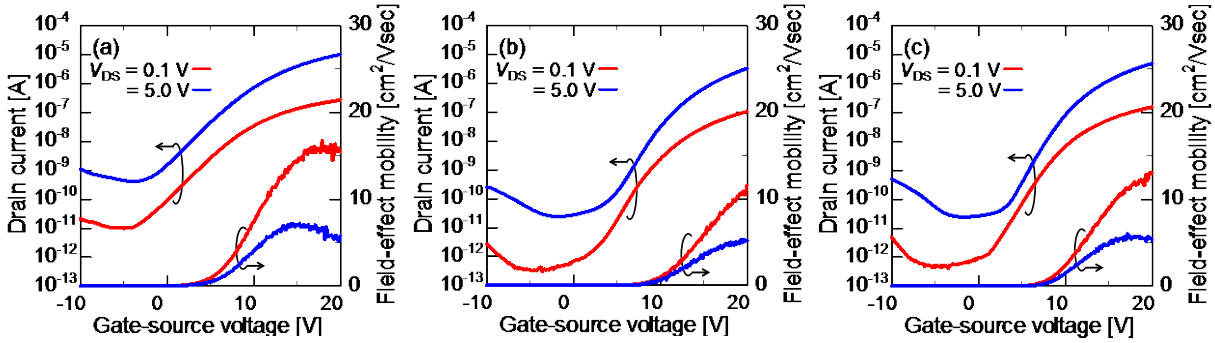


Figure 5.3: Typical transfer characteristics of TFTs using LA poly-Si as the channel. *W*/*L* = 10 μm/20 μm. V_{DS} = 0.1 and 5.0 V. The average grain sizes of (a) 600 mJ/cm^2, (b) 650 mJ/cm^2, and (c) 700 mJ/cm^2 were 197 nm, 175 nm, and 96 nm, respectively.

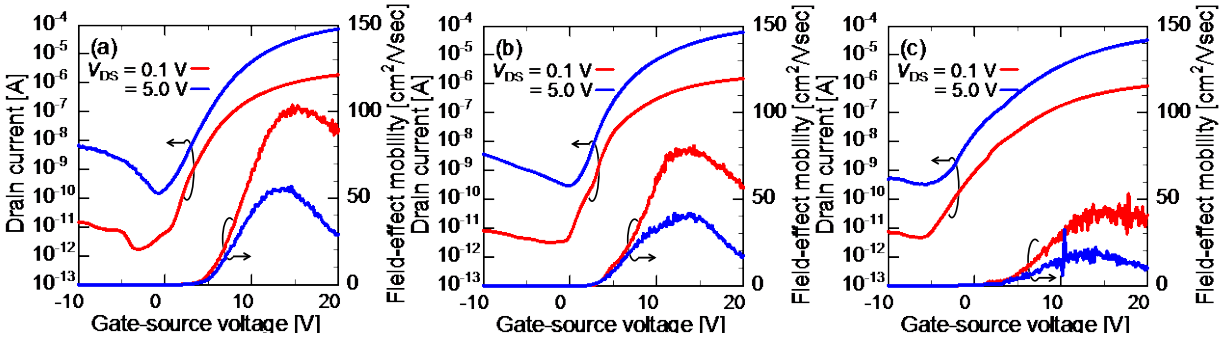


Figure 5.4: Typical transfer characteristics of TFTs using WLA poly-Si as the channel. *W*/*L* = 10 μm/20 μm. V_{DS} = 0.1 and 5.0 V. The average grain size of (a) 600 mJ/cm^2, (b) 650 mJ/cm^2, and (c) 700 mJ/cm^2 were 543 nm, 487 nm, and 197nm, respectively.

Table 5.2: Comparison of extracted LTPS TFT parameters at linear region (V_{DS} = 0.1 V).

	LA poly-Si TFT		
	600 mJ/cm^2	650 mJ/cm^2	700 mJ/cm^2
Average grain size [nm]	197	175	96
μ_{lin} [cm^2/Vsec]	17	13	15
I_{on}/I_{off} [-]	3×10^4	7×10^5	7×10^5
S.S. [V/dec]	3.3	2.0	1.9
V_{th} [V]	2.5	8.1	6.9

	WLA poly-Si TFT		
	600 mJ/cm^2	650 mJ/cm^2	700 mJ/cm^2
Average grain size [nm]	543	487	197
μ_{lin} [cm^2/Vsec]	101	79	45
I_{on}/I_{off} [-]	1×10^6	5×10^5	2×10^5
S.S. [V/dec]	0.8	0.8	1.6
V_{th} [V]	2.8	2.9	-0.6

5.4.3 Characteristic variation

Figure 5.5 shows optical microscope image of crystallized poly-Si substrate surface and LTPS TFT pattern in the poly-Si substrate. The size of the poly-Si substrate and TFT pattern was 10 mm × 13 mm and 3 mm × 5 mm, respectively, and thus, there are 6 TFT patterns in the substrate. In this experiment, 4 TFTs (W/L = 10 μm/20 μm) were extracted from each TFT pattern and the characteristic variation in the TFT substrate was evaluated.

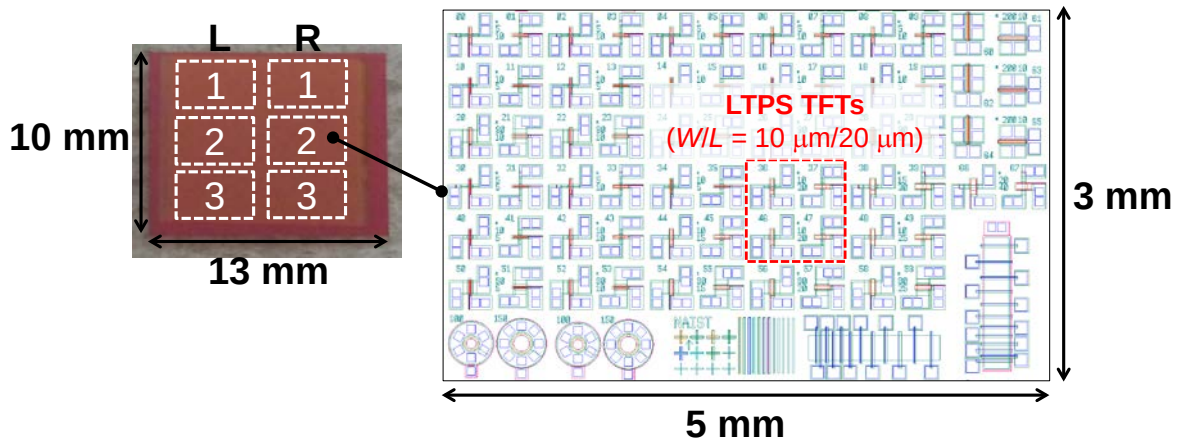
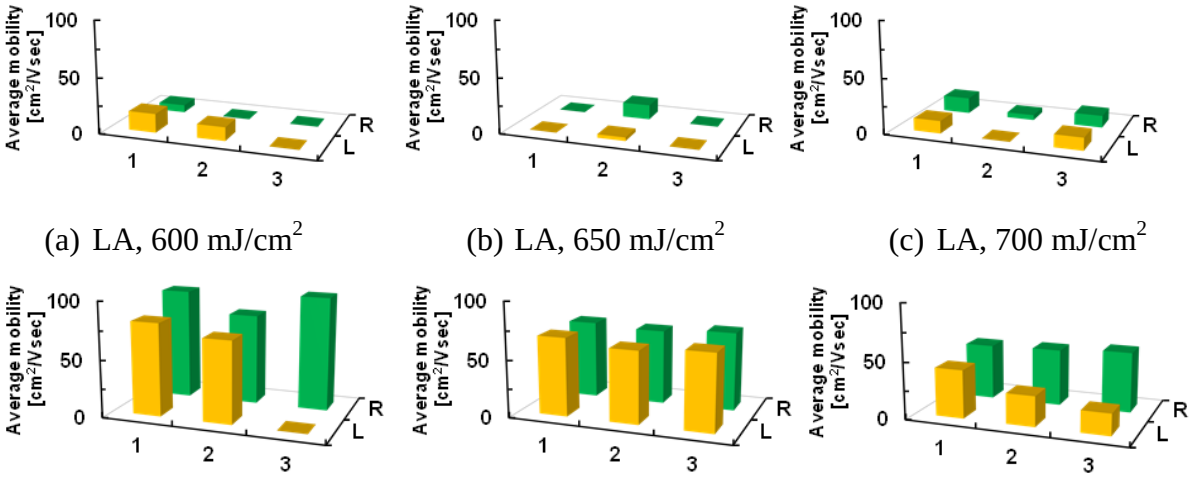


Figure 5.5 Optical microscope image of crystallized poly-Si substrate surface and TFT patterns in the poly-Si substrate.

Figure 5.6 and **Table 5.3** and **5.4** show the characteristic variation in LTPS TFT substrates crystallized by **(a-c)** LA and **(d-f)** WLA. The average μ_{lin} of LA poly-Si TFTs was around 10 cm^2/Vsec and the yield rate of the TFT was 8~58%, indicating that the TFT characteristic variation of LA poly-Si is poor. In contrast, the average μ_{lin} of WLA poly-Si TFTs was about 4-8 times larger than that of LA poly-Si TFTs, and the yield rate of the TFT was equal to or more than 63%. WLA poly-Si TFTs have not only higher device characteristics but also better uniformity in characteristic variation as compare to LA poly-Si TFTs.



(a) LA, 600 mJ/cm^2 (b) LA, 650 mJ/cm^2 (c) LA, 700 mJ/cm^2

(d) WLA, 600 mJ/cm^2 (e) WLA, 650 mJ/cm^2 (f) WLA, 700 mJ/cm^2

Figure 5.6 Characteristic variation in mobility at linear region (V_{DS} = 0.1 V).

Table 5.3: Comparison of the average mobility of TFTs between WLA and LA.

	Average mobility in substrate		
	600 mJ/cm^2	650 mJ/cm^2	700 mJ/cm^2
WLA	81 cm^2/Vsec	67 cm^2/Vsec	40 cm^2/Vsec
LA	12 cm^2/Vsec	8 cm^2/Vsec	10 cm^2/Vsec

Table 5.4: Comparison of the yield rate of TFTs between WLA and LA.

	Yield rate		
	600 mJ/cm^2	650 mJ/cm^2	700 mJ/cm^2
WLA	84%	79%	63%
LA	25%	8%	58%

5.5 Summary

Top-gate type n-channel LTPS TFTs using the poly-Si thin film formed by WLA or LA were

fabricated and their device performance was evaluated. As the result, it is clarified that WLA poly-Si films are applicable to the channel layer for the electrical devices. The WLA poly-Si TFTs showed clearly switching operation, and higher device characteristics as compared to LA poly-Si TFTs. Moreover, the performance uniformity of LTPS TFTs using WLA poly-Si is much better than those using LA poly-Si. Furthermore, the field-effect mobility of the WLA poly-Si TFT was equal or higher than general LTPS TFTs (>50cm^2/Vsec), and other TFT factors were also the same level or higher. Consequently, WLA poly-Si thin film has excellent electrical characteristics attributed to high-crystallinity and/or lower dense electrical defects.

References

[1] Y. Kuo, *Thin Film Transistors vol. 2*, Kluwer Academic, Norwell, (2004).

Chapter 6
Conclusions

6.1 Conclusions

For the realization of next-generation display such as high-definition display, multiple function display, or SOP using transparent flexible plastic substrates, high-quality poly-Si thin films formed at super low-temperature using the new laser annealing method utilizing flowing water has been demonstrated. Effects on grain growth, the crystallinity, electrical characteristics, and temperature distribution induced due to the laser irradiation of a-Si thin films in flowing water ambient have been investigated. In addition, new electrical characterization methods with the purpose of the understanding of the local electrical conduction property of the poly-Si films have been studied. Electrical characterization, which is able to distinguish electrical property of grain from grain boundary, is demonstrated. The main conclusions obtained in the present study are summarized as follows.

In chapter 2, local electrical characterization to distinguish grain boundary from grain in the poly-Si has been studied. Behavior of the electrons at defect sites in the poly-Si and the change in current distribution by area or hydrogenation process are determined using C-AFM and KFM measurements. In the grain, the reduction of current is induced due to the electron

emission from isolated defect sites. In grain boundary, current shows little changing, because there are dense defect sites. Hydrogen termination reduces the change in current drastically, meaning that electrical defects are almost inactivated. In addition, *I-V* curves of grain and grain boundary became similar to semiconductor conduction mechanism behavior due to the passivation of electrical defects in the poly-Si films after hydrogenation. Furthermore, it is suggested that hydrogen termination does not randomly progress, and there are regions which cannot be easily inactivated near grain boundaries. From C-AFM and KFM measurements, it is demonstrated that grain and grain boundary have different conduction mechanism. Conduction mechanism of grain and grain boundary changed after hydrogenation treatment, indicating that electrical defects within the poly-Si films are inactivated. SPM measurements can be certainly realized local electrical characterization.

In chapter 3, the WLA as super low-temperature laser annealing technique for poly-Si formation has been demonstrated. The crystallization of a-Si thin films on glass and plastic substrates has been achieved by WLA. It is determined that WLA promotes giant and uniform grain growth by decreasing surface temperature of substrate and homogenization of temperature distribution within the Si films. In addition, the energy margin for the crystallization without thermal damage to substrates is reduced in the WLA. The peak reflectivity of microwave in the μ-PCD measurement from WLA poly-Si is larger than that of LA poly-Si although both poly-Si films have the same average grain size. Furthermore, WLA

poly-Si films contain more hydrogen than LA poly-Si films and indicate lower current attributed to fewer electrical defects. Hydrogen in water vapor generated during WLA inactivates electrical defects, and WLA poly-Si indicates better electrical properties than LA poly-Si films. Hydrogen concentration of WLA poly-Si films was the same level as FGA poly-Si films. Although short processing time and low-substrate temperature as compared to the case of FGA, WLA succeeded in the diffusion of hydrogen to poly-Si layer and improvement of its electrical properties. It is obvious that WLA is very promising technique for low-temperature fabrication technique of LTPS TFTs, and electrical devices using WLA poly-Si films must have excellent electrical properties.

In chapter 4, WLA techniques have been applied to other high-temperature processes for LTPS TFT fabrication. Firstly, the dopant activation treatment by WLA has been studied. WLA successfully conducted activation annealing more effectively than conventional laser annealing, LA. The contact resistance and the sheet resistance of WLA samples are comparable to those of FA samples. It is concluded that the dopant activation by WLA is acceptable for LTPS TFT fabrication. Secondary, the inactivation of electrical defects in LTPS TFTs has been accomplished by WLA, and their electrical performance is improved at ambient temperature of RT. It is demonstrated that WLA has more inactivation ability as compared to the LA. The mobility was increased 30% after WLA while that of LA was 5%. WLA also improved other TFT factors such as *S.S.*, V_{th}, and I_{on}/I_{off} more than LA. In addition,

hydrogen concentrations within the WLA poly-Si and gate-SiO_2 films were higher than that of non-annealed and LA poly-Si films, although those of oxygen and hydroxyl were the same level. It is thought that hydrogen which is diffused from water vapor generated by WLA inactivates electrical defects in gate-SiO_2 and/or poly-Si film, and improves TFT characteristics.

In chapter 5, top-gate type n-channel LTPS TFTs using the poly-Si thin film formed by WLA are fabricated and their device performance has been investigated. LTPS TFTs using WLA poly-Si films show clearly switching operation. It is demonstrated that WLA poly-Si films are applicable to the active layer for the electrical devices. The field-effect mobility of the WLA poly-Si TFT was equal or higher than general LTPS TFTs (> 50cm^2/Vsec), and *S.S.* was also the same level or higher. Therefore, WLA poly-Si thin film has excellent electrical characteristics attributed to high-crystallinity and/or lower dense defects.

6.2 Future Work

Through this work, several bases for fabrication of thin film devices on plastic substrates at super low-temperature or confirmation of SPM methods as local characterization in poly-Si films have been established. However, there are still several issues to be solved and some challenges to be accomplished in the future.

- **Further clarification of local electrical characterization in SPM measurements for association with conventional characterization methods:**

  Although C-AFM and KFM measurements are powerful tools for the understanding of electrical properties, more investigation are needed. In this study, intrinsic poly-Si films are used for measurements, however, there are intrinsic and high-doped areas in micrometer or nanometer scale region in the TFT. SPM should distinguish the change in carrier density as well as other device characterization. From creation an association between SPM measurements and conventional device characterization such as Hall effect measurements, SPM will be well-established way of characterization.

- **Temperature reduction in other fabrication process of LTPS TFT:**

  There still remain some high-temperature processes in LTPS TFT fabrication: deposition of a-Si, gate-insulator layers. Although each high-temperature process is confirmed of fungible to super low-temperature process such as RF sputtering, the fabrication and characterization of thin film devices through a set of super low-temperature process is necessary for the use of plastic substrates.

List of Publications

A. Full Length Papers and Letters

1. E. Machida, Y. Uraoka, T. Fuyuki, R. Kokawa, T. Ito and H. Ikenoue
   "Characterization of Local Electrical Properties of Polycrystalline Silicon Thin Films and Hydrogen Termination Effect by Conductive Atomic Force Microscopy",
   Appl. Phys. Lett. **94**, 182104 (2009).

2. E. Machida, M. Horita, Y. Ishikawa, Y. Uraoka, and H. Ikenoue
   "Crystallization to Polycrystalline Silicon Thin Film and Simultaneous Inactivation of Electrical Defects by Underwater Laser Annealing",
   Appl. Phys. Lett. **101**, 252106 (2012).

3. E. Machida, M. Horita, K. Yamasaki, Y. Ishikawa, Y. Uraoka, and H. Ikenoue
   "Impact of Underwater Laser Annealing on Polycrystalline Silicon Thin Film Transistor for Inactivation of Electrical Defects at Super Low-Temperature",
   IEEE/OSA J. Disp. Technol. **PP**, 1 (2013).

4. E. Machida, M. Horita, Y. Ishikawa, Y. Uraoka, and H. Ikenoue
   "Super Low-Temperature Formation of Polycrystalline Silicon Films on Plastic Substrates by Underwater Laser Annealing",
   to be submitted to *J. SID.*

5. E. Machida, M. Horita, Y. Ishikawa, Y. Uraoka, and H. Ikenoue
   "Electrical Characterization of Polycrystalline Silicon Thin Films by Scanning Probe Microscopy",
   to be submitted to *J. Appl. Phys.*

B. Conferences Proceedings

1. E. Machida, Y. Uraoka, T. Fuyuki, M. Deki, M. Tani, and H. Ikenoue
   "Characterization of Local Electrical Properties of Poly-Si Thin Films by Conductive Atomic Force Microscopy and Effect of Hydrogen Termination",
   Proc. of the 5th Thin-Films Materials and Devices Meeting, 4-1 (2009).

C. Related Publications

1. K. Yamasaki, E. Machida, M. Horita, Y. Ishikawa, and Y. Uraoka
   "Thin-Film Devices Fabricated on Double-Layered Polycrystalline Silicon Films Formed by Green Laser Annealing",
   Jpn. J. Appl. Phys., Part 1 **51**, 03CA03 (2012).