Development and Analysis of High-Performance SiC Metal-Oxide-Semiconductor Devices with Phosphorus-Doped Gate Oxide

By

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To my parents and my brother

Abstract

To reduce both energy consumption and CO_2 emission, it is important to efficiently control electrical energy by using power devices. Over the past few decades, power electronics has been developed using Si-based power devices. However, Si-based devices have reached the limits of their material properties, and further progress is thought to be difficult. Therefore, wide-bandgap semiconductors, such as silicon carbide (SiC), have attracted much attention because their material properties are superior to those of conventional Si semiconductors.

SiC is the only wide-bandgap semiconductor that grows a thermal oxide (SiO_2), making it suitable for fabricating metal–oxide–semiconductor field-effect transistors (MOSFETs). However, significant challenges remain in commercializing SiC MOS devices. Most of the difficulties are associated with the high density of interface states at the SiO_2/SiC interface. Despite many years of development of SiC MOSFET devices by research groups worldwide, interface state density (D_{it}) is extremely high, resulting in low inversion channel electron mobility. Therefore, reducing D_{it} and consequently improving channel mobility of SiC MOSFETs is a key issue for the realization of competitive power SiC devices. In this study, an original technique that uses P atoms to improve the properties of the SiO_2/SiC interface is proposed, and the effect of P is discussed. This thesis consists of the following chapters.

In Chapter 2, overoxidation of ion-implanted substrates is employed as a technique to search for an element that effectively reduces D_{it}. The elements B, N, F, Al, P, and Cl were selected and incorporated into the SiO_2/SiC interface using overoxidation technique. The interface state density near the conduction band edge for Al-, B-, F-, and Cl-implanted MOS capacitors increased with implantation dose. In contrast, the

interface state density for N- and P-implanted samples decreased when the implantation dose was larger than 5.0×10^{12} cm^{-2}. Therefore, both N and P can reduce the interface state density.

In Chapter 3, a thermal anneal using phosphoryl chloride ($POCl_3$) is proposed to incorporate P atoms into the SiO_2/SiC interface without implantation damage. By annealing $POCl_3$ at 1000 °C, the interface state density near the conduction band edge decreased significantly, and channel mobility increased to 89 cm^2/Vs. This value of channel mobility is three times higher than that of standard 4H-SiC MOSFETs fabricated by NO annealing.

In Chapter 4, the presence of near-interface traps (NITs) in SiO_2/4H-SiC (0001) structures through phosphorus incorporation is investigated. Low-temperature capacitance–voltage and thermal dielectric relaxation current measurements were employed to investigate NITs in oxides prepared by dry oxidation, NO annealing, and $POCl_3$ annealing. These measurements showed that the density of electrons trapped in NITs in $POCl_3$-annealed oxide is lower than that of electrons trapped in NITs in dry and NO-annealed oxides. The drastic elimination of NITs in $POCl_3$-annealed oxide lowers D_{it} near the 4H-SiC conduction band edge and increases channel mobility in 4H-SiC MOSFETs. This result suggests that P atoms directly remove the strain at the interface and thus eliminate NITs.

In Chapter 5, charge-pumping measurements performed on 4H-SiC MOSFETs is discussed as a new technique to characterize interface states. These measurements showed that the unwanted geometric current component is included in the charge-pumping current, and the obtained data have a margin of error. The results indicate that the geometric component arises because of low channel mobility of

4H-SiC MOSFETs fabricated using conventional pyrogenic or NO annealing. A sufficiently long pulse fall time, in the order of 1–10 μs for n-channel 4H-SiC MOSFETs with a 10-μm gate length, is required to minimize the effect of the geometric component. In contrast, the geometric component is small for $POCl_3$-annealed MOSFETs because of high channel mobility. This study indicates that the charge-pumping method is useful for evaluating D_{it} of SiC MOSFETs, but the geometric component must be considered carefully in the measurements.

In Chapter 6, the effects of two different oxidation techniques, NO direct oxidation and $POCl_3$ post-oxidation annealing, on a C-face MOS interface were investigated. The results indicated that both NO and $POCl_3$ processes reduce D_{it} and improve channel mobility; however, for the C-face 4H-SiC MOSFET structure, both NO and $POCl_3$ processes generate extremely slow interface traps. Further, unloading the samples at room temperature reduced the density of interface states and slow traps. Therefore, in the case of the C-face, it is important to reduce not only the density of interface states but also the density of NITs.

In Chapter 7, the conclusions and outlook of this study are summarized. In addition, problems of the proposed method are summarized, and suggestions for future work to solve the problems are provided.

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Contents

Chapter 1
Introduction

1.1 Background

Human beings are faced with an unprecedented environmental crisis: global warming. In recent centuries, particularly after the industrial revolution in the late 18th century, human activity such as fossil fuel burning has increased the concentrations of atmospheric greenhouse gases. The increased concentration of gases blocks the escape of thermal infrared radiation, leading to elevated global surface temperatures. This temperature rise will cause long-term climate change worldwide and will gradually devastate the world's ecosystems. The concentration of CO_2 in the air is the highest since the past 600,000 years. To eliminate the problems caused by climate change and to create a sustainable society, we must develop a new technology to save energy.

Electricity that operates many of the devices in our society is generated from power plants that burn fossil fuels to generate electrical power. The percentage of energy consumed in the form of electricity is more than 40% in developed countries, and it is projected to increase in the future. To reduce both energy consumption and CO_2 emission, it is important to efficiently control electrical energy by using the technology of power electronics. Power electronics is the application of solid-state electronics for the control and conversion of electric power. It enables DC/DC, DC/AC, AC/DC, and AC/AC power conversion. This power conversion is essential for use in inverters or converters for air conditioners, photovoltaics, electric trains, electric vehicles, hybrid electric vehicles, and high-voltage electrical power transmission. Hence, power

electronics plays an important role in our daily lives. Reducing energy loss during the power conversion process is important for reducing energy consumption and thus greenhouse gas emission.

Over the past few decades, power electronics has been developed using Si-based power devices, such as metal–oxide–semiconductor field-effect transistors (MOSFETs), gate turn-off thyristors (GTOs), and insulated gate bipolar transistors (IGBTs). However, Si-based devices have reached the limit of their material properties, and further progress is thought to be difficult. Therefore, wide-bandgap semiconductors, such as SiC, GaN, and diamond, have attracted much attention because their material properties are superior to those of conventional Si semiconductors. Among the wide-bandgap semiconductors, SiC is the only semiconductor that can form native oxide (SiO_2). This feature enables SiC to be fabricated into insulated-gate power devices such as MOSFETs and IGBTs by thermal oxidation. In addition, GaN and diamond wafers are low-quality and expensive, and their commercialization would take a long time. Therefore, SiC is the front runner in next-generation power electronics. However, significant challenges remain in commercializing SiC power devices, as described in the following sections.

1.2 SiC materials and device properties

1.2.1 Materials properties

SiC is a group-IV compound semiconductor that consists of tetrahedrally bonded Si and C atoms that always maintain 50%-50% composition. A SiC crystal has 88% of covalent bonds and 12% of ionic bonds and is thermally, chemically and physically stable. SiC is known as a material existing in many different polytypes. There are more than 250 polytypes; however, the lattice structure can only be cubic (C), hexagonal (H) and rhombohedral (R). The Si–C bond length is 0.189 nm for all polytypes, indicating a stronger atomic interaction than in Si where the Si–Si bond length is 0.235 nm. The difference among the polytypes is the stacking order between bilayers of C and Si atoms. In a close-packed structure, each Si–C bilayer can be situated in one of three possible positions, which are denoted by A, B, and C as illustrated in Fig. 1.1. Using this notation, the stacking orders of 3C-, 4H-, and 6H-SiC are illustrated in Fig 1.2 [1].

The different polytypes have widely ranging properties. The most important polytypes for power devices are 3C-, 4H-, and 6H-SiC. Table 1.1 lists physical properties of 3C-, 4H-, and 6H-SiC [1]. Most of the recent reports for power electronics applications are based on 4H-SiC devices because of the superior material properties. The wide bandgap of 3.26 eV at room temperature enables that the device can be operated at high temperatures over 300 °C. The breakdown field of about 2.8 MV/cm is one order of magnitude higher than Si, leading to low on resistance in power devices as described later. The high thermal conductivity originates from lighter C atoms that easily vibrate in a crystal. This feature allows better dissipation of the heat in power devices. Because of these excellent properties, SiC is expected for high-power,

high-frequency, and high-temperature device operations [1].

The hexagonal unit cell is shown in Fig. 1.3. Because of the hexagonal lattice system, the crystal faces are represented using the Bravais-Miller index with 4 numbers. The commonly used faces for device manufacturing are (0001) Si-face, $(000\bar{1})$ C-face, and $(11\bar{2}0)$ a-face. The surface density of Si and C atoms is different for each face. The Si-face has 100% Si atoms, C-face has 100% C atoms and a-face has 50% of each. The fabricated device properties and chemical behaviors are absolutely different for each face as will be described in Section 1.3.

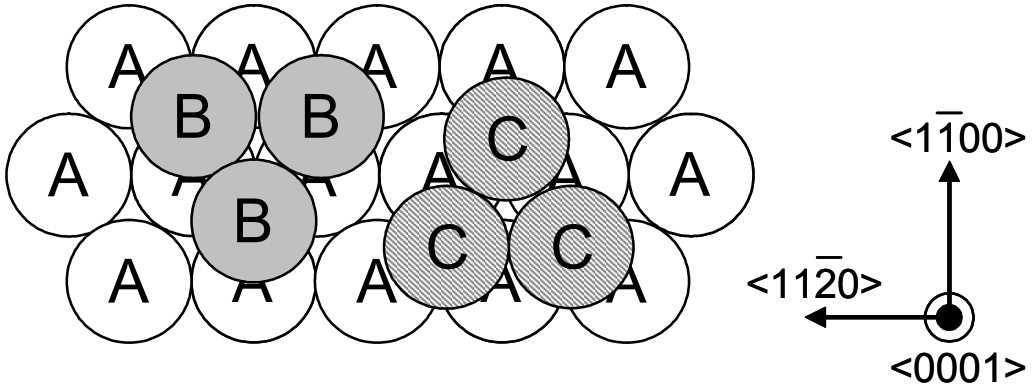
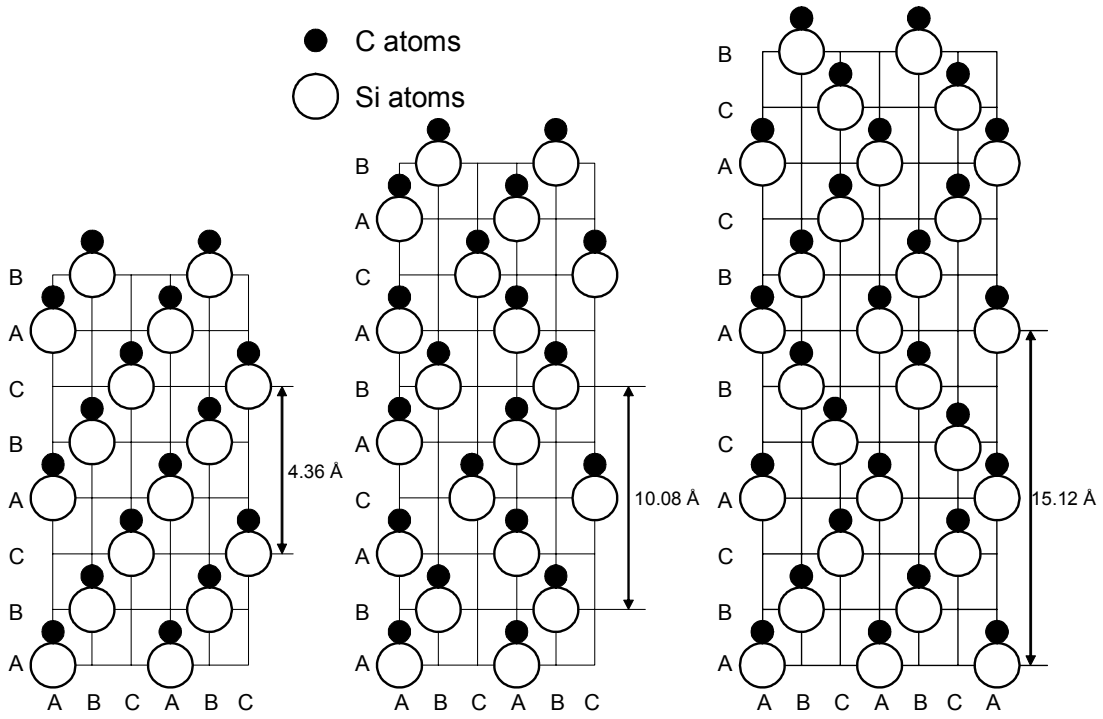


Fig. 1.1. Close-packed structure filled up with many balls. Each Si–C bilayer can be situated in one of three possible positions, which are denoted by A, B, and C.



(a) 3C-SiC (b) 4H-SiC (c) 6H-SiC

Fig. 1.2. Stacking orders of (a) 3C-, (b) 4H-, and (c) 6H-SiC. Open and closed circles indicate Si and C atoms, respectively.

Table 1.1 Physical properties of 3C-, 4H-, and 6H-SiC [1]

	3C-SiC	4H-SiC	6H-SiC
Lattice constant (Å)	4.36	$\boldsymbol{a}$ = 3.09 $\boldsymbol{c}$ = 10.08	$\boldsymbol{a}$ = 3.09 $\boldsymbol{c}$ = 15.12
Bandgap (eV)	2.23	3.26	3.02
Electron mobility (cm^2/Vs)	1000	1000 ($\perp c$) 1200 ($//c$)	450 ($\perp c$) 100 ($//c$)
Hole mobility (cm^2/Vs)	50	120	100
Breakdown field (MV/cm)	1.5	2.8	3
Saturation drift velocity (cm/s)	2.7×10^7	2.2×10^7	1.9×10^7
Thermal conductivity (W/cmK)	4.9	4.9	4.9
Permittivity	9.72	9.7 ($\perp c$) 10.2 ($//c$)	9.7 ($\perp c$) 10.2 ($//c$)

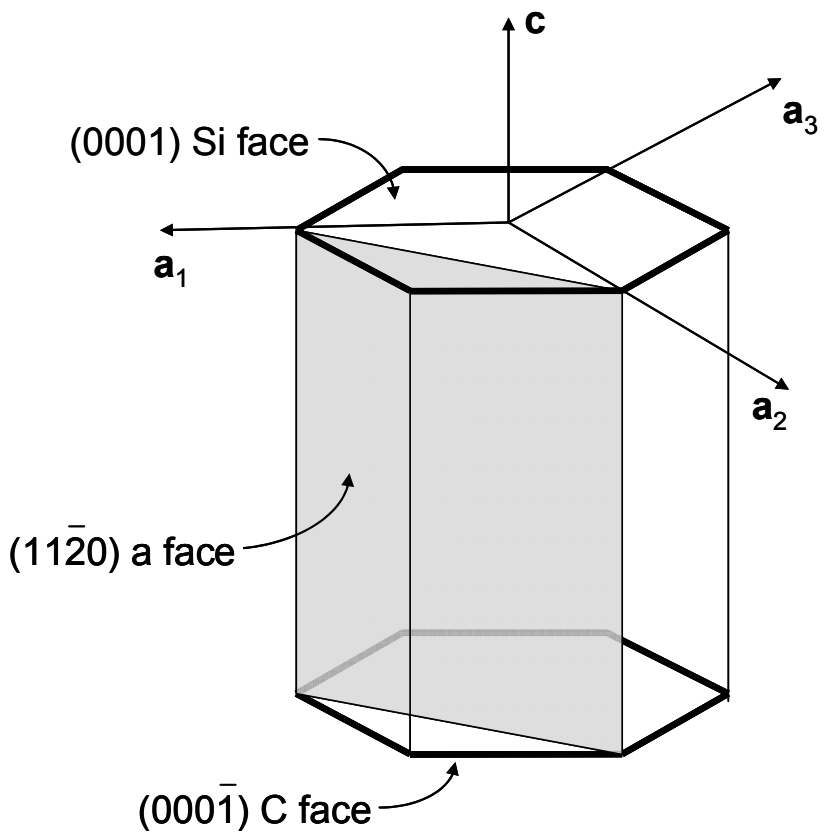


Fig. 1.3. Hexagonal unit cell and important crystal orientations.

1.2.2 SiC device physics

A basic structure of SiC power MOSFETs is double-implanted MOSFET (DMOSFET) illustrated in Fig. 1.4. The p-type channel and n^+-type source and drain regions are formed by double implantation of Al and P, respectively. The on-resistance of a DMOSFET is determined by various contributions along the path of electrons as shown in Fig. 1.4: source contact resistance R_{cs}, source resistance R_n, channel resistance R_{ch}, junction FET (JFET) resistance R_j, drift resistance R_{drift}, substrate resistance R_{sub}, and drain contact resistance R_{cd}.

Power devices block reverse voltage by the depletion layer at the p-n junction. Figure 1.5 illustrates the relationship between the electric field and distance in a drift

layer with a one-sided abrupt p^+-n junction. In the case of non-punch-thorough design, breakdown occurs before the entire drift layer is depleted. The area of the triangle in Fig. 1.5 is equivalent to the blocking voltage (V_B) as given by

$$V_B = \frac{1}{2}\mathcal{E}_{s,max} W_d = \frac{\varepsilon_s \mathcal{E}_{s,max}^2}{2qN_D}. \quad (1.1)$$

where $\mathcal{E}_{s,max}$ is electric field at the surface, W_d is depletion layer width, ε_s is permittivity of the semiconductor, q is elementary charge and N_D is doping concentration of the drift layer [2]. SiC has about ten times higher breakdown field strength ($\mathcal{E}_c$) and, thus, allows ten times higher $\mathcal{E}_{s,max}$ compared to Si. Hence, the thickness of drift layer (d_{drift}) can be about ten times thinner in SiC than in Si to maintain the same blocking voltage. In addition, the doping concentration, namely, the slope of the lines in Fig. 1.5, can be about 100 times higher in SiC. The specific on-resistance of the drift layer is simply given by

$$R_{drift} = \frac{d_{drift}}{q\mu_n N_D} \quad (1.2)$$

where μ_n is the bulk electron mobility in the drift region [3]. Note that the current spreading was ignored. The d_{drift} can be about 1/10 and N_D can be 100 times higher, but the electron mobility in SiC is smaller than that in Si. Therefore, the drift resistance of SiC devices becomes about 1/300 compared to that of Si devices.

In a non-punch-thorough structure, the suitable thickness and doping concentration of the drift layer can be obtained from Fig. 1.5. The maximum electric field at the surface ($\mathcal{E}_{s,max}$) can be obtained when the electric field becomes zero at the drift layer/substrate interface ($W_d = d_{drift}$). Namely, the suitable design is obtained when

$$d_{drift} = \frac{2V_B}{\mathcal{E}_{s,max}} \quad (1.3)$$

and

$$N_{\mathrm{D}} = \frac{\varepsilon_{\mathrm{s}} \mathcal{E}_{\mathrm{s,max}}}{q d_{\mathrm{drift}}}. \tag{1.4}$$

Using Eqs. (1.3) and (1.4), N_{D} in Eq. (1.2) can be eliminated as

$$R_{\mathrm{drift}} = \frac{4 V_{\mathrm{B}}^2}{\mu_{\mathrm{n}} \varepsilon_{\mathrm{s}} \mathcal{E}_{\mathrm{s,max}}^3}. \tag{1.5}$$

The theoretical limit of on-resistance in power devices can be estimated using Eq. (1.5).

Another large contribution to the on-resistance is channel resistance (R_{ch}). The channel resistance of a MOSFET inversion layer is given by

$$R_{\mathrm{ch}} = \frac{LP}{2\mu_{\mathrm{ch}} C_{\mathrm{ox}} \left(V_{\mathrm{G}} - V_{\mathrm{T}} \right)} \tag{1.6}$$

where L is the channel length, P is the cell pitch, μ_{ch} is the electron mobility in the inversion layer, C_{ox} is the oxide capacitance per unit area, V_{G} is the gate voltage and V_{T} is the threshold voltage [3]. $C_{\mathrm{ox}}(V_{\mathrm{G}} - V_{\mathrm{T}}) = \varepsilon_{\mathrm{ox}} \mathcal{E}_{\mathrm{ox}}$, where $\varepsilon_{\mathrm{ox}}$ is permittivity of the oxide and $\mathcal{E}_{\mathrm{ox}}$ is the oxide electric field. It is clear that the channel mobility is inversely proportional to the channel resistance.

Figure 1.6 shows the theoretical limit of on-resistance as a function of blocking voltage. The impact of R_{ch} on the specific resistance is also shown by assuming typical values (L = 1 μm, P = 15 μm, $\mathcal{E}_{\mathrm{ox}}$ = 3 MV/cm). It is evident that the on-resistance of power MOS devices strongly depends on the channel mobility. However, as described in Section 1.3, the interface state density at SiO_2/SiC interface is high, resulting in low inversion channel electron mobility and thus high channel resistance. Therefore, the low drift resistance of SiC is cancelled out by the high channel resistance. In order to reap the full benefits of silicon carbide, channel mobility must be improved as high as possible. One of the main purposes of this work is to reduce the high density of

interface states and improves the channel mobility.

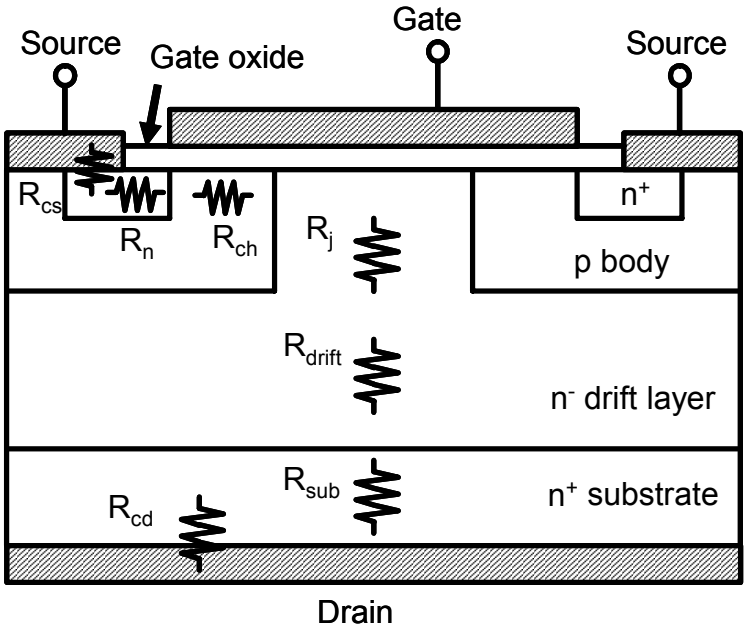


Fig. 1.4. Typical structure of a SiC DMOSFET and various contributions to the on-resistance.

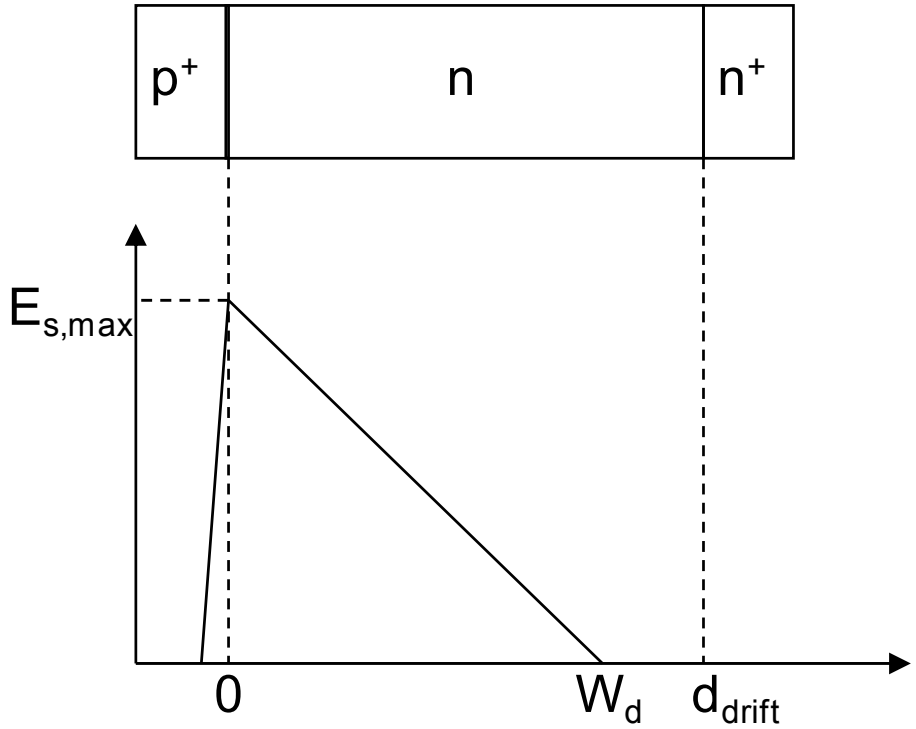


Fig. 1.5. The relationship between the electric field and distance in a drift layer with a one-sided abrupt p^+-n junction.

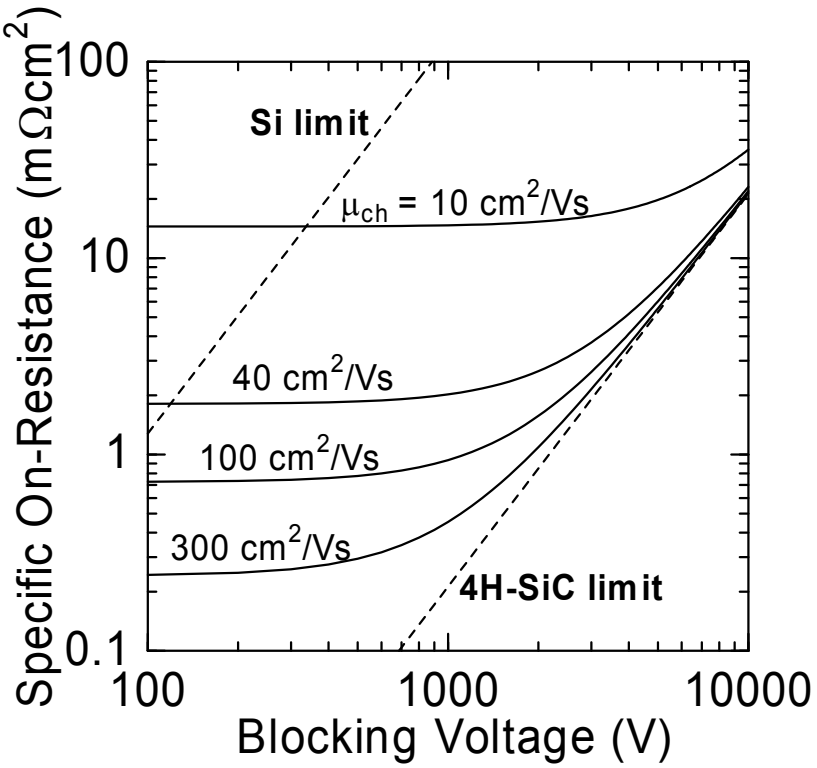


Fig. 1.6. Limit of specific on-resistance in Si and 4H-SiC power DMOSFETs as a function of blocking voltage and channel mobility, assuming that L = 1 μm, P = 15 μm, $\mathcal{E}_{ox}$ = 3 MV/cm.

1.3 SiC MOS structure

1.3.1 Oxidation of SiC

Significant challenges remain in commercializing the SiC MOS devices. Most of the difficult issues are associated with the high density of interface states exist at SiO_2/SiC interface. Despite many years of process development among research groups around the world on the SiC MOS devices, the interface state density (D_{it}) is extremely high, resulting in low inversion channel electron mobility.

SiC is the only wide-bandgap semiconductor that grows a thermal oxide (SiO_2). The dry oxidation of SiC is governed by the following reaction:

$$2SiC + 3O_2 \rightarrow 2SiO_2 + 2CO\,. \qquad (1.7)$$

The oxidation rate of Si-face 4H-SiC is about ten times slower than that of Si (001) but that of C-face 4H-SiC is only about five times slower [4, 5]. It is believed that the oxidation rate in the thick oxide regime is limited by the in-diffusion of oxidant or out-diffusion of CO [4, 5]. Recently, Hijikata *et al*. indicated that Si and C atoms are emitted from the interface during the oxidation, and the oxidation rate is limited by the accumulated Si and/or C atoms near the interface [6]. This complex oxidation process may be a cause of the high density of interface states at the SiO_2/SiC interface. The presence of excess carbon at the SiO_2/SiC interface is supposed to induce the interface traps at first. However, because of the complexity, there are many models and theories of the interface structures and origin of interface traps.

1.3.2 Nature of SiO_2/SiC interfaces

Charges at the interface and in the oxide

The charges at the interface and in the oxide affect the ideal MOS characteristics. Figure 1.7 illustrates the basic classifications of the charges at the interface and in the oxide [7]. There are mobile ionic charges (Q_m), fixed oxide charges (Q_f), oxide trapped charges (Q_{ot}), and interface trapped charges (Q_{it}).

The mobile ionic charges (Q_m) can move in the oxide depending on the gate bias and cause threshold voltage instability of MOSFETs. They are alkali ions, such as Na^+ and K^+, in the oxide introduced during processing. Their presence is minimized by controlling the cleanness of semiconductor surface before thermal oxidation. In addition, the Na^+ ions can be fixed by P treatment. Thus, the mobile ionic charges are not a big problem nowadays.

The fixed oxide charges (Q_f) are fixed and cannot be charged and discharged so that they do not depend on the position of the Fermi level. They are generally positive and depend on oxidation and annealing conditions. Cations due to excess Si are thought to be the origin of Q_f.

The oxide trapped charges (Q_{ot}) originate from the structural defects in the oxide. These defects are electrically neutral. However, they capture carriers and can be positively or negatively charged.

The interface trapped charges (Q_{it}) are charges nominally located at the SiO_2/SiC interface and exist within the bandgap of SiC due to the interruption of the periodic lattice structure at the interface. Depending on the gate bias, the interface states capture the electrons or holes and become negatively or positively charged. In the case of n-channel SiC MOSFETs, the channel electrons in the inversion layer are captured by the high density of interface states, decreasing the number of channel mobile electrons. The captured electrons act as negative charges at the interface and deteriorate channel mobility due to the Coulomb scattering. Interface state density (D_{it}) is defined as

$$D_{it} = \frac{1}{q}\frac{dQ_{it}}{dE} \tag{1.8}$$

where E is energy and the unit of D_{it} is in $cm^{-2}eV^{-1}$ [8]. The details of the interface states will be described later in this section.

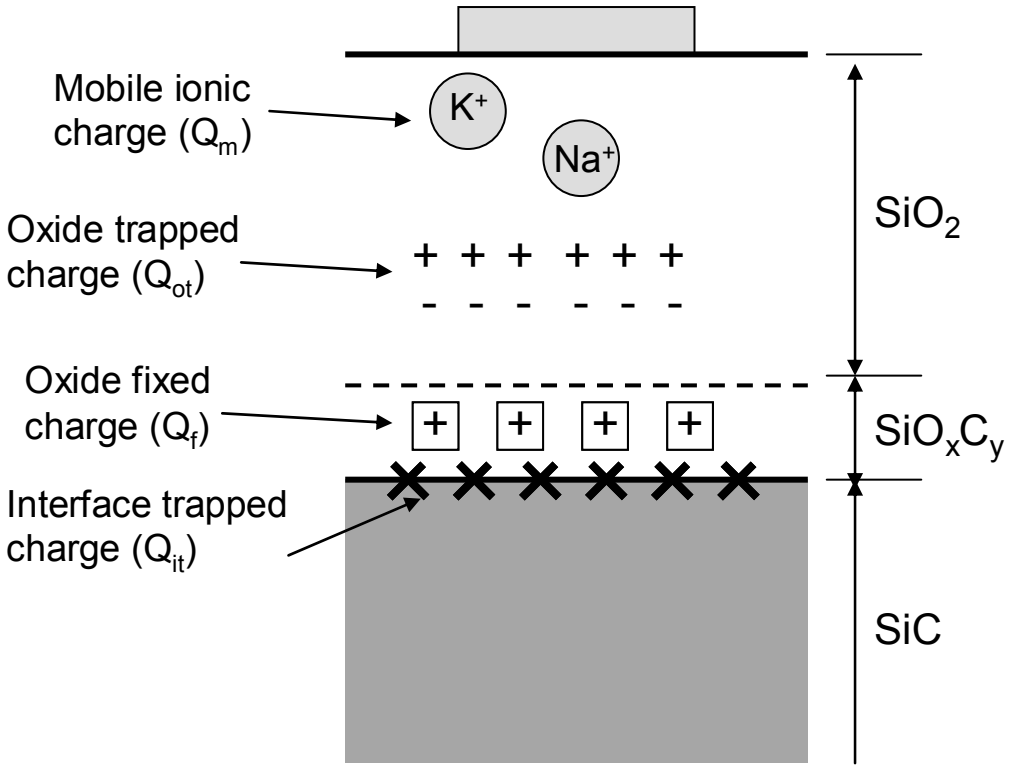


Fig. 1.7. The basic classifications of the charges at the interface and in the oxide [7].

Interface defects

The poor channel mobility of SiC MOSFETs is attributed to the high density of interface states located close to the conduction band edge (E_c) of SiC [9-13]. Whereas the D_{it} at the SiO_2/Si interface is nowadays less than 10^{10} $cm^{-2}eV^{-1}$, it reaches 10^{13} $cm^{-2}eV^{-1}$ or more at the SiO_2/4H-SiC interface [11]. Pensl *et al*. proposed that the high density of interface states is the combination of three individual defects: (i) Si and C dangling bonds, (ii) sp^2-bonded C clusters, and (iii) near-interface oxide defects [14].

Si and C dangling bonds

It is well known that Si dangling bonds called P_b centers are the main origin of interface states at the SiO_2/Si interface [15]. These defects can be easily passivated by annealing in H_2 at moderate temperatures [16]. Isoya *et al*. detected the presence of Si

dangling bonds at the SiO_2/SiC interface by electron spin resonance (ESR) [17]. However, in contrast with SiO_2/Si interfaces, annealing in H_2 up to 400 °C does not lead to any appreciable passivation of interface states [14, 18, 19], suggesting that the Si dangling bonds does not account for the majority of electrically active defect centers at the SiO_2/SiC interface. On the other hand, the H_2 annealing above 700 °C reduces the D_{it} [19]. Fukuda *et al*. considered the C dangling bond centers are passivated by H atoms [19]. Several years later, the C dangling bond (P_{bC}) centers were detected by some researchers [20, 21], and the successful passivation by H_2 at a low temperature was demonstrated [21, 22]. Wang *et al*. also reported that treatment using atomic H is effective for reducing the interface states due to C dangling bonds [23]. The C dangling bonds create interface states mainly in the lower part of the bandgap of SiC; however, their density is not high.

C clusters

Afanas'ev *et al*. suggested that the two types of carbons, the carbon originated from surface of the substrate prior to the oxidation [24] and the carbon generated at the interface during the oxidation [18], are detrimental to the SiO_2/SiC interface and oxide quality. He and his coworkers found that that the internal photoemission (IPE) signals of a-C:H and SiO_2/SiC are relatively similar, although the spectra are not identical [18, 25, 26]. Based on the experimental results of IPE, the C cluster model was proposed [18, 26]. In their model, the π orbital of sp^2-bonded C is considered to generate a distribution of defects with isolated carbon atoms deep in the gap and larger clusters closer to the band edge [18, 26]. The energy is determined by the number of six-fold rings in the cluster [18, 26]. This model was supported by atomic force microscopy (AFM)

experiments where nanometer-sized platelet-shaped inhomogeneities were assigned to C clusters [27]. However, the absolute identification of C clusters remains problematic because several subsequent studies have questioned the presence of such clusters. Pippel *et al*. reported that the C clusters and graphitic regions at or near the interface cannot be observed by the combination of high-resolution transmission electron microscopy (HRTEM) and electron energy-loss spectroscopy (EELS) [28]. Virojanadara *et al*. reported high-resolution photoelectron spectroscopy (PES) studies using surface-controlled samples [29-31]. They concluded that no carbon clusters or carbon containing by products could detect at the interface [29-31]. Zhu *et al*. also indicated no excess carbon greater than 1.8×10^{14} cm^{-2} at the interface by medium energy ion scattering (MEIS) measurements [32]. Of course, these reports can not rule out the occurrence of C clusters, but the model is questionable.

Near-interface oxide defects

By using photon-stimulated tunneling (PST), Afanas'ev *et al*. found that the presence of near-interface traps (NITs) located approximately 2.77 eV below the conduction band edge of SiO_2 [18, 33, 34]. The 2.77 eV deep traps have been observed in all the oxides both grown on Si and SiC [18, 33]. In addition, the same energy value is obtained for both 4H- and 6H-SiC/SiO_2 interfaces [18, 34]. Thus, the traps seem to be related to native oxide defects unintentionally incorporated into SiO_2 during the oxidation.

Schörner *et al*. suggested that the high density of acceptor-like interface states exists at the same energy position above the valence band edge of all polytypes of SiC (4H, 6H and 15R) as illustrated in Fig. 1.8 [35]. This acceptor-like interface states are

believed to be NITs [36]. The energy position of these acceptor-like states varies with respect to the conduction band edge of SiC because the different polytypes have different bandgap. The energy position of NITs locates in the bandgap near the conduction band edge of 4H-SiC and, thus, the interface properties of 4H-SiC MOS structures are the worse among the polytypes. The donor-like interface states occupy the remaining parts of the band gap [35, 36].

By thermal dielectric relaxation current (TDRC), Rudenko *et al*. also identified the presence of NITs with the activation energy of 110 meV which agrees with the energy position of NITs determined by Afanas'ev *et al*. [37]. They assumed that the NITs are intrinsic interfacial defects energetically located near the conduction band edge of 4H-SiC and spatially distributed from the interface into the oxycarbide transition region [37]. Knaup *et al*. considered both intrinsic and C-related defects in the oxide near the SiO_2/4H-SiC interface [38]. They identified that C_O=C_O dimmers are a possible origin of NITs on the basis of their energy level in the 4H-SiC bandgap [38]. However, the C_O=C_O dimmers cannot explains the results of PST by which the same energy position of NITs were detected both at SiO_2/Si and SiO_2/SiC interfaces [28, 33, 34].

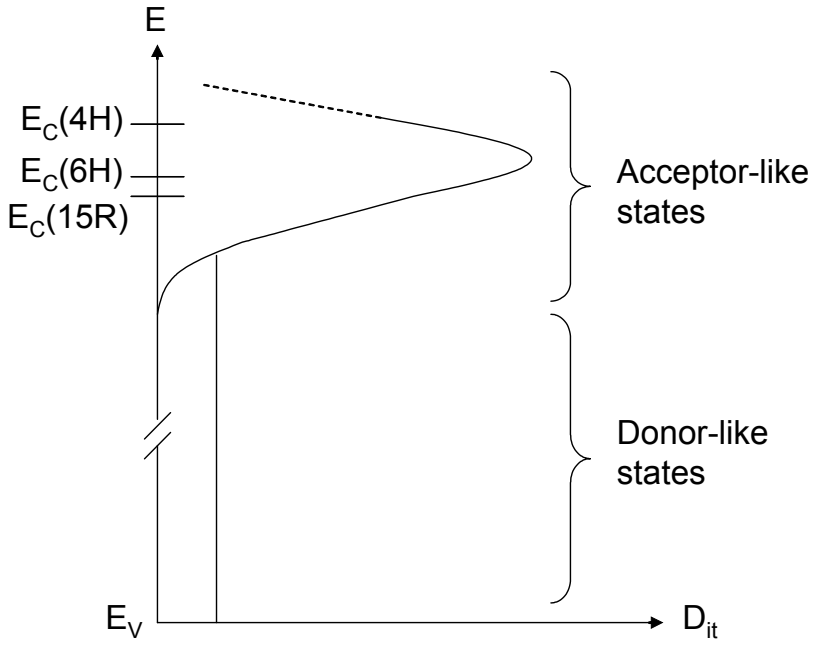


Fig. 1.8. Model for the distribution of interface states proposed by Schörner *et al*. [35].

1.3.3 Review of passivation techniques for interface states

In this section, passivation techniques for reducing the interface state density are reviewed. The features of each technique and reported values of channel mobility in 4H-SiC MOSFETs are summarized. Note that the channel mobility depends on the doping concentration of the substrate, and the reported values cannot be simply compared.

Dry and wet oxidation

The inversion channel mobility of Si-face 4H-SiC MOSFETs fabricated by standard dry and wet oxidation is far below the expected value from their bulk electron mobility. The typical values of channel mobility are 5–10 cm^2/Vs for 4H-SiC(0001) MOSFETs [9, 35, 39].

Lipkin *et al*. reported that wet reoxidation annealing (ROA) using pyrogenic steam at low temperatures around 900 °C reduces the density of deep interface states and effective fixed oxide charges [40]. Kosugi *et al*. showed that the suitable condition of wet ROA and achieved field-effect mobility as high as 47.6 cm^2/Vs on 4H-SiC MOSFETs when the water content of pyrogenic steam is 50% [41]. It is thought that the wet ROA reduces the amount of C atoms near the interface, reducing the density of deep interface states. However, the density of NITs is not affected by the ROA [28].

Hydrogen treatment

The effect of H_2 annealing have already been mentioned in Section 1.3.2. Whereas the H_2 annealing at 400 °C has almost no effect on the interface properties of Si-face SiO_2/4H-SiC interface, the H_2 annealing at high temperatures above 700 °C reduces D_{it} [14, 18, 19]. The D_{it} was reduced to as low as 2×10^{12} $cm^{-2}eV^{-1}$ at $E_c - E = 0.2$ eV and 1×10^{11} $cm^{-2}eV^{-1}$ at $E_c - E = 0.6$ eV by H_2 annealing above 800 °C [19], where $E_c - E$ is the energy between a trap level and the conduction band edge of 4H-SiC [19]. Thus the H_2 anneal seems to be effective for the relatively deep interface states in the energy range of 0.2–0.6 from E_c, rather than the shallow interface states near the E_c [19, 23]. The reduction in D_{it} is attributed to the passivation of C- dangling bonds [19, 22]. However, the improvement in channel mobility by H_2 annealing is small. For example, the field-effect mobility of 7.4 cm^2/Vs has been reported [10].

Nitridation

In 1997, Li *et al*. demonstrated that the D_{it} at a SiO_2/6H-SiC(0001) interface can be significantly reduced by NO annealing [42]. It was found that the NO annealing also

reduces the D_{it} at the SiO_2/4H-SiC(0001) interfaces [43-45]. In 2001, Chung *et al*. demonstrated that the field-effect mobility of Si-face 4H-SiC MOSFETs can be increased to 30–35 cm^2/Vs by NO annealing [46]. These pioneering works triggered a lot of interests in the field and, since then, the nitridation techniques have been intensively investigated.

The effect of nitridation depends on the density of N atoms incorporated at the interface [47]. By increasing the N density, the channel mobility can be improved up to about 50 cm^2/Vs [48, 49]. Das *et al*. reported that the field-effect mobility of 73 cm^2/Vs was obtained with a low-pressure chemical-vapor-deposited SiO_2 followed by a nitridation process when the N is highly incorporated at the interface [50]. The direct oxide growth or post-oxidation annealing in N_2O is also effective to improve the interface properties [51-54]. However, the N_2O treatment is not efficient as NO because N_2O decomposes into a small fragment of NO and a large percentage of N_2 and O_2 at a high temperature; such byproducts lead to competing reactions [51]. Another good method to incorporate N atoms into the interface is overoxidation of N-implanted substrates [55-59]. N atoms are introduced at the interface by ion implantation prior to the thermal oxidation. The D_{it} near E_c is strongly reduced by this technique [55-59]. Drawback of the N-implantation process is the increase of positive fixed charges. These charges increase with implantation dose, giving rise to an unwanted shift of the flatband and threshold voltages. However, Moscatelli *et al*. demonstrated the normally-off Si-face 4H-SiC MOSFETs with peak field-effect mobility of 22 cm^2/Vs at room temperature by optimizing the conditions of N implantation and wet oxidation [57]. In order to compensate the positive fixed charges, co-implantation of N and Al was proposed [58, 59]. Reshanov *et al*. fabricated normally-off Si-face 4H-SiC MOSFETs

with peak field-effect mobility of 31 cm^2/Vs by overoxidation of N/Al co-implanted substrates [59].

The mechanisms of the reduction in D_{it} by N atoms are controversial. Li *et al*. investigated the N1*s* core-level spectrum and obtained the peak close to the binding energy of stoichiometric Si_3N_4 [60]. They suggested that nitridation has two effects: (i) Si dangling bonds are passivated by creation of strong Si≡N bonds and (ii) carbon and other siliconoxycarbide compounds are removed from the interface [51, 60]. However, the reduced D_{it} cannot be explained by these postulates because the Si dangling bonds and residual C are not dominant components for the high D_{it}. McDonald *et al*. speculated that the incorporated N atoms reduce the stress between the SiO_2 and SiC because the mismatch between Si_3N_4 and SiC is smaller than that between SiO_2 and SiC [61]. Li *et al*. suggests the existence of C–N bonds in the oxide [60] but other authors did not detect the C–N bonds [31, 62]. Some authors considered that C clusters can be passivated by N atoms and the traps located upper part of the bandgap move to lower part of the bandgap [45, 63]. Afanas'ev *et al*. also suggested that the NO annealing reduces the π-bonded C based on the IPE results [64]. They suggested that the NO annealing reduces the residual C atoms near the interface by providing an extra pathway in the form of a compact CN molecule [64]. Again, the C cluster model is no longer reliable because of the previously mentioned reason. However, Afanas'ev *et al*. also revealed that slow interface traps, probably NITs, are effectively removed by NO annealing [64]. They stressed that the reduction in the slow interface states is much larger than the reduction in the fast interface states by one order of magnitude or more [64]. This fact is very important to understand the mechanism of nitridation and would be responsible for the reduced D_{it}.

There are a couple of studies of investigating nitrided interface using photoelectron spectroscopy. As mentioned before, Li *et al*. interpreted the peak close to the binding energy of Si_3N_4 as the presence of Si≡N bonds. However, the peak of Si_3N_4 is generally interpreted as three-fold coordinated N atoms (Si–N–Si bridges) [65]. Virojanadara *et al*. investigated the effect of NO exposures on the √3×√3 R30° reconstructed 4H-SiC(0001) surface using *in-situ* synchrotron PES [31]. They indicated that NO annealing forms a Si_3N_4 at the interface and a N–Si–O layer between the Si_3N_4 and SiO_2 layers [31].

There are a number of theoretical studies of N incorporation, but it seems to be difficult to predict a realistic interface. Wang *et al*. suggested the creation of a bonded Si–C–N–O interlayer [23]. Chatterjee *et al*. concluded that n-type doping of the SiC layer near the interface can lead to improved channel mobility and lower threshold voltage [62]. Umeda *et al*. reported that the C-dangling bond centers cannot be detected in NO-nitrided interface by electrically detected magnetic resonance (EDMR) [21]. They suggested that the improved channel mobility in NO-annealed MOSFETs can be attributed to the passivation of C dangling bonds by N atoms and the effect of N doping in the channel region [21].

The thermal nitridation processes, such as NO, N_2O, and NH_3 anneals, are suitable for fabricating practical devices because the reliability of the oxide is excellent [66, 67] as well as the high channel mobility.

Contaminated oxides

Gudjónsson *et al*. demonstrated that the channel mobility can be improved to about 150–170 cm^2/Vs by the thermal oxidation in the presence of metal impurities such as Na and K [68-70]. This process is called sodium-enhanced oxidation (SEO) because the

oxidation rate is much faster than standard dry oxidation [71]. Using thermal dielectric relaxation current (TDRC) method, it was found that the NITs are almost completely removed by the effect of both Na [71, 72] and K [73]. The Na^+ ions remove NITs more effectively than the K^+ ions [73]. The drawback of this process is the threshold voltage instability in MOSFETs due to the mobile Na^+ ions and can hardly be used in practice.

Deposited dielectrics

The deposited SiO_2 can decrease the number of residual C atoms near the interface; however, the increase in the channel mobility is marginal [74]. This may be attributed to the fact that the intrinsic SiO_2 defects (NITs) cannot be removed even in the deposited SiO_2 [28]. Also, the deposition of Si_3N_4 is not effective because thermal oxidation inevitably takes place during the deposition, leading to the formation of thermal SiO_2 at the interface and consequent creation of NITs [28].

In 2008, Hino *et al*. demonstrated that Al_2O_3/SiO_x/4H-SiC(0001) MOSFETs, which have an ultrathin thermally grown SiO_x layer between Al_2O_3 and 4H-SiC(0001), exhibited the peak field-effect mobility of 284 cm^2/Vs [75]. By optimizing the thickness of the ultrathin SiO_x, the peak field-effect mobility of 294 cm^2/Vs was obtained [76]. Lichtenwalner *et al*. fabricated 4H-SiC MOSFETs with the peak field-effect mobility of 106 cm^2/Vs by NO anneal to form a thin nitrided SiO_2 surface layer on SiC, and subsequent deposition of Al_2O_3 gate dielectric [77]. However, they reported the instability of threshold voltage [77], which might be a drawback of the deposited Al_2O_3 gate dielectric. The reliability of the Al_2O_3 formed on SiC has not reported at present.

Utilization of different crystal faces

Early studies of SiC MOS structures are on (0001) Si-face. However, the improvement in channel mobility had been hindered by the high density of interface states on the Si-face. In 1999, Yano *et al*. demonstrated that the low-field channel mobility of 4H-SiC MOSFETs on the $(11\bar{2}0)$ a-face can be 17 times higher than that on the (0001) Si-face [78]. Senzaki *et al*. reported the 4H-SiC MOSFETs on the $(11\bar{2}0)$ a-face with the peak field-effect mobility of 68.3 cm^2/Vs by pyrogenic reoxidation annealing [79]. After that, they improved the peak field-effect mobility to 110 and then 210 cm^2/Vs by wet oxidation followed by H_2 annealing [80, 81]. Endo *et al*. achieved the peak field-effect mobility of 244 cm^2/Vs on the $(11\bar{2}0)$ face by maintaining a wet atmosphere during the cooling-down period to 600 °C after wet oxidation [82]. Dhar *et al*. reported the field-effect mobility of 100 cm^2/Vs by the combination of nitrogen and hydrogen [83]. Thus, high channel mobility can be obtained on the $(11\bar{2}0)$ face. However, mass production of the a-face substrate is difficult and the cost is high. In addition, the breakdown voltage on the $(11\bar{2}0)$ face is much smaller than the theoretical value due to the crystal defects parallel to the $<11\bar{2}0>$ direction—probably basal plane dislocations (BPDs) [84]. Therefore, the $(11\bar{2}0)$ face is suitable for UMOS structures rather than DMOS structures. There is also a concern of oxide reliability because wet oxidation must be used to obtain the high channel mobility.

Fukuda *et al*. demonstrated a reduction in D_{it} by utilizing the wet oxides grown on $(000\bar{1})$ C-face [85] and a consequent increase in field-effect mobility as high as 127 cm^2/Vs [86, 87]. Nitridation is also effective for the C-face MOS interfaces [88-90]. However, the threshold voltage of 4H-SiC MOSFETs with a nitrided gate oxide on C-face is instable due to the occurrence of slow interface traps [89, 90]. The details are discussed in Chapter 6 of this thesis. Wet oxidation and H_2 annealing are effective for

C-face and a-face. This implies that the type of dominating defect for the C- and a-faces is different from that of Si-face; however, the mechanisms are not clear.

Yano *et al*. reported a low D_{it} value utilizing $(03\bar{3}8)$ face which is semi-equivalent to the (100) face of Si [91]. However, the $(03\bar{3}8)$ face is not commercially available.

Table 1.2 The peak values of channel mobility (μ_{ch}) reported to date for different processes and crystal faces. FE, EFF, and LF denote field-effect mobility, effective mobility, and low-field mobility, respectively.

	μ_{ch} (cm^2/Vs)	Process	Drawbacks	Ref.
(0001)	<10	Dry	-	
Si-face	47.6 (FE)	Dry +Wet ROA	Bad reliability	[41]
	20-50 (FE)	Dry + NO	-	[48]
	25 (EFF)	N_2O	-	[53]
	31 (FE)	N/Al impla.	Bad reliability	[59]
	~170 (FE)	SEO	V_T instability *etc*.	[69]
	294 (FE)	Dry + Al_2O_3	Bad high temp. immunity *etc*.	[76]
$(000\bar{1})$	<1	Dry	-	
C-face	65 (FE)	Dry + NO	V_T instability, μ_{ch} degradation	[90]
	118 (FE)	Wet	Large leakage current	[86]
	127 (FE)	Wet + H_2	Large leakage current	[87]
$(11\bar{2}0)$	96 (LF)	Wet	Low blocking voltage *etc*.	[78]
a-face	210 (FE)	Wet + H_2	Low blocking voltage *etc*.	[81]
	244 (FE)	Wet	Low blocking voltage *etc*.	[82]

Table 1.2 lists the peak values of channel mobility reported to date for different processes and crystal faces. Some processes yield very high channel mobility, but they also have drawbacks such as bad reliability, low blocking voltage, degradation of the device performance, bad immunity against high temperature process, and threshold voltage (V_T) instability. In particular, the problem of gate oxide formed on SiC is main

concern. The coming commercial devices will utilize nitrided SiO_2 formed on Si-face because reasonable channel mobility can be obtained and the reliability of the oxide is excellent [66, 67]. It is important not only to improve the channel mobility but also to maintain the reliability of the gate oxide. The problem of reliability is summarized in the next section.

1.3.4 Reliability of gate oxide on SiC

Another key issue for the success of SiC power MOS devices is the reliability of gate oxide formed on SiC. As for failure mechanisms of gate oxide, there are time-zero dielectric breakdown (TZDB) and time-dependent dielectric breakdown (TDDB). TZDB is immediate breakdown, which is caused by strong electric field (around 10 MV/cm). TDDB is a failure mechanism in MOSFETs, when the gate oxide breaks down as a result of long-time application of relatively low electric field. The breakdown is caused by formation of a conducting path through the gate oxide to substrate mainly due to electron tunneling current.

It is well known that the reliability of gate oxide depends on the crystal face and oxidation process. Fujihira *et al*. indicated that the nitridation of the gate oxide improves not only the channel mobility but also TDDB characteristics [67]. Senzaki *et al*. showed that the hydrogen POA improves the reliability but wet ROA degrades the reliability, especially when the water vapor content is high [92]. There is a concern in the reliability of gate oxides formed on C-face, although the reported charge to breakdown value is relatively high [93]. The problem is the band offset between the conduction band edges of SiC and SiO_2 is small, arising large leakage current [93].

In addition, the reliability is strongly affected by the wafer quality. Senzeki *et al*. showed that the reliability of thermal oxides degrades with the increase in the number of dislocations in the substrates [94]. In general, the dislocations in the SiC epitaxial layer are classified into three types of dislocations: basal plane dislocation (BPD), threading edge dislocation (TED), and threading screw dislocation (TSD). Most of the thermal oxides broke down at the BPDs and TSDs [94, 95]. The dislocation density is decreasing year by year and the density of less than 100 cm^{-2} has been achieved [96].

1.4 Objectives and outline of this thesis

The improvement in the channel mobility of SiC MOSFETs is the key issue for the realization of competitive power SiC devices. As mentioned above, many techniques have been proposed to improve the interface properties, but most of them accompanies with drawbacks such as bad reliability, low blocking voltage, and threshold voltage instability. Therefore, the most standard technique to improve the characteristics has been nitridation of the interface on Si-face of 4H-SiC. The Si-face is the most basic crystal face and has advantages such as good reliability and large band offset of conduction band between SiO_2 and 4H-SiC. However, it seems to be difficult to further improve the channel mobility on Si-face, and the SiC community has been waiting for a new efficient process to improve the channel mobility of Si-face 4H-SiC MOSFETs.

The fact that the channel mobility can be improved by Na means D_{it} can be reduced by other elements than N. Therefore, the author decided to try to incorporate other elements into the gate oxide, aiming to improve the interface properties. This thesis mainly focuses on the development of a new efficient process to improve the SiO_2/SiC interface properties on Si-face (Chapter 6 briefly describes about C-face). An original

technique that uses P atoms to improve the interface properties is proposed for the first time. In addition, mechanisms behind the improved characteristics are discussed based on electrical and physical analysis. The reliability of the oxide produced in the new technique is also shown and discussed.

In Chapter 2, overoxidation of ion-implanted substrates is employed to search for the effective element to reduce D_{it}. B, N, F, Al, P, and Cl were chosen and incorporated into the interface by the overoxidation technique. From electrical measurements, it was found for the first time that the interface state density can be reduced by P as well as N.

In Chapter 3, a thermal annealing technique to improve the channel mobility of 4H-SiC MOSFETs is proposed. This technique uses $POCl_3$ as a source of P. The excellent characteristics of MOS capacitors and MOSFETs fabricated by the $POCl_3$ annealing are presented.

In Chapter 4, low-temperature capacitance–voltage (*C–V*) and thermal dielectric relaxation current (TDRC) measurements were employed to investigate near-interface traps (NITs). In addition, structure of interface is investigated by photoelectron spectroscopy. Based on the obtained results, mechanisms responsible for the improved properties are discussed.

In Chapter 5, charge-pumping measurements were investigated as a new characterization method for 4H-SiC MOSFETs. Some problems were found for interface state characterization of SiC MOSFETs using charge-pumping measurement due to an unwanted current component. In order to avoid the unwanted component, criteria for the accurate charge-pumping measurement were established. The $POCl_3$-annealed MOSFETs were also characterized by the established charge-pumping measurements.

In Chapter 6, the effect of two different oxidation techniques, NO direct oxidation and $POCl_3$ post oxidation annealing, on C-face MOS interface was investigated. Interface state density was reduced and channel mobility was improved by both NO and $POCl_3$ processes. On the other hand, it was found that extreamly slow interface traps are generated by both NO and $POCl_3$ processes. The mechanisms are discussed based on the results of electrical measurements.

In Chapter 7, the conclusions and outlook of this study are summarized. In addition, problems of the proposed method are summarized, and suggestions for future work to solve the problems are provided.

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Chapter 2
Investigation of Interface Properties in 4H-SiC MOS Structures Prepared by Overoxidation of Ion-Implanted Substrates

2.1 Introduction

It is well known that interface state density (D_{it}), channel mobility, and reliability of 4H-SiC MOS devices strongly depend on the crystal face and oxidation process. N incorporation into the SiO_2/SiC interface by annealing in NO or N_2O ambient has been accepted as a good method to improve both the reliability and channel mobility of 4H-SiC MOSFETs [1-4]. Besides N, it has been reported that incorporation of H [5, 6] and Na [7] can also modify the interface properties. Thus, there is a possibility that other elements can reduce D_{it}. One good method to incorporate various elements into the SiO_2/SiC interface is overoxidation of ion-implanted substrates [8-12]. Overoxidation of N-implanted 4H-SiC substrates significantly reduces D_{it} near the conduction band edge [8-12]. It has been reported that both flatband voltage and D_{it} can be modified by the N/Al co-implantation technique [11, 12]. Therefore, this technique can be useful to search for the proper elements to reduce D_{it}.

There are many candidate elements to incorporate into SiO_2/SiC interface. For the SiO_2/Si interface, it is known that the fluorine (F) and chlorine (Cl) atoms can effectively improve the hot electron immunity and reduce the D_{it} by forming Si–F and Si–Cl bonds [13-19]. The D_{it} could be reduced by F or Cl if the origin of the interface

states was dangling bonds. In addition, B_2O_3, Al_2O_3, P_2O_5 are known as glass formers that modify the network structure of SiO_2. Thus, there is a possibility that the D_{it} can be reduced by the structural change of oxide network by incorporation of B, Al, and P atoms.

In this chapter, the change in interface properties by incorporation of various elements into the SiO_2/4H-SiC interface is described. B, N, F, Al, P, and Cl atoms were introduced by overoxidation of ion-implanted substrates and the change in the interface state density and the flatband voltage in MOS capacitors were investigated.

2.2 Fabrication of MOS capacitors

4°-off, Si-face, n-type 4H-SiC epitaxial wafers were employed in this study. B, N, F, Al, P, and Cl ions were implanted at room temperature with different doses of 1.0×10^{12}, 5.0×10^{12}, and 1.0×10^{13} cm^{-2}. Figure 2.1 shows as-implanted concentration profiles for each sample calculated with a SRIM code, where the ordinate can be converted into a density distribution (atoms/cm^3) by multiplying the ion dose (atoms/cm^2). The implantation energy was varied depending on the elements so that peaks of the as-implanted profile (R_p) are located around 30 nm as shown in Fig. 2.1. The as-implanted atomic density at R_p is in the order of 10^{17}–10^{18} cm^{-3}. The implantation conditions are listed in Table 2.1. The gate oxide was formed by dry oxidation at 1100 °C for 18.5 h. After the oxidation, all the samples were cooled in N_2 with a ramping rate of −5 °C/min and unloaded at room temperature in order to avoid any unwanted change in electrical properties by quenching. The oxide thickness (t_{ox}) estimated from the accumulation capacitance of high-frequency capacitance–voltage (C–V) curves was ~60 nm. The thickness of the consumed SiC layers (t_{con}) during oxidation is caluculated as

the ratio of (mole number of SiO_2 per unit volume)/(mole number of SiC per unit volume). Taking into account the density of 2.2 and 3.2 g/cm^3 and weights per mole of 60.1 and 40.1 g/mol for SiO_2 and SiC, respectively, the ratio of t_{ox}/t_{con} is 0.47. Therefore, the SiO_2/SiC interface and R_p are at almost the same position. Al was evaporated to form the gate and backside electrodes. Post-metallization annealing was performed in N_2 at 400 °C for 30 min.

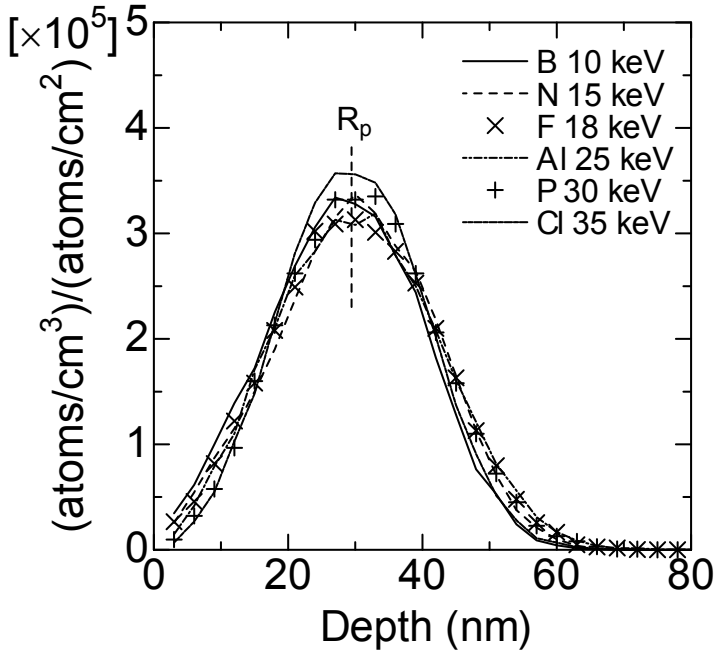


Fig. 2.1. Implantation profile for each element calculated with a SRIM code.

Table 2.1. Implantation energy (E_{impla}) and implantation dose (N_{impla}) for each element.

Species	E_{impla} (keV)	N_{impla} (cm^{-2})
B	10	1.0×10^{12}, 5.0×10^{12}, 1.0×10^{13}
N	15	1.0×10^{12}, 5.0×10^{12}, 1.0×10^{13}
F	18	1.0×10^{12}, 5.0×10^{12}, 1.0×10^{13}
Al	25	1.0×10^{12}, 5.0×10^{12}, 1.0×10^{13}
P	30	1.0×10^{12}, 5.0×10^{12}, 1.0×10^{13}
Cl	35	1.0×10^{12}, 5.0×10^{12}, 1.0×10^{13}

2.3 Characterization of interface properties

The analysis of MOS capacitors can yield considerable information regarding the properties of the oxide, the underlying semiconductor substrate, and the oxide/semiconductor interface. In order to extract these properties, several capacitance-voltage (*C–V*) measurement techniques have been developed. The hi-lo *C–V* method [20], which combines high-frequency and low-frequency *C–V* measurements, is widely used to characterize SiC MOS capacitors.

Extraction of interface state density

To understand the characterization method, it is important to consider the capture and emission process of electrons. Figure 2.2 illustrates the capture and emission process of an electron between the conduction band and a trap state. Similar mechanism can be considered for the capture and emission process of holes, but the process for electrons is considered here because only the measurements of electron traps have been performed in this study. An electron in the conduction band is captured by a trap state in very short time depending on the electron capture cross section (σ_n) of the trap state.

The capture time constant (τ_c) is given by

$$\tau_c = \frac{1}{\sigma_n v_{th} n} \tag{2.1}$$

where v_{th} is the thermal velocity of electrons, and n is the electron concentration. It should be noted that the capture process is independent of the trap energy. The process of electron emission from a trap state to the conduction band is described as

$$\tau_e = \frac{1}{v_{th}\sigma_n N_C}\exp\left(\frac{E_c - E}{kT}\right) \tag{2.2}$$

where τ_e is the emission time constant, N_C is effective density of states in the conduction band, E_c is the energy of the conduction band edge, E is the energy of a trap, k is the Boltzmann constant, and T is absolute temperature. The response time of interface states increases exponentially with energy from the conduction band edge.

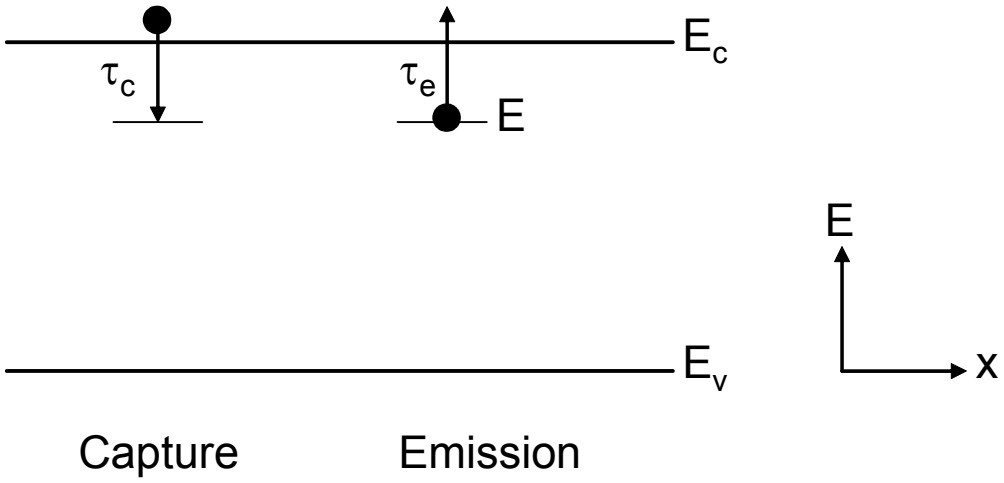


Fig. 2.2. Schematic illustration of the capture and emission process of an electron.

The most common method for characterizing interface properties of MOS capacitors is *C*–*V* measurements. There are (i) small signal and (ii) quasistatic *C*–*V* measurements. In the small signal *C*–*V* measurement, dc voltage is applied to the gate which brings the device from accumulation to depletion and vice versa, while a small ac signal (typically, ~20 mV) is superimposed onto the dc bias. The real and imaginary parts of the impedance are calculated from the amplitude and phase difference of the measured current. The quasistatic *C*–*V* measurement is substantially a current–voltage measurement. The capacitance is extracted by setting the ramp rate of gate voltage and measuring the gate current which is the time derivative of the gate voltage. This method is effective for low frequency *C*–*V* measurements because the small signal measurements usually cause large noise at low frequency below 100 Hz.

Figure 2.3 illustrates the equivalent circuit of a MOS capacitor measured at (a) low frequency and (b) high frequency. The capacitance at low frequency is given by

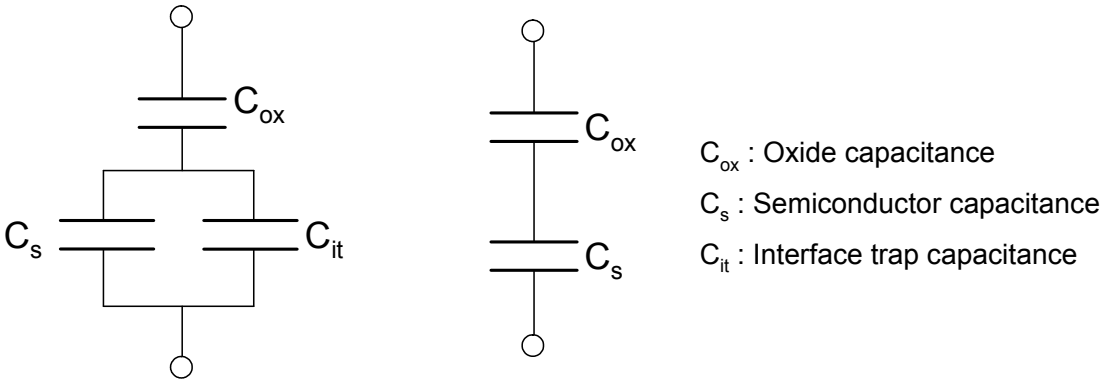
$$C_{\mathrm{LF}} = \left(C_{\mathrm{s}} + C_{\mathrm{it}}\right)\frac{C_{\mathrm{ox}}}{C_{\mathrm{ox}} + C_{\mathrm{s}} + C_{\mathrm{it}}}. \tag{2.3}$$

The part of interface traps responds to the slow ramp rate of gate bias for the low-frequency *C*–*V* measurements. However, the interface traps do not fully respond to the small signal ac variation in the high-frequency *C*–*V* measurements. The capacitance at high frequency (C_{HF}) is given by

$$C_{\mathrm{HF}} = \frac{C_{\mathrm{s}}C_{\mathrm{ox}}}{C_{\mathrm{s}} + C_{\mathrm{ox}}}. \tag{2.4}$$

Interface state capacitance (C_{it}) can be calculated from the difference between C_{HF} and C_{LF}. Therefore, D_{it} is given by

$$D_{\mathrm{it}} = \frac{1}{q}\left(\frac{C_{\mathrm{ox}}C_{\mathrm{LF}}}{C_{\mathrm{ox}} - C_{\mathrm{LF}}} - \frac{C_{\mathrm{ox}}C_{\mathrm{HF}}}{C_{\mathrm{ox}} - C_{\mathrm{HF}}}\right). \tag{2.5}$$



(a) Low frequency (b) High frequency

Fig. 2.3. (a) Low-frequency and (b) high-frequency equivalent circuits of the MOS capacitor.

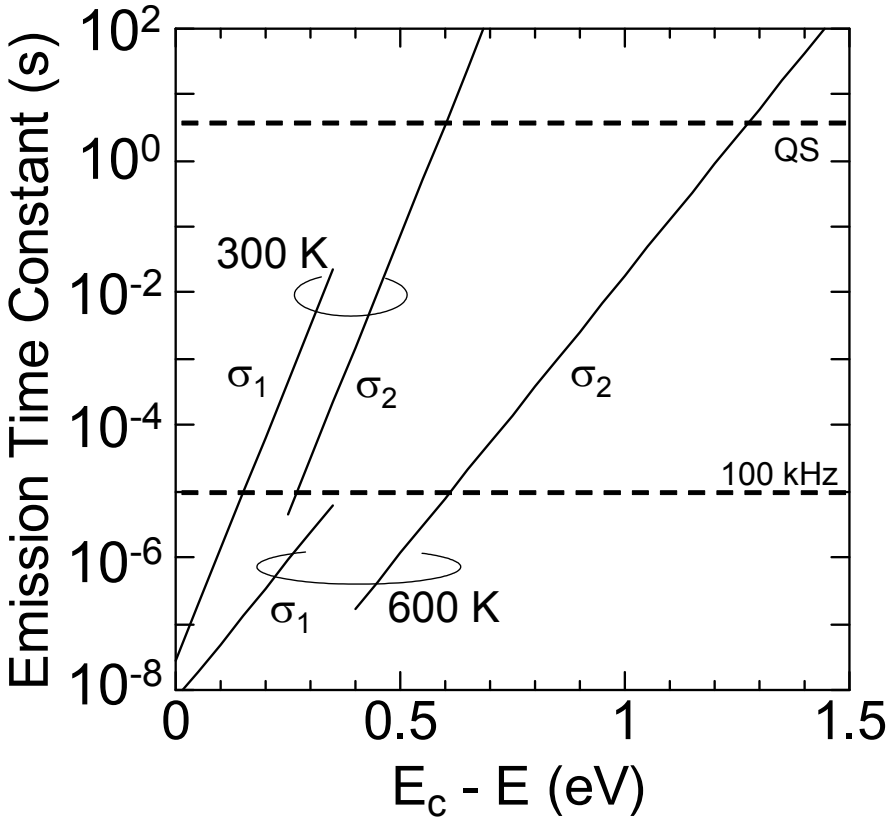


Fig. 2.4. Emission time constant as a function of trap energy level (E) from the conduction band edge (E_c). The capture cross section was assumed to be independent of temperature and 1×10^{-19} cm^2 for shallower states (σ_1) and 1×10^{-17} cm^2 for deeper states (σ_2) [22].

It should be noted that there is an energy window in which the extracted D_{it} is valid [21]. The hi-lo method is valid only over that portion of the bandgap for which interface states do not follow high-frequency measurement signal but follow the dc bias sweep [21]. Figure 2.4 shows the emission time calculated using Eq. (2.2) as a function of trap energy level (E) from the conduction band edge (E_c). The capture cross section was assumed to be independent of temperature and 1×10^{-19} cm^2 for shallower traps (σ_1) and 1×10^{-17} cm^2 for deeper traps (σ_2) [22]. The assumed valid range is between 0.2 and 0.6 eV from the E_c for a frequency of 100 kHz and a ramp rate of 0.01 V/s. This energy range moves to deeper energy range at higher temperatures.

Charges in the oxide or at the interface can be analyzed by examining the shift in the C–V curves. The flatband voltage is given by

$$V_{FB} = \phi_{ms} - \frac{Q_f + Q_{it} + \gamma Q_m}{C_{ox}} \tag{2.6}$$

where $q\phi_{ms}$ is the work function difference between the metal and the semiconductor, Q_f is the fixed oxide charge, Q_{it} is the interface trapped charge at the flatband conditions, and γQ_m is the mobile charge. The flatband voltage deviates from the ideal value if the unwanted charges exist in the oxide or at the interface. Distinguishing Q_f and Q_{it} is not always easy. Thus, effective fixed charge ($Q_{eff} = Q_f + Q_{it} + \gamma Q_m$) is usually used.

In this study, high-frequency C–V curves were measured using an Agilent 4284A LCR meter with a bias sweep rate of 0.1 V/s and a frequency of 100 kHz. Quasistatic C–V measurements were implemented using a Keithley model 595 quasistatic C–V meter with a bias sweep rate of 0.01 V/s. The measurements were conducted under dark conditions.

2.4 Interface properties of MOS capacitors

Figure 2.5 shows High-frequency and quasistatic *C–V* curves for (a) B-, (b) N-, (c) F-, (d) Al-, (e) P-, and (f) Cl-implanted samples. The implantation dose is 1.0×10^{13} cm^{-2}. The difference between high- and low-frequency curves reflects the density of interface states. The difference is relatively small for the N- and P-implanted samples. For the B-, F-, Al- and Cl-implanted samples, the difference is large, depending on the implanted elements. Among these elements, the larger implantation dose results in the larger difference in the high and low *C–V* curves.

Figure 2.6 shows the dependence of high-frequency and quasistatic *C–V* curves of P-implanted samples on implantation dose measured at room temperature. Although the slope of the *C–V* curve for high implantation dose seems to be stretched out, this is the result of the graded P profile in the SiC side where P atoms work as a donor. Similar curves can be found in N-implanted curves as in Fig. 2.7, in agreement with other reports [8, 11]. With increasing P dose, the *C–V* curves shift toward negative voltage. The flatband voltage shift (ΔV_{FB}) for all samples is summarized in Table 2.2. A similar negative shift of V_{FB} can be observed in N-implanted samples, in agreement with the previous reports [8, 11]. On the other hand, V_{FB} shifts in the positive direction for Al-, B-, F-, and Cl-implanted samples (Table 2.2). The positive increase in V_{FB} implies an increase in negative charges at the interface.

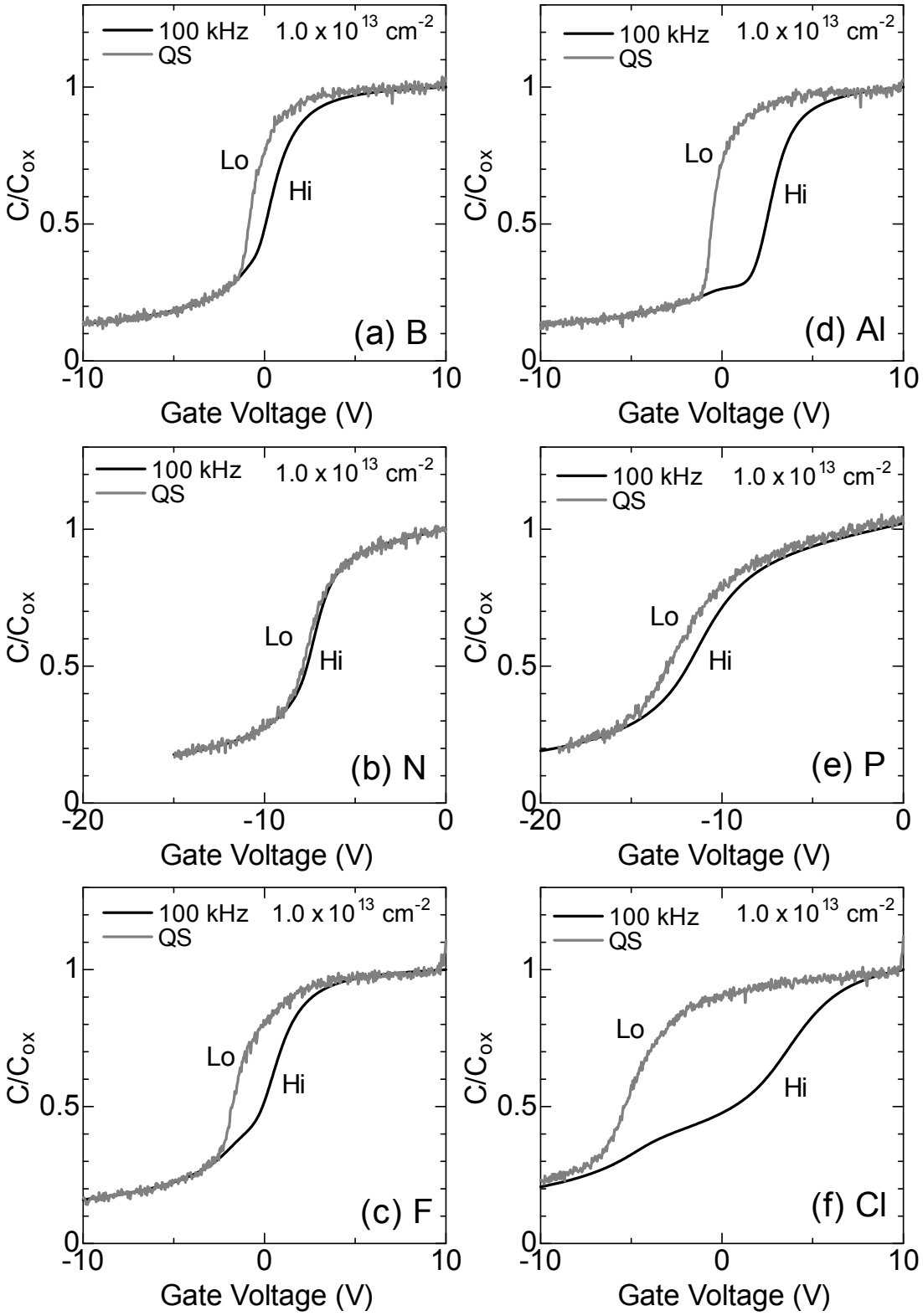


Fig. 2.5. High-frequency and quasistatic *C–V* curves for (a) B-, (b) N-, (c) F-, (d) Al-, (e) P-, and (f) Cl-implanted samples. The implantation dose is 1.0×10^{13} cm^{-2}.

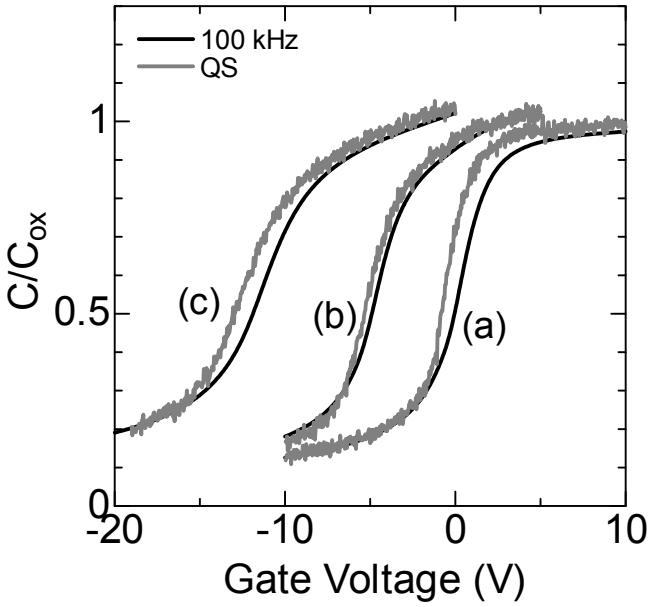


Fig. 2.6. High-frequency and quasistatic *C*–*V* curves of P-implanted MOS capacitors with implantation dose of (a) 1.0×10^{12}, (b) 5.0×10^{12}, and (c) 1.0×10^{13} cm^{-2}.

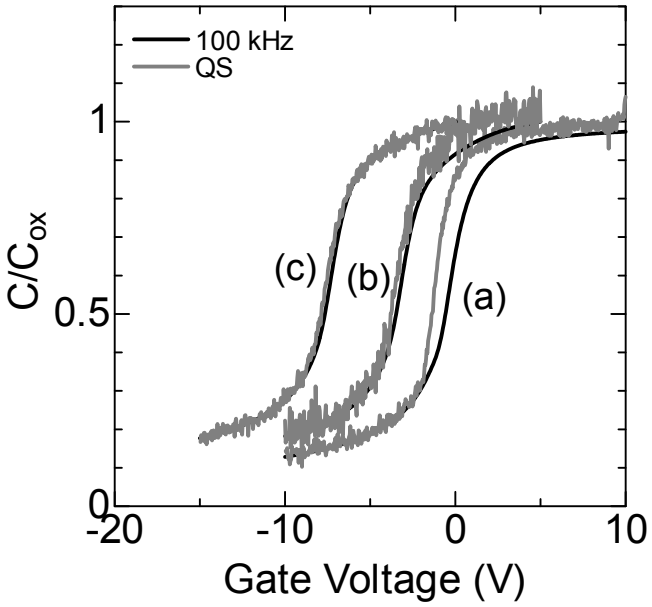


Fig. 2.7. High-frequency and quasistatic *C*–*V* curves of N-implanted MOS capacitors with implantation dose of (a) 1.0×10^{12}, (b) 5.0×10^{12}, and (c) 1.0×10^{13} cm^{-2}.

Table 2.2. Implantation energy (E_{impla}), implantation dose (N_{impla}), flatband voltage shift (ΔV_{FB}), effective fixed charge (Q_{eff}/q) and interface state density (D_{it}) at 0.2 and 0.6 eV from the conduction band edge.

Species	E_{impla} (keV)	N_{impla} (cm^{-2})	ΔV_{FB} (V)	Q_{eff}/q ($\times 10^{11}$ cm^{-2})	D_{it} at 0.2/0.6 eV ($cm^{-2}eV^{-1}$)
w/o	-	-	0.1	−0.2	2×10^{12} / 2×10^{11}
B	10	1.0×10^{12}	−0.3	0.9	2×10^{12} / 2×10^{11}
		5.0×10^{12}	0.5	−2.0	2×10^{12} / 2×10^{11}
		1.0×10^{13}	0.5	−2.1	2×10^{12} / 3×10^{11}
N	15	1.0×10^{12}	−0.2	0.6	2×10^{12} / 2×10^{11}
		5.0×10^{12}	−2.7	8.4	5×10^{11} / 9×10^{10}
		1.0×10^{13}	−6.6	23.5	7×10^{10} / 1×10^{11}
F	18	1.0×10^{12}	0.1	−0.4	2×10^{12} / 3×10^{11}
		5.0×10^{12}	0.7	−2.3	2×10^{12} / 3×10^{11}
		1.0×10^{13}	0.8	−3.2	2×10^{12} / 7×10^{11}
Al	25	1.0×10^{12}	0.6	−2.1	2×10^{12} / 5×10^{11}
		5.0×10^{12}	0.8	−3.3	4×10^{12} / 5×10^{11}
		1.0×10^{13}	2.8	−10.2	1×10^{13} / 7×10^{11}
P	30	1.0×10^{12}	0.6	−2.1	2×10^{12} / 3×10^{11}
		5.0×10^{12}	−2.9	10.7	3×10^{11} / 2×10^{11}
		1.0×10^{13}	−5.6	21.9	2×10^{11} / 2×10^{11}
Cl	35	1.0×10^{12}	0.3	−1.2	3×10^{12} / 6×10^{11}
		5.0×10^{12}	2.5	−8.5	7×10^{12} / 1×10^{12}
		1.0×10^{13}	3.9	−15.2	2×10^{13} / 2×10^{12}

Figure 2.8 shows the distribution of D_{it} near the conduction band edge estimated by the hi-lo *C*–*V* technique for (a) B-, (b) N-, (c) F-, (d) Al-, (e) P-, and (f) Cl-implanted samples for different implantation doses. D_{it} near the conduction band edge for Al-, B-, F-, and Cl-implanted samples increases with increasing implantation dose. On the other hand, strong reduction of D_{it} is observed for N- and P-implanted samples when the implantation dose is larger than 5.0×10^{12} cm^{-2}. The values of D_{it} at 0.2 and 0.6 eV from the conduction band edge are listed in Table 2.2. D_{it} of around 2×10^{11} $cm^{-2}eV^{-1}$ near the conduction band edge for the P-implanted sample is slightly higher than that of N-implanted samples. It can be observed that the increase in D_{it} correlates with the increase in implantation energy and dose for B-, F-, Al-, and Cl-implanted samples, *i.e.*, a MOS capacitor fabricated by higher implantation energy and dose exhibits higher D_{it} and ΔV_{FB}. The passivation effect of N and P is considered to exceed the effect of implantation damage, whereas it is very small or little for Al, B, F, and Cl. The slightly higher D_{it} for the P-implanted sample compared to the N-implanted one might be due to larger implantation damage because the implantation energy of P is higher than that of N due to the heavier ion.

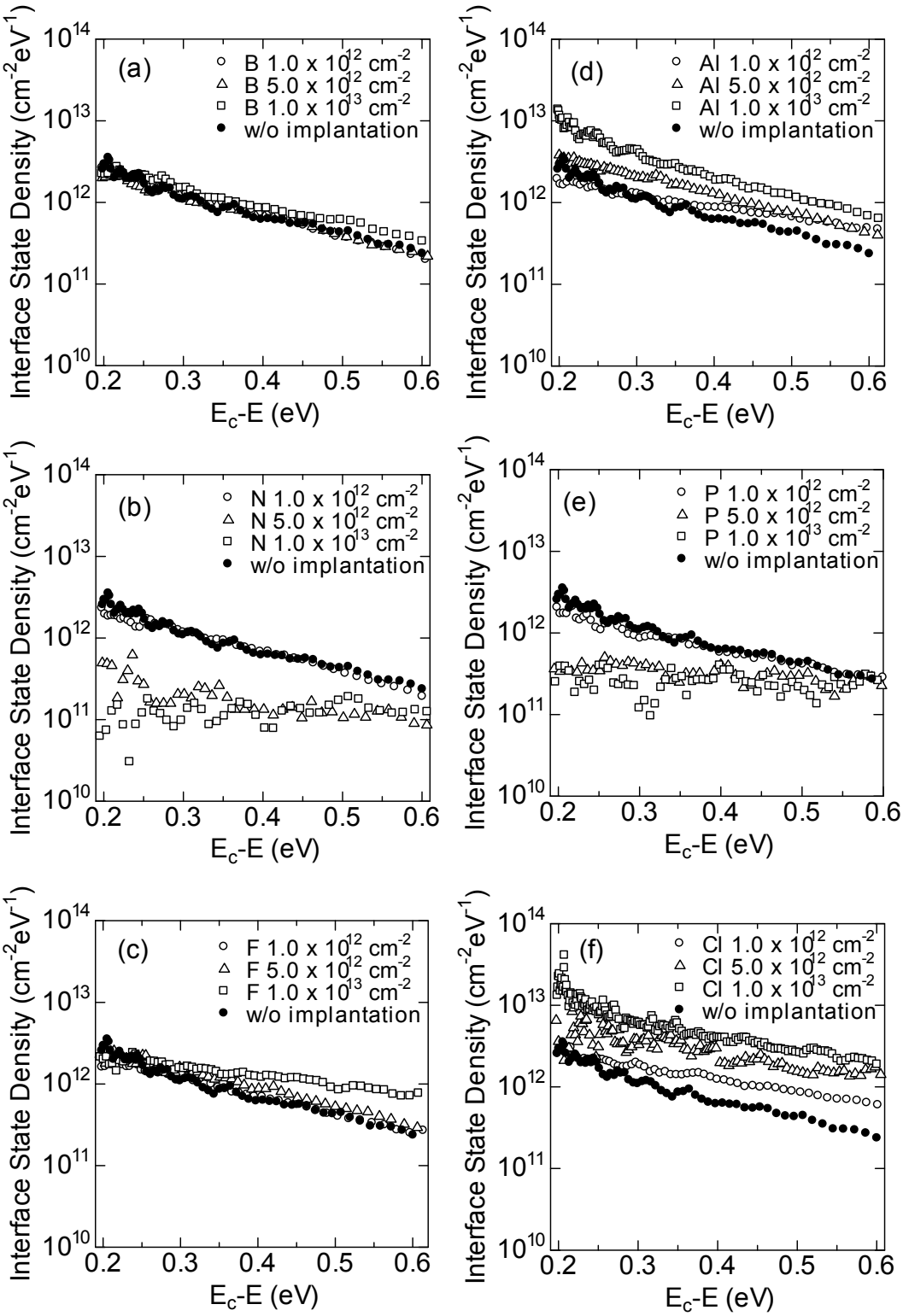


Fig. 2.8. Interface state density near the conduction band edge for (a) B-, (b) N-, (c) F-, (d) Al-, (e) P-, and (f) Cl-implanted samples.

2.5 Discussion

This is the first repot that the D_{it} can be reduced by P atoms. However, the large implantation damage due to heavy P ions is not negligible. Therefore, the development of new technique to incorporate P atoms into the interface without implantation damage is required. Even though D_{it} for the P-implanted sample is slightly inferior to the N-implanted one, the result described here is very important to understand the passivation mechanism of 4H-SiC MOS interface. F and Cl did not reduce the D_{it}. This implies that the dangling bond centers are not main origin of D_{it} at SiO_2/SiC interface. The major cause of high-density interface states near the conduction band edge is usually assumed to be near-interface traps (NITs) [3, 6, 23] that is related to the structural defects in SiO_2 near the interface [23]. P atoms may be incorporated into the interlayer and reduce the strain, leading to the low D_{it} value. The details will be discussed in Chapter 4.

2.6 Summary

A change in the D_{it} in 4H-SiC MOS structures by incorporation of various elements was systematically investigated. B, N, F, Al, P, and Cl ions were implanted prior to the oxidation and introduced at the SiO_2/SiC interface by subsequent thermal oxidation. D_{it} near the conduction band edge for Al-, B-, F-, and Cl-implanted MOS capacitors increased with implantation dose. On the other hand, a strong reduction in D_{it} was observed for N- and P-implanted samples when the implantation dose was larger than 5.0×10^{12} cm^{-2}. It was found that the interface state density can be reduced by P as well as N.

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Chapter 3
Improved Inversion Channel Mobility in 4H-SiC MOSFETs on Si-Face Utilizing Phosphorus-Doped Gate Oxide

3.1 Introduction

As described in Chapter 1, the inversion channel mobility of 4H-SiC MOSFETs is deteriorated by a high density of interface states at SiO_2/4H-SiC [1]. It is well known that the performance of 4H-SiC MOSFETs strongly depends on the crystal face and oxidation process. One of the standard methods for improving MOS interface properties on 4H-SiC (0001) has been nitridation of the gate oxide using NO or N_2O [2-4]. Relatively high values of channel mobility, up to about 50 cm^2/Vs, can be obtained via nitridation [3, 4]. However, it seems to be difficult to further improve the channel mobility by nitridation, even after optimizing the nitridation conditions.

In addition to N atoms, the incorporation of Na atoms into the SiO_2/4H-SiC (0001) interface improves the peak channel mobility to above 150 cm^2/Vs [5]. However, this method is not suitable for practical use because Na atoms act as mobile ions in the SiO_2 layer. Some groups have claimed extremely high channel mobility by utilizing deposited Al_2O_3 gate dielectrics [6, 7]. However, studies on improving the quality of thermal oxides are still important. As described in Chapter 2, it was found that the interface state density can be decreased by overoxidation of P-implanted 4H-SiC (0001) substrates. However, this method has drawbacks, such as large implantation damage due

to heavy P ions and a negative flatband voltage due to the implanted P donors beneath the gate oxide.

In this chapter, a simple technique to improve the channel mobility of 4H-SiC MOSFETs is proposed. P atoms are incorporated in the SiO_2 side of the interface (not the 4H-SiC side) by thermal annealing using phosphoryl chloride ($POCl_3$). The interface properties of MOS capacitors and the inversion channel mobility of MOSFETs on the (0001) Si face were drastically improved by postoxidation annealing with $POCl_3$.

3.2 $POCl_3$ annealing

Figure 3.1 illustrates the $POCl_3$ annealing system used in this study. It consists of high-purity O_2 and N_2 gases, a babbler of $POCl_3$, and a quartz tube furnace. A bubbler containing $POCl_3$ was maintained at a certain temperature. $POCl_3$ is introduced from the bubbler into the tube by N_2. In addition, pure O_2 and N_2 are directly introduced to the tube. The annealing is conducted at a high temperature such as 1000 °C. In most cases, the $POCl_3$ annealing is followed by N_2 annealing at the same temperature. When these gases are introduced to the furnace tube, P-doped SiO_2 (SiO_2-P_2O_5) is formed by the chemical reaction of $POCl_3$, O_2, SiO_2 and SiC. Both SiO_2 and P_2O_5 can be network formers that can form glasses by themselves. P_2O_5 is made of phosphorus tetrahedra with four P-O bonds, among which one is double bonded, so that it is not connected to the rest of the network.

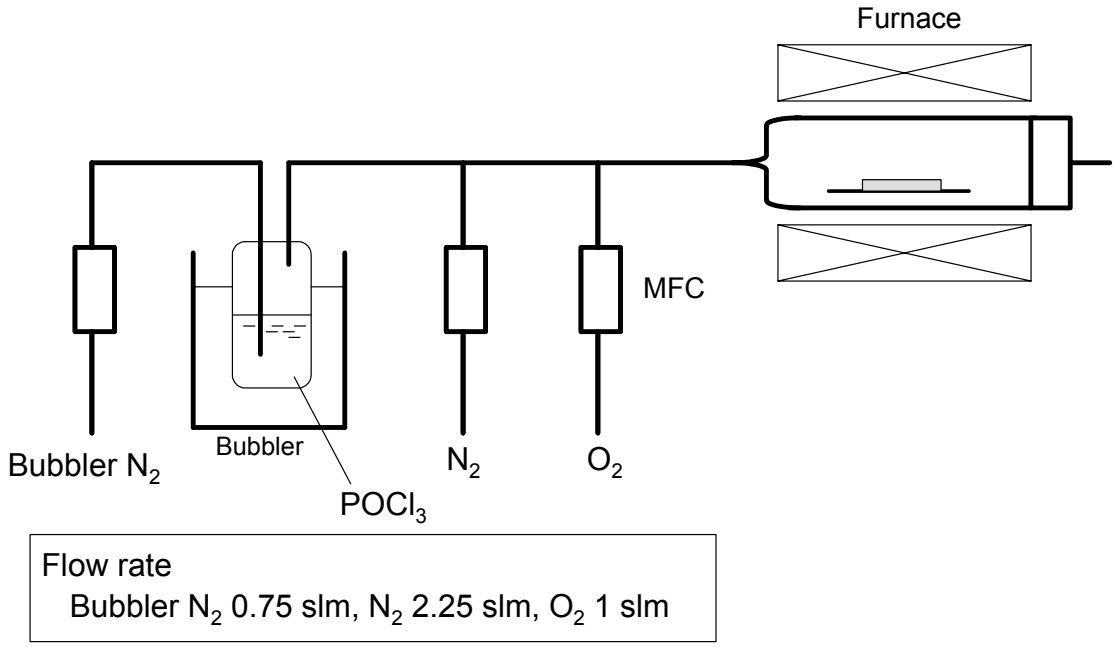

Fig. 3.1. $POCl_3$ annealing system used in this study.

The vapor pressure of $POCl_3$ is given by

$$\log_{10}(P) = A - \frac{B}{T + C} \quad \text{[bar]} \tag{3.X}$$

where P is the vapor pressure, T is the temperature, A = 4.28, B = 1446, and C = −40.2 [8]. Figure 3.2 shows the calculated vapor pressure of $POCl_3$. The vapor pressure can be controlled by changing the temperature of bubbler. When the temperature of the bubbler is 15 °C, the vapor pressure of $POCl_3$ is 2.8 kPa and the bubbling N_2 contains 2.8% of $POCl_3$.

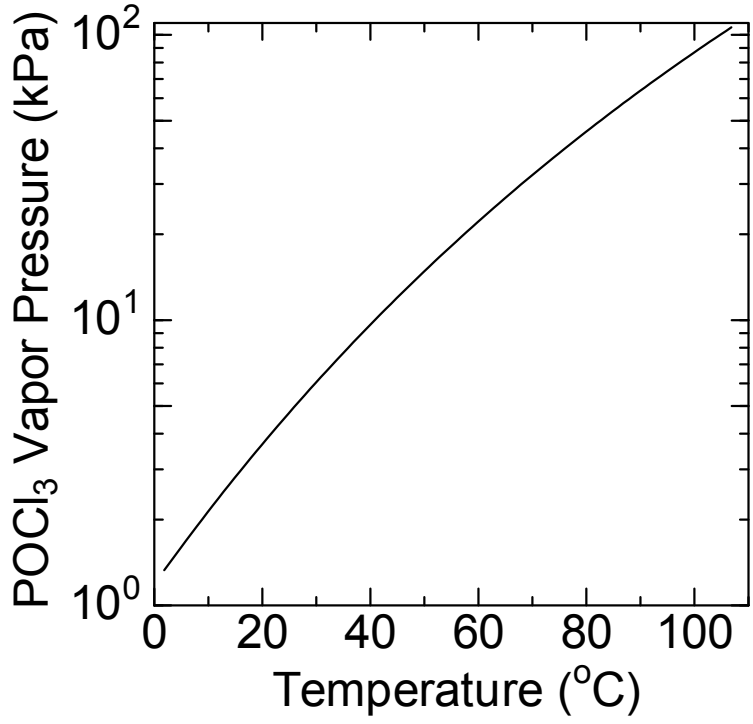

Fig. 3.2. Vapor pressure of $POCl_3$.

3.3 Fabrication of MOS capacitors and MOSEFTs

N-type 4°-off 4H-SiC (0001) Si-face epilayers with a net donor concentration of 8 × 10^{15} cm^{-3} were used to fabricate n-type MOS capacitors. After standard Radio Corporation of America (RCA) cleaning, approximately 55-nm-thick oxides were formed by dry oxidation at 1200 °C for 160 min. Then, the samples were annealed at 900 °C, 950 °C, 1000 °C for 10 min in a gas mixture of $POCl_3$, O_2, and N_2. A bubbler containing $POCl_3$ was maintained at 15 °C. Pure N_2 (0.75 slm) bubbled through the bubbler and led the $POCl_3$ into a furnace tube, while a mixture of pure O_2 (1.0 slm) and N_2 (2.25 slm) flowed directly through the tube. Subsequently, the samples were annealed in N_2 for 30 min at the same temperature. The oxide thickness was nearly

unchanged after annealing. The dielectric constant of P-doped oxide was roughly estimated to be around 3.8–4.1, which does not significantly deviate from the one of a pure SiO_2 gate oxide (3.9). Al was evaporated to form gate and backside electrodes. Post-metallization annealing was performed in N_2 at 400 °C for 30 min. For comparison, MOS capacitors were also fabricated by dry oxidation followed by NO annealing at 1250 °C for 90 min.

Planar n-channel MOSFETs were fabricated on p-type epilayers on n-type 4H-SiC substrates (4°-off; Si face). The net acceptor concentration of the p-epilayers was 7×10^{15} cm^{-3}. P^+ and Al^+ ions were implanted to form source/drain and body regions, respectively. Gate oxide was formed by dry oxidation, followed by $POCl_3$ annealing at 1000 °C under the same conditions as for the fabrication of the MOS capacitors. Al was evaporated to form gate, source, drain, and body electrodes. Post-metallization annealing was performed in N_2 at 400 °C for 30 min. For comparison, 4H-SiC MOSFETs with dry and NO-annealed oxides were also fabricated. The channel length (L) and width (W) were 30 and 200 μm, respectively.

3.4 Interface properties of MOS capacitors

Figure 3.3 shows high-frequency (100 kHz) and quasistatic *C*–*V* curves for the dry and $POCl_3$-annealed oxides. Unlike the case of P-implanted MOS capacitors, the flat-band voltage is very small for the $POCl_3$-annealed samples. In high-frequency *C*–*V* measurements, hysteresis was not observed for all the samples.

The energy distribution of interface state density (D_{it}) near the conduction band edge (E_c) of 4H-SiC estimated using the hi-lo *C*–*V* method [9] is shown in Fig. 3.4. The D_{it} near E_c does not change by $POCl_3$ annealing at 900 °C but decreases when the annealing temperature is above 950 °C. The D_{it} at 0.2 eV from E_c is reduced to around 9×10^{10} $cm^{-2}eV^{-1}$ by the $POCl_3$ annealing at 1000 °C. This value is smaller than those of dry and NO-annealed oxides. The decrease in D_{it} saturates at 1000 °C. In the *C*–*V* measurements at room temperature, hysteresis was not observed for any of the samples; therefore, contamination of Na^+ ions is negligible. The mean values of equivalent oxide thickness (EOT), assuming a dielectric constant of 3.9, D_{it} at 0.2 eV from E_c, and effective fixed charges (Q_{eff}/q) estimated from high-frequency *C*–*V* curves, are listed in Table 3.1. Unlike the P-implanted MOS capacitors where large positive fixed charge density was observed (Chapter 2), the effective fixed charge density, *i.e.*, flatband voltage shift, is small for the $POCl_3$-annealed samples.

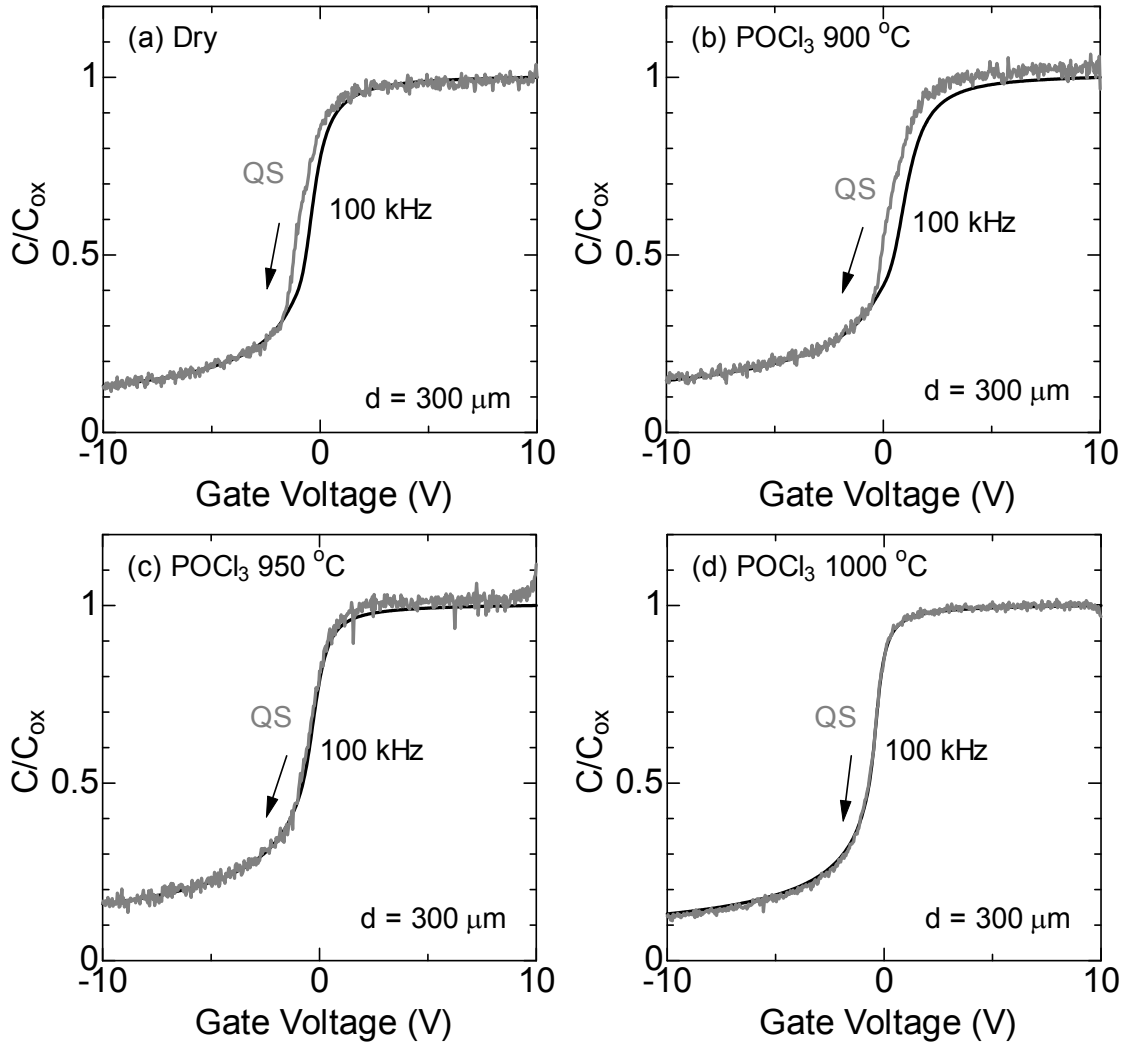

Fig. 3.3. High-frequency (100 kHz) and quasistatic (QS) *C–V* curves for the dry and $POCl_3$-annealed oxides: (a) dry, (b) $POCl_3$ annealing at 900 °C, (c) $POCl_3$ annealing at 950 °C, and (d) $POCl_3$ annealing at 1000 °C.

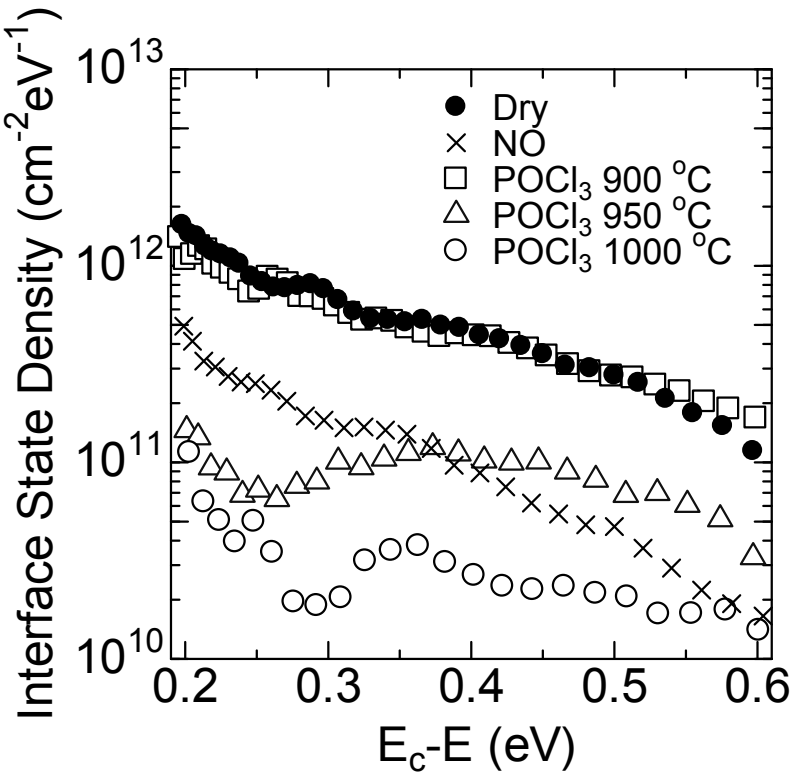

Fig. 3.4. Energy distribution of interface state density near the conduction band edge obtained from the hi-lo *C–V* method for P-doped oxides annealed at 900 °C, 950 °C, and 1000 °C. The results of dry and NO-annealed oxides are also shown.

Table 3.1 Equivalent oxide thickness (EOT), interface state density at 0.2 eV from E_c, and effective fixed charges

Gate Oxide	EOT (nm)	D_{it} ($cm^{-2}eV^{-1}$)	Q_{eff}/q (cm^{-2})
Dry (1200 °C)	55	1×10^{12}	-2×10^{10}
Dry + NO (1250 °C)	58	4×10^{11}	9×10^{10}
Dry + $POCl_3$ (900 °C)	56	1×10^{12}	-2×10^{10}
Dry + $POCl_3$ (950 °C)	56	1×10^{11}	3×10^{11}
Dry + $POCl_3$ (1000 °C)	56	9×10^{10}	4×10^{11}

3.5 Electrical properties of MOSFETs

Figure 3.5 shows the (a) drain-current–drain-voltage (I_D–V_D) and (b) drain-current–gate-voltage (I_D–V_G) characteristics of MOSFETs fabricated by $POCl_3$ annealing at 1000 °C. The I_D–V_D curves clearly show linear and saturation regions. The threshold voltage (V_T) of $POCl_3$-annealed MOSFETs, determined by linear extrapolation of the I_D–V_G curves to zero, is 0.0 V. The small threshold voltage implies a small number of interface-trapped charges. Positive fixed charges also contribute to the small threshold voltage. Threshold voltage instability due to mobile ions was not observed. This threshold voltage is small for the power devices, but it can be easily controlled by increasing p-well concentration.

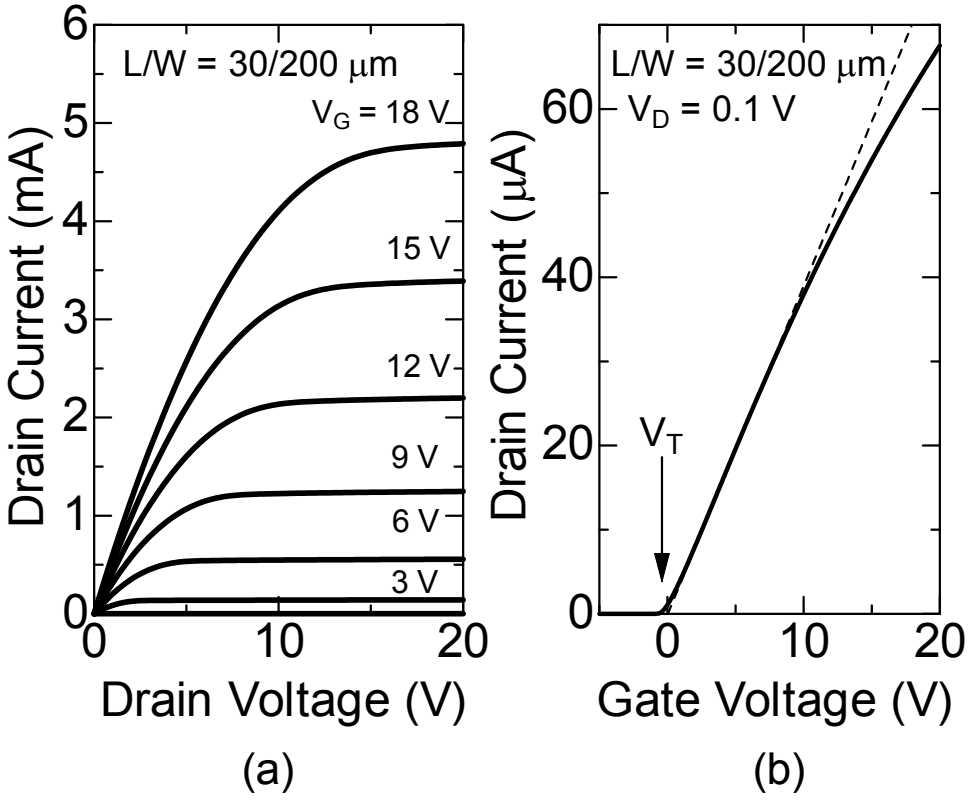

Fig. 3.5. (a) Output and (b) transfer characteristics of 4H-SiC MOSFETs fabricated on the Si-face by $POCl_3$ annealing at 1000 °C.

The field-effect mobility (μ_{FE}) was determined from the MOSFET transconductance ($g_m = dI_D/dV_G$) using

$$\mu_{FE} = \frac{L}{WC_{ox}V_D}\left(\frac{dI_D}{dV_G}\right) \tag{3.1}$$

where C_{ox} is the oxide capacitance per unit area. Note that the field-effect mobility used in this study is not identical to the *actual* electron mobility in an inversion layer because the number of free electrons in the inversion layer is decreased by trapping due to interface states [10]. Figure 3.6 shows the field-effect mobility of 4H-SiC MOSFETs fabricated by $POCl_3$ annealing at 1000 °C. The characteristics of dry and NO-annealed MOSFETs are also shown. The peak field-effect mobility was 89 cm^2/Vs—much higher than the typical channel mobility of NO-annealed MOSFETs. The channel mobility gradually decreases as the gate voltage increases, probably due to acoustic phonon or surface roughness scattering [11, 12]; however, it is still about 65 cm^2/Vs at 3 MV/cm—close to the actual operating gate field.

Figure 3.7 shows the subthreshold characteristics (log plot of I_D–V_G curves) of 4H-SiC MOSFETs fabricated by dry oxidation, NO annealing, and $POCl_3$ annealing at 1000 °C. The three curves can be directly compared because the oxide thicknesses are almost the same and the device geometry (L/W) values are identical for the three samples. The subthreshold swing (S) is determined by

$$S = \log 10 \frac{dV_G}{d\ln I_D} \cong \ln 10 \frac{kT}{q}\left(1 + \frac{C_D + C_{it}}{C_{ox}}\right) \tag{3.2}$$

where q is the electronic charge, k is the Boltzmann constant, C_D is the depletion layer capacitance, and $C_{it} = qD_{it}$ [13]. The mean values of peak field-effect mobility ($\mu_{FE,max}$), threshold voltage (V_T), subthreshold swing (S) calculated from I_D between 10^{-8} and 10^{-9}

A, and interface state density (D_{it}) estimated from S values are listed in Table 3.2. The D_{it} estimated from S values only reflects a small fragment of the interface states that lie between flatband and weak inversion conditions. The S values and D_{it} for $POCl_3$-annealed samples are smaller than those of dry and NO-annealed samples. An S value of 0.1 V/decade is very close to the ideal value of 0.08 V/decade. Thus, the high channel mobility is consistent with a low D_{it}.

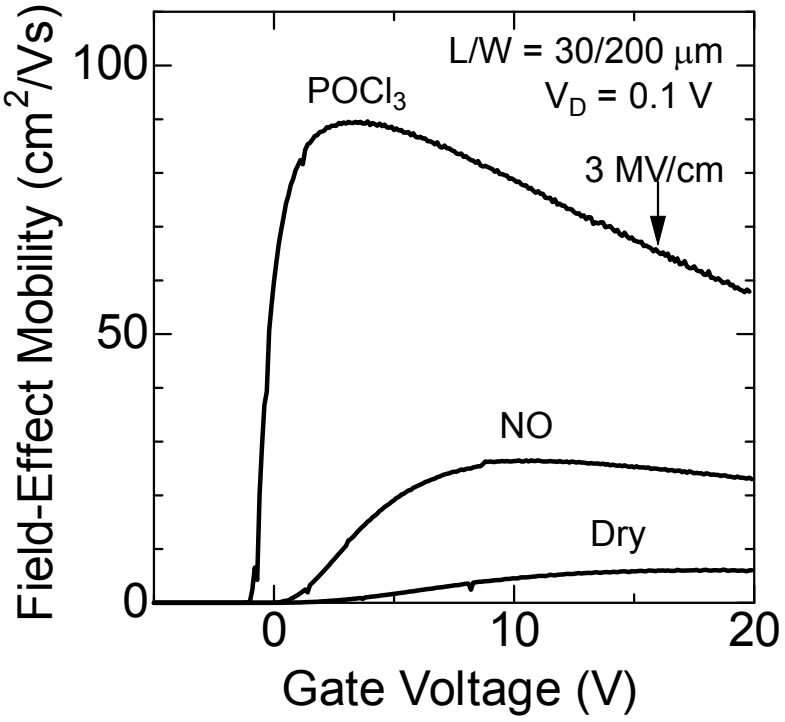

Fig.3.6. Field-effect mobility of 4H-SiC MOSFETs fabricated on the Si-face by dry oxidation, NO annealing, and the $POCl_3$ annealing at 1000 °C.

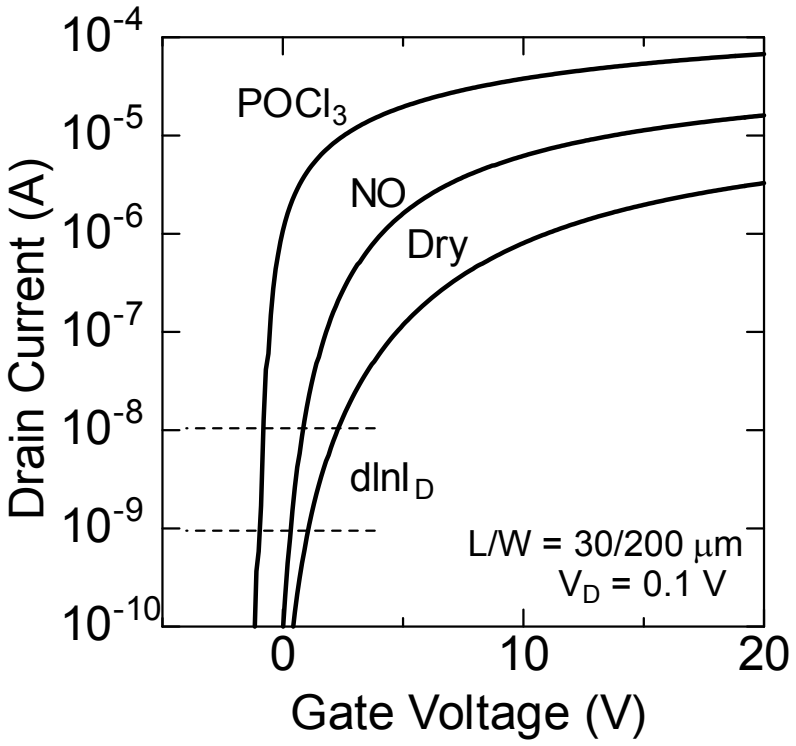

Fig.3.7. Subthreshold characteristics of 4H–SiC MOSFETs fabricated on the Si-face by dry oxidation, NO annealing, and the $POCl_3$ annealing at 1000 °C.

Table 3.2 Peak field effect mobility ($\mu_{FE,\ max}$), threshold voltage (V_T), subthreshold swing (S), and interface state density (D_{it})

Gate Oxide	$\mu_{FE,\ max}$ (cm^2/Vs)	V_T (V)	S (V/dec.)	D_{it} ($cm^{-2}eV^{-1}$)
Dry (1200 °C)	6	7.5	1.2	8×10^{12}
Dry+NO (1250 °C)	26	3.4	0.6	3×10^{12}
Dry+$POCl_3$ (1000 °C)	89	0.0	0.1	1×10^{11}

3.6 Depth profile analysis of phosphorus-doped oxide

Secondary ion mass spectrometry (SIMS) was used to reveal the profile of the P, C, and Cl atoms in the SiO_2 and near the interface. Figure 3.8 shows the depth profile for the oxide formed by the $POCl_3$ annealing at 1000 °C. Note that the change of etching rate in the interlayer [14] was not considered and, hence, the horizontal axis could have a margin of error. The P atoms are uniformly distributed in the oxide with a concentration of 2×10^{21} cm^{-3} and reach the SiO_2/4H-SiC interface, and are not diffused into the SiC side because of the small diffusion coefficient [15]. Therefore, the channel is not a so-called buried channel structure. On the other hand, the concentration of Cl atoms is less than the detection limit. This result means that P atoms play an important role to reduce the interface state density.

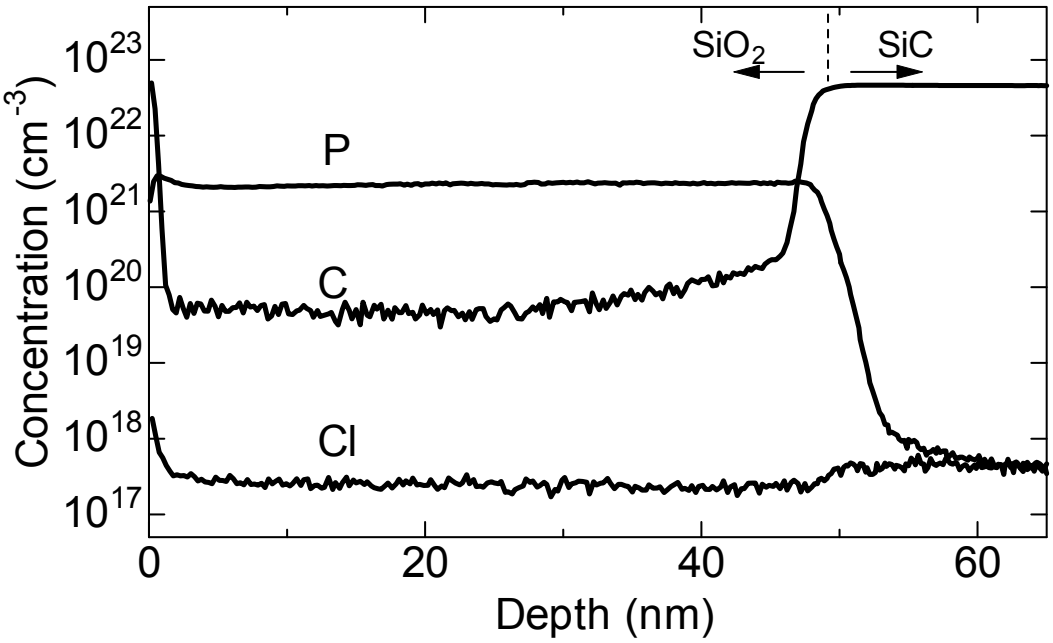

Fig. 3.8. P, C, and Cl atom profiles in the oxide and near the SiO_2/4H-SiC interface annealed with $POCl_3$ at 1000 °C determined by SIMS measurements.

3.7 Reliability of phosphorus-doped gate oxide

As described in Section 1.3.4, the reliability of gate oxide is another important issue to be solved before the commercialization of SiC MOSFETs. Therefore, it is important to investigate the oxide reliability. In this section, time-zero dielectric breakdown (TZDB) and time-dependent dielectric breakdown (TDDB) measurements were performed on the dry, NO-annealed and $POCl_3$-annealed MOS capacitors.

Fabrication of test element group

Figure 3.9 illustrates a MOS capacitor for the reliability tests. First, a 1-μm field oxide was deposited on a Si-face 4H-SiC epitaxial substrate by plasma-enhanced chemical vapor deposition (PE-CVD) using tetraethoxysilane (TEOS). Using photolithography, circular window with a 50-μm diameter was patterned. Then, the field oxide was etched by reactive ion etching (RIE) followed by buffered hydrofluoric acid (BHF) etching. Before thermal oxidation, the surface of the substrate was cleaned by standard RCA cleaning. Three types of gate oxides, dry, NO-annealed, and $POCl_3$-annealed oxides, were formed by the same oxidation procedures described in Section 3.3. Al was evaporated on the sample and properly etched using photolithography and wet etching.

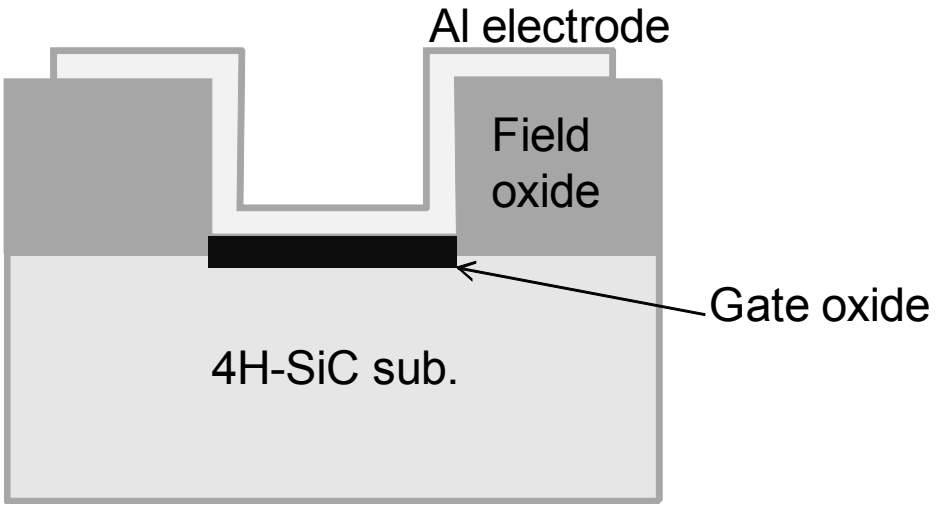

Fig. 3.9. Cross section of a MOS capacitor for the reliability measurements.

TZDB measurements

TZDB is immediate breakdown, which is caused by strong electric field (around 10 MV/cm). In the measurement, gate voltage is gradually increased and gate current is monitored; then, the electric field at the breakdown (field-to-breakdown, $\mathcal{E}_{BD}$) is recorded. The measurements were carried out at room temperature. In this study, the electric field across the gate oxide is approximated by

$$\mathcal{E}_{ox} = \frac{V_G - \phi_{ms}}{t_{ox}} \tag{3.3}$$

where ϕ_{ms} is the work function difference between the gate metal and the semiconductor. In the ideal interface without oxide and interface charges, the flatband voltage equals to the work function difference ($V_{FB} = \phi_{ms}$). For the SiO_2/Si interface, the approximation that $V_{FB} = \phi_{ms}$ is often used. However, in the case of SiO_2/SiC interface, there are a number of oxide charges and interface-trapped charges; thus, $V_{FB} \neq \phi_{ms}$ because the charges must be mirrored in the metal. It should be noted that it is assumed that the charges are localized at the interface in Eq. (3.3), and this is not always true.

Figure 3.10 shows the field-to-breakdown ($\mathcal{E}_{BD}$) distributions of dry, NO-annealed, and $POCl_3$-annealed oxides on 4H-SiC. For the $POCl_3$-annealed oxide, the $POCl_3$ annealing was performed at 1000 °C. More than 20 capacitors were tested for each oxide. Most of the breakdown occurs above 9 MV/cm, indicating that the oxides break down due to the intrinsic dielectric breakdown mechanism generally known as mode C type (>8 MV/cm) in Si MOS technology. The $\mathcal{E}_{BD}$ of $POCl_3$-annealed oxide is smaller than that of dry and NO-annealed oxides. The mode values of $\mathcal{E}_{BD}$ were 10.6, 10.0, and 9.6 MV/cm for dry, NO-annealed, and $POCl_3$-annealed oxides, respectively. This implies that the incorporated elements weaken the oxide immunity against strong electric field.

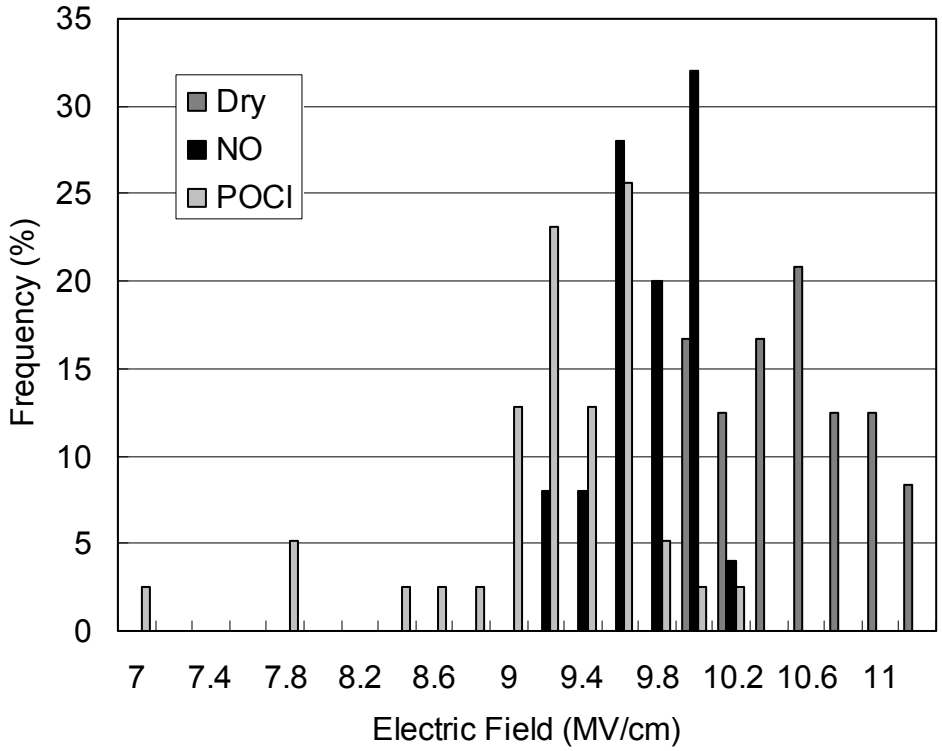

Fig. 3.10. Distributions of field-to-breakdown ($\mathcal{E}_{DB}$) of dry, NO-annealed, and $POCl_3$-annealed oxides obtained from TZDB measurements at room temperature.

TDDB measurements

Time-dependent dielectric breakdown (TDDB) is a failure mechanism in MOS structures, when the gate oxide breaks down as a result of long-time application of relatively low electrical stress. The charge needed to break the oxide is determined by measuring the time after which oxide breakdown occurs. In this study, constant-current TDDB (CC-TDDB) measurements were conducted on the dry, NO-annealed, and $POCl_3$-anenaled MOS capacitors. In the measurements, the constant current density of 0.3 mA/cm^2 was applied to the gate of a MOS capacitor and the time-to-breakdown was measured. The time-to-breakdown can be converted into charge-to-breakdown (Q_{BD}) which is equal to the total charge passing through the oxide before failure.

Figure 3.11 shows the distribution of cumulative failure rate for dry, NO-annealed, and $POCl_3$-annealed MOS capacitors. It is clear that the Q_{BD} of dry oxide is very small and that of NO-annealed oxide is relatively large. The Q_{BD} of $POCl_3$-annealed oxide is similar to that of dry oxide. However, the distributions are different for the two types of gate oxide. For the dry oxide, the Q_{BD} distribution has gradual and sharp slopes with a changing point. The gradual part is early failure due to roughness or defects of the substrate, and the steep part is intrinsic failure of the oxide. However, the distribution of the $POCl_3$-annealed oxide is a straight line with a steep slope. This indicates that the P-doped gate oxide mainly breaks down due to the intrinsic failure of the oxide. The improved quality of MOS interface by $POCl_3$ annealing may result in the better reliability at early failures. It is also supposed that some substrate defects that affect the oxide reliability can be passivated by $POCl_3$ annealing. However, the quality of the phosphorus-doped oxide is inferior to the pure SiO_2 because P atoms are distributed throughout the oxide. Therefore, the breakdown mode is dominated by intrinsic oxide

breakdown due to the incorporated P atoms.

The reliability of P-doped gate oxide on 4H-SiC is comparable to the dry oxide. However, the reliability of P-doped gate oxide is inferior to the NO-annealed gate oxide. This would be due to the uniformly distributed P atoms throughout the oxide. In the case of NO annealing, the incorporated N atoms are piled up only at the interface and the rest of the oxide network consists of almost pure SiO_2 [16]. Such distribution of incorporated atoms is desirable both for the good reliability and improvement in channel mobility. Further study is needed to improve the oxide reliability by controlling the P distribution in the oxide.

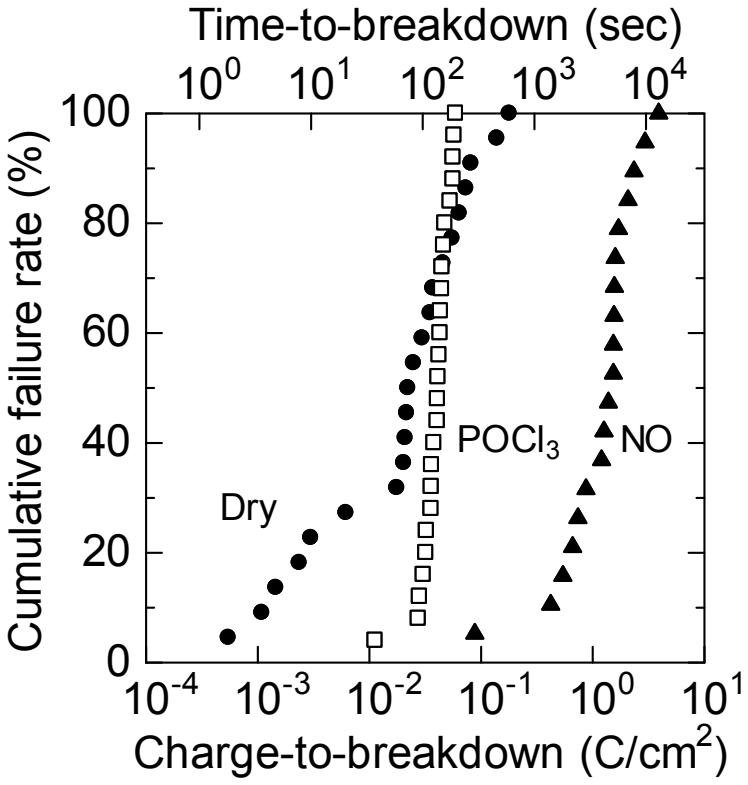

Fig. 3.11. The distribution of cumulative failure rate for dry, NO-annealed, and $POCl_3$-annealed MOS capacitors.

3.8 Summary

The excellent effect of $POCl_3$ annealing on the interface properties of the Si face of the SiO_2/4H-SiC structure was demonstrated. $POCl_3$ annealing at 1000 °C significantly reduced the interface state density near the conduction band edge, and the channel mobility increased to 89 cm^2/Vs. The high channel mobility is attributed to the reduced shallow interface state density. The method proposed in this chapter is one possible candidate for fabricating SiC power MOSFETs with high channel mobility.

The reliability of $POCl_3$-annealed oxide on 4H-SiC is comparable to the dry oxide. However, the reliability of P-doped gate oxide is inferior to the NO-annealed gate oxide. Further study is needed to obtain better reliability with maintaining the high channel mobility by P incorporation.

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Chapter 4
Removal of Near-Interface Traps at SiO_2/4H-SiC Interfaces by Phosphorus Incorporation

4.1 Introduction

As described in Chapter 3, the incorporation of P atoms into the SiO_2/4H-SiC interface significantly reduces the interface state density (D_{it}). The channel mobility of 4H-SiC MOSFETs on the (0001) Si face increases to 89 cm^2/Vs by thermal annealing using phosphoryl chloride ($POCl_3$) at 1000 °C. However, the mechanism behind this improved channel mobility is unclear, and detailed studies are required.

One possible origin of interface states at the SiO_2/4H-SiC interface is near-interface traps (NITs) [1-3]. Although the origin of NITs is still unclear, they are considered as native oxide defects that lie 2.8 eV below the conduction band edge of SiO_2 [1]. Their energy level is considered to be very close to the conduction band edge of 4H-SiC [1-3], allowing substantial trapping of channel electrons. The density of NITs at the SiO_2/SiC interface can be decreased by NO or N_2O annealing [4] or sodium-enhanced oxidation (SEO) [5]. As a result of these annealing techniques, the channel mobility of 4H-SiC MOSFETs is greatly improved [6, 7]. Therefore, it is important to examine the nature of NITs, because their density is apparently related to the channel mobility of 4H-SiC MOSFETs.

In this chapter, the density of trapped electrons in NITs in $POCl_3$-annealed oxides is described in comparison with that in conventional dry and NO-annealed oxides. Cyclic *C–V* measurements at a low temperature [3, 4] and thermal dielectric relaxation current

(TDRC) technique [2, 5, 8] were employed to analyze the NITs. In addition, interface structure was investigated by X-ray photoelectron spectroscopy (XPS).

4.2 Low temperature capacitance–voltage measurement

In order to investigate the presence of NITs, low temperature *C–V* method proposed by Afanas'ev *et al*. was employed [3, 4]. The emission time constant of NITs is very large. For example, the time constant of 3 ns at room temperature and 80 s at 80 K is reported [9]. With decreasing temperature, part of the NITs can no longer emit electrons because the emission time constant becomes smaller. At a low temperature, NITs are filled with electrons by accumulation bias and are not able to immediately emit them within the measurement time. This causes additional fixed charges (ΔQ_{eff}) which lead to the flatband voltage shift (ΔV_{FB}) in *C–V* curves. Basically, such shift is not observed at room temperature because of the small time constant.

The analyzed MOS capacitors were fabricated under the same conditions as in Chapter 3. The dry, NO, and $POCl_3$ (1000 °C) samples were investigated. Figure 4.1 shows the start voltage dependence of high-frequency (100 kHz) *C–V* curves measured at 80 K for (a) dry, (b) NO-annealed, and (c) $POCl_3$-annealed oxides. Dashed lines denote flatband capacitance (C_{FB}). The gate voltage was swept from accumulation to depletion, and *C–V* curves were repeatedly measured as the start voltage increased from 2 to 18 V in 2-V steps. A positive shift of the *C–V* curves was observed for the dry and NO-annealed samples depending on the start voltage. Positive shifts occur between the capacitances in flatband and accumulation regions where the acceptor-like interface states are filled with electrons. The electrons are captured by NITs and most of them are not thermally emitted during measurements at 80 K [3]. The trapped electrons in NITs

act like negative fixed charges at low temperature; thus, a positive shift of the *C–V* curves was observed. Start voltage dependence almost disappeared for $POCl_3$-annealed MOS capacitors. This result indicates that the density of NITs decreased more significantly in $POCl_3$-annealed samples than in NO-annealed ones.

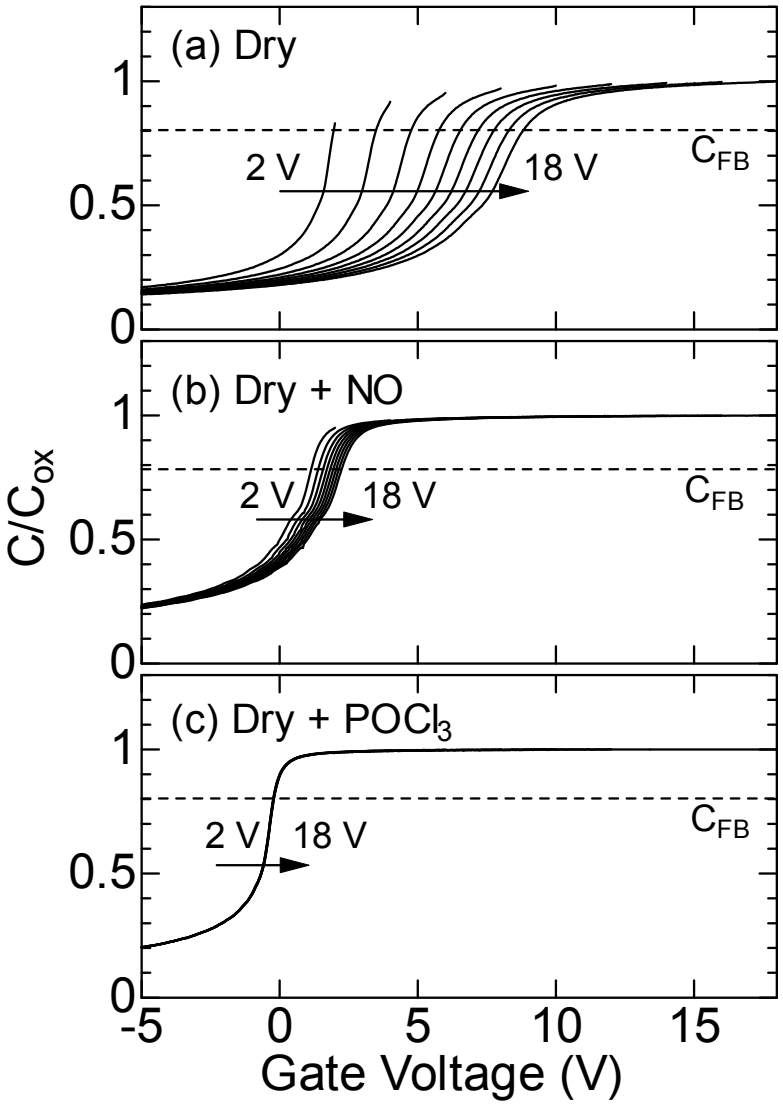

Fig. 4.1. Start voltage dependence of high-frequency (100 kHz) *C–V* curves measured at 80 K for (a) dry, (b) NO-annealed, and (c) $POCl_3$-annealed oxides. The gate voltage was swept from accumulation to depletion (positive to negative). Start voltage was increased from 2 to 18 V in a 2-V step. Dashed lines denote the flatband capacitance (C_{FB}).

4.3 Thermal dielectric relaxation current measurement

In order to quantify the density of trapped electrons in the NITs, thermal dielectric relaxation current (TDRC) measurements were employed [2, 8]. Note that TDRC method is sometimes referred as thermally stimulated current (TSC) method.

Figure 4.2 schematically illustrates the overview of the TDRC method as a function of time [2, 8]. In this method, a forward charging voltage (V_{ch}) was applied to the MOS capacitors at a relatively high temperature, bringing the surface into the accumulation condition. Then, the samples were cooled under a constant charging voltage. After the samples were adequately cooled, a reverse discharging voltage (V_{dis}) was applied, and the samples were subsequently heated at a constant rate. Trapped electrons were gradually released from NITs during heating, and they were recorded as a TDRC spectrum. The area underneath a TDRC curve is proportional to the total charge trapped in interface traps (N_{it}) as given by

$$N_{it} = \frac{1}{q\beta}\int_{T_0}^{\infty} |J(T)| dT \tag{4.1}$$

where q, β, T_0, and $J(T)$ are the elemental charge, heating rate, initial temperature, and current density at temperature T, respectively [8].

In this study, a forward charging voltage (V_{ch}) was applied to the MOS capacitors at 250 K. Then, the samples were cooled below 40 K under a constant charging voltage. The reverse discharging voltage (V_{dis}) was −5 V, and the samples were subsequently heated at a constant rate (β = 0.333 K/s).

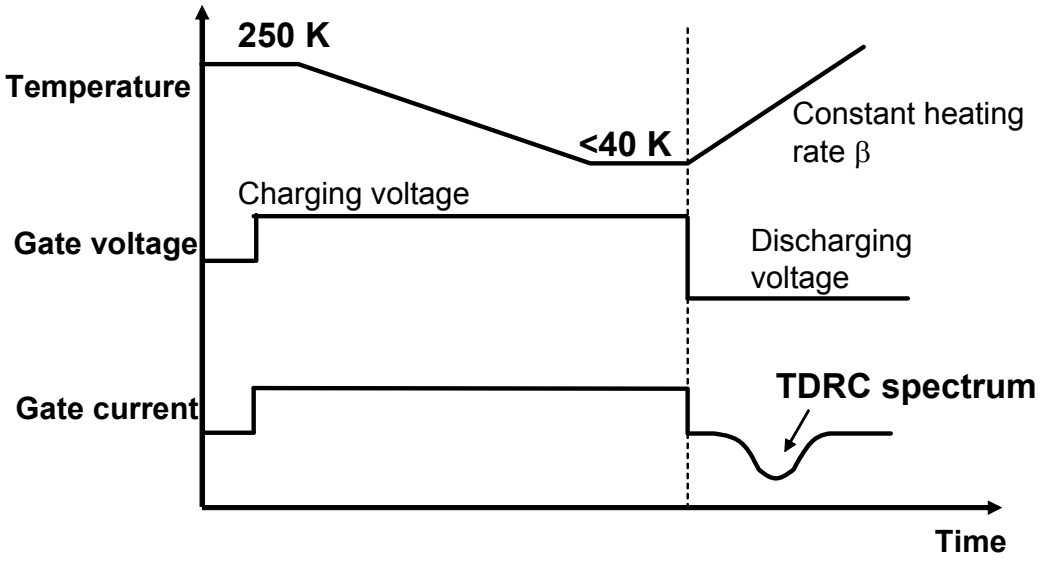

Fig. 4.2. Overview of thermal dielectric relaxation current (TDRC) method.

Figure 4.3 shows TDRC spectra for different types of gate oxides when the electric field across the oxide ($\mathcal{E}_{ox}$) during charging was approximately 4.5 MV/cm. The results can be interpreted by considering Rudenko's interface model, which assumes that NITs are intrinsic interfacial defects energetically located near the conduction band edge of 4H-SiC and spatially distributed from the interface into the oxycarbide transition region as illustrated in Fig. 4.4 [2]. For the dry oxide, a large signal with a peak at ~105 K is observed, showing a significantly large density of NITs. The wide peak between 50 and 200 K represents the emission of electrons from the NITs with activation energies of 0.1–0.7 eV [2]. The signal of NO-annealed oxide was weaker than that of dry oxide, but some NITs still exist in the NO-annealed oxide. In contrast, an extremely small signal of less than 0.1 pA can be found for the $POCl_3$-annealed oxide. Spectrum for the $POCl_3$-annealed oxide is featureless and lacks specific peaks. This TDRC spectrum resembles that of a contaminated oxide formed by SEO [5], indicating that NITs are almost completely removed by $POCl_3$ annealing.

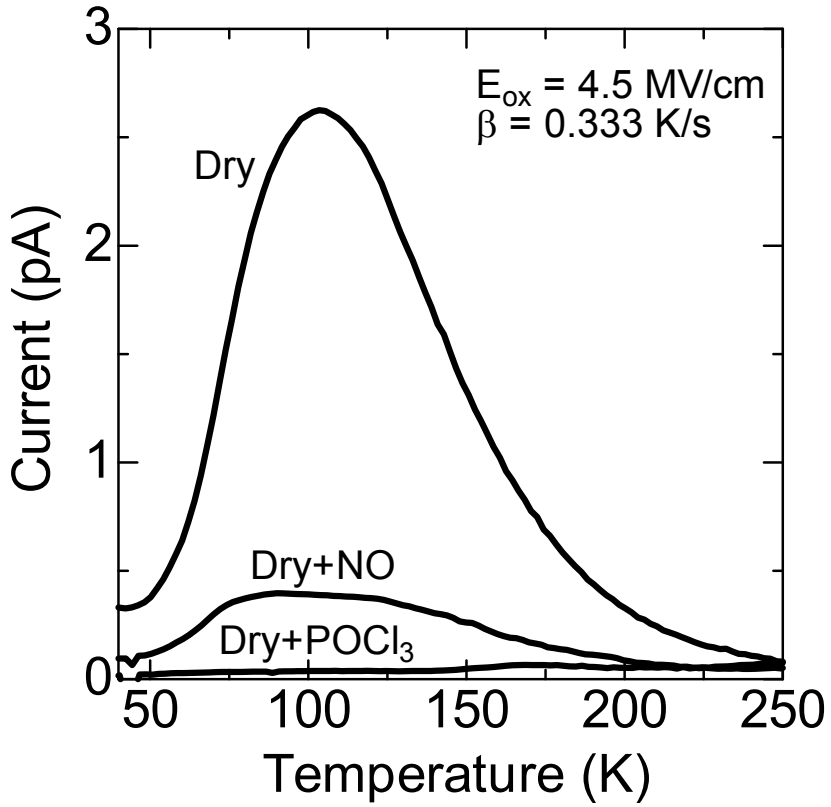

Fig. 4.3. TDRC spectra for dry, NO-annealed, and $POCl_3$-annealed oxides. Electric field across the oxide during charging was approximately 4.5 MV/cm. Heating rate (β) is 0.333 K/s. Discharging voltage (V_{dis}) is −5 V.

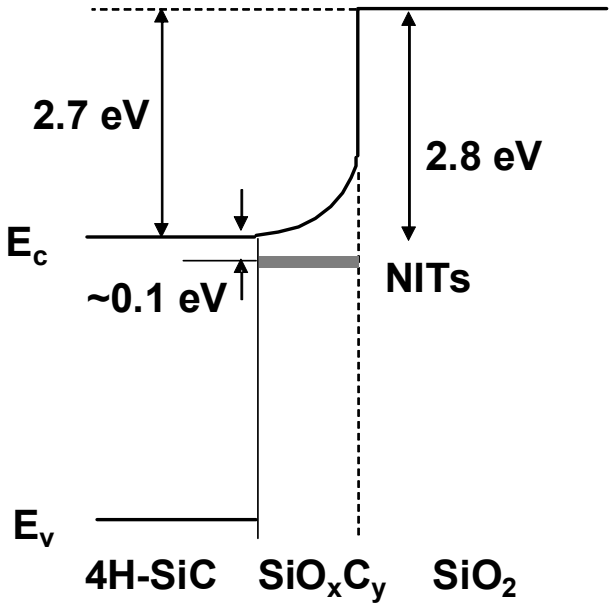

Fig. 4.4. Rudenko's interface model [2]. Near-interface traps (NITs) are assumed to be intrinsic interfacial defects energetically located near the conduction band edge of 4H-SiC and spatially distributed from the interface into the oxycarbide transition region.

Figures 4.5, 4.6, and 4.7 show charging-voltage dependence of TDRC curves for dry, NO-annealed, and $POCl_3$-anenaled oxides, respectively. Figure 4.8 shows the density of electrons trapped in interface traps estimated by integrating TDRC spectra as a function of the electric field across the oxide ($\mathcal{E}_{ox}$) during charging. The dashed line shows the total accumulated charges, given by $N_{acc} = \varepsilon_{ox}\mathcal{E}_{ox}/q$, where ε_{ox} is the permittivity of SiO_2. In the dry oxide samples, most of the electrons in the accumulation layer are trapped into NITs. The number of trapped electrons increases with the electric field and does not saturate. The absence of saturation implies that the true total density of NITs is larger than 10^{13} cm^{-2} for the dry oxide. On the other hand, the number of trapped electrons in $POCl_3$-annealed oxides is two orders of magnitude lower than that in dry oxide. Thus, these results clearly show that the density of NITs is strongly reduced by $POCl_3$ annealing.

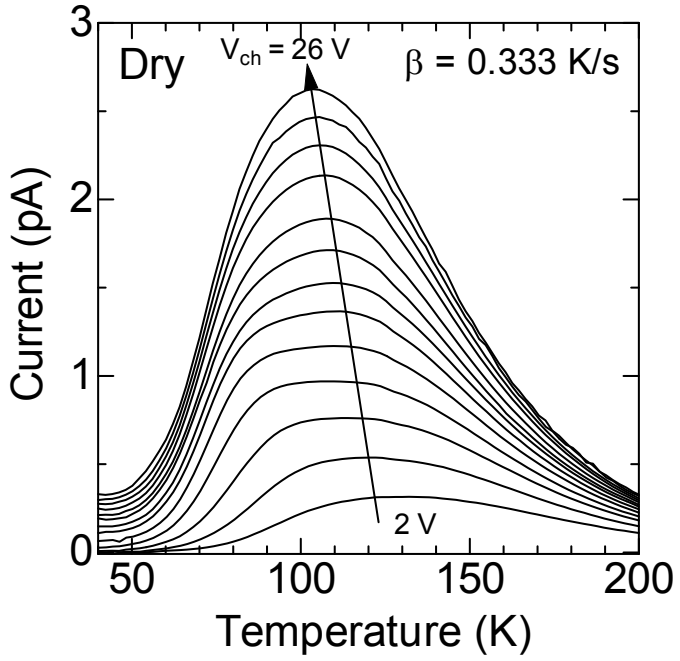

Fig. 4.5. Charging-voltage dependence of TDRC curves for the dry oxide.

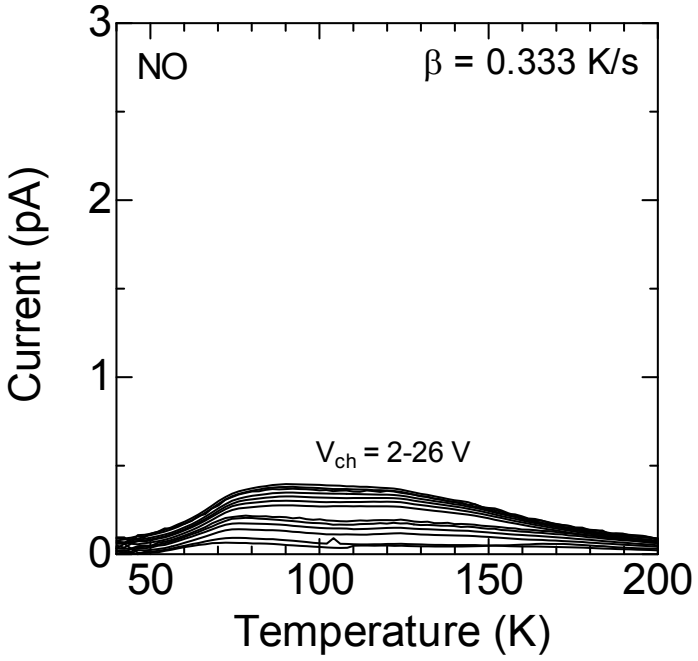

Fig. 4.6. Charging-voltage dependence of TDRC curves for the NO-annealed oxide.

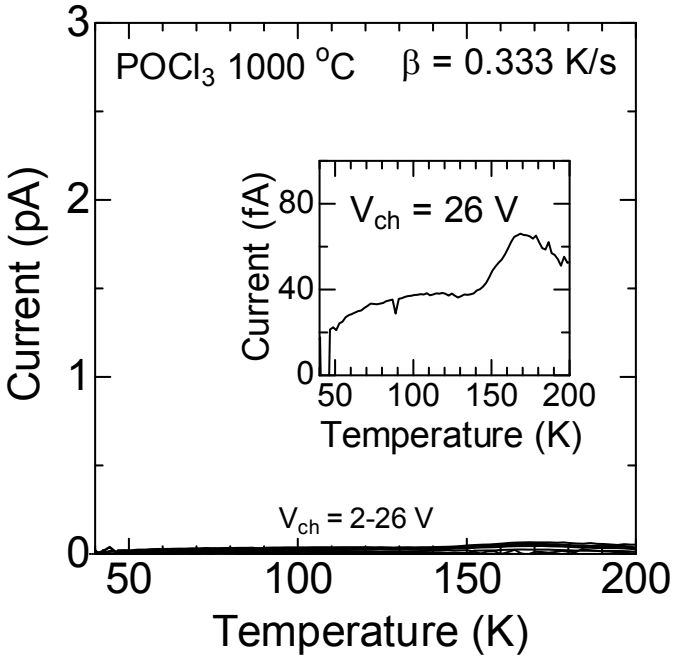

Fig. 4.7. Charging-voltage dependence of TDRC curves for the $POCl_3$-annealed oxide.

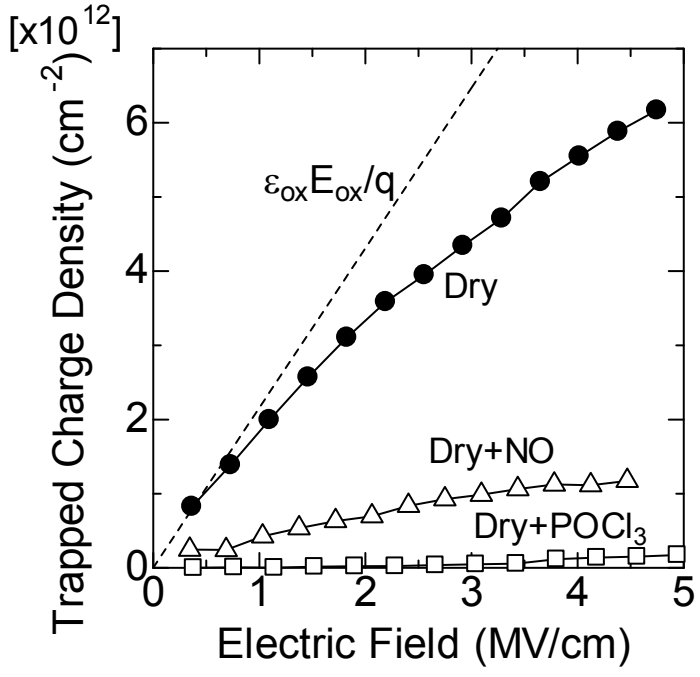

Fig. 4.8. Density of trapped electrons in interface traps as a function of electric field across the oxide during charging. Dashed line denotes the total accumulated charge at the SiO_2/4H-SiC interface during charging.

4.4 Structure of phosphorus-doped oxides and the interface

The results described above suggests that the reduction of the density of NITs that exist near the conduction band edge (E_c) of 4H-SiC is a main reason for the high channel mobility of MOSFETs with P-doped gate oxide. However, the mechanism of D_{it} reduction still remains unclear. In order to elucidate the structure of the P-doped oxides and at the P-doped SiO_2/SiC interface, XPS measurements were carried out on the $POCl_3$-annealed oxides.

The samples for XPS measurements were gradually etched by 0.1% diluted hydrogen fluoride (HF) solution. Ar ion sputtering was not used in order to avoid structural change at the interface. The oxide thickness was measured with a spectroscopic ellipsometer. XPS measurements were performed with the monochromatized Al Kα line (1486.6 eV). Au was evaporated on some samples and the spectra were charge compensated using a reference Au peak at 84.0 eV.

Figure 4.9 shows the P2*p* core-level spectra of the $POCl_3$-annealed oxide. The oxide thickness was approximately 20.5 and 2.6 nm. The take-off angle was 90°; therefore, the electron escape depth is about 3.9 nm. While the XPS spectrum includes the information at the interface for the thickness of ~2.6 nm, it only consists of the information of the oxide for the thickness of ~20.5 nm. The obtained XPS spectra were referenced against reported spectra [10]. It was found that the peak of P2$p_{3/2}$ was at 133.9 eV for both thicknesses, which indicates that there are four P–O bonds and one of which forms a terminal P=O bond as in Fig. 4.10 [10]. The terminal P=O bond is not connected to the rest of the network. The terminal oxygen atom is non-bridging oxygen. Therefore, the structure of oxide network becomes weak and soft [10]. This result indicates that the incorporated P atoms in the oxide network induce the structural

change near the interface as similar to the case of P-doped SiO_2/Si case [10]. However, the reliability of the oxide may become worse due to the weak oxide network.

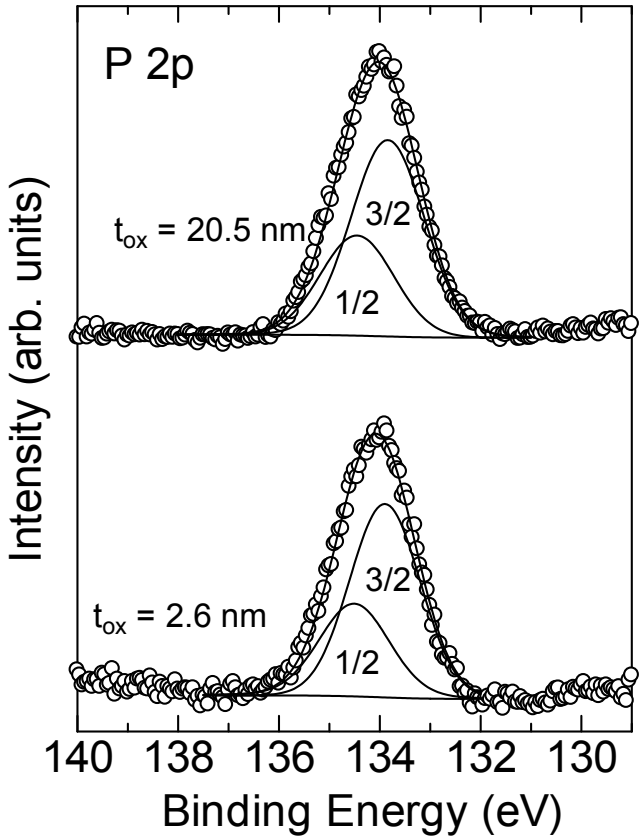

Fig. 4.9. P2*p* XPS spectrum of the $POCl_3$-annealed oxide. The oxide thickness was about 20.5 and 2.6 nm. The take-off angle was 90°.

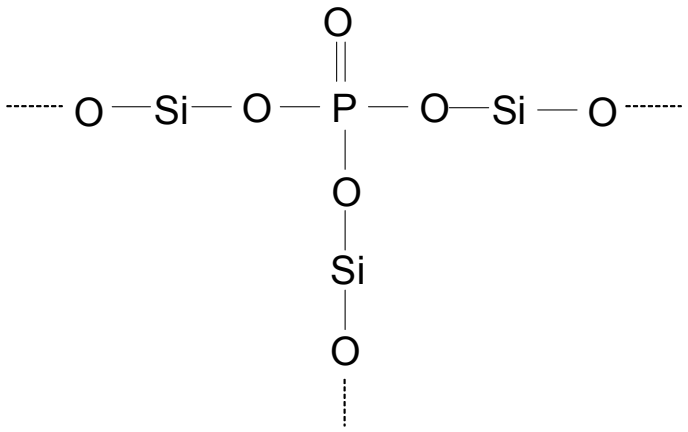

Fig. 4.10. Structure of P-doped SiO_2 formed by $POCl_3$ annealing of 4H-SiC.

4.5 Discussion

As described in Chapter 1, Pensl *et al*. suggested that the origins of the interface states is the combination of (i) dangling bonds of Si and/or C atoms, (ii) sp^2-bonded carbon clusters, and (iii) NITs [9]. In contrast with SiO_2/Si interfaces, annealing in H_2 up to 400 °C is not effective for SiO_2/SiC interfaces [9]. This suggests that Si dangling bonds are not dominant defects at the SiO_2/4H-SiC interface. C dangling bonds were identified and their successful passivation by H_2 was demonstrated [11]. However, the C dangling bonds create deeper traps [11] and are not the origin of shallow traps detected in this study. Bassler *et al*. proposed the C cluster model based on the fact that the internal photo emission (IPE) signals of a-C:H and SiO_2/SiC are relatively similar [12]; however, the two spectra are not identical. The C clusters have not been directly observed so far [13, 14], although this cannot rule out their presence.

Considering the discussion above, NITs would represent the high density of traps near the E_c. Although no one has identified the origin of NITs, the author assumes that the origin is excess Si atoms or strained Si–Si bonds (equivalent to O vacancies) near the interface. This assumption may be reasonable because the NITs are native oxide traps that exist in both the SiO_2/Si and SiO_2/SiC structures, and their energy always lie 2.8 eV below the conduction band edge of SiO_2 [1]. During thermal oxidation of both Si and SiC, Si atoms are emitted as interstitials into the oxide, which is caused by the strain due to the expansion of Si lattices during oxidation [15, 16]. In the case of SiO_2/Si interface, first principle investigation has suggested that the excess Si flown into the oxide is thought to have the O-vacancy-like structure with suboxide Si–Si bonds [17]. From this report, it is speculated that the accumulated Si atoms near the interface for SiO_2/Si and SiO_2/SiC interface create the same trap level at 2.8 eV from the E_c of SiO_2

[1]. The trap levels due to Si–Si bonds depend on the Si–Si bond length because the bonding-antibonding splitting varies with the bond length [18] and possibly locate near the E_c of 4H-SiC as shown in Fig. 4.11.

For NO-annealed oxides, N atoms are piled up near the interface and form Si_3N_4 [18, 19], probably in the form of Si–N–Si bridges. The density of Si_3N_4 is 3.44 g/cm^3, which is close to that of SiC (3.2 g/cm^3). This leads to a more compact structure of the oxide network and reduce the mismatch between the SiO_2 and SiC, resulting in the lower density of NITs. For $POCl_3$-annealed oxides, the network becomes soft and weak by incorporating P atoms into the oxide. As a result, the local strain is released by the relaxation of the surrounding bond network [17], and a Si–Si bond is removed by these three possible reasons; (i) structural relaxation by the formation of soft network, (ii) suppression of Si emission from the interface during oxidation and the subsequent reduction of Si–Si bonds, and (iii) change in the Si–Si bond length and subsequent removal of the antibonding state from the bandgap of 4H-SiC. The interface structure is not clear and further study is required.

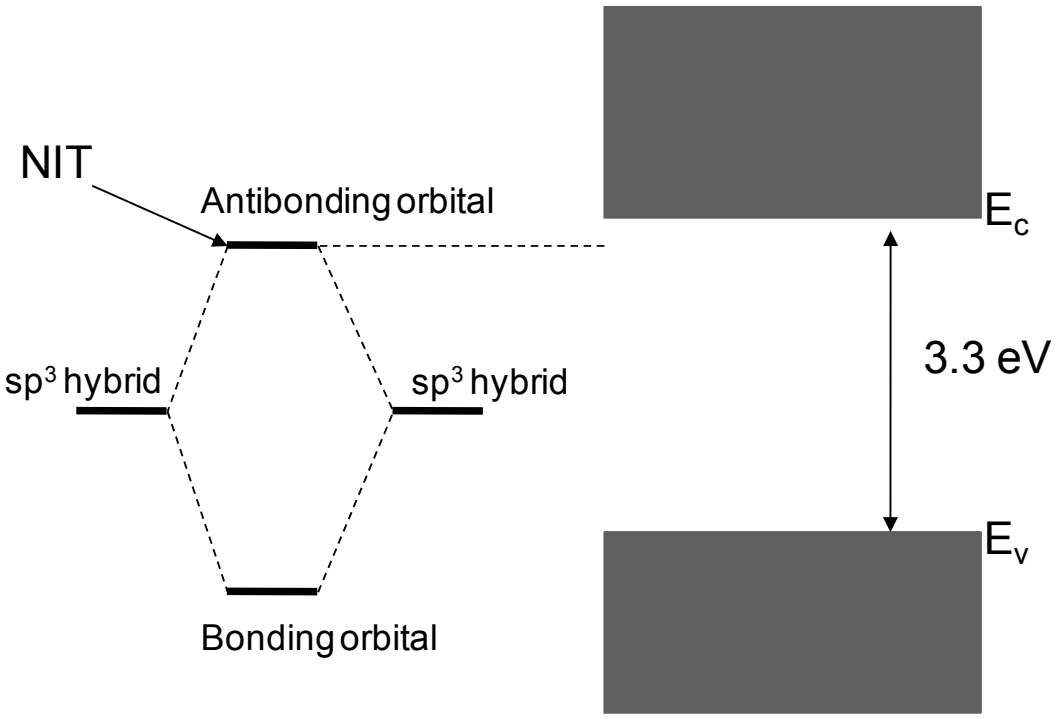

Fig. 4.11. Schematic of Si–Si bonding-antibonding states. Si–Si bonds have bonding-antibonding energy splittings depending on the bond length and could give rise to localized states near the band edges [17].

4.6 Summary

Effective removal of NITs in SiO_2/4H-SiC (0001) structures through phosphorus incorporation is demonstrated in this chapter. Low-temperature *C–V* and TDRC measurements were employed to investigate NITs in oxides prepared by dry oxidation, NO annealing, and $POCl_3$ annealing. Both the measurements revealed that the density of electrons trapped in NITs in $POCl_3$-annealed oxide is smaller than that in dry and NO-annealed oxides. For $POCl_3$-annealed oxides, the incorporated P atoms induce the structural relaxation near the interface, resulting in the lower density of NITs. The drastic elimination of NITs lowers the interface state density and increases the channel mobility in 4H-SiC MOSFETs.

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Chapter 5
Charge-Pumping Measurement on 4H-SiC MOSFETs and Its Application to Phosphorus-Doped Gate Oxide

5.1 Introduction

To investigate device performance, it is important to accurately characterize the SiO_2/SiC interface properties. In general, the interface state properties that affect the n-channel MOSFET performance are characterized using MOS capacitors fabricated on n-type SiC substrates, because the intrinsic carrier density of SiC is extremely small [1], [2]. This interface characterization is based on the assumption that the MOS interface properties of p- and n-type substrates are identical. However, it is preferred to evaluate the interface states using n-channel SiC MOSFETs because MOS capacitors are not directly related to real device operation. A few methods have been proposed to use gate controlled diodes fabricated on p-type SiC substrates to access the interface states located near the conduction band edge [3, 4]. Although these methods are appropriate for evaluating the interface properties, a test element group with a larger gate size is required.

A useful and reliable method of directly measuring MOSFET interface properties is to use charge-pumping technique [5-8], which is frequently used to evaluate the interface properties of Si MOSFETs. This method involves measuring the substrate charge-pumping current while applying voltage pulses to the MOSFET gates. The

interface state density of MOSFETs can be accurately determined by this method, because the charge-pumping current I_{CP} is directly related to the interface state density. The details of the measurement are described in Section 5.2 and other studies [5, 8].

In addition, the charge-pumping technique can be applied to the evaluation of MOSFET degradation [9]. This method also enables the characterization of the MOS interface fabricated on a trench sidewall (UMOS interface), which is usually difficult to measure with the capacitance–voltage (*C*–*V*) method because of its complicated structure [10]. If SiC MOSFETs can be directly characterized by the charge-pumping technique, more useful information regarding real device operation can be obtained.

However, few results have been reported on charge-pumping measurements of SiC MOSFETs. Scozzie *et al*. compared the charge-pumping curves for 6H-SiC and Si MOSFETs [11]. They obtained trapezoid-like curves with sharp rising and falling edges for Si MOSFETs, whereas they observed distorted curves with a long current tail for SiC MOSFETs. These unusual charge-pumping curves of SiC MOSFETs have not been thoroughly discussed. Thus, speculation arises whether this method is applicable for SiC MOSFETs. Therefore, it is crucial to understand the distorted charge-pumping curves for SiC MOSFETs.

In this chapter, charge-pumping measurements were performed on 4H-SiC MOSFETs to determine the cause of distortion of charge-pumping curves for SiC MOSFETs. The measurement conditions that should be used to obtain reliable charge-pumping curves were discussed. In addition, the 4H-SiC MOSFETs with P-doped gate oxide is also examined utilizing the established CP technique.

5.2 Charge-pumping method

Figure 5.1 illustrates the basic configuration of the charge-pumping measurement on an n-channel MOSFET [6]. The source and drain are connected and grounded. In some cases, reverse bias (V_R) is applied to the source and drain, but it is not applied in this study (V_R = 0). In order to repeat on and off states of the MOSFET, pulse trains with large enough amplitude (V_a) is applied to the gate. The band diagram of the MOSFET during the inversion to accumulation transition is shown in Fig. 5.2 (a). The MOSFET is in inversion condition when the positive bias is applied to the gate. A part of the electrons in the inversion layer are captured at the interface states. When the gate pulse changes from positive to negative bias and the band bending becomes gentle, electrons in the inversion layer moves toward source and drain regions by drift and diffusion. In

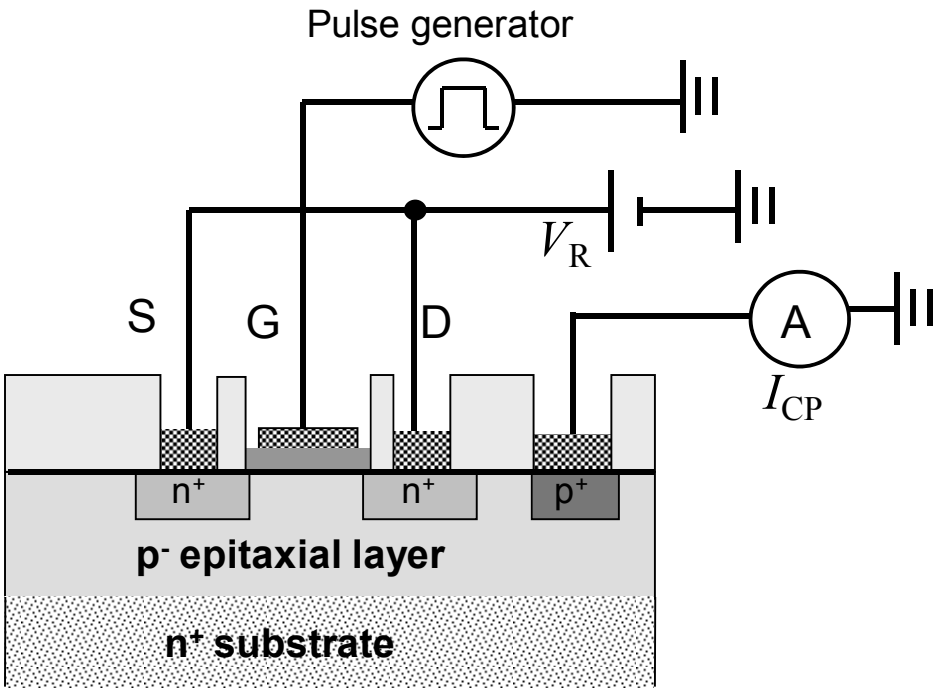


Fig. 5.1. Basic experimental setup for charge pumping measurements.

addition, the electrons trapped at the shallow interface states are thermally emitted to the conduction band and move toward source and drain regions as well. The energy levels from which the electrons are emitted are determined by the Shockley-Read-Hall (SRH) model. The range is between the conduction band edge (E_c) and an energy level E_{eme} in Fig. 5.2 (a). E_{eme} is given by

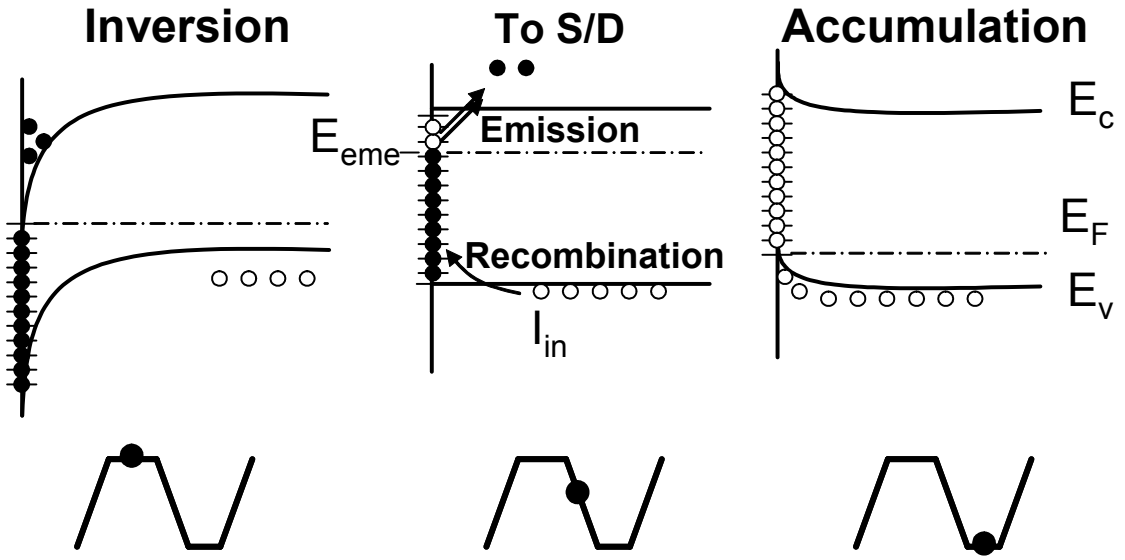
$$E_{eme} = E_i - kT \ln\left[\sigma_n v_{th} n_i \frac{V_T - V_{FB}}{V_a} t_f \right] \tag{5.1}$$

where E_i is the intrinsic Fermi level, k is the Boltzmann constant, T is the temperature, σ_n is the electron capture cross section, v_{th} is electron thermal velocity, V_T is the threshold voltage of the MOSFET, V_{FB} is the flatband voltage of the MOSFET, V_a is the pulse amplitude and t_f is the pulse fall time [9]. The electrons trapped at the interface states which locate deeper than E_{eme} are not thermally emitted to the conduction band and remain in the interface states. After that, negative voltage becomes larger and holes are subsequently flown from the substrate into the interface. Then the holes recombine with the electrons at the interface states between E_{eme} and valence band edge (E_v). These processes are occurred during the inversion to accumulation transition of MOSFETs.

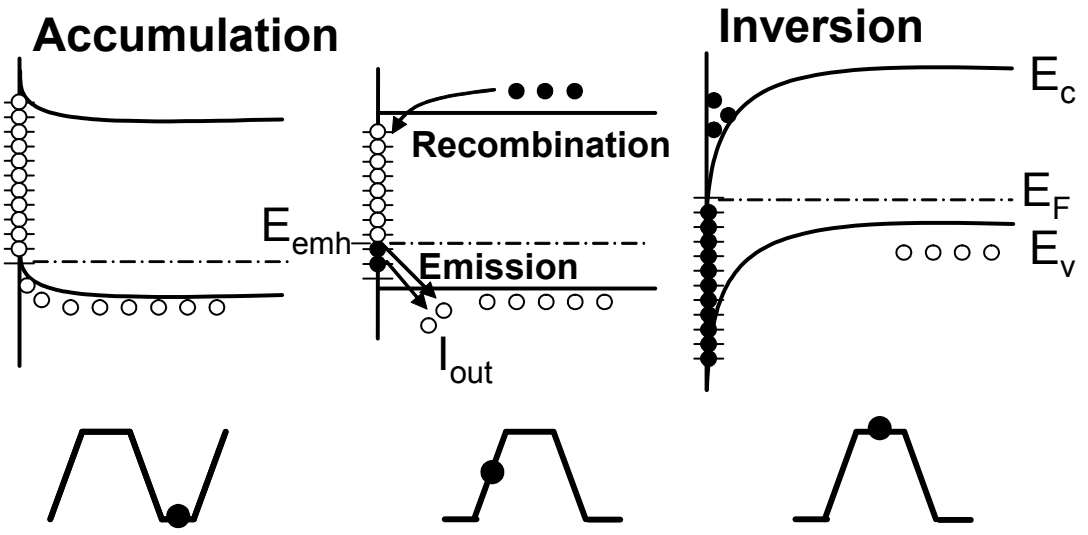
Figure 5.2 (b) illustrates the band diagram of an n-channel MOSFET during accumulation to inversion transition. In this case, the holes in the interface states between E_v and E_{emh} are thermally emitted to the conduction band. E_{emh} is given by

$$E_{emh} = E_i + kT \ln\left[\sigma_p v_{th} n_i \frac{V_T - V_{FB}}{V_a} t_r \right] \tag{5.2}$$

where σ_p is the hole capture cross section, and t_r is the pulse rise time [9]. When the gate voltage exceeds the threshold voltage of the MOSFET and the inversion layer is



(a) Inversion to accumulation transition



(b) Accumulation to inversion transition

Fig. 5.2. Band diagram of the MOSFET during the inversion to accumulation and the accumulation to inversion transitions.

formed, holes remaining at the interface states between E_c and E_{emh} recombine with electrons in the inversion layer. The number of the holes flown from the substrate and recombine with electrons at the interface during inversion to accumulation transition is larger than the number of the holes thermally emitted to the valence band during inversion to accumulation transition. This difference in the hole current ($I_{in} - I_{out}$) is measured as the charge-pumping current which directly related to the interface state density located between E_{eme} and E_{emh}. Therefore, the charge-pumping measurement can quantify the interface states located within an energy range (ΔE) which is determined by

$$\Delta E = E_g - (E_c - E_{eme}) - (E_{emh} - E_v) = (E_{eme} - E_{emh}). \quad (5.3)$$

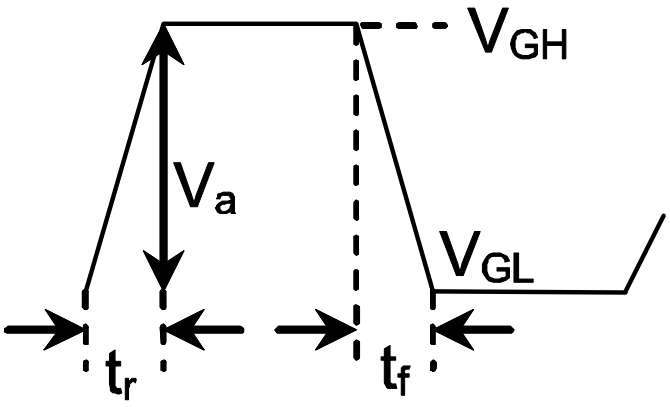
The charge-pumping current is proportional to the number of carriers trapped in the interface states located within ΔE, the gate area (A_G), and the pulse frequency (f). Therefore, the charge-pumping current (I_{CP}) is given by

$$I_{CP} = I_{in} - I_{out} = A_G f q \overline{D}_{it} \Delta E \quad (5.4)$$

where $\overline{D}_{it}$ is the mean interface state density, averaged over the energy interval ΔE, swept during the voltage pulses.

In this study, charge-pumping measurements were performed using a Keithley semiconductor characterization system (4200-SCS) with a pulse generator. Two types of charge-pumping measurements—a variable amplitude-sweep mode and base-sweep mode—were performed using a trapezoidal pulse train with a 50% duty cycle. Figure 5.3 shows the trapezoidal pulse wave form used in the charge-pumping measurements. Figure 5.4 (a) shows the pulse train used in the base-sweep charge-pumping measurement. In the base-sweep mode, pulse amplitude (V_a) is fixed and pulse base level (V_{GL}) is swept. The pulse amplitude (V_a) should be large enough to fully repeat

inversion and accumulation conditions of the MOSFET; namely, V_a should be larger that the difference of flatband and threshold voltages of the MOSFET ($V_a > V_T - V_{FB}$). The charge-pumping current flows only when the V_{GL} is smaller than V_{FB} and V_{GH} is larger than V_T for n-channel MOSFETs. Figure 5.4 (b) shows the pulse train used in the amplitude-sweep charge-pumping measurement. In the amplitude-sweep mode, pulse base level (V_{GL}) is fixed and pulse amplitude (V_a) is increased. The charge-pumping current flows when the pulse top level (V_{GH}) is larger than V_T.



V_a : Pulse amplitude
V_{GH} : Pulse top level
V_{GL} : Pulse base level
t_r : Pulse rise time
t_f : Pulse fall time

Fig. 5.3. Gate pulse waveform used in charge-pumping measurements. The parameters are the pulse amplitude (V_a), pulse top level (V_{GH}), pulse base level (V_{GL}), pulse rise time (t_r), and pulse fall time (t_f).

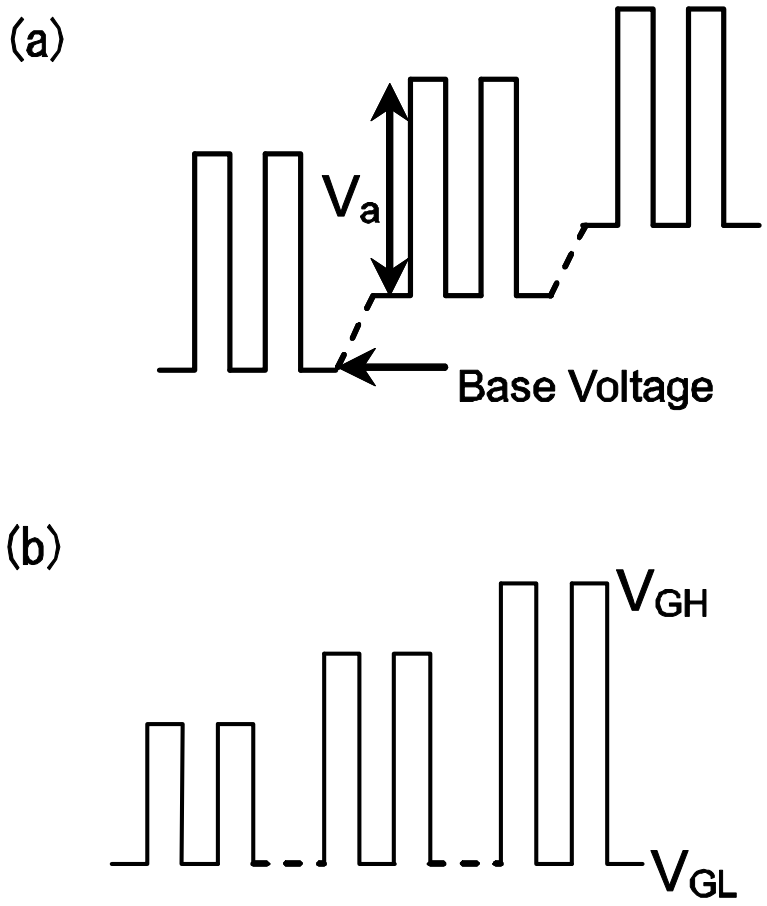


Fig. 5.4. Pulse trains for (a) base-sweep and (b) amplitude-sweep charge-pumping measurements.

5.3 Charge-pumping measurements on conventional SiC MOSFETs

In order to apply the charge-pumping measurement to SiC MOSFETs, it is important to investigate the basic charge-pumping characteristics on 4H-SiC MOSFETs fabricated by conventional oxidation process. Thus, the charge-pumping measurements were performed on the conventional 4H-SiC MOSFETs fabricated by pyrogenic wet oxidation and NO annealing.

Before investigating 4H-SiC MOSFETs, the charge-pumping measurements were

conducted on standard Si MOSFETs with the same geometry as the 4H-SiC MOSFETs. Base-sweep measurements were performed on the Si MOSFETs under standard conditions, *i.e.*, pulse amplitude V_a = 6 V, pulse frequency f = 100 kHz, and pulse rise and fall times $t_r = t_f$ = 100 ns. The charge-pumping curve for the Si MOSFET is shown in Fig. 5.5. A nearly symmetrical curve with a flat upper base was obtained, which is the standard charge-pumping curve.

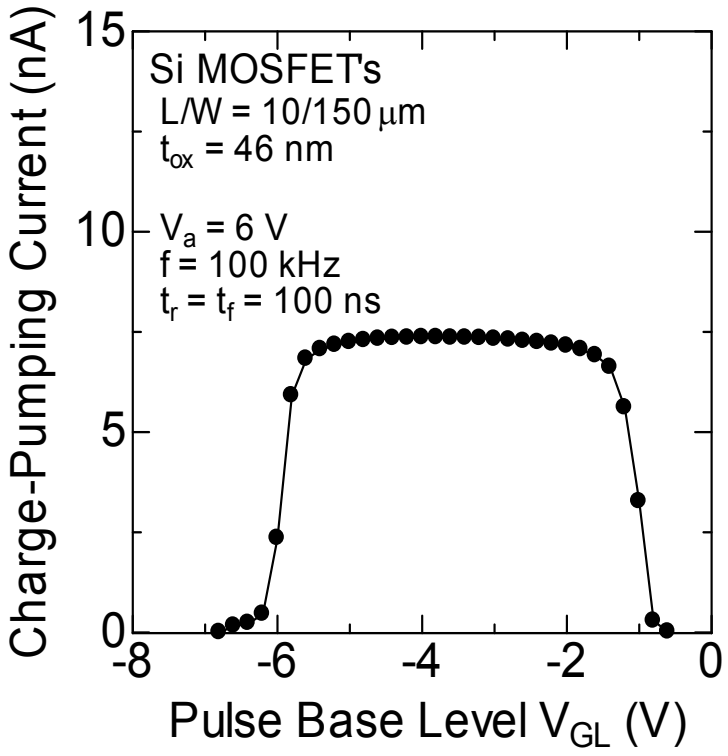


Fig. 5.5. Base-sweep charge-pumping curves for n-channel Si MOSFETs with a gate length L = 10 μm and gate width W = 150 μm. Pulse amplitude V_a = 6 V, pulse frequency f = 100 kHz, and pulse rise and fall times of $t_r = t_f$ = 100 ns.

Next, charge-pumping measurements were implemented on n-channel 4H-SiC MOSFETs. Planar n-channel MOSFETs were fabricated on n-type 4H-SiC substrates (4°-off, Si-face) with 5-μm-thick, p-type epilayers. The net acceptor concentration of the p-epilayers was 7×10^{15} cm^{-3}. P^+ and Al^+ ions were implanted as source/drain and body contacts, respectively. Two types of gate oxides were produced by (1) pyrogenic oxidation at 1200 °C for 45 min [denoted as (pyro.)] and (2) step 1 followed by post-oxidation annealing in NO at 1250 °C for 60 min [denoted as (pyro.+ NO)]. Ti/Al was used for source, drain, and body contacts, and Al was used for gate electrodes. The gate length L and width W were 10 and 150 μm, respectively. Table 5.1 lists the device properties for n-channel 4H-SiC MOSFETs, *i.e.*, the peak field-effect mobility μ_{FE}, estimated from the transconductance; the threshold voltage V_T*, determined by linear extrapolation of I_D–V_G curves to zero; and flat-band voltage V_{FB}*, determined from the C–V curves of p-MOS capacitors, which were fabricated on the same substrate with the MOSFETs. The asterisks distinguish these symbols from the charge-pumping threshold and flat-band voltages, which appear in the latter part of this thesis.

Table 5.1
Field-effect mobility, threshold voltage and flatband voltage for the fabricated SiC MOSFETs

Gate Oxide	μ_{FE} (cm^2/Vs)	V_T* (V)	V_{FB}* (V)
pyro.	6.2	5.8	–7.8
pyro.+ NO	30.4	2.7	–5.8

Figure 5.6 shows the pulse fall time dependence of base sweep charge-pumping curves for (a) 4H-SiC MOSFETs without NO annealing, and (b) 4H-SiC MOSFETs with NO annealing. The pulse rise time was maintained at 100 ns during measurements. 4H-SiC MOSFETs require large pulse amplitude because of the large difference between their threshold and flatband voltages. Ideally, the charge-pumping curve should be trapezoid-like, as in Fig. 5.5. However, SiC charge-pumping curves are asymmetrical, and have a long current tail on the right side of the curves, which is similar to the curves reported for SiC MOSFETs [11]. The current tail becomes longer as the gate length increases. Even in Si MOSFETs, the current tail can be observed in the case of a long gate length of 100 μm. The length of the long current tail seen in Fig. 5.6(a) reduces as the pulse fall time increases. The right-side edge of the curves is relatively steep for NO-annealed MOSFETs with gate length of 10 μm, as in Fig. 5.6(b). However, we confirmed that the current tail become longer for the NO-annealed MOSFETs with longer gate length ($L > 30$ μm).

Similar measurements were performed with variable amplitude sweep measurements using various pulse fall times. The pulse rise time was maintained at 100 ns. The charge-pumping characteristics for the unannealed and NO-annealed 4H-SiC MOSFETs are shown in Fig. 5.7(a) and (b), respectively. For ideal charge-pumping characteristics, the current saturates if non-ideal effects are absent. However, when the pulse fall time is short, an increase in the current is observed as the gate pulse-top level V_{GH} increases above 10 V, because the current includes an additional component.

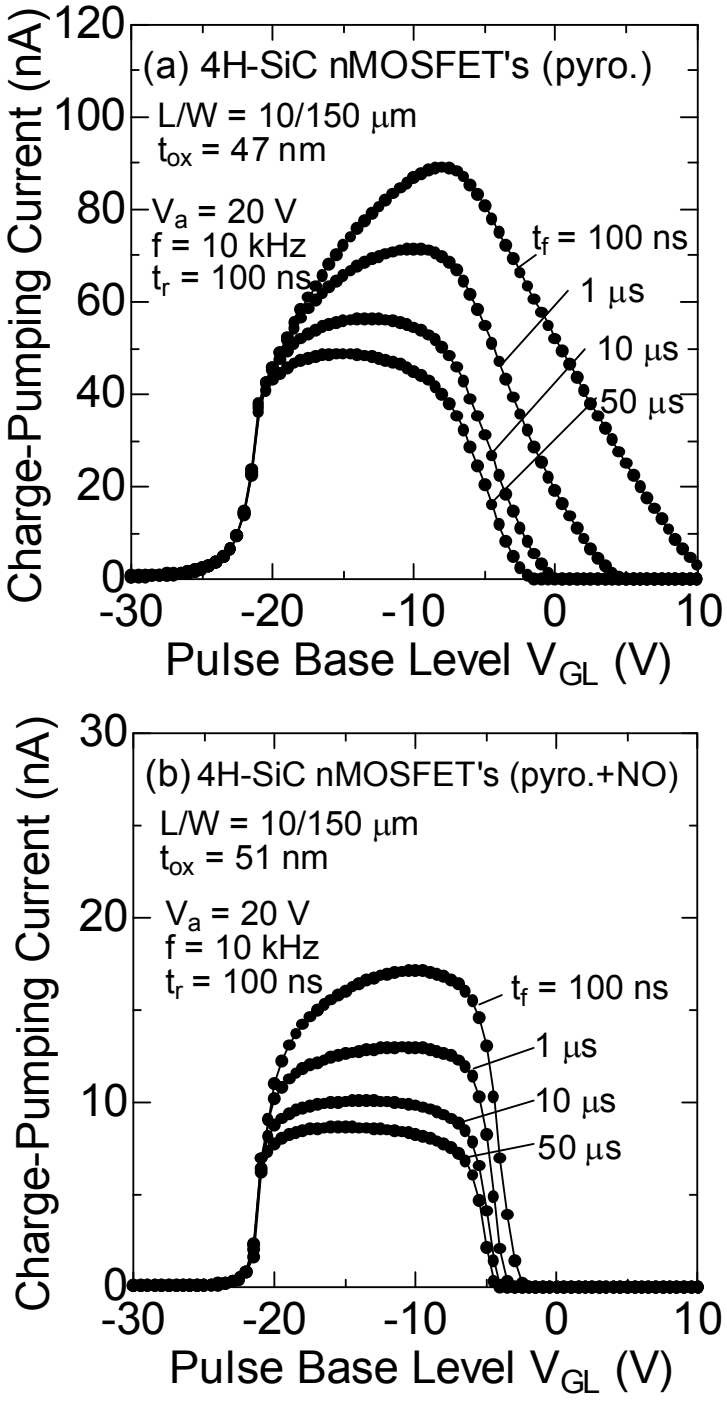


Fig. 5.6. Pulse-fall-time dependence of base-voltage sweep charge-pumping curves for (a) unannealed n-channel 4H-SiC MOSFETs and (b) NO-annealed 4H-SiC n-channel MOSFETs with gate length L = 10 μm and gate width W = 150 μm. Pulse amplitude V_a = 20 V, pulse frequency f = 10 kHz, and pulse rise time t_r = 100 ns.

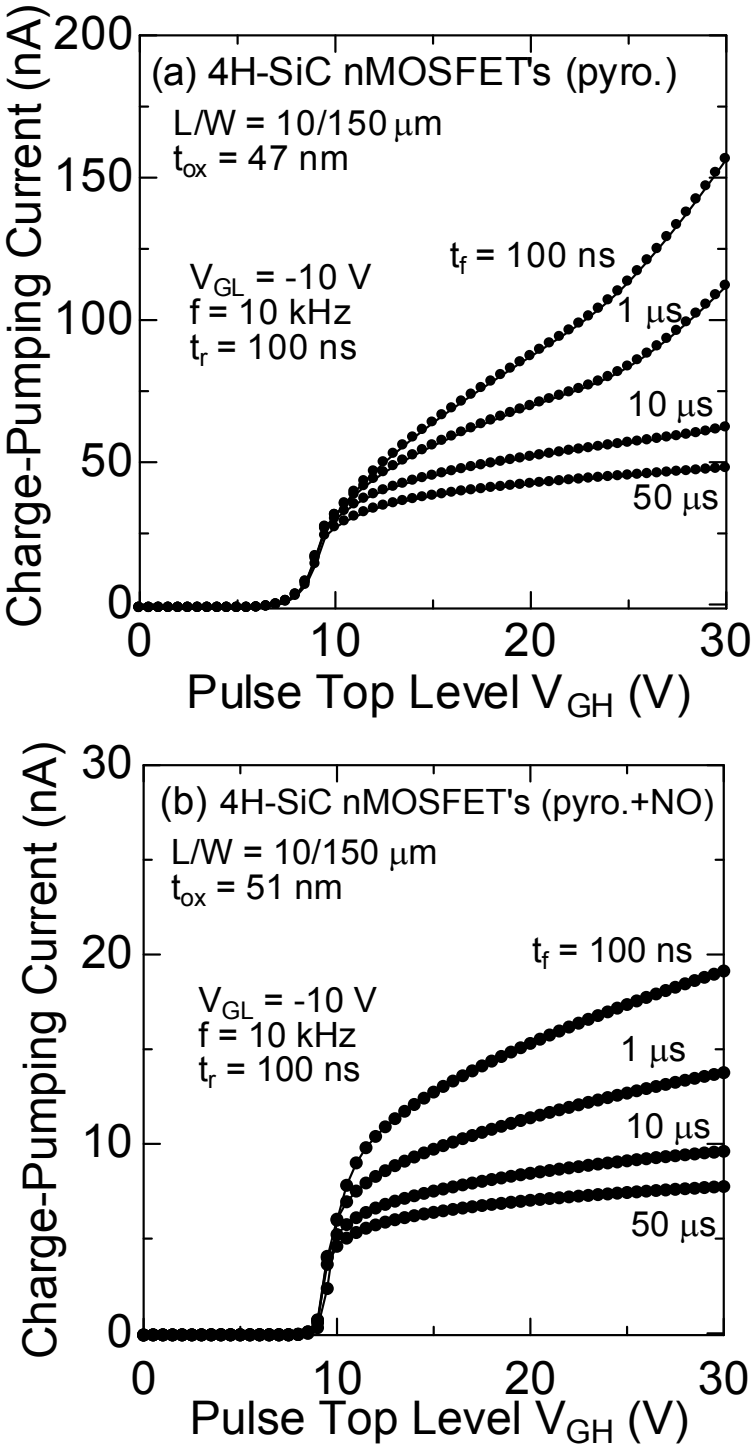


Fig. 5.7. Pulse-fall-time dependence of amplitude-sweep charge-pumping curves for (a) unannealed n-channel 4H-SiC MOSFETs and (b) NO-annealed 4H-SiC n-channel MOSFETs with a gate length L = 10 μm, and gate width W = 150 μm. Pulse base level V_{GL} is fixed at –10 V. Pulse frequency f = 10 kHz, and pulse rise time t_r = 100 ns.

These results imply that there exists a large geometric component in the charge-pumping curves of 4H-SiC MOSFETs. The geometric component is an additional current component, which arises when some electrons cannot reach the source or drain region during the inversion to accumulation transition, and therefore, these electrons recombine with holes flowing from the substrate [6, 8, 12]. When the pulse fall time t_f is adequate, the channel electrons can reach the source or drain region before incoming holes, and therefore, reduce the geometric component in the curve. If the gate length is long, the geometric component increases because only a few channel electrons will be able to reach the source and drain region. The effect of the geometric component is smaller in the NO-annealed 4H-SiC MOSFETs, because the interface state density near the conduction band edge is smaller [13, 14], and the channel mobility is higher, compared to unannealed MOSFETs.

In both base- and amplitude-sweep measurements with fixed fall time of 100 ns, the curves are almost independent of the pulse rise time between 100 ns and 50 μs (not shown). If the hole removal process is impeded by substrate resistance, the curve strongly depends on pulse rise time [15]. Therefore, the geometric component exists primarily because of the low channel mobility of SiC MOSFETs rather than the substrate resistance.

Although the geometric component for SiC MOSFETs was identified in a study of light emission from SiC MOS interfaces [16], a detailed study of the geometric component of SiC MOSFETs has not yet been reported. For Si MOSFETs, this undesirable component can be neglected by performing measurements only in short channel MOSFETs ($L < 10$ μm and/or $W/L >> 1$) with standard pulse fall times (100 ns) [8]. However, this criterion is not valid for SiC MOSFETs because of the small channel

mobility. Unfortunately, some SiC MOS investigators do not care the presence of the geometric component, and consequently, their results may include errors because of overestimation.

5.4 Influence of interface states

The influence of donor-like interface states on the charge-pumping curve has been discussed in a previous study [9]. Although this effect is small for Si charge-pumping measurements, it poses a problem for SiC charge-pumping measurement, because SiC MOS interface consists of both acceptor- and donor-like interface states at high densities. In the case of SiC, both donor- and acceptor-like interface states should be considered with introducing neutrality level E_N that divides the acceptor- and donor-like interface states. It is generally accepted that acceptor-like interface states are located in the upper part of the band-gap, and donor-like interface states occupy the remaining parts of the band-gap, as illustrated in Fig. 5.8 [17, 18].

In charge-pumping measurements, the threshold and flatband voltages are continuously varied by repetitive charging and discharging of interface states [9]. Therefore, the edge of the charge-pumping curves is spread, as illustrated in Fig. 5.9, where the dashed line indicates the ideal charge-pumping curve where all interface states are assumed to be neutral, and the solid line indicates the spread curve. The ideal threshold and flat-band voltages are denoted as V_T and V_{FB}, respectively. The negatively shifted flat-band and threshold voltages due to positively charged donor-like interface states are denoted as V_T' and V_{FB}', respectively. The positively shifted flat-band and threshold voltages due to negatively charged acceptor-like interface states are denoted as V_T'' and V_{FB}'', respectively. When the MOSFET channel is in the accumulation

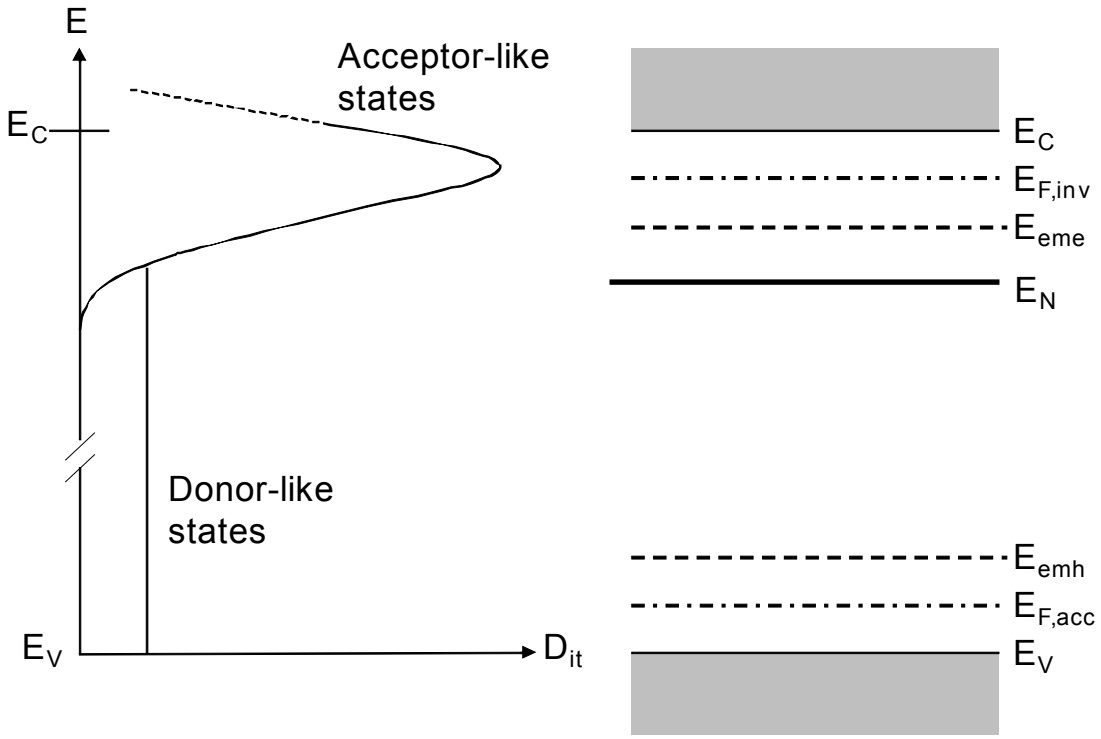


Fig. 5.8. Schematic illustration of the distribution of interface state density and band diagram.

condition, the charge state of the interface states above the Fermi level for accumulation $E_{F,acc}$ is positive, because donor-like interface states are filled with holes. Thus, the flatband voltage shifts to V_{FB}' in Fig. 5.9 because of the positively charged donor-like interface states between E_N and $E_{F,acc}$ in Fig. 5.8. When the gate voltage increases toward inversion, holes trapped below the energy level E_{emh} are thermally emitted to the valence band. When the electrons begin to flow into the channel region, the threshold voltage is V_T' because of the positively charged interface states between E_N and E_{emh}. After the recombination of the inflowing electrons and remaining holes in the interface states, the threshold voltage shifts to V_T'' because of the negatively charged acceptor-like interface states between the Fermi level for inversion $E_{F,inv}$ and E_N. During the inversion to accumulation transition, electrons trapped above the energy level E_{emh}

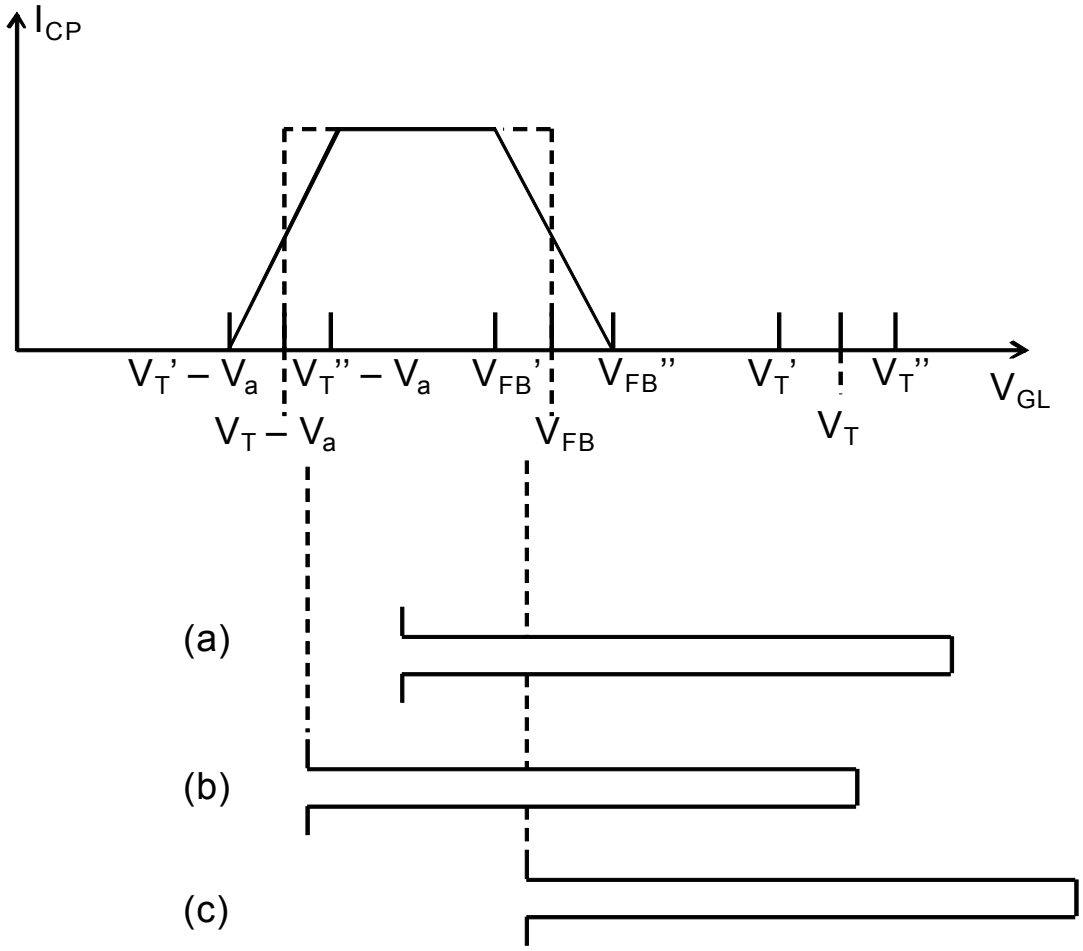


Fig. 5.9. Influence of interface states on charge-pumping curves for n-channel MOSFETs, assuming both donor- and acceptor-like interface states.

are thermally emitted to the conduction band. When the holes begin to flow into the channel region, the flat-band voltage is V_{FB}'', because of the negatively charged interface states between E_{eme} and E_N. When the applied pulse is pulse (a) in Fig. 5.9, full charge-pumping current is measured. However, in the case of pulse (b) in Fig. 5.9, the pulse top level can reach V_T', but not V_T''. As a result, the recombination becomes partial, and the charge-pumping current decreases, because of the voltage shift from V_T' to V_T'' during the accumulation to inversion transition. Likewise, in the case of pulse (c)

in Fig. 5.9, the recombination process ends because of a lack of incoming holes. Consequently, the left- and right-side edges of the charge-pumping curves are expected to be spread, as indicated by the solid line in Fig. 5.9.

For n-channel 4H-SiC MOSFET's without NO annealing, the spread is expected to be significant in both the left- and right-side edges of the curve, because a larger number of acceptor-like interface states exist near the conduction band edge. As shown in Fig. 5.6, the left- and right-side edges of the charge-pumping curves are rounded for unannealed 4H-SiC n-channel MOSFETs, whereas the edges are relatively sharp for NO-annealed 4H-SiC n-channel MOSFETs.

5.5 Criteria for accurate charge-pumping measurement

To minimize the effect of geometric component, it is important to choose a sufficiently long fall time. The pulse fall time needed to minimize its effect was calculated using a model that is based on the theory of charge-coupled devices (CCDs) [12]. This calculation has been shown to be valid for Si MOSFETs and provides a good approximation because channel charge removal process of charge-pumping measurement is similar to the charge transport process of CCDs [12]. Based on the theory, the critical transition time (time required to reduce the density of surface electrons from 10^{13} to 10^{9} cm^{-2}) was calculated for various channel mobilities and lengths. The results, shown in Fig. 5.10, clearly indicate that the critical time is strongly dependent on gate length and channel mobility.

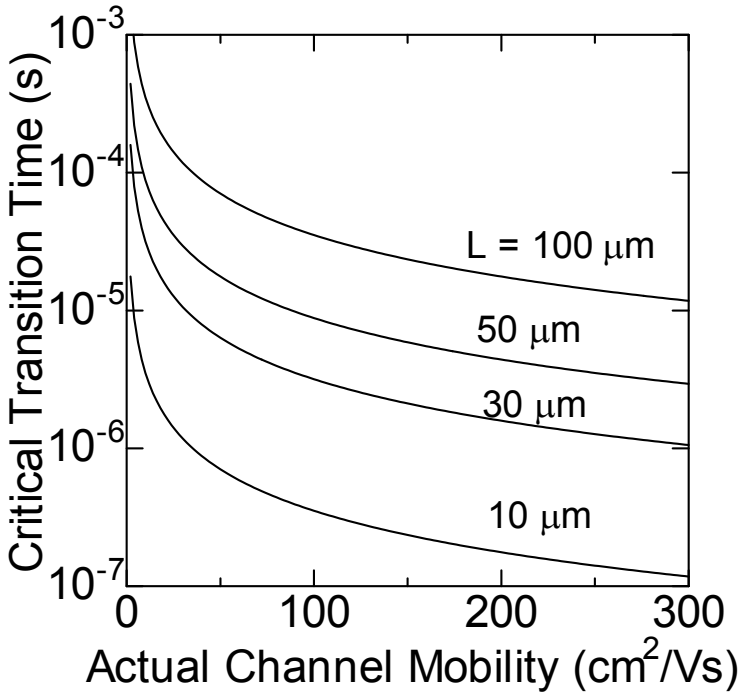


Fig. 5.10. Calculated critical transition time as a function of *actual* channel mobility for gate lengths of 10, 30, 50, and 100 μm. The critical transition time is defined as the time required to reduce the density of channel electrons from 10^{13} to 10^{9} cm^{-2}.

Note that *actual* inversion channel mobility differs from the field-effect mobility, calculated using transconductance. The field-effect mobility of the 4H-SiC MOSFETs is lower than their *actual* mobility, estimated by the Hall-effect measurement, because of a reduction in the free electron density caused by electron trapping [19]. The channel mobility can be assumed to be 30 and 60 cm^2/Vs for the unannealed and NO-annealed 4H-SiC MOSFETs, respectively, which is derived from the reported *actual* channel mobility measured using MOS-gated Hall bar structures [20, 21]. Subsequently, from Fig. 5.10, the critical transition times can be estimated to be 1.2 and 0.6 μs.

The transition time during which electrons can migrate back to the source/drain region without recombination is given by

$$t_{\mathrm{trans,n}} = \frac{\left|V_{\mathrm{GH}} - V''_{\mathrm{FB}}\right|}{\left|V_{\mathrm{GH}} - V_{\mathrm{GL}}\right|} \cdot t_{\mathrm{f}} , \tag{5.5}$$

because holes are supplied when the gate voltage is below the shifted flatband voltage (V_{FB}''). As mentioned, V_{FB}'' is shifted positively because of negatively charged acceptor-like interface states. Although accurate determination of V_{FB}'' from the measured charge-pumping data is difficult, it can be roughly estimated from Fig. 4 to be approximately −1 V for unannealed 4H-SiC MOSFETs, and −4 V for NO-annealed 4H-SiC MOSFETs. Assuming V_{GH} = 5 V and V_{GL} = −15 V, and using Eq. (5.5), the critical pulse fall time is estimated at approximately 4 μs for unannealed 4H-SiC MOSFETs and 1 μs for NO-annealed 4H-SiC MOSFETs with a gate length of 10 μm. Although this is a rough estimation, a pulse fall time of 100 ns, which is commonly used in square-pulse charge-pumping measurement of Si MOSFETs, is insufficient to remove the channel electrons for SiC MOSFETs.

Although charge-pumping current seems to satisfactorily saturate with a longer pulse fall time, the current increases slightly with pulse amplitude, as shown in Fig. 5.7 (a) and (b). This slight increase in current was also observed in the Si MOSFETs. This increase is because of the change in scanning energy interval, which depends on pulse amplitude [8]. As the pulse amplitude increases, the scanning energy range slightly approaches the conduction band edge (E_{c}), where the interface state density is higher. Therefore, the charge-pumping current increases slightly with pulse amplitude, and perfect horizontal lines cannot be obtained.

The scanning energy interval (ΔE) in the charge-pumping measurement depends on the pulse rise and fall times [8]. The scanning energy interval for 4H-SiC MOSFETs is shown in Fig. 5.11. The energy difference $|E_{\mathrm{eme}}(t_{\mathrm{f}}) - E_{\mathrm{emh}}(t_{\mathrm{r}})|$ corresponds to the

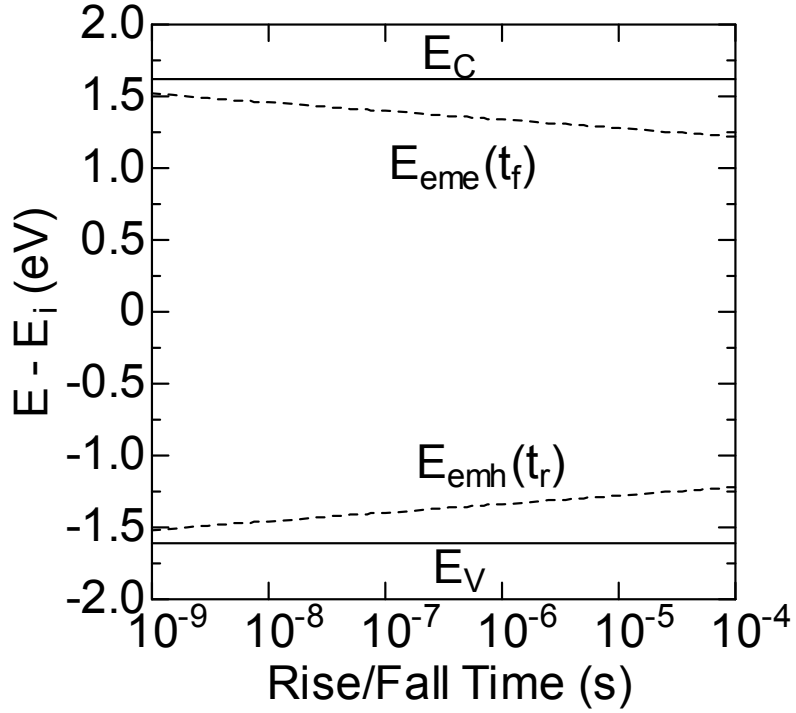


Fig. 5.11. Scannable energy interval for 4H-SiC MOSFETs as a function of pulse rise and fall times. Conduction and valence band edge are shown by solid lines. Dashed lines represent the energy level reached at the end of hole and electron emission. The energy difference $|E_{eme}(t_f) - E_{emh}(t_r)|$ corresponds to the scanning energy range ΔE.

scanning energy range in the charge-pumping measurements. To avoid the geometric component, a pulse fall time of 10 μs was chosen. From the peak value of the base-sweep charge-pumping curve, measured with pulse rise and fall times of 100 ns and 10 μs, respectively, mean interface state densities were estimated to be 7.1×10^{11} and 1.3×10^{11} $cm^{-2}eV^{-1}$ for the unannealed and NO-annealed n-channel 4H-SiC MOSFETs, respectively. In this case, scanning energy range is between 0.36 eV below the conduction band edge, and 0.24 eV above the valence band edge. It is difficult to scan the interface states close to the conduction band edge of the unannealed 4H-SiC n-channel MOSFETs as a short pulse fall time cannot be used because of the geometric

component.

There are constraints on the measurable energy range because of the geometric component. However, the charge-pumping technique can characterize the interface states closer to the conduction band edge by using MOSFETs with higher channel mobility and shorter gate length.

5.6 Application of charge-pumping method to phosphorus-doped gate oxide

In this section, the charge-pumping method is applied to the $POCl_3$-annealed MOSFETs described in Chapter 3. The charge-pumping method becomes useful tool to evaluate the MOSFETs with high channel mobility because the less geometric component is expected. In addition, the evaluation using hi-lo *C*–*V* method becomes difficult when the D_{it} is less than 1×10^{11} $cm^{-2}eV^{-1}$.

Charge-pumping measurement was conducted on the 4H-SiC MOSFETs fabricated by $POCl_3$ annealing at 1000 °C. The fabrication of the MOSFETs was described in Chapter 3. Figure 5.12 shows the pulse-fall-time dependence of base-voltage sweep charge-pumping curves for the $POCl_3$-annealed 4H-SiC MOSFETs with different gate lengths. It can be found that the pulse-fall-time dependence was absent for the $POCl_3$-annealed MOSFET with L = 10 mm. This indicates that the geometric component is negligible for the $POCl_3$-annealed MOSFETs with short gate length because of the high channel mobility. With increasing the gate length, the right side of the charge-pumping curves becomes distorted due to the geometric component. The tail on the right hand side of the charge-pumping curve becomes large for the gate length of

above 50 μm. Figure 5.13 shows the mean values of D_{it} as a function of gate length. In the case of t_f = 100 ns, the estimated values significantly deviate from the dashed line, indicating the large contribution of geometric component. Unfortunately, it is difficult to predict the critical pulse-fall time because *actual* channel mobility has not been reported for the $POCl_3$-annealed MOSFETs. In order to know the *actual* channel mobility, Hall-effect measurement using using MOS-gated Hall bar structures [20, 21], but this experiment is very difficult. Further study is needed to investigate the critical time. Nevertheless, the results described here clearly indicate that the geometric component becomes small for the MOSFETs with high channel mobility. The mean value of interface state density for the $POCl_3$-annealed MOSFET with L = 10 μm is 9.4×10^{11} $cm^{-2}eV^{-1}$ which is higher than those of unannealed and NO-annealed MOSFETs. This means that high density of interface states was generated in the lower part of the 4H-SiC bandgap by $POCl_3$ annealing although the D_{it} near the conduction band edge (E_c) was significantly reduced. Most part of D_{it} in the bandgap can be scanned by the charge-pumping method, where as the conventional *C–V* method only scans the upper part of the bandgap (see Section 2.3). The generated interface states do not affect the electrical properties of MOSFETs because the interface states in the lower part of the bandgap is donor-like traps [18] which do not capture channel electrons. The generated D_{it} in the lower part of the bandgap may be due to the disordered oxide network due to the incorporated P atoms. However, the mechanism is unclear at present and further study is needed. The charge-pumping method enables diversified analysis of D_{it} distributed in the bandgap, and would be a useful method for the characterization of MOSFETs.

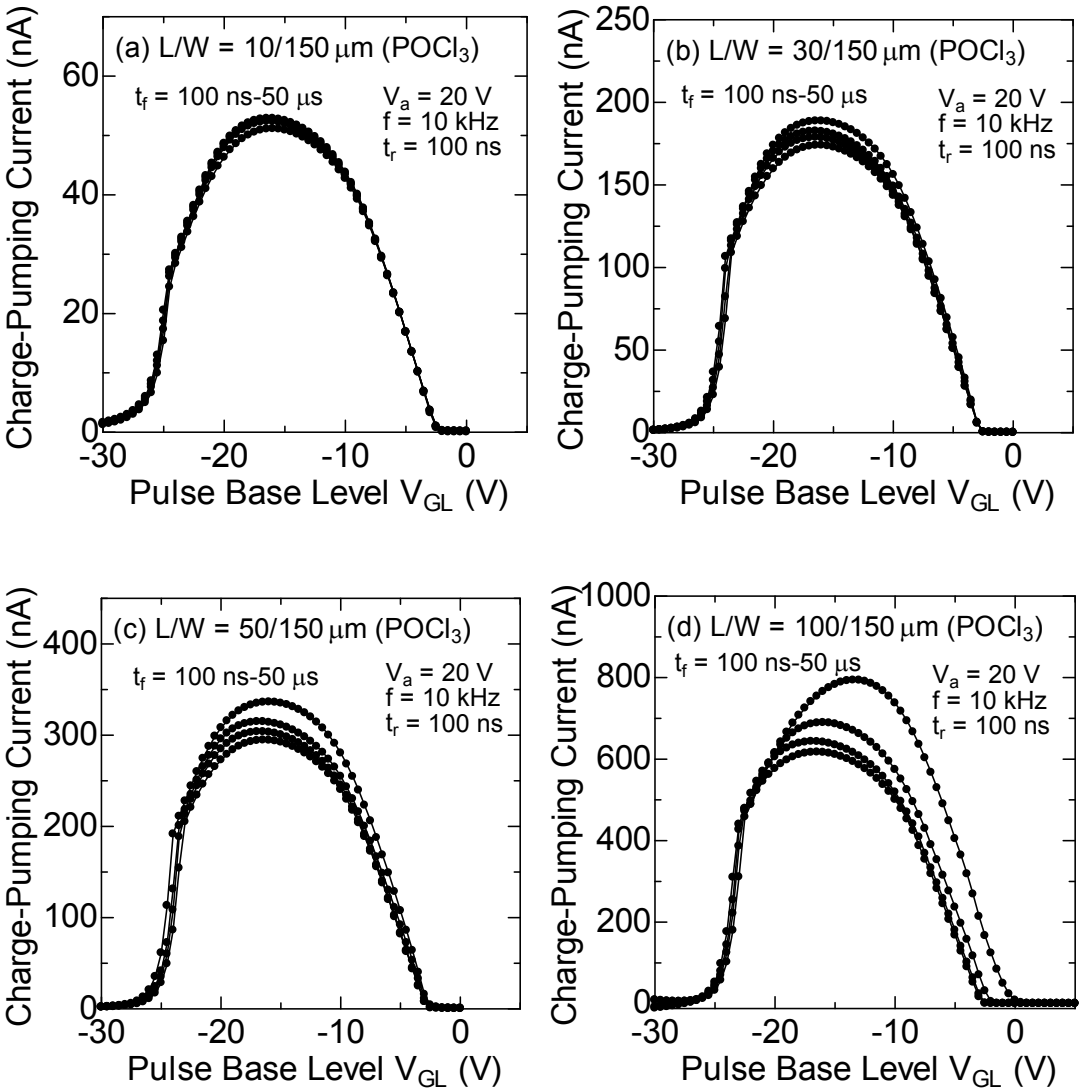


Fig. 5.12. Pulse-fall-time dependence of base-voltage sweep charge-pumping curves for $POCl_3$-annealed 4H-SiC MOSFETs with gate length L = 10, 30, 50, 100 μm and gate width W = 150 μm. Pulse amplitude V_a = 20 V, pulse frequency f = 10 kHz, and pulse rise time t_r = 100 ns.

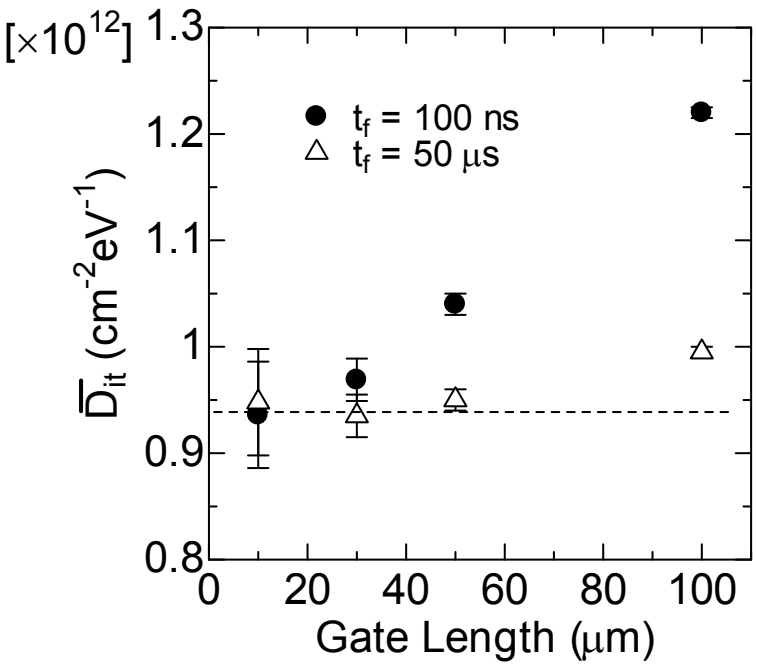


Fig. 5.13. Estimated mean interface state density as a function of gate length.

5.7 Summary

Charge-pumping measurements were performed on 4H-SiC MOSFETs, and the distorted shape of the charge-pumping curves was discussed. This distortion of the charge-pumping curves occurs because of the geometric component and acceptor-like interface states. These two effects are especially large in unannealed n-channel 4H-SiC MOSFETs with low channel mobility. However, the geometric component is negligible for the $POCl_3$-annealed MOSFETs with short gate length because of the high channel mobility. The geometric component in SiC MOSFETs arises easily, and therefore, it must be considered carefully in the measurements. Charge-pumping measurement can be made a useful and reliable tool using a sufficiently long pulse fall-time for interface state characterization of SiC MOSFETs.

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Chapter 6
Investigation of SiO_2/4H-SiC Interfaces Formed on C-face Substrates

6.1 Introduction

The results described from Chapter 2 to 5 were focused on the (0001) Si-face, the most basic crystal face of 4H-SiC. However, it is well known that the channel mobility of 4H-SiC MOSFETs depends strongly on the crystal face and oxidation process. $(000\bar{1})$ C-face is another suitable crystal face for fabricating double-implanted MOS (DMOS) devices because high inversion channel mobility [1], high field strength [2], and high oxidation rate [3] have been reported. Fukuda *et al*. reported that the interface state density in 4H-SiC MOS structures fabricated on C-face can be reduced and the peak field-effect mobility of C-face MOSFETs can be greater than 110 cm^2/Vs by pyrogenic oxidation followed by post-oxidation annealing in hydrogen at a high temperature [1, 4].

Another effective way to passivate interface traps and improve MOSFET performance is oxidation or post-oxidation annealing in a nitrogen-containing atmosphere [5, 6]. Post-oxidation annealing or direct oxidation with gaseous NO or N_2O on C-face 4H-SiC is also of particular interest because good interface quality with reduced interface state density have been reported [7, 8]. Time-dependent dielectric breakdown (TDDB) characteristics are also improved in the N_2O-grown 4H-SiC MOS structure on C-face [9]. The reported channel mobility of MOSFETs fabricated by direct oxidation of C-face 4H-SiC in N_2O is about 45 cm^2/Vs [8]. However, there are only a

few studies on the properties of nitrided 4H-SiC MOS interface on C-face substrates. Therefore, to investigate the interface properties of nitrtided 4H-SiC MOS structures on C-face is important.

On the other hand, the incorporation of phosphorus is demonstrated to be very effective to improve the interface properties of 4H-SiC MOS structures on Si-face, as described from Chapter 2 to 5. Similar to the Si-face, it is expected that the channel mobility of 4H-SiC MOSFETs fabricated on C-face can be improved by $POCl_3$ annealing.

In this chapter, the effect of two different oxidation techniques, NO direct oxidation and $POCl_3$ post oxidation annealing, on C-face MOS interface was investigated. Fabricated devices on C-face showed different characterisctics from those on Si-face. Based on the obtained results, the difference of interface properties on Si-face and C-face is discussed.

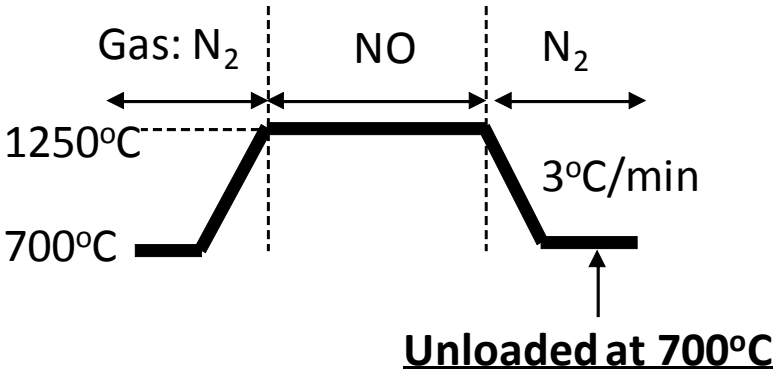
6.2 Investigation of oxide films prepared by direct oxidation of C-face 4H-SiC in nitric oxide

The aim of this section is to clarify the interface properties of 4H-SiC MOS structures with nitrided gate oxides on C-face. Characteristics of MOS capacitors and MOSFETs fabricated by direct oxidation of C-face 4H-SiC in NO have been investigated with *cycle* capacitance–voltage (*C–V*) technique [10] and other electrical measurements.

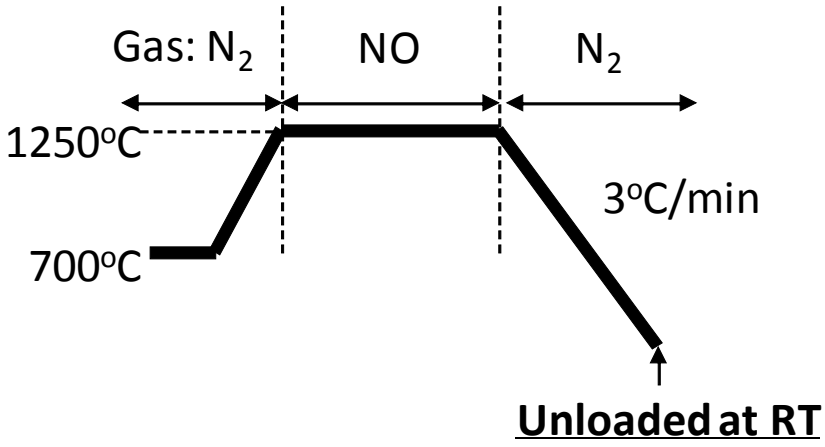
6.2.1 Device fabrication

N-type, 8°-off 4H-SiC (000$\bar{1}$) C-face epilayers with a net donor concentration of 1 × 10^{16} cm^{-3} were used to fabricate MOS capacitors. After the standard Radio Corporation of America (RCA) cleaning, gate oxides were formed by oxidation in pure oxygen at 1250 °C for 15 min (denoted as Dry-700) or in pure NO at 1250 °C for 90 min (denoted as NO-700). After the oxidation, these two samples were cooled in N_2 with a ramping rate of –3 °C/min, and unloaded at 700 °C. Another oxide was formed by oxidation in pure NO at 1250 °C for 90 min and the sample was unloaded at room temperature (denoted as NO-RT) as shown in Fig. 6.1. The oxide thickness estimated from the accumulation capacitance of high-frequency *C–V* curves was approximately 60 nm for all samples. Al was evaporated to form gate and backside electrodes. Post-metallization annealing was performed in forming gas at 400 °C for 30 min. High-frequency (100 kHz) *C–V* curves were measured using Agilent 4284A or E4980A precision LCR meters. Quasistatic *C–V* measurements were performed using a Keithley model 595 quasistatic *C–V* meter.

N-channel planar MOSFETs were fabricated on p-type, 4°-off 4H-SiC(000$\bar{1}$) C-face epilayers with a net acceptor concentration of 8 × 10^{15} cm^{-3}. P^+ and Al^+ ions were appropriately implanted and activated for source/drain and body contacts, respectively. The oxidation process is the same as the processes described above. Al was deposited to form gate, source, drain, and body electrodes. Post-metallization annealing was performed in forming gas at 400 °C for 30 min. High-temperature contact annealing was not performed. The channel length (L) and width (W) were 100 and 150 μm, respectively. Electrical properties of the MOSFETs were measured using a Keithley 4200 semiconductor characterization system. All electrical measurements were carried out at room temperature under dark conditions.



(a) NO-700 sample



(b) NO-RT sample

Fig. 6.1. Temperature profiles of NO direct oxidation. The samples are unloaded at 700 °C ((a) NO-700 sample) and room temperature ((b) NO-RT sample).

6.2.2 Properties of fabricated devices

The start voltage dependence of high-frequency *C–V* curves was measured at room temperature to investigate the interfacial traps that have a long time constant (*cycle C–V* measurements) [10]. Figure 6.2 shows the start voltage dependence of high-frequency *C–V* curves of a MOS capacitor fabricated with the NO-700 process. In this measurement, gate voltage was swept from accumulation to depletion, and the start

voltage was increased from 2 to 18 V with a 2-V step, and *C–V* curves were repeatedly measured [10]. With increasing the start voltage, a positive and parallel shift of the *C–V* curves was observed, showing that effective negative fixed charges increase with increasing the start voltage. This result indicates that the electrons in the accumulation layer are captured by traps with a long time constant and are not thermally emitted even at room temperature during the measurement. Once electrons are captured by these traps, the original curve is no longer obtainable. The original curves can be obtained again by illuminating the capacitor with ultraviolet light. Hijikata *et al*. reported that similar start voltage dependence was observed in Si-face 4H-SiC MOS capacitors oxidized in dry oxygen and quenched to room temperature [10]. In their results, the positive shift of *C–V* curves occurred in deep-depletion regions; and they considered that a large number of acceptor-like deep interface states exist around the energy level corresponding to the capacitance in deep depletion [10]. In contrast, the obtained result indicates that the positive shift occurs between capacitances in flatband and accumulation regions where the acceptor-like deep interface states are filled with electrons. Therefore, it can be said that the electrons are captured by the near-interface traps (NITs) in the oxide, which also have a long time constant [11, 12]. The start voltage dependence of *C–V* curves for 4H-SiC MOS capacitors fabricated on (0001) Si-face with annealing in NO is negligibly small (not shown). In addition, for the Si-face, such shift can be observed only at low temperatures as described in Chapter 4. Therefore, the energy position of NITs is thought to be deeper than that of Si-face; the details are discussed in Section 6.5.

Figure 6.3 shows the relationship between the start voltage (V_{start}) and the flatband voltage shift (ΔV_{FB}) for C-face 4H-SiC MOS capacitors fabricated with the Dry-700, NO-700 and NO-RT processes. ΔV_{FB} was estimated from the difference between the

measured and the theoretical flatband voltages. This comparison reflects the increase in effective negative fixed charges at the interface because all three samples have almost the same oxide thickness. The slopes of the Dry-700 and NO-RT samples are almost the same, whereas the slope of the NO-700 sample is steeper than those of other samples. This means that the electrons are more easily captured by the *deep* NITs in the NO-700 sample. It is also apparent that electron trapping in the gate oxide was greatly suppressed by unloading the sample at room temperature after direct oxidation in NO.

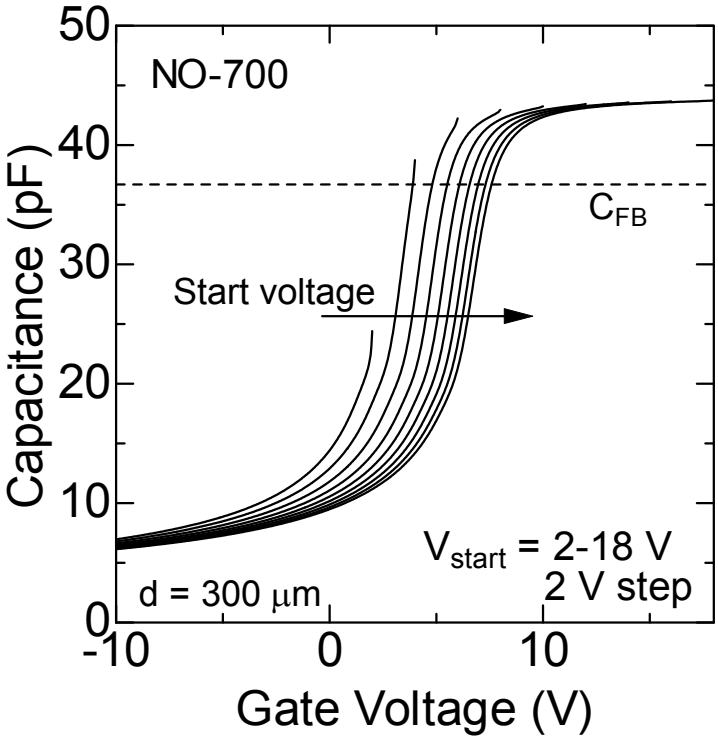


Fig. 6.2. Start voltage dependence of high-frequency *C–V* curves for a C-face 4H-SiC MOS capacitor fabricated by the NO-700 process. Diameter of the circular gate electrode is 300 μm. The gate voltage was swept from accumulation to depletion. The start voltage was increased from 2 to 18 V with a 2-V step.

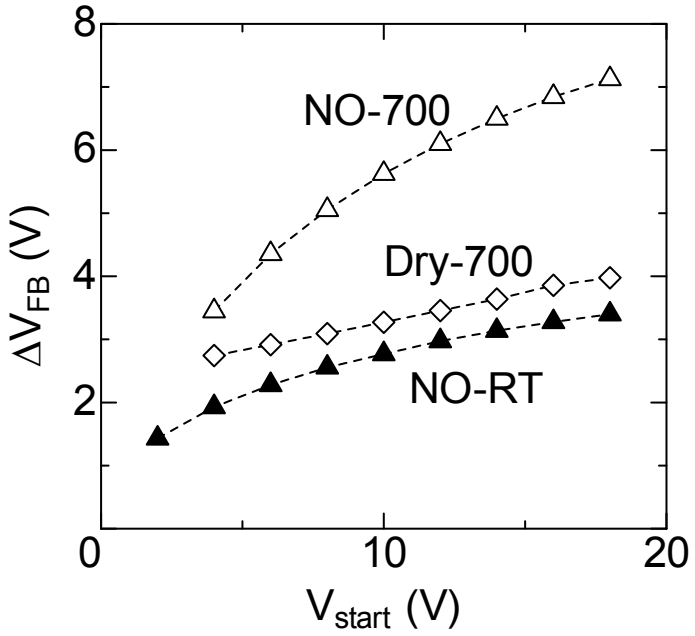


Fig. 6.3. Relationship between start voltage (V_{start}) and flatband voltage shift (ΔV_{FB}) in high-frequency *C–V* measurements for C-face 4H-SiC MOS capacitors fabricated by the Dry-700, NO-700 and NO-RT processes.

Figure 6.4 shows the high-frequency (100 kHz) and quasi-static *C–V* curves of C-face 4H-SiC MOS capacitors fabricated by the Dry-700, NO-700 and NO-RT processes. The difference in high and quasistatic curves is smaller for the NO-700 and NO-RT samples, indicating smaller D_{it} values. Figure 6.5 shows the distribution of interface state density (D_{it}) at energies near the conduction band edge determined by the hi-lo *C–V* method. This method can detect only the interface states which have a short time constant, because the near-interface traps are filled with electrons during the measurement. The value of D_{it} near the conduction band edge for the NO-700 sample is lower than that of the Dry-700 sample, although the shift in the cycle *C–V* characteristics is larger. Thus, the interface states with a short time constant are reduced by the incorporation of nitrogen while deep NITs are generated. Both the interface states and the deep NITs can be reduced by unloading the samples at room temperature.

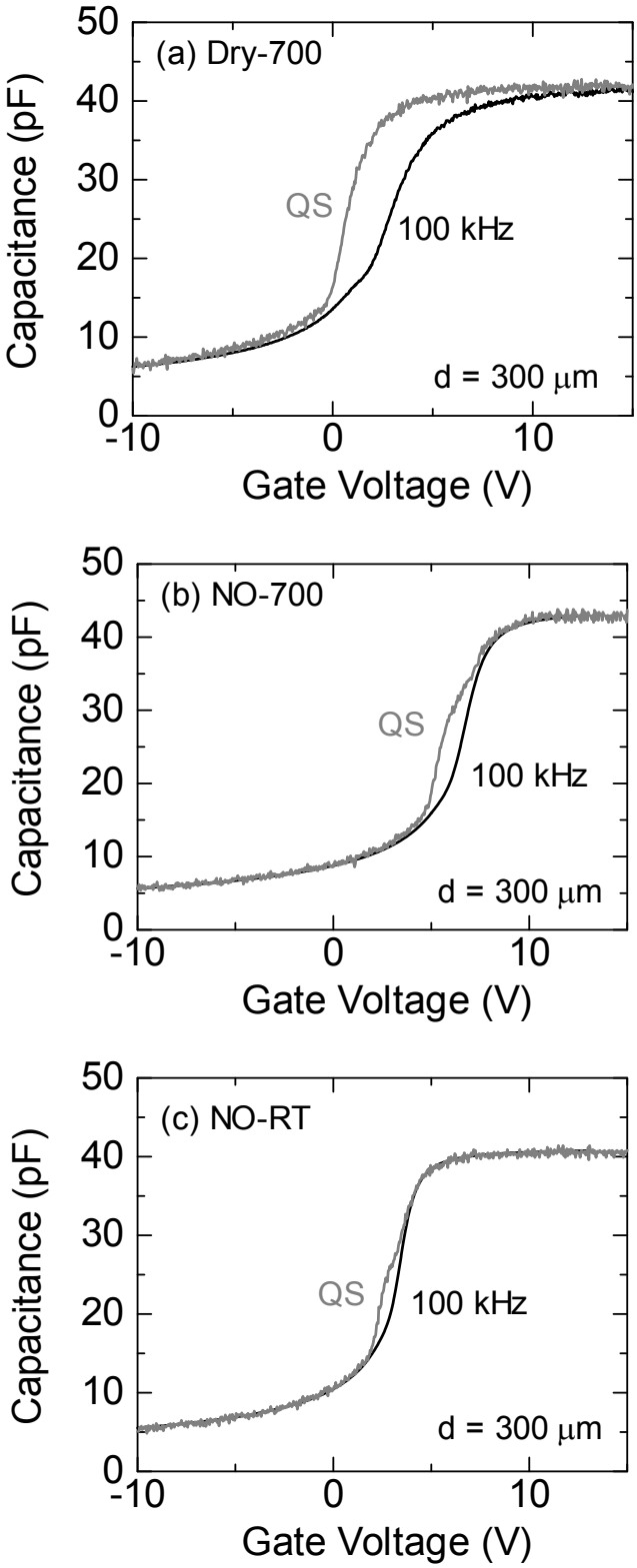


Fig. 6.4. high-frequency (100 kHz) and quasi-static *C–V* curves of C-face 4H-SiC MOS capacitors fabricated by the (a) Dry-700, (b) NO-700 and (c) NO-RT processes.

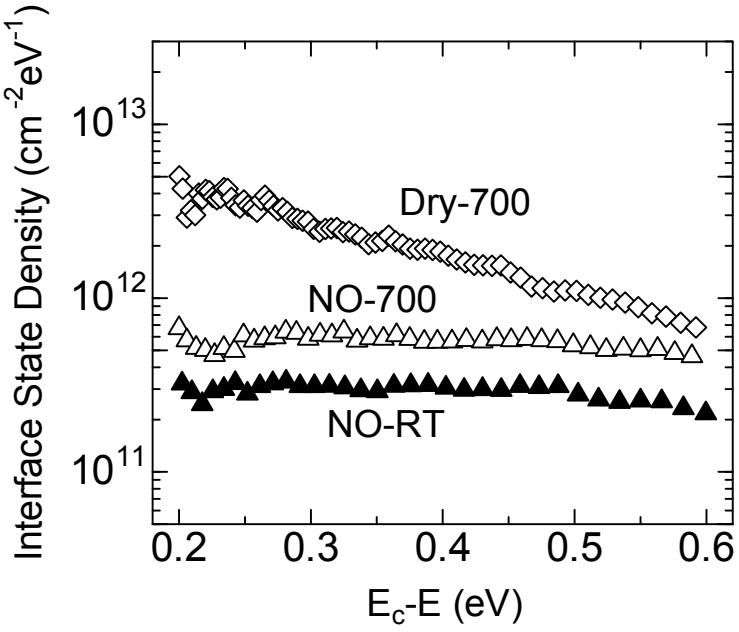


Fig. 6.5. Distribution of interface state density near the conduction band edge of C-face 4H-SiC MOS capacitors fabricated by the Dry-700, NO-700 and NO-RT processes.

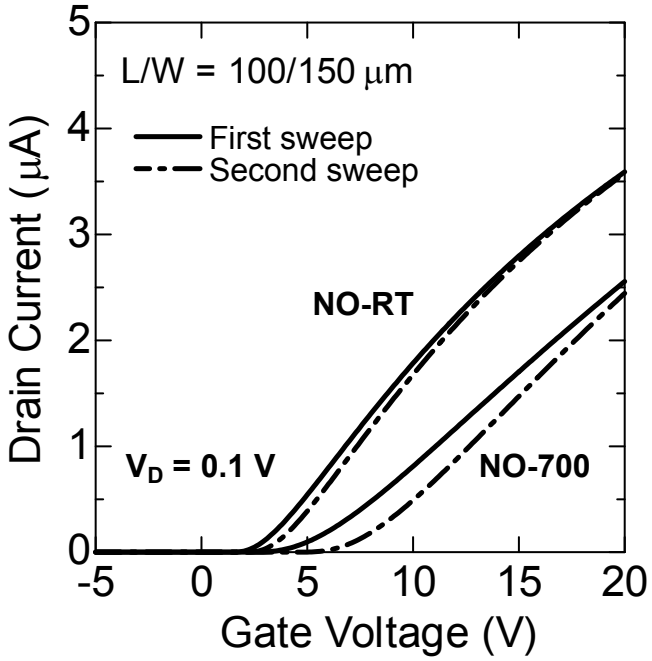


Fig. 6.6. I_D–V_G characteristics at V_D = 0.1 V for C-face 4H-SiC MOSFETs fabricated by the NO-700 and NO-RT processes. The solid line shows the first sweep and the dashed line shows the second sweep.

Figure 6.6 shows drain current–gate voltage (I_D–V_G) characteristics at a drain voltage (V_D) of 0.1 V for 4H-SiC MOSFETs fabricated with the NO-700 and NO-RT processes. The gate voltage was swept from negative to positive. In the second sweep, the I_D–V_G curves show a positive shift, although the measurement condition is the same as the first sweep. The threshold voltages, determined by the linear extrapolation of I_D–V_G curves to zero, increased from 5.5 to 7.6 V for the NO-700 sample and from 2.8 to 3.5 V for the NO-RT sample, respectively. The larger increment of the threshold voltage for the NO-700 sample (2.1 V) compared to that of the NO-RT sample (0.7 V) suggests that more electrons are captured by the near-interface traps in the NO-700 sample. The peak field-effect mobility estimated from the second sweep of I_D–V_G curves in Fig. 6.6 is approximately 22 cm^2/Vs for the sample NO-700 sample and 29 cm^2/Vs for the NO-RT sample as shown in Fig. 6.7. The mobility is lower than 1 cm^2/Vs for the Dry-700 sample (not shown). These results suggest that the channel mobile electrons are captured not only by the interface states but also by the near-interface traps during inversion. Capturing of electrons by these traps leads to a reduction in number of mobile electrons and an increase in Coulomb scattering, resulting in lower channel mobility.

The results described above may be due to the difference in the passivation mechanisms of the Si- and C-face interface states. The oxide layer near the interface is thought to be a transition layer containing C atoms. The structure and chemical-bonding state of the transition layer are different for Si- and C-faces [13, 14]. Therefore, it can be expected that the structure of the transition layer in the nitrided oxide is also different for Si- and C-faces. It is speculated that new traps are generated in the oxide layer near the interface when nitrogen atoms are incorporated in the transition layer. In addition,

stress between nitrided SiO_2 and C-face 4H-SiC may be easily induced by the high reactivity of C-face as expected from, for example, higher oxidation and etching rate in than those of Si-face [3, 15]. Therefore, the deep NITs and interface states may also be generated by the stress due to the abrupt temperature change after the oxide growth. These deep NITs and interface states can be reduced by unloading the samples at room temperature. The quantitative relationship between nitrogen concentration and the density of near-interface traps is currently unclear, and further investigation is needed.

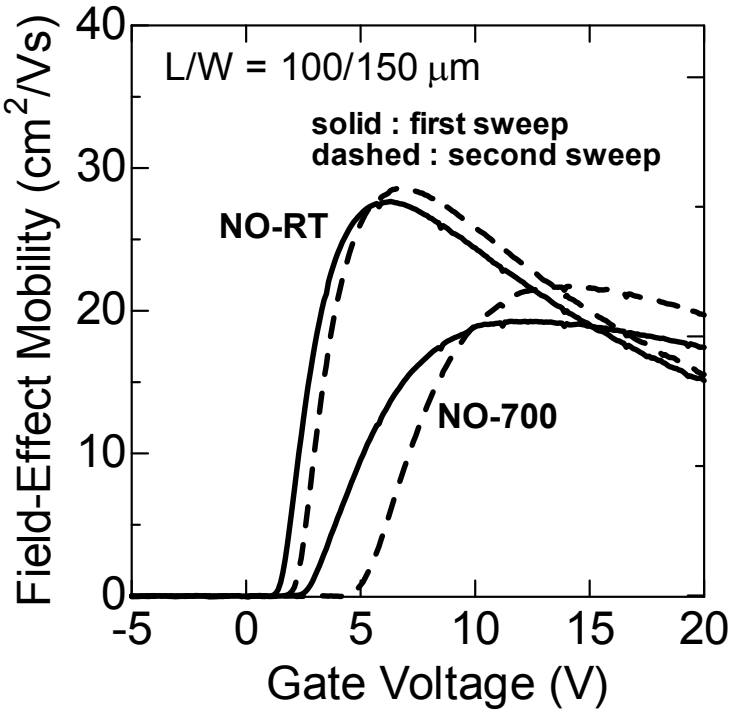


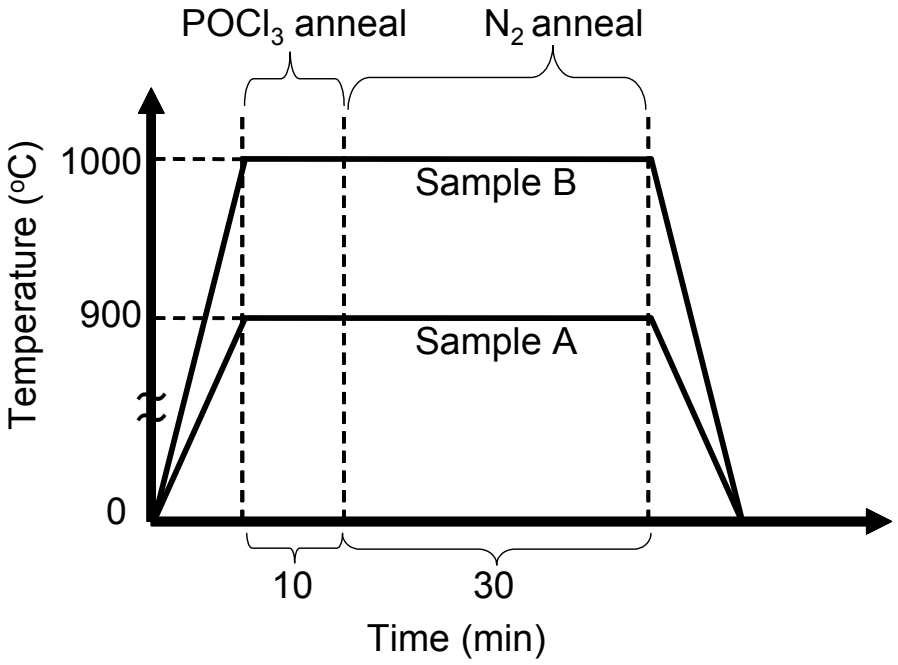
Fig. 6.7. Field-effect mobility of C-face 4H-SiC MOSFETs fabricated by the NO-700 and NO-RT processes.

6.3 Investigation of oxide films prepared by $POCl_3$ annealing of C-face 4H-SiC

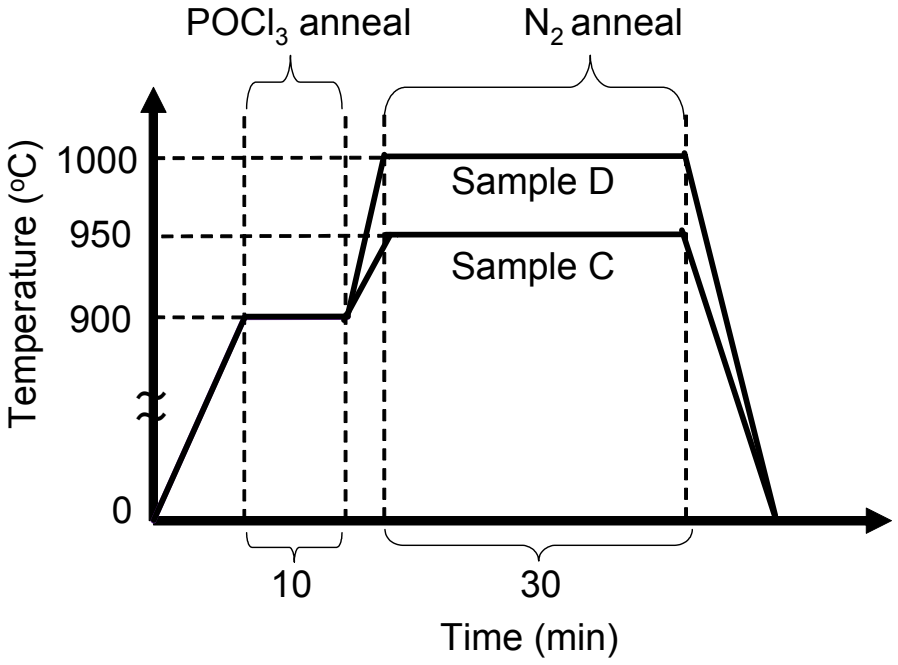
The aim of this section is to investigate the effect of $POCl_3$ annealing on the C-face 4H-SiC MOS interface properties. MOS capacitors and MOSFETs were fabricated on the C-face 4H-SiC by $POCl_3$ annealing. It is described that $POCl_3/N_2$ annealing performed at 1000 °C did not reduce the interface state density (D_{it}) for C-face 4H-SiC MOS structures. Thus, a new process suitable for the C-face MOS structures to introduce phosphorus atoms into the interface is proposed.

6.3.1 Device fabrication

N-type MOS capacitors were fabricated on C-face 4H-SiC epitaxial wafers with a net donor concentration of 8×10^{15} cm^{-3}. Thermal oxides were grown in dry O_2 at 1250 °C for 10 min. The thickness of the oxides was approximately 43 nm. After the dry oxidation, $POCl_3$ annealing was performed at 900 or 1000 °C for 10 min using a gas mixture of $POCl_3$, N_2, and O_2. Subsequently, N_2 annealing was carried out at 900, 950, or 1000 °C for 30 min to diffuse phosphorus atoms into the interface. The temperature profile of $POCl_3/N_2$ annealing is shown in Fig. 6.8. Aluminum was evaporated to form gate electrodes (d = 300 μm) and backside ohmic contacts. The D_{it} was calculated from the hi-lo capacitance–voltage (C–V) method.



(a) Basic temperature profile

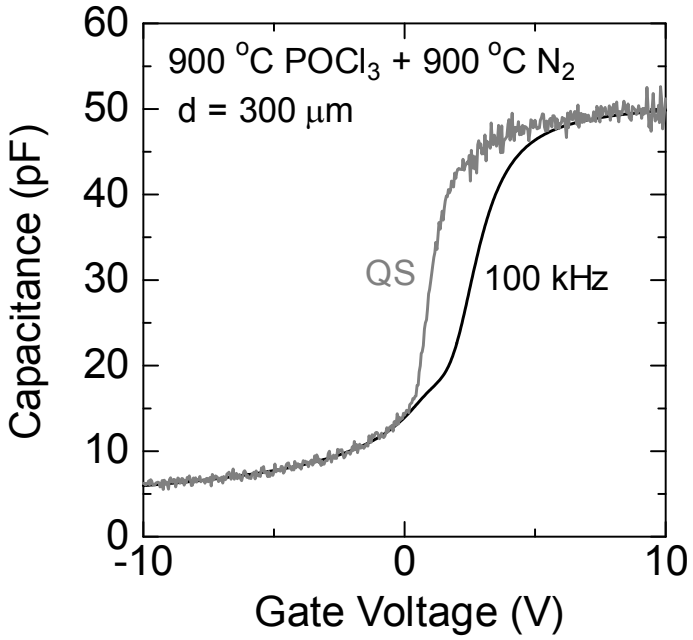


(b) Modified temperature profile

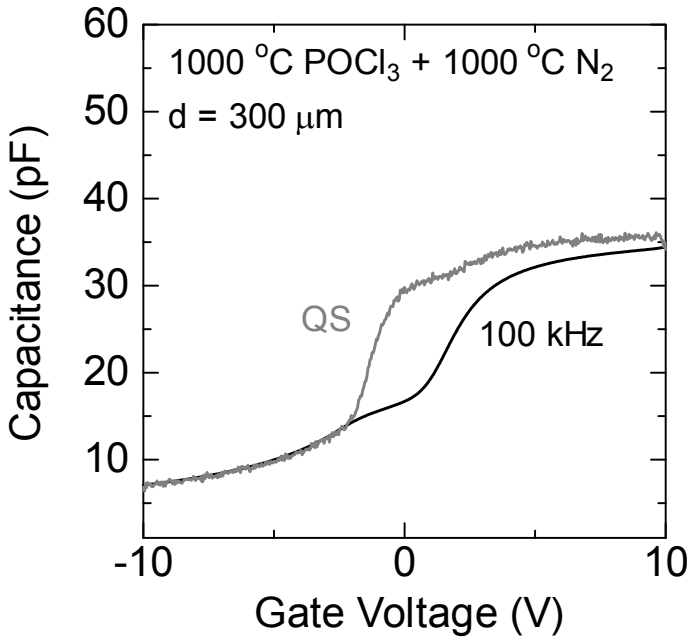
Fig. 6.8. Temperature profiles of $POCl_3$ and subsequent N_2 annealing for C-face.

6.3.2 Improvement in interface properties

Figure 6.9 shows the high-frequency (100 kHz) and quasi-static *C*–*V* curves of samples with $POCl_3/N_2$ annealing performed at 900 or 1000 °C (samples A, and B). Flatband voltage shift increased to positive direction after the $POCl_3/N_2$ annealing, whereas the capacitance difference between high- and low-frequency curves did not change significantly. The accumulation capacitance decreased after the $POCl_3/N_2$ annealing, indicating increased SiO_2 thickness. Figure 6.10 shows the D_{it} distribution for samples A, B and w/o. In the case of Si-face 4H-SiC, $POCl_3/N_2$ annealing at 1000 °C is the most effective process to reduce the D_{it}. However, in the case of C-face 4H-SiC, the annealing at 1000 °C did not reduce D_{it}. Additional SiO_2 growth was observed during $POCl_3$ annealing as shown in Table 6.1. Assuming that the dielectric constant of the oxides (ε_{ox}) is 3.9, equivalent oxide thickness (EOT) was calculated for the obtained accumulation capacitances of the high-frequency *C*–*V* curves. From the table, the EOT was increased by the $POCl_3$ annealing. The O_2 gas has to be added to the gas mixture to form a SiO_2-P_2O_5 layer by the reaction among SiO_2, $POCl_3$ and O_2. At the same time, O_2 in the gas mixture grows new SiO_2 layer near the interface because of the high oxidation rate of the C-face. At this time, poor-quality SiO_2 layer near the interface was formed by $POCl_3$ annealing at 900 °C or 1000 °C. The increment of the oxide thickness after the $POCl_3/N_2$ annealing at 1000 °C is approximately 26 nm. Although the $POCl_3/N_2$ annealing both at 900 °C can suppress the increment of the oxide thickness to 5.6 nm, little decrease in D_{it} was observed. It may be difficult to diffuse the phosphorus atoms into the interface through the thick SiO_2 layer by the N_2 annealing at 900 °C.



(a) $POCl_3$ annealing at 900 °C followed by N_2 annealing at 900 °C



(b) $POCl_3$ annealing at 1000 °C followed by N_2 annealing at 1000 °C

Fig. 6.9. Hi-lo *C–V* curves for the C-face 4H-SiC MOS capacitors fabricated by (a) $POCl_3$ annealing at 900 °C followed by N_2 annealing at 900 °C (sample A), and (b) $POCl_3$ annealing at 1000 °C followed by N_2 annealing at 1000 °C (sample B).

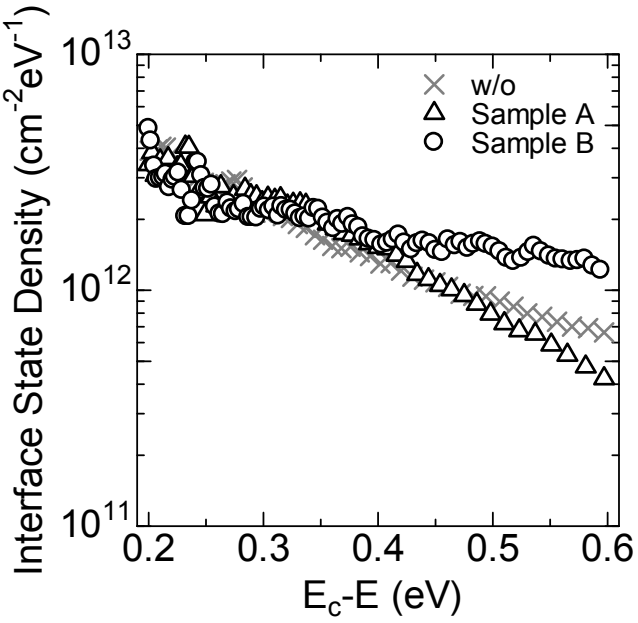
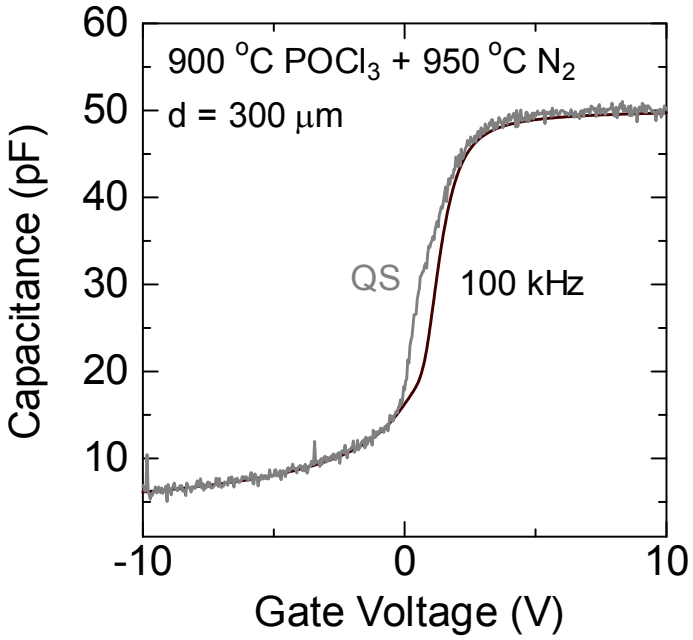


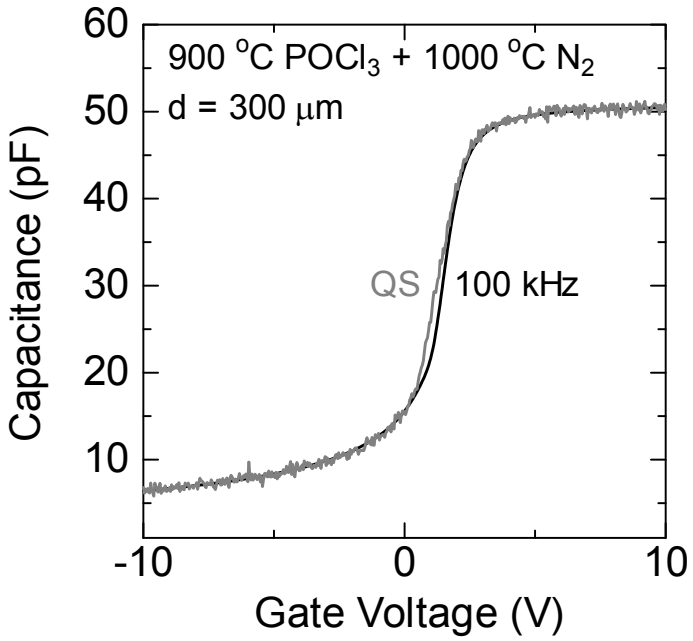
Fig. 6.10. Distribution of D_{it} for samples A and B estimated by the hi-lo *C–V* method.

Table 6.1. Accumulation capacitance and equivalent oxide thickness (EOT)

Sample	Anneal temp. [°C]		Accumulation capacitance [pF]	EOT [nm]	Increase in EOT after $POCl_3$ annealing [nm]
	$POCl_3$	N_2			
w/o	Dry only		56.3	43.4	-
A	900	900	49.8	49.0	5.6
B	1000	1000	35.1	69.5	26.1
C	900	950	49.7	49.1	5.7
D	900	1000	50.4	48.4	5.0



(a) $POCl_3$ annealing at 900 °C followed by N_2 annealing at 950 °C (sample C)



(b) $POCl_3$ annealing at 900 °C followed by N_2 annealing at 1000 °C (sample D)

Fig. 6.11. Hi-lo *C–V* curves for the MOS capacitors fabricated by (a) $POCl_3$ annealing at 900 °C followed by N_2 annealing at 950 °C (sample C), and (b) $POCl_3$ annealing at 900 °C followed by N_2 annealing at 1000 °C (sample D).

Then, a new sequential process was proposed for C-face 4H-SiC to introduce phosphorus atoms to the interface as illustrated in Fig. 6.8 (b). Additional SiO_2 growth during $POCl_3$ annealing was suppressed by the low-temperature $POCl_3$ annealing at 900 °C and phosphorus atoms were diffused to the interface by the subsequent N_2 annealing at 950 or 1000 °C. The hi-lo *C*–*V* curves for the samples C and D are shown in Fig. 6.11, indicating smaller capacitance difference for the higher N_2 annealing temperature. The D_{it} was drastically decreased to less than 3×10^{11} $cm^{-2}eV^{-1}$ in the whole energy range of 0.2–0.6 eV from the conduction band edge (E_c) of 4H-SiC as shown in Fig. 6.12. Figure 6.13 shows the distribution of carbon, oxygen and phosphorus atoms in the oxide and near the interface measured by secondary ion mass spectroscopy (SIMS) for the sample D, annealed in $POCl_3$ at 900 °C and in N_2 at 1000 °C. Note that the change of etching rate in the interlayer and knock-on effect were not considered and, hence, the horizontal axis could have a margin of error. The phosphorus atoms are uniformly distributed throughout the oxide and reach the SiO_2/4H-SiC interface and they are not diffused into the SiC side because of the small diffusion coefficient.

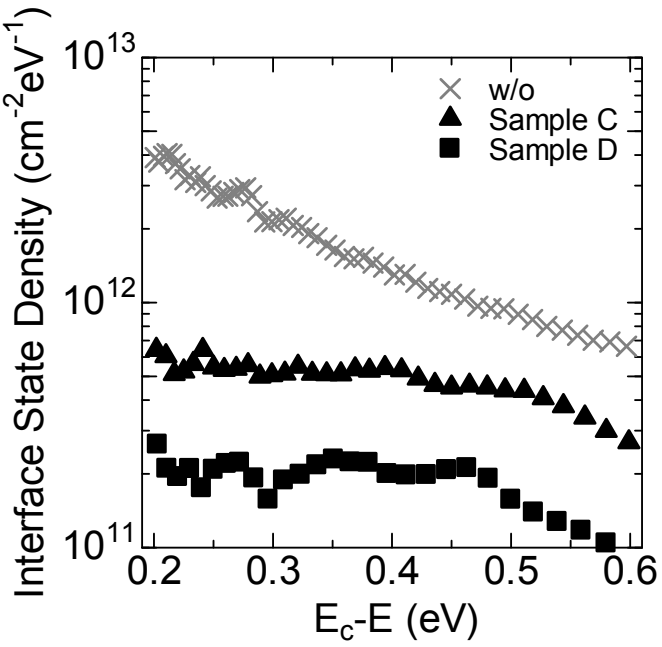


Fig. 6.12. Distribution of D_{it} for samples C and D estimated by the hi-lo *C–V* method.

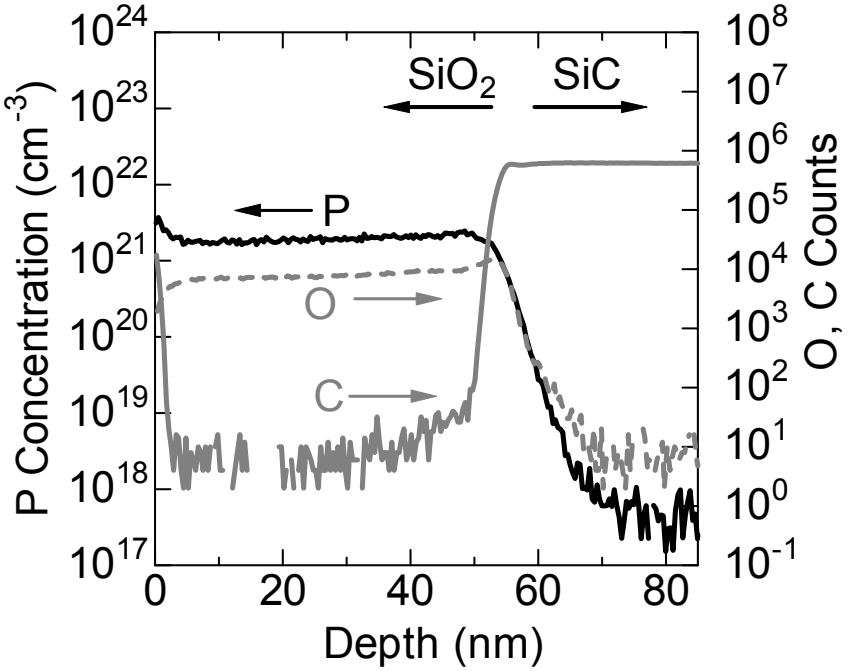


Fig. 6.13. SIMS profile for the sample D which was fabricated by $POCl_3$ annealing at 900 °C followed by N_2 annealing at 1000 °C.

N-channel MOSFETs were fabricated on C-face 4H-SiC p-type epitaxial layers ($N_a - N_d = 8 \times 10^{15}$ cm^{-3}) under the same conditions as MOS capacitors. Figure 6.14 shows the I_D–V_G characteristics of MOSFETs with a channel length and width of 30 μm and 200 μm, respectively. The drain voltage (V_D) was 0.1 V during the measurements. Larger drain current was observed for the sample annealed in N_2 at a higher temperature (sample D). Little current was observed for the dry-oxidized and low-temperature-annealed samples (samples w/o and A). The curve of the sample w/o was concealed in that of sample D.

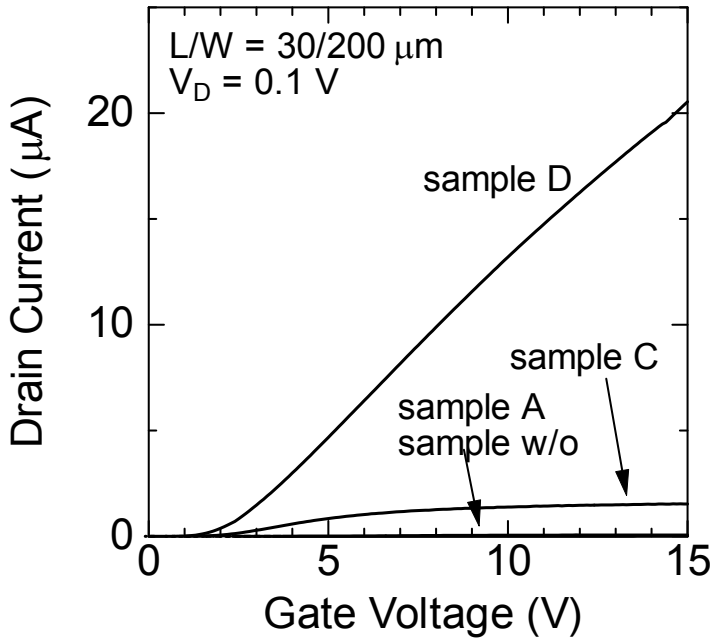


Fig. 6.14. Transfer characteristics of 4H-SiC MOSFETs fabricated on the C-face by $POCl_3$ annealing followed by N_2 annealing at various temperatures. The best result was obtained for the sample D which was fabricated by $POCl_3$ annealing at 900 °C followed by N_2 annealing at 1000 °C. The current was very small for samples A and w/o.

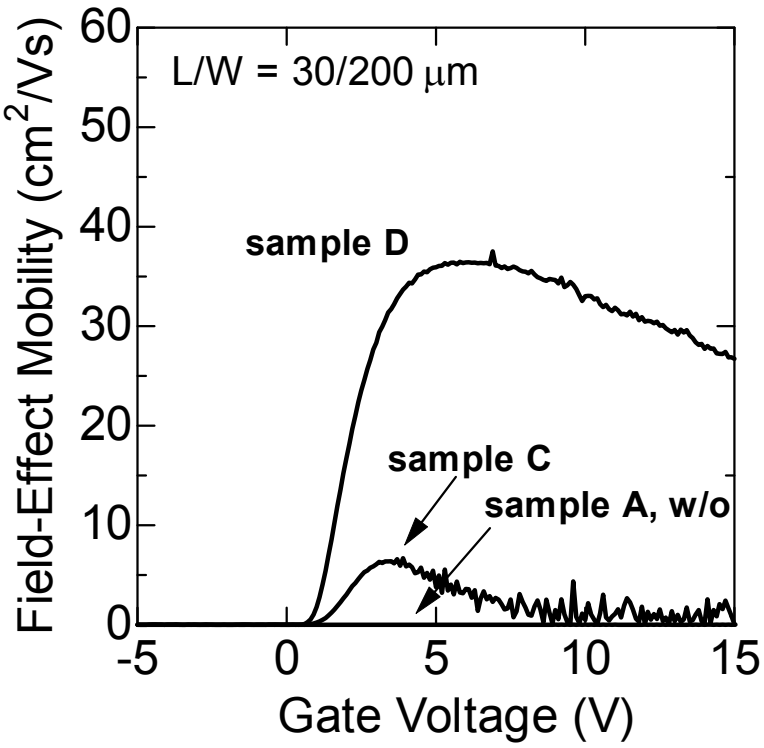


Fig. 6.15. Field-effect mobility of 4H-SiC MOSFETs fabricated on the C-face by $POCl_3$ annealing followed by N_2 annealing at various temperatures. The best result was obtained for the sample D which was fabricated by $POCl_3$ annealing at 900 °C followed by N_2 annealing at 1000 °C. The mobility was very small for samples A and w/o.

Figure 6.15 shows the field-effect mobility estimated from the I_D–V_G curves. The peak field-effect mobility of the sample D increased to approximately 37 cm^2/Vs. When the gate electric field is 3 MV/cm, the field-effect mobility of the sample D maintains about 32 cm^2/Vs. The threshold voltage was 2.5 V and the subthreshold swing was 297 mV/decade.

As stated above, the incorporation of phosphorus into the SiO_2/SiC interface is also effective to improve the characteristics of C-face MOSFETs. However, the channel mobility of the C-face MOSFETs is less than half the mobility of Si-face ones. These results may be due to the increasing of the SiO_2 layer near the interface during the

$POCl_3$ annealing at 900 °C. The low-temperature $POCl_3$ annealing can suppress the increment of the SiO_2 layer. However, the oxides formed by the low-temperature oxidation impair the quality of the SiO_2/SiC interface. In the case of the C-face, the increase in EOT after $POCl_3$ annealing at 900 °C is more than 5 nm. Therefore, the effect of $POCl_3$ annealing on the C-face MOS structures is weaker than that on the Si-face ones. Another possible explanation is that the phosphorus atoms are not effectively incorporated into the interface due to the $POCl_3$ annealing conducted at a low temperature.

6.3.3 Investigation of slow interface traps

Figure 6.16 shows the start voltage dependence of high-frequency *C–V* (cycle *C–V*) curves [10] of a MOS capacitor fabricated by $POCl_3$ annealing at 900 °C followed by N_2 annealing at 1000 °C (sample D). Similar to the NO samples, a positive and parallel shift of the *C–V* curves was observed with increasing start voltage. In general, such shift is not observed for the Si-face MOS capacitors at room temperature. The shift is relatively small because the sample was unloaded at room temperature. However, there are slow interface traps that degrade the device stability. The slow interface traps seem to be inevitably generated whenever the C-face MOS interface is annealed in NO or $POCl_3$-containing gases.

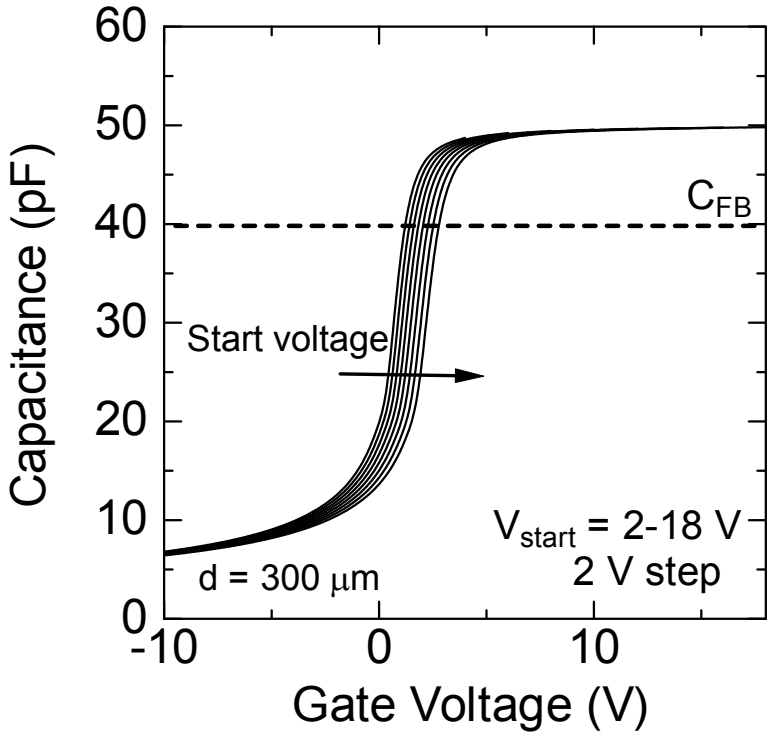


Fig. 6.16. Start voltage dependence of high-frequency *C–V* curves for a C-face 4H-SiC MOS capacitor fabricated by $POCl_3$ annealing at 900 °C followed by N_2 annealing at 1000 °C (sample D). Diameter of the circular gate electrode is 300 μm. The gate voltage was swept from accumulation to depletion. The start voltage was increased from 2 to 18 V with a 2-V step.

6.4 Conduction band offset on C-face 4H-SiC

One of the important properties of C-face MOS interface is conduction band offset between SiO_2 and 4H-SiC. Hatakeyama *et al*. reported that the conduction band offset at SiO_2/4H-SiC interface on C-face is smaller than that on Si-face [17]. The reduction in the conduction band offset at the C-face interface was also confirmed by the study of photoelectron spectroscopy [18]. The mechanism of the reduction is completely unclear. However, it is important to investigate the conduction band offset because its reduction causes gate leakage current.

To investigate the conduction band offset, current–voltage (*I–V*) measurements were

performed applying positive bias to the gate of MOS capacitors. Figure 6.17 shows the current density–oxide electric field (J–$\mathcal{E}_{ox}$) characteristics of dry, NO-700, NO-RT, and $POCl_3$-anenaled (sample D) MOS capacitors on C-face 4H-SiC. The leakage current flows due to Fowler-Nordheim (FN) tunneling when $\mathcal{E}_{ox}$ is larger than ~5 MV/cm. The relationship between FN current (J_{FN}) and electric field ($\mathcal{E}_{ox}$) is given by

$$J_{FN} = \frac{q^2 m^* \mathcal{E}_{ox}^2}{8\pi h \phi_b m_0} \exp\left(-\frac{8\pi \left(2qm^* \phi_b^3\right)^{1/2}}{3h\mathcal{E}_{ox}} \right) \tag{6.1}$$

where q is the elemental charge, m^* is the effective mass of tunneling electron, m_0 is the electron rest mass, h is the Planck's constant, and ϕ_b is the conduction band offset [19]. The conduction band offset (ϕ_b) can be extracted from the slope of a $\ln(J_{FN}/\mathcal{E}_{ox}^2)$ vs. $1/\mathcal{E}_{ox}$ plot which is referred to as the FN plot. Figure 6.18 shows the FN plots of dry, NO-700, NO-RT, and $POCl_3$-anenaled (sample D) MOS capacitors.

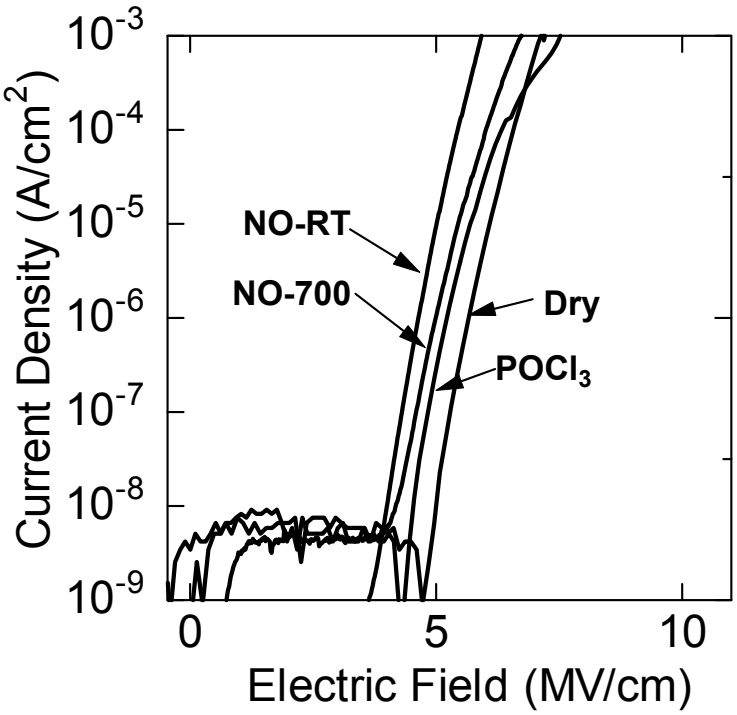


Fig. 6.17. J–$\mathcal{E}_{ox}$ characteristics of dry, NO-700, NO-RT, and $POCl_3$-anenaled (sample D) MOS capacitors on C-face 4H-SiC.

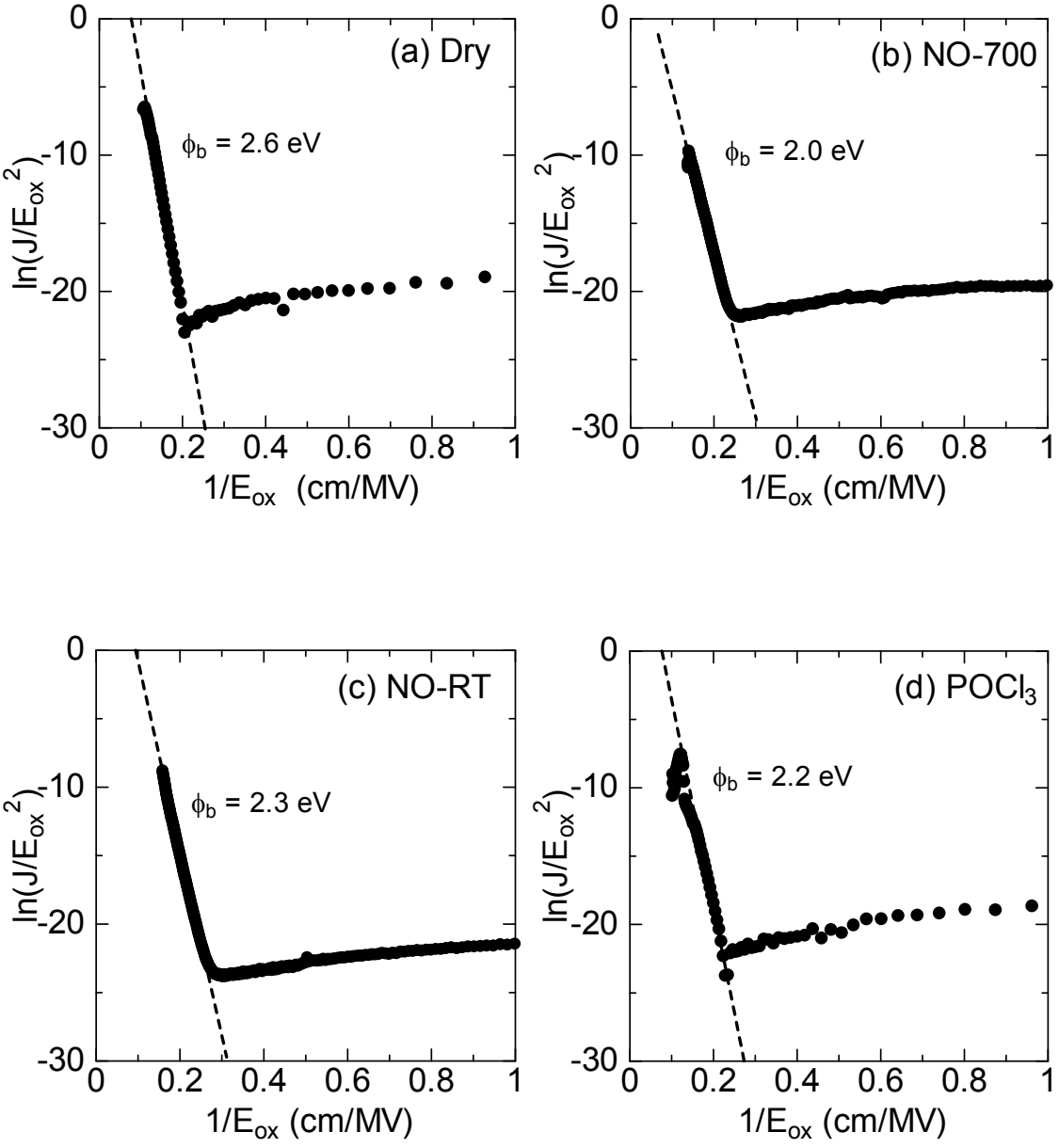


Fig. 6.18. FN plots of (a) dry, (b) NO-700, (c) NO-RT, and (d) $POCl_3$-anenaled (sample D) MOS capacitors on C-face 4H-SiC.

Table 6.2. Estimated values of the conduction band offset for dry, NO-700, NO-RT, and $POCl_3$-anenaled (sample D) MOS capacitors on C-face 4H-SiC.

Gate oxide	Conduction band offset (eV)
Dry	2.6
NO-700	2.0
NO-RT	2.3
$POCl_3$	2.2

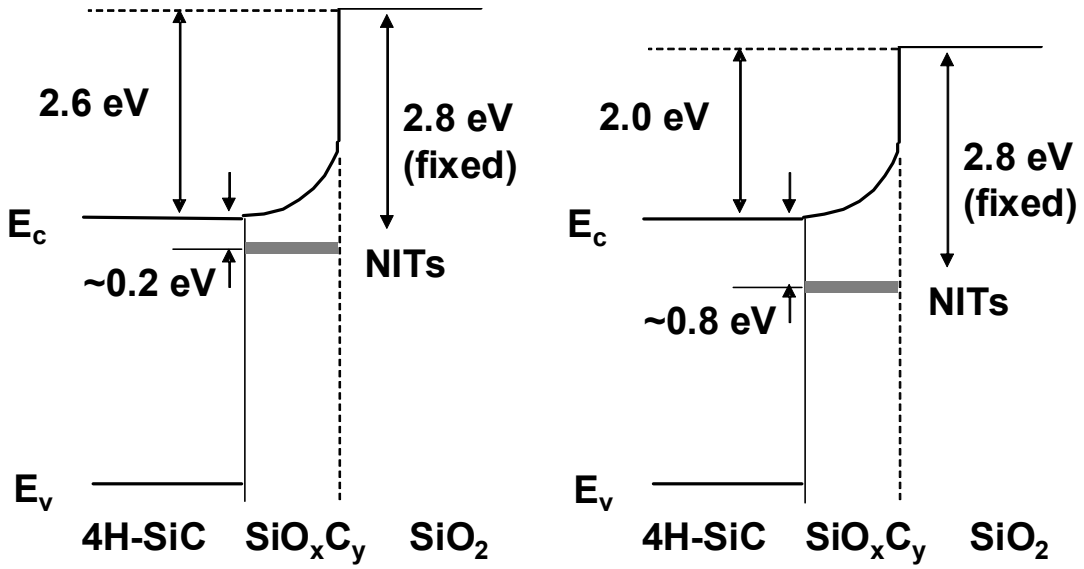
The estimated conduction band offset is listed in Table 6.2. It should be noted that conduction band offset estimated by FN plot is subject to errors because the effective mass of carriers in the oxide is not clearly determined and the charge distribution in the oxide is not known. The typical value of the band offset is 2.7 eV for Si-face [11, 12]. Therefore, the estimated values of band offset for C-face are smaller than those for Si-face. One possible answer to this is attributed to the generation of interface dipole [18]. However, the reason for the reduced conduction band edge is still obscure in the SiC community.

6.5 Discussion

As described in Chapter 4, the $POCl_3$ annealing and NO treatment effectively removes near-interface traps (NITs) for the Si-face MOS structures. For the C-face MOS structures, pyrogenic oxidation and high-temperature hydrogen annealing are very effective to reduce the D_{it} [1]. However, these processes has small effect on the Si-face MOS structures [1]. These facts imply that the interface states in the C-face MOS

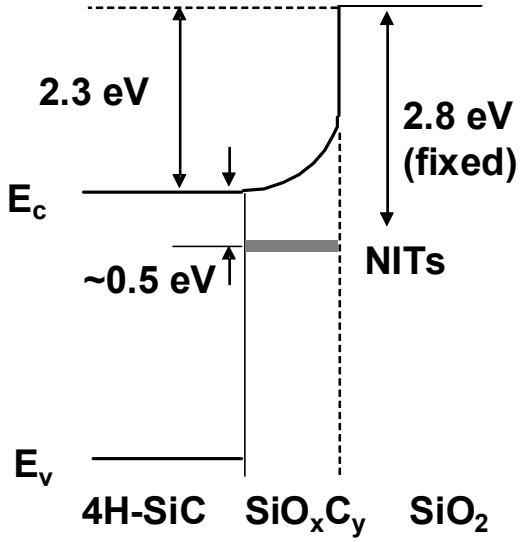
structures are mainly due to C dangling bonds, which can be passivated by hydrogen atoms [16]. The effect of NITs on the C-face MOS devices would be smaller than that of C dangling bonds. Therefore, the effect of $POCl_3$ annealing on the C-face MOS structures is weaker than that on the Si-face ones.

The slow interface traps, referred to as *deep* NITs, were observed in C-face MOS capacitors. The *C–V* curves were shifted at room temperature depending on start voltage of the measurement. Such shift is observed for Si-face MOS capacitors only when the measurement is conducted at a low temperature, as described in Chapter 4. This fact implies that the energy position of NITs in C-face MOS capacitors is different from that in Si-face ones. This difference would be explained by considering the difference in the conduction band offset. As described in Section 6.4, the conduction band offset of C-face MOS capacitors is smaller than that of Si-face ones. On the other hand, the NITs are native oxide traps that locate 2.8 eV below the conduction band edge (E_c) of SiO_2 [11, 12]. Therefore, the energy position of NITs shift to deeper position for C-face because the energy position of NITs is fixed at 2.8 eV for all samples but the conduction band offset is smaller in the C-face MOS capacitors. Figure 6.19 illustrates the speculated model of deep NITs for C-face MOS structures. The density of NITs could be reduced by NO or $POCl_3$ treatments (this speculation should be investigated by TDRC). However, the energy position of NITs is apart from the conduction band edge of the SiO_xC_y interlayer. Therefore, it takes very long time to emit electrons from the NITs. This causes the large shift in the *C–V* curves even at room temperature depending on the start voltage.

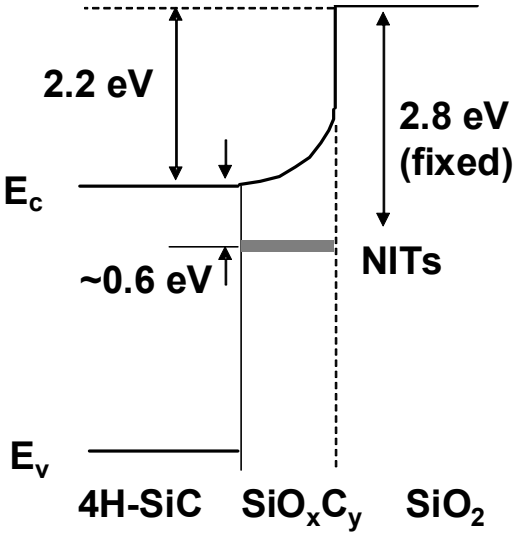


(a) Dry

(b) NO-700



(c) NO-RT



(d) $POCl_3$ (sample D)

Fig. 6.19. Speculated models of deep NITs for C-face MOS structures. The energy position of NITs changes with the conduction band offset between 4H-SiC and SiO_2 because the energy position of NITs are 2.8 eV below the conduction band edge of SiO_2 [11, 12].

6.6 Summary

It was found that extremely slow interface traps are generated by direct oxidation in NO for the C-face 4H-SiC MOS structure. In these structures, interface state density at energies near the conduction band edge estimated from the hi-lo *C–V* method is relatively small. The slow traps and interface states were reduced by unloading the samples at room temperature. These results suggest that deep NITs capture channel mobile electrons and degrade the performance of MOSFETs.

$POCl_3/N_2$ annealing performed at 1000 °C did not reduce the interface state density (D_{it}) in MOS strucrture on the C-face. By establishing a $POCl_3/N_2$ annealing process suitable for C-face MOS structures, D_{it} was decreased to less than 3×10^{11} $cm^{-2}eV^{-1}$ in the energy range of 0.2–0.6 eV from the E_c. The peak field-effect mobility was increased to approximately 37 cm^2/Vs. The incorporation of phosphorus atoms into the SiO_2/SiC interface is also effective for improving the performance of C-face 4H-SiC MOSFETs. It was found that slow interface traps are also generated by $POCl_3$ annealing for the C-face 4H-SiC MOS structure.

The interface properties of Si- and C-faces are different. Therefore, it is important to reduce not only the interface states but also the near-interface traps to fabricate high-performance C-face 4H-SiC MOSFETs.

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Chapter 7
Conclusions

7.1 Conclusions

In order to manufacture high-performance SiC power devices and realize ultra low loss power converter, the improvement in channel mobility of SiC MOSFETs is the most critical issue, as described in Chapter 1. In this study, some techniques were proposed to reduce the interface state density (D_{it}) and improve the channel mobility. The most important result obtained in this study is that the D_{it} can be significantly reduced by incorporation of P atoms into the SiO_2/SiC interface. Therefore, this thesis mainly described the effect of P incorporation on the interface properties. In addition, some part of this thesis used the conventional nitridation technique and discussed the effect of N atoms, comparing to the effect of P atoms. The results obtained in this study would be important from scientific and engineering point of view.

In Chapter 2, B, N, F, Al, P, and Cl ions were implanted prior to the oxidation and introduced at the SiO_2/SiC interface by subsequent thermal oxidation. Interface state density near the conduction band edge increased with implantation dose for Al-, B-, F-, and Cl-implanted MOS capacitors. On the other hand, a strong reduction of the interface state density was observed for N- and P-implanted samples when the implantation dose was larger than 5.0×10^{12} cm^{-2}. It was found that the interface state density can be reduced by P as well as N. This is the first report that the D_{it} can be reduced by P atoms. However, a MOS capacitor fabricated by higher implantation energy and dose exhibits a higher D_{it} value. The slightly higher D_{it} for the P-implanted sample compared to the

N-implanted one might be due to larger implantation damage because the implantation energy of P is higher than that of N due to the heavier ion.

In Chapter 3, a thermal anneal using phosphoryl chloride ($POCl_3$) was proposed in order to incorporate P atoms without implantation damage. The interface state density near the conduction band edge was reduced significantly and the channel mobility increased to 89 cm^2/Vs by the $POCl_3$ annealing at 1000 °C. The high channel mobility is attributed to the reduced shallow interface state density. The proposed method is one of the possible candidates for fabricating SiC power MOSFETs with high channel mobility.

In Chapter 4, effective removal of near-interface traps (NITs) in SiO_2/4H-SiC (0001) structures through phosphorus incorporation is demonstrated. Low-temperature capacitance–voltage (*C–V*) and thermal dielectric relaxation current (TDRC) measurements were used to investigate NITs in the oxides prepared by dry oxidation, NO annealing, and $POCl_3$ annealing. Both the measurements revealed that the density of electrons trapped in NITs in $POCl_3$-annealed oxide is smaller than that in dry and NO-annealed oxides. The drastic elimination of NITs lowers the interface state density and increases the channel mobility in 4H-SiC MOSFETs. It was implied that the incorporated P atoms induce the structural relaxation near the interface, reading to the low density of NITs.

In Chapter 5, charge-pumping measurements were performed on 4H-SiC MOSFETs. The charge-pumping technique is one of useful and reliable methods of directly measuring MOSFET interface properties. Measurements using various pulse fall times revealed that the unwanted geometric component exists in n-channel 4H-SiC MOSFETs and is particularly large in unannealed n-channel 4H-SiC MOSFETs with low channel

mobility. In addition, influence of interface states on the charge-pumping curves is significant in the unannealed 4H-SiC MOSFETs. The charge-pumping curves are distorted by these two non-ideal effects, making the analysis of the charge-pumping curves difficult. A sufficiently long pulse fall-time, in the order of 1–10 μs for n-channel 4H-SiC MOSFETs with a 10 μm gate length, is required to minimize the effect of the geometric component. On the contrary, the geometric component is small for the $POCl_3$-annealed MOSFETs because of the high channel mobility. The geometric component in SiC MOSFETs arises easily, and therefore, it must be considered carefully in the measurements. The charge-pumping measurement can be made a useful and reliable tool using a sufficiently long pulse fall time for interface state characterization of SiC MOSFETs.

In Chapter 6, the effect of two different oxidation techniques, NO direct oxidation and $POCl_3$ post oxidation annealing, on C-face MOS interface was investigated. It was found that extremely slow interface traps are generated by both direct oxidation in NO and $POCl_3$ post oxidation annealing for the C-face 4H-SiC MOS structures. It was found that the slow traps and interface states were reduced by unloading the samples at room temperature. $POCl_3/N_2$ annealing performed at 1000 °C did not reduce the interface state density (D_{it}) in MOS strucrture on the C-face. By establishing a $POCl_3/N_2$ annealing process suitable for C-face MOS structures, D_{it} was decreased to less than 3×10^{11} $cm^{-2}eV^{-1}$ in the energy range of 0.2–0.6 eV from E_c. The peak field-effect mobility was increased to approximately 37 cm^2/Vs. The incorporation of phosphorus atoms into the SiO_2/SiC interface is also effective for improving the performance of C-face 4H-SiC MOSFETs. In the case of C-face, it is important to reduce not only the interface states but also the near-interface traps.

7.2 Suggestions for future work

The most important result obtained in this study is that the incorporation of P atoms into SiO_2/SiC interface using $POCl_3$ annealing is effective for improving the interface properties. However, this study is a fundamental study of the $POCl_3$-annealed MOS interfaces. However, there are many challenges and problems in the phosphorus-doped gate oxide. In addition, there remain issues regarding the mechanisms of interface states.

1. Reliability of P-doped gate oxide

The reliability of gate oxide is important for the practical devices. As described in Chapter 3, the reliability of P-doped gate oxide on 4H-SiC is comparable to the dry oxide. However, the reliability is inferior to the NO-annealed gate oxide. The problem would be the P atoms are distributed throughout the gate oxide and the oxide network become weak. On the other hand, for NO-annealed oxides, it is well known that the N atoms are piled up only at the interface and the rest of the oxide network consists of pure SiO_2. Such distribution of incorporated atoms is desirable both for the good reliability and improvement in channel mobility. The local distribution of P atoms only at the interface may be realized by direct oxidation using $POCl_3$ for short time followed by the deposition of SiO_2. In addition, there is a possibility that the distribution can be controlled by the gas ratio in the $POCl_3$ annealing. Further study is needed to obtain better reliability with maintaining the high channel mobility by P incorporation.

2. Mechanism of the interface states

Over the past 10 years, many SiC researchers around the world tried to identify the

origins of the interface states and the mechanisms of D_{it} passivation. Although many models have been proposed to date, no one knows the perfect answer. In this study, mechanisms responsible for the reduced D_{it} was discussed based on some physical investigations and a model for the $POCl_3$-annealed oxide was proposed. Especially, the investigation of chemical structures at the interface is not enough because only the P2*p* peak could be investigated in this study. The investigation of other peaks such as Si2*p*, O1*s*, and C1*s* is difficult by the standard XPS setup due to the lack of resolution. High resolution photoelectron spectroscopy using synchrotron is needed for more detailed analysis. In addition, first principle study may be needed to investigate the interface configuration.

3. Development of new annealing process

In this study, $POCl_3$ was used as a source of phosphorus. There are other sources of phosphorus such as phosphine (PH_3). PH_3 is more toxic than $POCl_3$, but is widely used in the Si industry. More effective passivation is expected by use of gaseous PH_3 because the contamination due to the use of a bubbler can be avoided. In addition, PH_3 contains hydrogen, which may improve the reliability of the gate oxide.

4. Further investigation of C-face MOS structures

This study revealed that the slow interface states are generated in the C-face MOS devices. These traps cause the instability of threshold voltage in MOSFETs. The origin of slow traps would be deep NITs which are located at the deeper energy; this would be due to the reduction in conduction band offset. Despite the many years of the investigation, the mechanism of the reduction in the conduction band offset is still

unclear in the SiC community; therefore, it should be investigated in the future. In addition, the density of NITs on C-face devices was not investigated in this study. It should be investigated using TDRC in the future.

List of Publications

A. Academic journals

1. **Dai Okamoto**, Hiroshi Yano, Tomoaki Hatayama, and Takashi Fuyuki, "Removal of Near-Interface Traps at SiO_2/4H-SiC (0001) Interfaces by Phosphorus Incorporation", *Appl*. *Phys*. *Lett*., **96** (2010) 203508.
2. **Dai Okamoto**, Hiroshi Yano, Kenji Hirata, Tomoaki Hatayama, and Takashi Fuyuki, "Improved Inversion Channel Mobility in 4H-SiC MOSFETs on Si face Utilizing Phosphorus-Doped Gate Oxide", *IEEE Electron Device Lett*., **31** (2010) 710.
3. **Dai Okamoto**, Hiroshi Yano, Yuki Oshiro, Tomoaki Hatayama, Yukiharu Uraoka, and Takashi Fuyuki, "Investigation of Near-Interface Traps Generated by NO Direct Oxidation in C-face 4H-SiC Metal-Oxide-Semiconductor Structures", *Appl*. *Phys*. *Express*, **2** (2009) 021201.
4. **Dai Okamoto**, Hiroshi Yano, Tomoaki Hatayama, Yukiharu Uraoka, and Takashi Fuyuki, "Analysis of Anomalous Charge-Pumping Characteristics on 4H-SiC MOSFETs", *IEEE Trans*. *Electron Devices*, **55** (2008) 2013.

B. Peer-reviewed conference proceedings

1. **Dai Okamoto**, Hiroshi Yano, Kenji Hirata, Tomoaki Hatayama, and Takashi Fuyuki, "Improved Inversion Channel Mobility in Si-face 4H-SiC MOSFETs by Phosphorus Incorporation Technique", *Mat*. *Res*. *Soc*. *Symp*. *Proc*., **1246** (2010) 1246-B06-06.
2. **Dai Okamoto**, Hiroshi Yano, Yuki Oshiro, Tomoaki Hatayama, and Takashi Fuyuki,

"Systematic Investigation of Interface Properties in 4H-SiC MOS Structures Prepared by Over-Oxidation of Ion-Implanted Substrates", *Mat. Sci. Forum*, **645-648** (2010) 495.

3. **Dai Okamoto**, Hiroshi Yano, Yuki Oshiro, Tomoaki Hatayama, Yukiharu Uraoka, and Takashi Fuyuki, "Investigation of Oxide Films Prepared by Direct Oxidation of C-face 4H-SiC in Nitric Oxide", *Mat. Sci. Forum*, **645-648** (2010) 515.
4. **Dai Okamoto**, Hiroshi Yano, Tomoaki Hatayama, Yukiharu Uraoka, and Takashi Fuyuki, "Criteria for Accurate Measurement of Charge-Pumping Current in 4H-SiC MOSFETs", *Mat. Sci. Forum*, **600-603** (2009) 747.

Presented Works

A. Presentations at international conferences

1. **Dai Okamoto**, Hiroshi Yano, Shinya Kotake, Tomoaki Hatayama, and Takashi Fuyuki, "Shallow traps at P-doped SiO_2/4H-SiC(0001) Interface", Euro. Conf. on Silicon Carbide and Related Materials 2010 (ECSCRM 2010), 2010.8
2. **Dai Okamoto**, Hiroshi Yano, Kenji Hirata, Shinya Kotake, Tomoaki Hatayama, and Takashi Fuyuki, "Demonstration of High Channel Mobility in 4H-SiC MOSFETs by Utilizing Phosphorus-Doped Gate Oxide", The 2010 Int'l Meeting for Future of Electron Devices, Kansai (2010IMFEDK), 2010.5
3. **Dai Okamoto**, Hiroshi Yano, Kenji Hirata, Shinya Kotake, Tomoaki Hatayama, and Takashi Fuyuki, "Improved Inversion Channel Mobility in Si-face 4H-SiC MOSFETs by Phosphorus Incorporation Technique", 2010 MRS Spring Meeting, 2010.4

4. **Dai Okamoto**, Hiroshi Yano, Tomoaki Hatayama, and Takashi Fuyuki, “Systematic Investigation of Interface Properties in 4H-SiC MOS Structures Prepared by Over-Oxidation of Ion-Implanted Substrates”, Int'l Conf. on Silicon Carbide and Related Materials 2009 (ICSCRM 2009), 2009.10
5. **Dai Okamoto**, Hiroshi Yano, Yuki Oshiro, Tomoaki Hatayama, Yukiharu Uraoka, and Takashi Fuyuki, “Investigation of Oxide Films Prepared by Direct Oxidation of C-face 4H-SiC in Nitric Oxide”, Int'l Conf. on Silicon Carbide and Related Materials 2009 (ICSCRM 2009), 2009.10
6. **Dai Okamoto**, Hiroshi Yano, Yuki Oshiro, Tomoaki Hatayama, Yukiharu Uraoka, and Takashi Fuyuki, “Interface Properties of C-face 4H-SiC Metal-Oxide-Semiconductor Structures Prepared by Direct Oxidation in Nitric Oxide”, 2009 Int'l Conf. on Solid State Devices and Materials (SSDM 2009), 2009.10
7. **Dai Okamoto**, Hiroshi Yano, Yuki Oshiro, Tomoaki Hatayama, Yukiharu Uraoka, and Takashi Fuyuki, “Electrical Properties of C-face 4H-SiC MOS Devices Fabricated by NO Direct Oxidation”, The 2009 Int'l Meeting for Future of Electron Devices, Kansai (2009IMFEDK), 2009.5
8. **Dai Okamoto**, Hiroshi Yano, Tomoaki Hatayama, Yukiharu Uraoka, and Takashi Fuyuki, “Direct Measurement of Interface State Density of SiC MOSFETs by Charge-Pumping Technique”, 2007 NAIST/GIST Joint Symposium on Advanced Materials, 2007.11
9. **Dai Okamoto**, Hiroshi Yano, Tomoaki Hatayama, Yukiharu Uraoka, and Takashi Fuyuki, “Criteria for Accurate Measurement of Charge Pumping Current in 4H-SiC MOSFETs”, Int'l Conf. on Silicon Carbide and Related Materials 2007 (ICSCRM2007), 2007.10

B. Related presentations

1. Shinya Kotake, Hiroshi Yano, **Dai Okamoto**, Tomoaki Hatayama, and Takashi Fuyuki, “Improved MOS interface properties of C-face 4H-SiC by $POCl_3$ annealing”, Euro. Conf. on Silicon Carbide and Related Materials 2010 (ECSCRM 2010), 2010.8
2. Yoshihiro Ueoka, Hiroshi Yano, **Dai Okamoto**, Tomoaki Hatayama, and Takashi Fuyuki, “Extraordinary characteristics of 4H-SiC trench MOSFETs on large off-angle substrates”, Euro. Conf. on Silicon Carbide and Related Materials 2010 (ECSCRM 2010), 2010.8
3. Hiroshi Yano, Yuki Oshiro, **Dai Okamoto**, Tomoaki Hatayama, and Takashi Fuyuki, “Instability of 4H-SiC MOSFET characteristics d ue to interface traps with long time constant”, Euro. Conf. on Silicon Carbide and Related Materials 2010 (ECSCRM 2010), 2010.8

Patents

Hiroshi Yano and **Dai Okamoto**, Japanese patent, No. 2009-285561.

Hiroshi Yano and **Dai Okamoto**, International PCT patent, PCT/JP2010/007231.