Laser Crystallization of Non Two-dimensional Silicon Substrate for Thin Film Device Application

（レーザー結晶化による非二次元シリコン基板作製と
その薄膜デバイス応用）

March 2009

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Abstract

Low temperature poly-Si (LTPS) thin film transistor (TFT) has attracted much attention due to its great potential as a key device to realize the next generation display 'System on Panel'. TFTs can also be applied to various non-flat panel display (FPD) areas where transistors are required to enhance specific functions or to stabilize operation of certain devices such as photo-sensors and DNA sensors. So far, various crystallization technique using laser annealing have been proposed to obtain larger crystal grains of the resulted poly-Si. However, all of those have utilized silicon thin films with conventional flat, two-dimensional substrates, and therefore their aim was limited only to the upgrading of TFT performance. Accordingly, this study developed a new work on the laser annealing crystallization of silicon thin films by introducing one-dimensional, and three-dimensional substrates, that is to say, non two-dimensional substrates which have not hitherto been employed. It aimed not only for the enhancement of the poly-Si crystallinity by making use of crystallization mechanism originating from each silicon substrate structure, but also for the creation of a efficient fabrication method of high-performance device by applying the substrate structure itself.

A concept of TFT fabrication on one-dimensional "fiber" substrate, named as Fiber-TFT, was newly proposed. Since TFTs can in principle be fabricated on any substrates in low temperature, if micro-electronic devices using semiconductor thin films are fabricated on a thin and line-shaped flexible substrate in high-speed and low-cost, there opens up a possibility of a novel processing technology in the manufacturing of a new product field of not only FPD but also non-FPD. As one demonstration, development of LTPS TFT was performed using thin quartz fibers as one-dimensional

substrates.

Laser crystallization using three-dimensional “double-layered” a-Si thin films substrate was investigated for the application to three-dimensional (3D) device fabrication. Because existing technology such as device transferring to make such 3D device have many process complexities, a more straightforward method was needed. For the choice of the laser for the crystallization, pulsed green laser was employed. Poly-Si crystallized by this method was evaluated in crystallinity and applied to TFT fabrication. Suitable laser annealing for this method was also investigated.

In Chapter 2, a basic fabrication process of LTPS TFTs using two-dimensional substrate was developed. Excimer laser anneaing crystallized poly-Si was used as a standard LTPS substrate. Top-gated self-aligned n-ch, and p-ch TFTs with the channel length and width of 5 μm were fabricated under the process temperature of 550 °C. Post metallization annealing condition of 400, 450, 475 (only for n-ch TFTs) °C, and the contact characteristics and TFT characteristics were evaluated. As a result, at the PMA condition of 450 °C, TFTs with highest performance in the contact and transistor characteristics was fabricated, which showed the field effect mobility of around 150 cm^2/Vs for n-ch TFTs and 50 cm^2/Vs for p-ch TFTs taken in the liner region.

In Chapter 3, development of poly-Si TFTs on a quartz fiber was demonstrated. The fiber was embedded into the trench formed in a quartz substrate, and handled as a whole through the TFT fabrication. The excimer laser crystallization of a-Si deposited on a quartz fiber was carried out, and a poly-Si layer with a crystal grain diameter of 300 nm was obtained. The top-gated self-aligned TFTs fabricated on the fiber using the poly-Si film showed a mobility of 10 cm^2 /Vs, The lower mobility is considered to be due to the poor quality of the interface of poly-Si / gate SiO_2 deposited on the fiber.

In Chapter 4, crystallization of double-layered a-Si thin films using solid state pulsed green laser annealing system was demonstrated. In the case of the double-layered

structure of a-Si / SiO_x / a-Si = 50 / 50 / 50 (nm), it was found that the crystallization laser energy of the double-layered a-Si films was 30 % less than that of conventional single layer a-Si films with the a-Si thickness of 50 nm. That both the upper and lower a-Si films were successfully crystallized without damaging the interlayer SiO_x was confirmed by cross-sectional TEM observations. Furthermore, in the condition of the crystallization of the lower a-Si film, a drastic enhancement of crystal growth over 2 μm was observed. It can be considered that crystallizing lower a-Si was playing a role of thermal storage, which causes the extension of the melting time of the upper a-Si and reduces the thermal gradient around the interface of the molten Si and interlayer SiO_x. TFTs using the large grained double-layered poly-Si were confirmed to possess superior electrical performance with the field effect mobility of up to 550 cm^2 / Vs.

In conclusion, the use of a-Si thin films substrates having novel one-dimensional and three-dimensional structure in the laser annealing crystallization was successfully demonstrated, and its effectiveness for the LTPS thin film devices was verified. The future works will be the detailed optimization of the structure of the a-Si films, and process simulations.

Acknowledgements

The author would like to express his special gratitude to Professor Takashi Fuyuki for the opportunity to accomplish this work and for his unfailing guidance, critical supervision, and encouragement throughout this study. He also would like to thank Professor Tadashi Shiosaki, Professor Jun Ohta and Associate Professor Aishi Yamamoto for their valuable discussion and critical comments on the manuscript.

He would like to extend his deep gratitude to Associate Professor Yukiharu Uraoka for his perspicacious advice and kind encouragement. He is very obliged to Research Associates Tomoaki Hatayama and Hiroshi Yano for critical comments on experiments and supporting daily works. He wishes to express his thanks to Ms. Yuko Kamikawa, Ms. Ayumi Tani and Ms. Kumi Hora for several supports.

He wishes to thank to Dr. Atsushi Miura, Mr. Hiroshi Terasawa, Dr. Akiyoshi Ogane and other students for their helpful discussion and encouragement.

He wishes to thank Dr. Yukie Yamamoto, Dr. Hidenori Mikami (now at Sumitomo Electronics Industry Corporation), Dr. Takio Hikono, Dr. Yu Takahashi (now at Sharp Corporation) for their useful discussions and perspicacious advices.

He would like to express special thanks to Dr. Akio Mimura (Advance Institute of Science and Technology). Without him, this thesis could never be accomplished.

Finally, the author really thanks his parents, brother for their understanding, continuing care, support and heartfelt encouragement.

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Chapter 1
Introduction

1.1 Background

1.1.1 TFT and LCD

Thin film transistor (TFT), one of thin film electric devices, which has accomplished its great advance today, was first born in the proposition made by Lilienfeld in 1930 [1]. Aiming to invent a replacement of expensive and complicated vacuum tubes which were widely prevailing at that time, he proposed a solid-state device using a functional thin film material and three electrodes formed on a glass substrate for the control of electric current. In 1934, Heil in Germany applied a patent of field effect, electric current amplifying device having three electrodes [2]. As shown in Fig. 1.1, the use of semiconductor material and gate insulator, which are the basic component materials of today's TFTs and metal-oxide-semiconductor field effect transistors (MOSFETs), was suggested in this patent. Although the concept of TFT was presented in this early 1930's, the first, actually operating TFT was reported by Weimer in 1961 [3]. It was composed of a microcrystalline cadmium sulfide (CdS) semiconductor layer, a gate dielectric layer, and gold (Au) source drain gate electrodes. All films were successively deposited by evaporation through mechanical masks on a glass substrate. After this, TFTs had been intensively researched for possible electronic and display

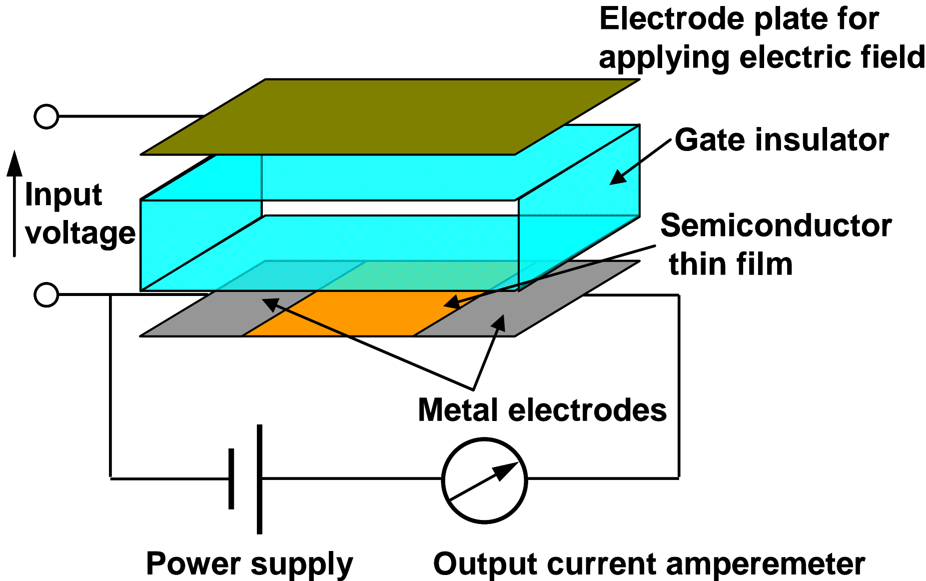


Figure 1.1: Schematic of the field effect TFT patented by Heil [2].

applications. In the 1960's, TFT technology was in competition with single crystal silicon MOSFET for the integrated circuit field. However, due to the rapid progress of the latter and the difficulty in consistently producing good quality devices of the former, TFTs were not successful.

In 1971, Active-Matrix (AM) liquid crystal display (LCD), that is, a TFT-driven, display device using liquid crystal, was proposed by Lechner [4]. This technology had greatly improved the image quality of LCDs, which had so far driven by Passive-Matrix scheme. After that, a worldwide competition of TFT-LCD development broke out. In 1979, TFT with good switching performance using hydrogenated a-Si (a-Si:H) thin film was reported by Le Comber and Spear [5]. This gave a powerful impact to the development of TFT-LCD technology. The deposition technique of a-Si:H developed by Spear had many superior features, such as large-area uniformity of film quality, reproducibility and stability of the process, safety of the deposition system operation and good fine-scale fabrication conformity, all of which were compatible with the semiconductor fabrication process. Furthermore, the a-Si:H film was capable in low-temperature (< 300 °C) deposition, which enabled the use of inexpensive glass substrate with poor thermal durability. Because the a-Si TFT was able to be operated in low-voltage range owing to its high electrical resistance, they were promptly employed to the TFT-LCDs development as promising pixel driving devices [6]. And now, the a-Si AM TFT-LCDs are equipped with flat panel televisions, mobile electronic devices such as cell phones, note-type personal computers, thus dominating other flat panel display devices.

1.1.2 Potential of low temperature poly-Si TFT technology

The success of the TFT technology, especially a-Si:H TFT, can be contributed to the unique fabrication characteristics such as large-area substrate capability and

low-process temperature, as mentioned above. In addition to these, TFT has its own unique feature that it can be fabricated on various structures. However, there is a major drawback in the a-Si:H TFT technology, i.e., its low field effect mobility less than 1.0 cm^2 / Vs. In the efforts in improving the mobility of TFTs, poly-crystalline silicon (poly-Si) thin film was employed to TFT-LCD fabrication [7, 8]. Poly-Si TFT has several advantages: (1) it can be fabricated in self-aligned structure, which enables a further scale down of device dimensions and reduction of parasitic capacitance the source / drain regions and the gate electrode, leading to enhancement of switching performance of TFT, (2) it has large current driving capability owing to its field effect mobility two orders of magnitude higher than that of a-Si TFT (10 ~ 600 cm^2 / Vs), (3) it enables the integration of complementary MOS (CMOS) logic circuits because poly-Si has large hole mobility, and so on. These enable finer resolution, higher aperture ratio, lower power consumption and faster response time of TFT-LCD and fabrication of integrated peripheral driving circuits onto the same LCD substrate, which realize light, compact, robust and low-cost LCDs with advanced functions such as image sensing or pen-input [9]. Poly-Si TFT can also be applied to many non TFT-LCD areas where transistors are required to enhance specific functions or to stabilize operation of certain devices. This includes electrical, optical, magnetic, mechanical and bio-chemical devices [10].

As for the poly-Si film formation, there are several methods to fabricate poly-Si thin films on the glass substrate at low temperature (under the distortion temperature of the glass substrate, around 600 °C), and they are roughly categorized into the three groups: (1) direct deposition on the substrate, (2) solid-phase crystallization of the precursor a-Si film through thermal annealing with or without the aid of metal catalysis and (3) liquid-phase crystallization through annealing of a-Si film by laser irradiation. Although these technologies have their own advantages and disadvantages, in point of

quality of the poly-Si crystallinity, the laser annealing crystallization of a-Si has been producing promising results and so far most actively studied. In addition, since laser annealing process, especially using pulsed laser with the pulse duration of nanosecond order, occurs during very short time scale within a few hundred nanosecond, it can anneal and crystallize the a-Si thin film without damaging the underling substrate with the use of proper thermal buffer layers to protect the substrate. Therefore, it is possible to use laser in annealing process for the formation of poly-Si not only on glass substrates but also on plastic substrates with poor thermal endurance, which enables fabrication of high-performance poly-Si TFT device on flexible substrates such as fine-resolution flexible LCD. For these reasons, fabrication of poly-Si at low temperatures, so-called low-temperature poly-Si (LTPS) technology has been actively investigated so far.

1.1.3 Poly-Si formation by laser crystallization and its issues

Among the laser annealing technologies excimer laser annealing (ELA) method has been one of promising techniques for high quality LTPS fabrication and many researched have been done so far [11, 12]. The excimer laser is an excellent source of high-power UV radiant energy; it can produce high energy pulses capable of crystallizing a-Si film. During excimer laser annealing of a-Si, the majority of the photon energy is absorbed in the surface of a-Si within the depth of 20 nm. When a-Si melts after laser irradiation, it cools down rapidly toward glass substrate and nucleation occurs at the interface between Si and SiO_2. Once the nuclei are formed, solidification is propagated from the nuclei to molten Si region with the speed of 1 ~ 10 m / s. Although the grain size of ELA poly-Si is range of tens to a few hundred nanometers, it is reported that there are small number of defects inside grains (intra-grains), thus the ELA poly-Si shows high quality electrical performances. Nowadays, mass-produced ELA poly-Si thin films have thickness less than 100 nm and the crystal grain size of around 0.3 μm.

Therefore, the standard sized TFT using ELA poly-Si with the gate length over 1 μm inevitably contains many crystal grain boundaries within that region. This leads degradation of electric performances of ELA poly-Si TFTs in contrast to TFT using crystal Si thin film (Silicon on Insulator) because of the scattering, capturing / emission and generation / recombination of carriers at the grain boundaries. For this reason, it is important to fabricate poly-Si thin films with large and location-controlled grains.

In the case of the laser annealing crystallization of a-Si thin films, the most crucial factor for the determination of the crystal growth length and direction is the temperature gradient of molten a-Si because the crystal growth proceeds from the lower temperature region to higher temperature region in the molten Si film. Therefore, by fixing the generation points of crystal nuclei in advance, the growing crystal grains can be made collide at the determined positions, thus, the grain boundary locations in the resulted poly-Si film can be controlled. The crystal nuclei generate in the gradually cooling molten Si film. Therefore, by intentionally setting certain temperature difference in the molten Si film, crystal nuclei generation in the low-temperature region can be promoted. Thus, the active control of temperature profile in the molten Si film leads to the increase of the crystal grain size and the control of the grain boundary locations in the resulted poly-Si film. For the reasons stated above, various laser annealing method to control the temperature gradient of the molten Si film have been proposed [13-17].

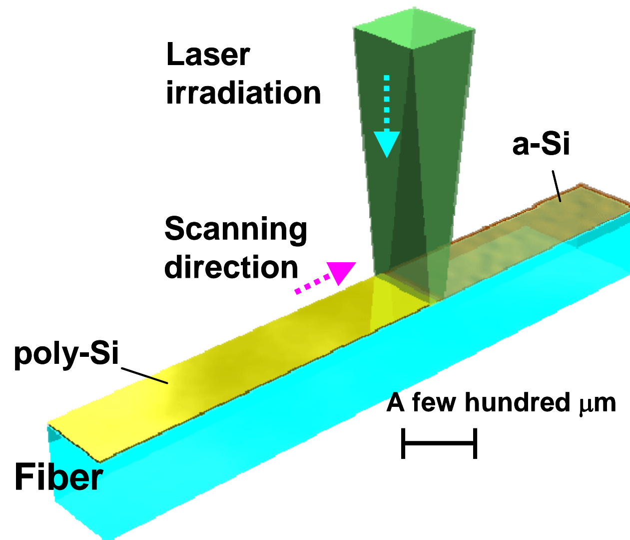
1.2 Non two-dimensional silicon substrate for laser crystallization

So far, many research groups have investigated how to fabricate a large crystal grain poly-Si film with location-controlled grain boundaries. However, they have their own technical obstacles; fabrication cost tends to increase owing to the requirement of

expensive optical systems and / or complex process, which make it more difficult for them to be applied to practical mass-production use. In reviewing this technological trend, one can noticed that all these developments were done by using plane, two-dimensional substrates. Compared with other solid-state devices, the main strength of the TFT technology lies in its flexibility in device structure, fabrication method, and substrate material and / or shape selection [18]. However, in the development of LTPS TFT history, so far the shape and the structure of the substrate in the laser annealing crystallization process of poly-Si formation have not been paid attention to.

Thus, in this thesis, a new approach to the laser annealing crystallization of a-Si thin films was proposed. Focusing attention on the primary feature of TFT that it can be fabricated on any insulating substrates in principle, it was considered that, what merits will be created by the use of substrates having shape and / or structure different from those of two-dimensional plane substrates, in other words, substrates with different "dimension", in the fabrication of high performance poly-Si TFT. Next, for the formation of high quality poly-Si thin films on such substrates, it was devised to utilize the shape and structure of such substrates themselves to the control of laser irradiation and heat transfer in the laser annealing crystallization of a-Si thin films.

That is the laser crystallization using non two-dimensional silicon thin films substrates. Fig. 1.2 shows the proposed laser crystallization using one-dimensional, and three-dimensional substrates. These are the laser crystallization methods using one-dimensionally long, transparent, fiber-like, flexible substrates, and three-dimensionally stacked silicon thin films substrates which have not been explored in the laser crystallization process of silicon thin film so far. By considering that, in utilizing these non two-dimensional substrates for laser crystallization of silicon thin films, for example, only the limited region of substrate was annealed and heated in the fiber substrate, and more than one silicon thin films are involved in the laser



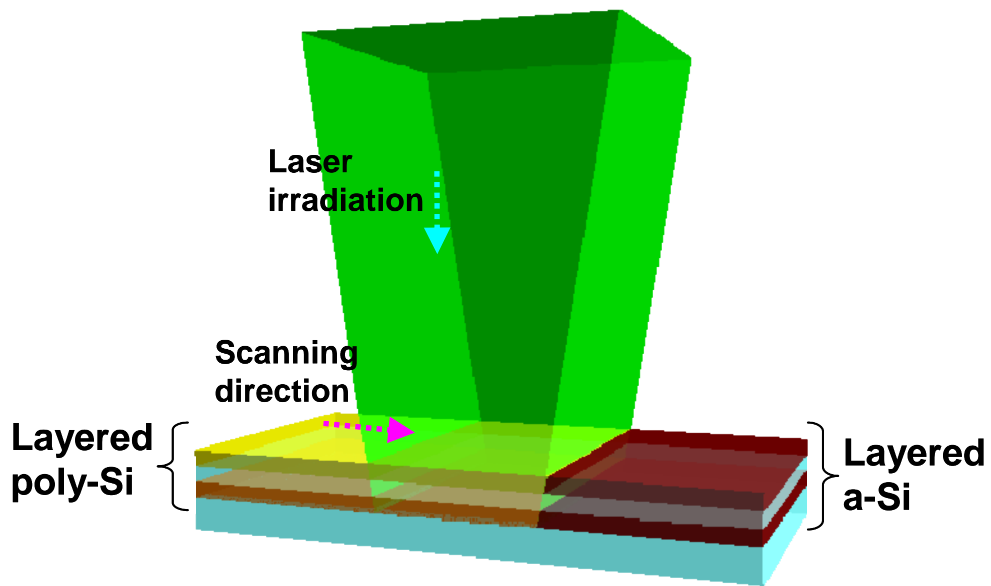


Figure 1.2: Conceptual schematics of “laser crystallization of non two-dimensional Si substrates”.

crystallization on stacked silicon thin films, it can be said that the behavior of laser light interaction and heat conduction much different from that of the laser crystallization of silicon thin film using two-dimensional plane substrate is expected.

In addition, by using these substrates, there opens a possibility that they are able to apply to a novel thin film device fabrication process where the substrates shape and structure are aggressively utilized. For example, such one-dimensional shape of fiber substrates increases their applicability to the reel-to-reel process which has great advantage in high-speed and low-cost device fabrication in a small-scale, low-emitting environment. Moreover, the laser crystallization of such stacked silicon thin films would provide a simpler fabrication scheme of three-dimensional thin film devices than so far proposed by using conventional two-dimensional substrates. Though the detailed explanations are given in the introduction in the later chapters, it is thought that these non two-dimensional silicon substrates have their own merits compared to that of conventional two dimensional plane substrate, which would lead to advanced application unlimited to the improvement of poly-Si TFT performance that exclusively have been pursued by the laser crystallization using two dimensional substrate. In this meaning, the study of laser crystallization using non two-dimensional silicon thin films substrates add a new page to the development of silicon thin film device technology.

1.3 Objectives and outline of this thesis

Thus, demonstration of this laser crystallization concept was aimed in this study. That is, it was intended to perform laser crystallization of silicon thin film on one-dimensional fiber substrate, and three-dimensionally stacked silicon thin films, and to actually apply the resulted poly-Si films to the TFT fabrication. By comparing the laser crystallization using conventional two-dimensional plane substrate with that using

these non two-dimensional substrates, crystallization mechanism using each substrate was considered. Moreover, by developing TFT fabrication process using these non two-dimensional poly-Si thin films, the relationship between the TFT electrical performance and the poly-Si crystallinity was investigated. Through these studies, knowledge on the device application of non two-dimensional silicon thin films was obtained.

The outline of this thesis is as follows. This study was originated by launching a basic poly-Si TFT fabrication process in the laboratory first time. In Chapter 2, the development of poly-Si TFT fabrication process using conventional two-dimensional poly-Si thin film substrates is treated. Then, on the basis of the newly established fabrication process, the development of TFT using the non two-dimensional poly-Si thin films substrates was demonstrated. In Chapter 3, the laser crystallization and development of poly-Si TFT using one-dimensional fiber substrate are described. In Chapter 4, the laser crystallization of three-dimensionally stacked silicon thin films and their crystallinity evaluation, and the investigation of the relationship between TFT performance using the poly-Si thin films and their crystallinity were elucidated. In the final chapter, this thesis is concluded and proposals to the future development are summarized.

As described above, the research and development of laser annealing crystallization technique aiming for high-quality poly-Si thin film has vigorously been dune so far by using two-dimensional substrates, but these studies were only aiming for the fabrication high-quality poly-Si. In point of the objectives, not only to realize crystallization mechanism to produce a high-quality poly-Si by changing the "dimension" of the precursor a-Si thin film substrate, but also to establish novel fabrication of functional high-performance thin film devices by effectively employing

the non-conventional dimensions of the substrates, this study entitled as 'Laser Crystallization of Non Two-dimensional Silicon Substrate for Thin Film Device Application' is considered to be a pioneering work which distinguishes itself from the existing studies of relating subject carried out so far.

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Chapter 2

Development of basic poly-Si TFT fabrication process using two-dimensional substrate

2.1 Introduction

The objective of this study is to investigate the poly-Si thin films formed by laser annealing crystallization using a-Si thin film substrate with “non two-dimensional” shape and structure and clarify their characteristics. The superiority of the fabricated poly-Si must be demonstrated by evaluating its electrical characteristics the TFT using the poly-Si. For the purpose of this, development of a basic fabrication process of LTPS TFT using conventional two-dimensional substrate was developed in the laboratory first time. In this chapter, the details of development and optimization of the TFT fabrication process are elucidated.

2.2 Fabrication of low-temperature poly-Si TFT

Fig. 2.1 shows a schematic cross-sectional image of a self-aligned top-gated poly-Si TFT. The self-aligned structure is that by which the edges of the source and drain regions are determined by the position of the gate electrode, and is formed by performing

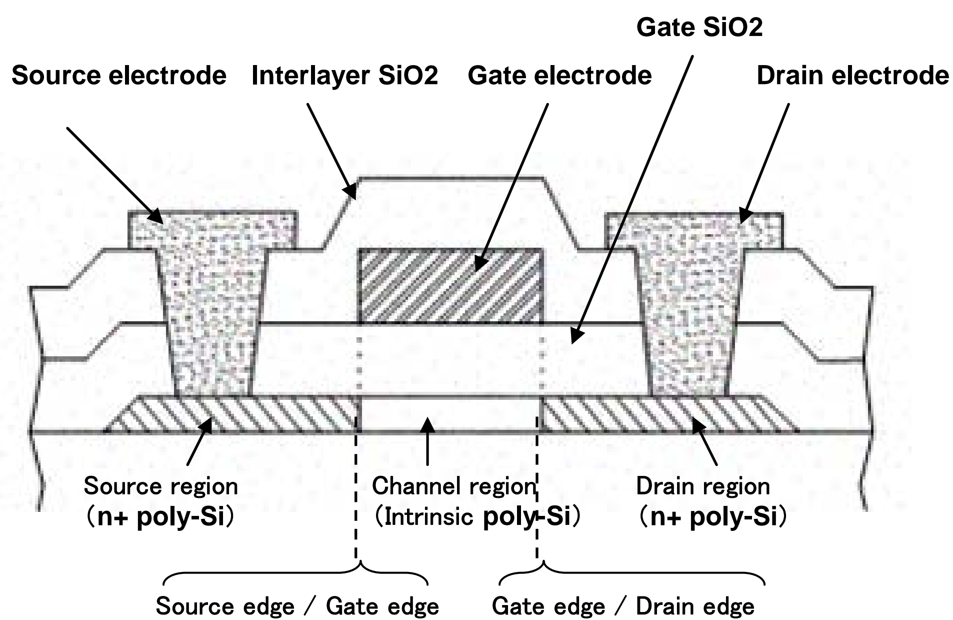


Figure 2.1: Schematic cross-sectional of a top-gated n-ch TFT with self-aligned structure.

impurity doping such as ion implantation or ion doping using the gate electrode as a mask. By doing this, it leads to reduction of parasitic capacitance at the edges of the gate electrode [1], which improves the electric performance of the TFT. Because this structure of poly-Si TFT is conventional and widely utilized in the LTPS TFT-LCD field, it was employed in the development of the basic fabrication process of LTPS TFT.

Fig.2.2 shows a process flow chart of the fabrication of LTPS TFTs. First, 50 nm thick precursor a-Si thin film was deposited on a non-alkaline glass substrate (Distortion temperature (DT): 550 ˚C) by plasma enhanced chemical vapor deposition (PECVD). (①) As buffer insulator films to prevent the defusion of contamination from the glass substrate into the Si film and improve the adhesion of the a-Si film to the glass substrate, SiN_x (50 nm) and SiO_2 (100 nm) films were deposited before the deposition of a-Si. Next, through excimer laser annealing, the a-Si film was crystallized to form a poly-Si. (②) The laser annealing crystallization was done after dehydrogenation which was carried out by annealing the a-Si at the temperature of 400 ˚C to degas H_2 in the a-Si film to prevent the increase of the surface roughness of the poly-Si due to the bumping of H_2 contained in the a-Si film in large amounts when the a-Si was irradiated by a laser pulse. In this development, the main purpose is to establish a process of making poly-Si thin film into TFTs, so conventional poly-Si thin film substrates (ELA poly-Si) were prepared in advance and utilized as standard poly-Si substrates for the development of the fabrication process of LTPS TFTs.

Table 2.1 shows the process conditions of the fabrication of LTPS TFTs. The processes after Si island formation were all done in the laboratory only except ion implantation, which was performed at TORAY RESEARCH CENTER, Inc. (TRC). In the following the fabrication process flow is explained. The Si island, which becomes as the channel layer of TFT, was formed by wet-etching of poly-Si using a mixture of diluted HF and HNO_3. After that, RCA cleaning of the substrate was performed as a

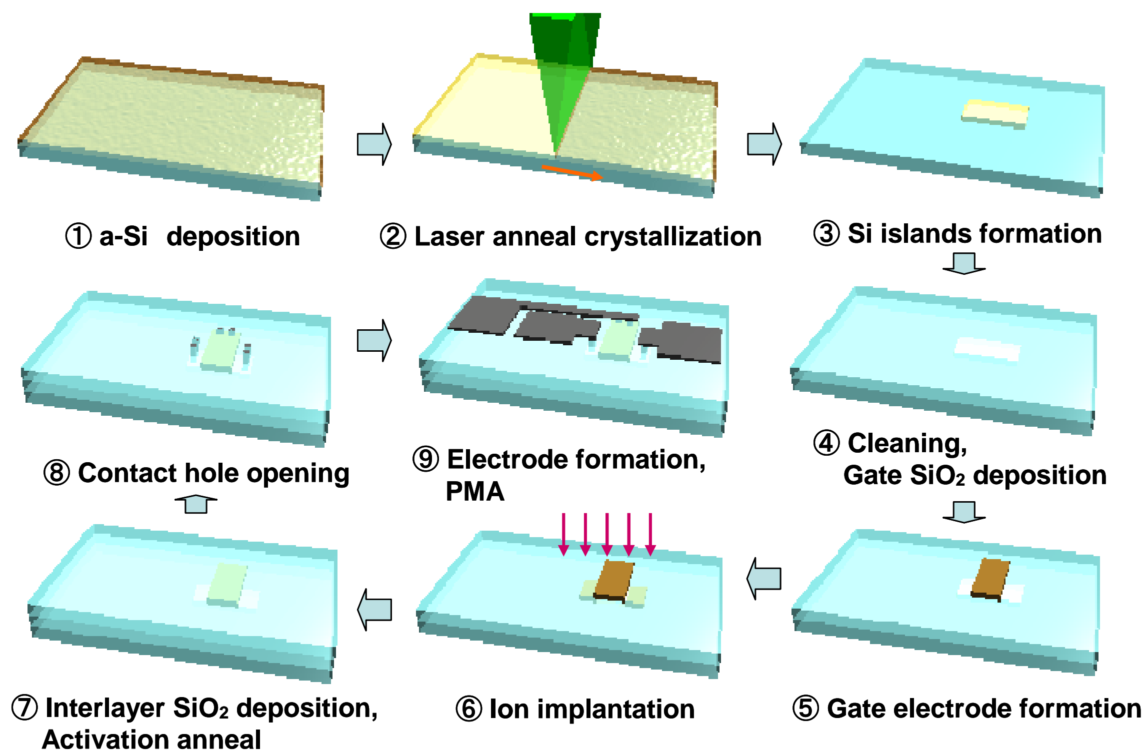


Figure 2.2: Process flow chart for the fabrication of LTPS TFT.

Table 2.1: Process conditions of LTPS TFT fabrication.

① a-Si deposition : 50 nm、 PE-CVD (SiH_4+H_2) @ 300 °C on non-alkaline glass (DT : 550 °C)	⑥ Ion-implantation n-ch TFT : P, 90keV, 1.2E15/cm^2 p-ch TFT : B, 30keV, 3.6E15/cm^2
② Laser annealing crystallization Excimer laser (XeCl : λ = 308 nm) Energy density : 300mJ/cm^2、 repetition number of irradiation : 20	⑦ Interlayer SiO_2 deposition : 400nm PE-CVD (TEOS+O_2) @ 300 °C & Activation annealing N_2, @ 500 °C, 1, 2, 4, 8 hour
③ Si island formation Wet-etching (DHF+HNO_3)	⑧ Contact hole opening Wet-etching (BHF)
④ RCA cleaning & Gate SiO_2 deposition : 100 nm PE-CVD (TEOS+O_2) @ 300 °C	⑨ Source/Drain electrode formation Ti(80 nm)/Al(500 nm)/Mo(80 nm), Electron beam deposition Wet-etching (HNO_3+H_3PO_4+H_2O) & PMA : N_2-diluted H_2 (10%) 400, 450, 475 °C , 1 hour
⑤ Gate electrode formation Mo deposition (250 nm, sputtering) Lift-off process	

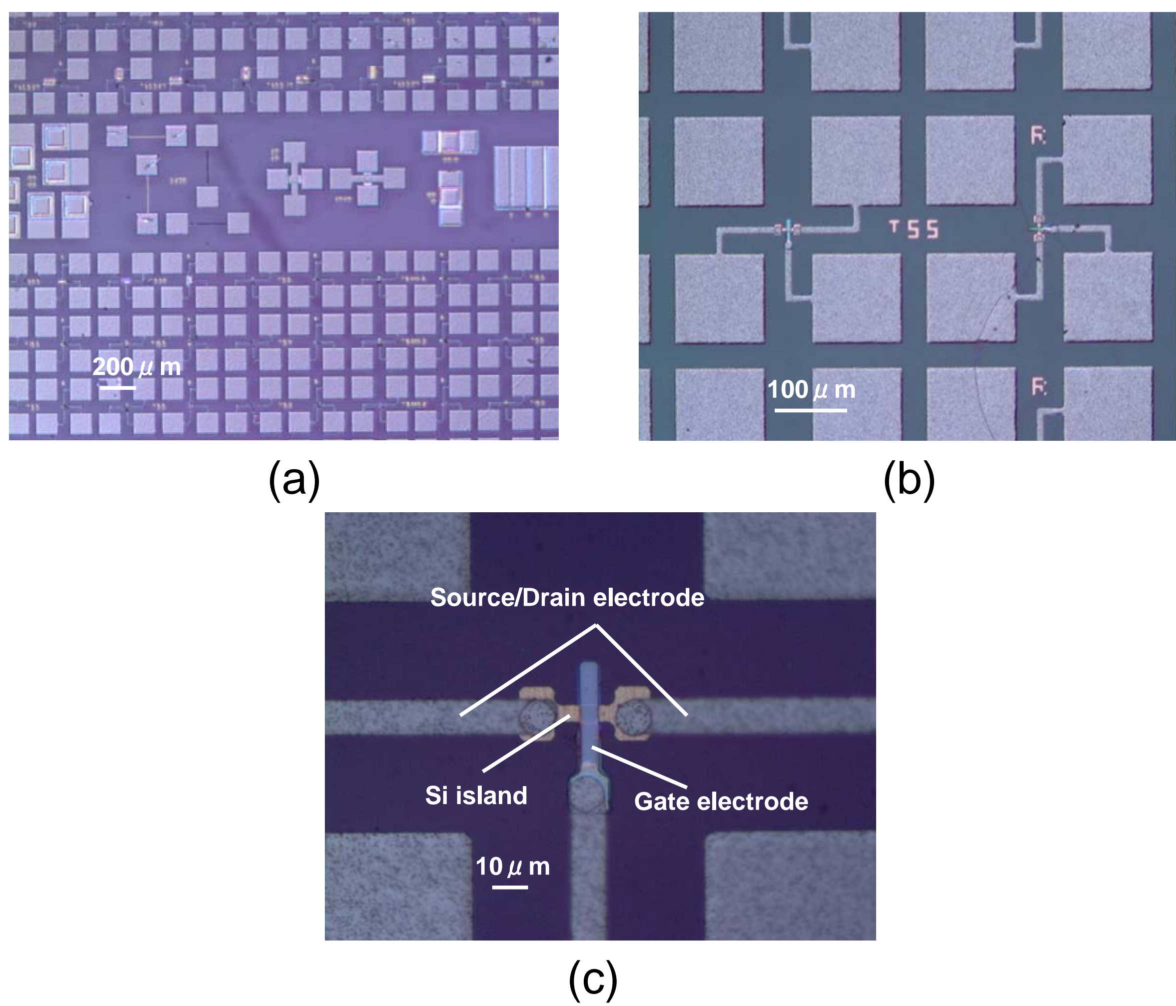


Figure 2.3: Optical microscope images of the completed LTPS TFTs; (a) whole cell image, (b) TFTs with different channel directions, (c) magnified image of a TFT.

cleaning of poly-Si surface before the gate SiO_2 deposition. The 100 nm thick gate SiO_2 was deposited by PE-CVD using tetra ethoxy silane (TEOS) gas and O_2 at the temperature of 300 ˚C. After resist patterning using photo lithography on the substrate, a 250 nm thick Mo film was deposited by spattering and the gate electrodes were formed by lift-off process. After that, ion implantation was performed (phosphorous for n-ch TFT and boron for p-ch TFT) using the gate electrode as mask to form source and drain regions in self-align manner. For the impurity activation and the recovering of the crystallinity of the poly-Si, activation annealing was performed by using an annealing furnace in N_2 ambient at 500 ˚C. After activation annealing, contact holes were opened by wet-etching of interlayer SiO_2 and gate SiO_2 using BHF, and source / drain electrodes were formed by the deposition of Ti/ Al /Mo and wet-etching. Finally, post metallization annealing was performed in an annealing furnace in N_2-diluted H_2 (10%) ambient. The underlined parts in the Table 2.1 were process conditions which were done for the purpose of optimization.

The patterning of the each film was carried out using photo-lithography. Figs. 2.3 show the microscope images of the completed TFTs with the channel length and width of both 5 μm. It can be seen that the patterning was successfully demonstrated.

2.3 Excimer laser annealing crystallized poly-Si

In this development of the fabrication of LTPS TFTs, conventional poly-Si thin films utilized in the actual fabrication of LCDs crystallized by XeCl excimer laser annealing (λ = 308 nm) with reliable quality of crystallinity were utilized as standard poly-Si thin film substrates. The a-Si film (50 nm) was deposited on a glass substrate by the plasma enhanced chemical vapor deposition (PECVD) method, and the structure of sample is a-Si (50 nm)/ SiO_2 (100 nm)/ SiN_x (50 nm)/ non-alkali glass. Prior to laser

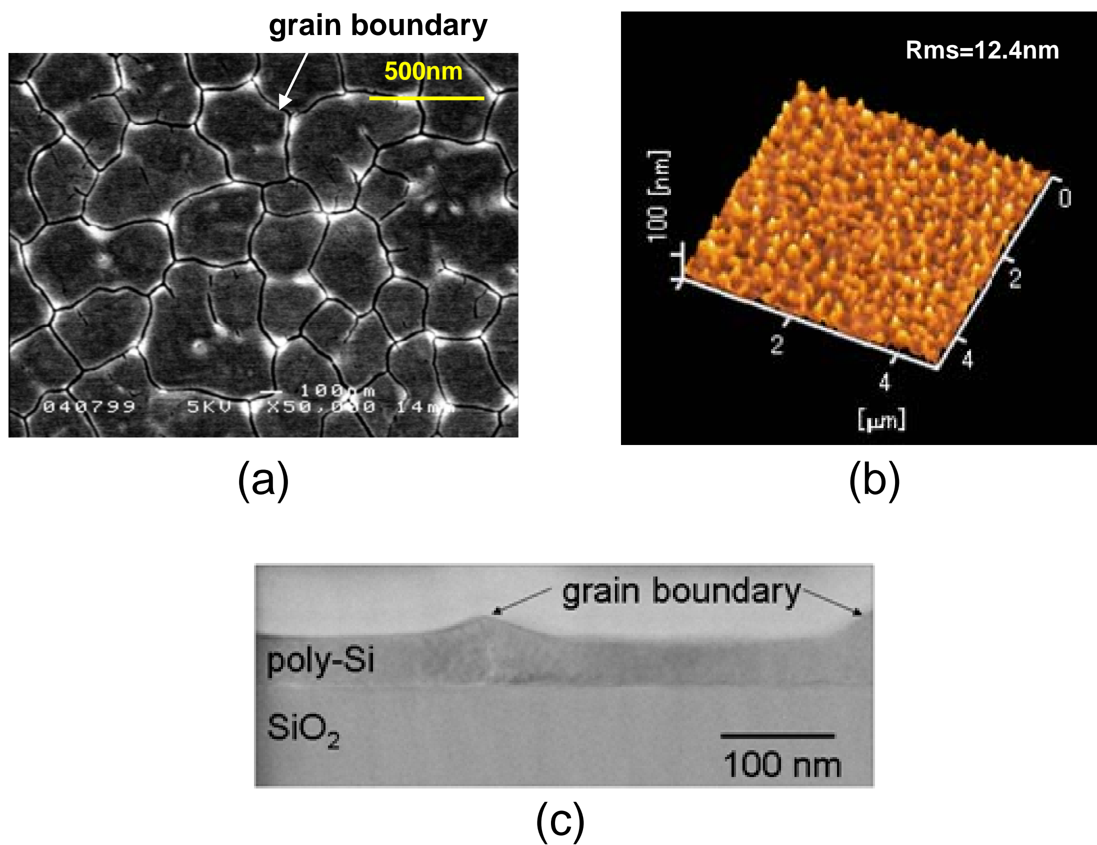


Figure 2.4: (a) SEM image (b) AFM image of the surface of ELA poly-Si. (c) Cross-sectional TEM image of ELA poly-Si.

annealing, the a-Si was dehydrogenated by annealing in a vacuum chamber at 400 ˚C. Fig.2.4 (a) shows a SEM image of the surface of ELA poly-Si after Secco-etching [2]. From the figure, this standard poly-Si has the crystal grains the size of which is 300 nm in average. Generally, the mobility of the carriers taking part in the electric conduction becomes greater in a poly-Si with larger sized crystal grains, and the switching properties of the TFTs using such a poly-Si will be improved.

The surface morphology of the poly-Si, as well as the crystal grain size, is important characteristics of poly-Si which has influence on the electrical performance, especially on the threshold voltage and gate voltage endurance. Fig.2.4 (b) shows the AFM image of the surface of the ELA poly-Si. Root mean square (Rms) was observed to be 12.4 nm. Fig.2.4 (c) shows the cross-sectional TEM image of the ELA poly-Si. It can be seen that there are projections at grain boundaries. The height of the projection was observed to be less than 50 nm. The mechanism of ridge formation was explained in the literature [3, 4]. Conventional thickness of the gate insulator SiO_2 is 100 nm, which is sufficient to cover the entire roughness of the ELA poly-Si thin film.

2.4 Optimization of process conditions

In this development, the following process conditions were investigated:

(1) Ion implantation condition

In the process of ion implantation, the acceleration voltage of the ionized impurity atoms is important because the ionized impurity ions were accelerated and have to be implanted to the proper depth (near the interface between the poly-Si and the gate SiO_2 of TFT). Also, it is needed to investigate the optimized doze amount of the impurity atoms to obtain a low sheet resistance of poly-Si. These were studied by simulation and reference of the literature.

(2) Activation annealing time

Because the distortion temperature of the glass substrate used was 550 ˚C, the thermal annealing at the temperature over that must be avoidable. For this reason, the activation annealing temperature was set to be 500 ˚C, and the sufficient annealing time for the activation was investigated.

(3) Post metallization annealing temperature

As the structure of the source / drain electrodes, Ti / Al / Mo (Mo for top metal) was employed. Ti is the barrier metal to prevent the diffusion of Al into poly-Si during the thermal annealing process, and Mo is deposited to cover Al film which dissolves into the developing solution in photo lithography process. By performing PMA, a good metal / poly-Si contact characteristics can be obtained by forming Ti silicide at the Ti / poly-Si interface, and the proper annealing temperature for PMA was investigated.

In the following subsections, the experimental results of the investigation of each process conditions are elucidated.

2.4.1 Ion implantation condition

In the fabrication of LTPS TFTs, standard poly-Si thickness is 50 nm, and thickness of 100 nm for gate SiO_2 to cover the poly-Si island with the height of 50 nm is conventionally employed. To form source / drain regions in self-align manner, the ionized impurity atoms have to be accelerated and implanted to reach the poly-Si film through the gate SiO_2. Fig. 2.5 shows the schematic of formation of a self-aligned structure of source / drain region by ion implantation. By using this structure, the depth profile of the implanted impurity atoms was simulated by SRIM (The **S**topping and **R**ange of **I**ons in **M**atter) [5]. It was found that, though it depends on the density of the gate SiO_2, for ionized P and B atoms, the acceleration voltage to obtain the acceleration

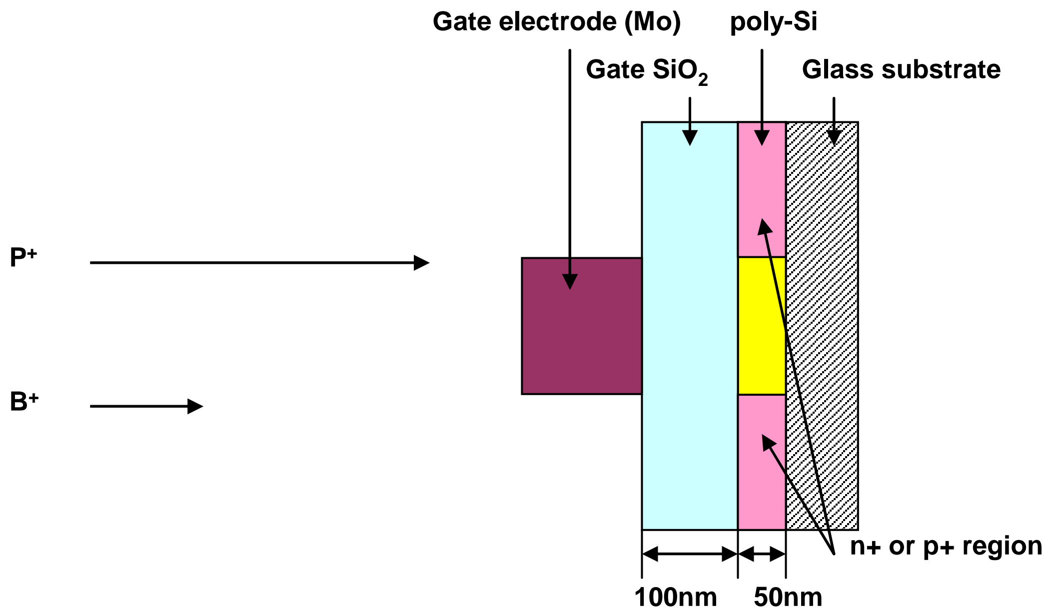


Figure 2.5: Schematic model of ion implantation of P or B atoms into 50 nm thick poly-Si through 100 nm thick gate SiO_2 for self-aligned formation of source / drain regions.

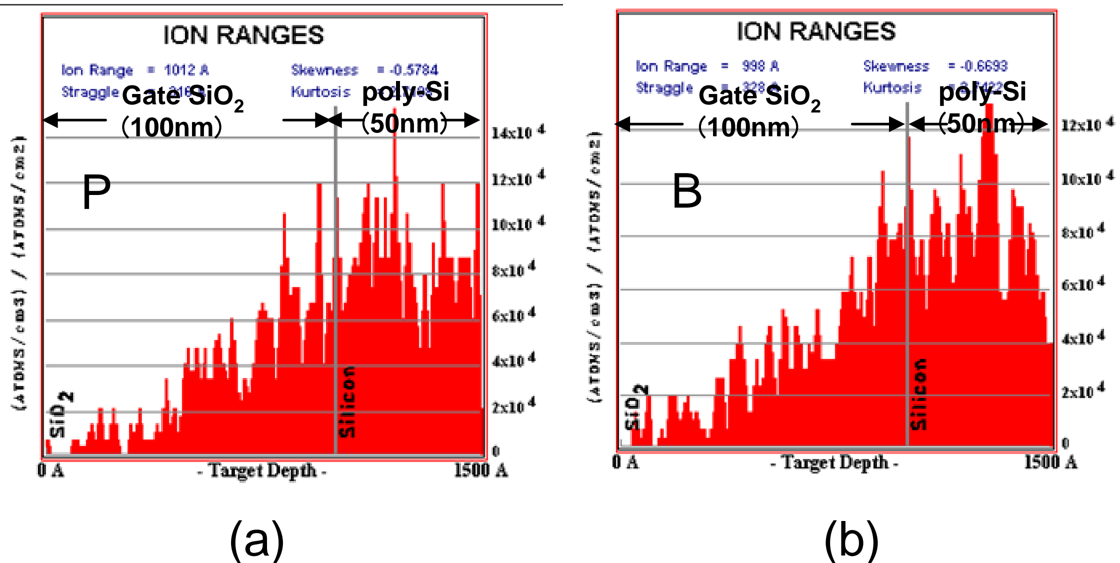
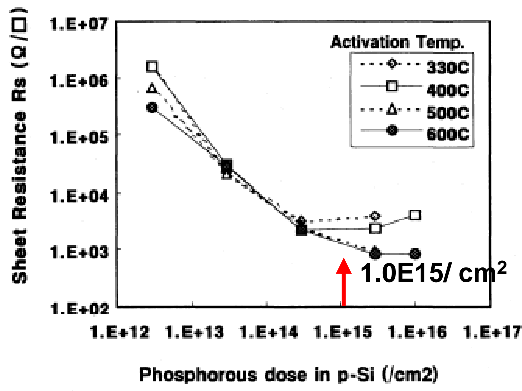
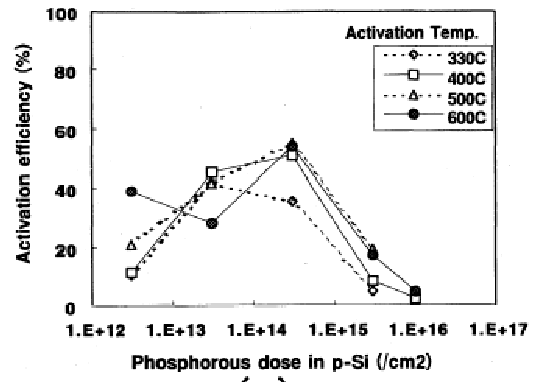


Figure 2.6: Depth profile of the concentration of implanted impurity atoms simulated by using SRIM; (a) P implanted by the acceleration voltage of 90 keV, (b) B implanted by the acceleration voltage of 30 keV.

energy to reach the poly-Si through the 100 nm thick gate SiO_2 is around 90 keV and 30 keV, respectively. In the simulations, the density of ideal thermal SiO_2 (2.21 g / cm^3) was used. Figs. 2.6 show the simulated depth profile of the implanted P and B atoms into poly-Si through 100 nm thick gate SiO_2. From the figures, it can be seen that the peak of the concentration profile is positioned at slightly poly-Si side from SiO_2 / poly-Si interface. To obtain good contact properties between the source / drain electrodes and poly-Si, it is desirable for the peak of the impurity concentration profile to be positioned around the SiO_2 / poly-Si interface. Although in the actual fabrication of TFT it is not usual for the thickness of the gate SiO_2 to be exactly 100 nm, and the density of the gate SiO_2 can become slightly different from the that of thermal SiO_2 with the change of its deposition conditions, these acceleration voltage for ion implantation was considered to be appropriate and was employed as reasonable condition in the development of the TFT fabrication.

For the doze amount of the implanted impurity atoms, the literature [6] is referred. Figs.2.7 show the graphs of the relationship between the doze amount and the sheet resistance poly-Si films and the activation ratio extracted from the reference. The activation ratio in this is defined as the ratio of the free carrier density evaluated by Hall effect measurement before and after the activation annealing. From the figure, it can be seen that at the doze of over 1.0E15 /cm^2, the poly-Si sheet resistance becomes saturated when annealed at the temperature of 500 and 600 ˚C for P atom. As for B atom, the sheet resistance of poly-Si increases at the doze of over 5.0E15 /cm^2. This is considered to be that the damage of Si lattices caused by the excess implantation cannot be recovered by the thermal annealing at the temperatures of 500 and 600 ˚C. By employing these results as reference, in this development of the LTPS TFT fabrication, the doze amount of 1.2E15 /cm^2 for P implantation and 3.6E15 /cm^2 for B implantation were set as experimental conditions.





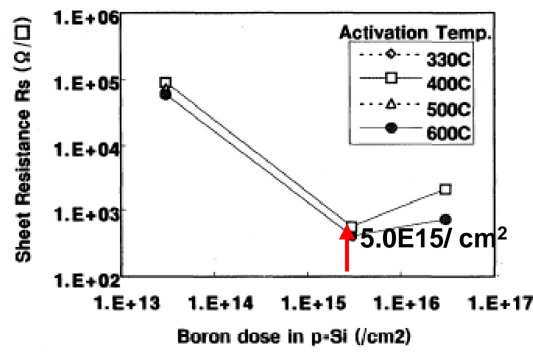


Fig.1 Dependence of sheet resistance on impurity dose.

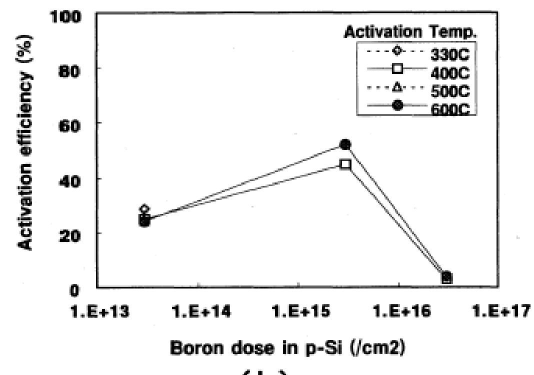


Fig.2 Dependence of activation efficiency on impurity dose.

Figure 2.7: Relationship between the doze amount and the sheet resistance of poly-Si (left), the activation ratio (right) [6].

2.4.2 Activation annealing time

Activation annealing is done to relocate the impurity atoms implanted into the poly-Si film in Si crystal lattice and to reduce the Si lattice defects generated by the implanted atoms. In this development the activation annealing at the temperature of 500 ˚C was performed, and to determine sufficient annealing time for activation the relationship between the annealing time and the poly-Si sheet resistance was investigated. Fig.2.8 shows the microscope image of the TEG (Test Element Group) for the evaluation of poly-Si sheet resistance. This TEG was designed to have large metal/poly-Si contact parts to reduce the effect of the contact resistance, and the part through which the electric current is flow to be thin and long so as for the current to flow in one direction. The current – voltage (I-V) measurement was carried out by using this TEG to obtain the resistance of the TEG, and the sheet resistance of the poly-Si was calculated by dividing the resistance by the area (1000 μm^2 ≡ 1000 □).

Figs. 2.9 show the relationship between the obtained sheet resistance of poly-Si and the activation annealing time. The measured values obtained from over ten TEGs were averaged to be plotted. From these graphs, it was not clearly readable that the sheet resistance of poly-Si is depended on the activation annealing time. However, it can be considered that the sheet resistance got saturated after the activation was progressed owing to the fact that for over 4 hour annealing, the sheet resistance became stable. From these results, the experimental activation annealing time was set to be 6 hours in this development of LTPS TFT fabrication.

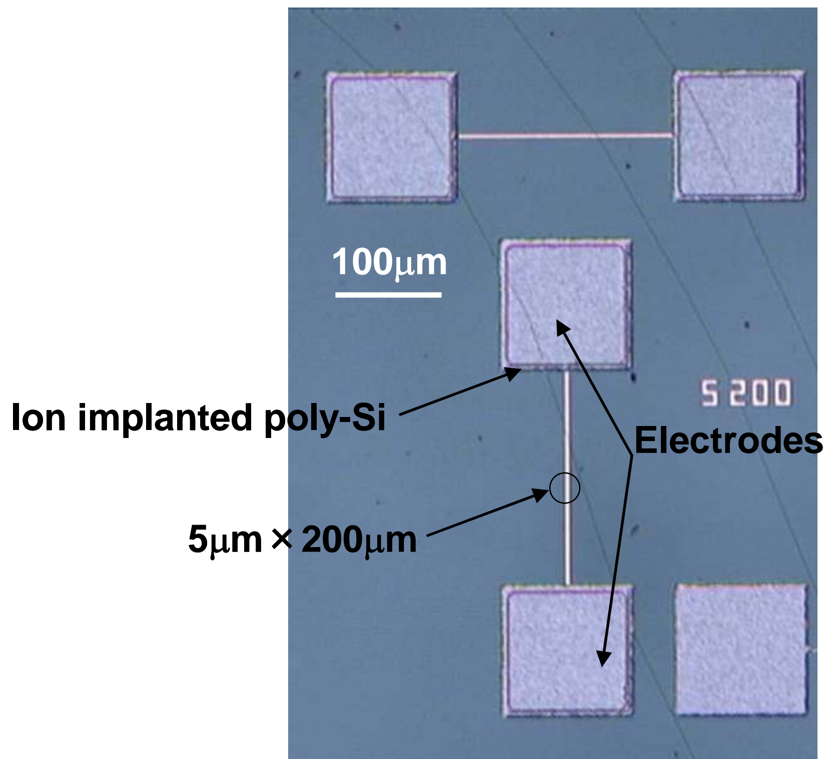


Figure 2.8: Test element group for the measurement of the sheet resistance of poly-Si.

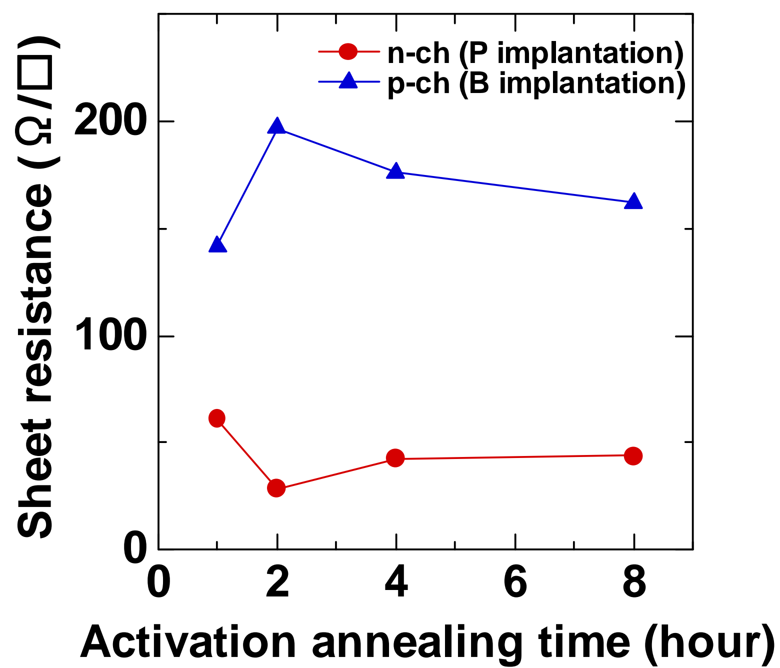


Figure 2.9: Relationship between the sheet resistance of poly-Si and the activation annealing time.

2.4.3 Post metallization annealing temperature

After the formation of the source / drain electrodes, thermal annealing (sintering) is performed to obtain good contact property between the electrode metal and poly-Si. This post metallization annealing (PMA) is generally done in the ambient of forming gas (N_2 gas in which H_2 is contained in volume ratio of around 10 %). This is an important process which leads to improvement of the device performance because the hydrogen in the forming gas has a passivation effect on the poly-Si / gate SiO_2 interface and the crystal defect such as the grain boundary. In this development of LTPS TFT fabrication, the contact metal to the poly-Si is Ti, and the PMA temperature dependence of contact resistance was investigated to determine the PMA temperature to obtain good contact characteristics between poly-Si and Ti. Fig. 2.10 shows the microscope image of the TEG for the evaluation of the contact resistance. The measurement of the contact resistance was performed by measuring the resistance calculated from the voltage drop between the electrode V1 and V2 and the current flowing between V3 and V4 when the difference of voltage between V3 and V4 was set to be 0.1 V, and multiply it with the area of the contact hole (400 μm^2).

Fig. 2.11 shows the relationship between the contact resistance and the PMA temperature. The contact resistance obtained by PMA of 450 ˚C was found to be lower than that obtained by PMA of 400 ˚C for both P implantation and B implantation. This is considered to be that the reaction of Ti and poly-Si to form Ti silicide at the poly-Si / Ti interface was more progressed in the PMA of 450 degree than in the PMA of 400 ˚C. When PMA of 475 ˚C was performed only for P implanted poly-Si, the contact resistance was found to be larger than that obtained by PMA of 400 ˚C, which can be due to the aggregation of Ti silicide associated with the increase in the annealing temperature. From these results, the PMA temperature was set to be 450 ˚C.

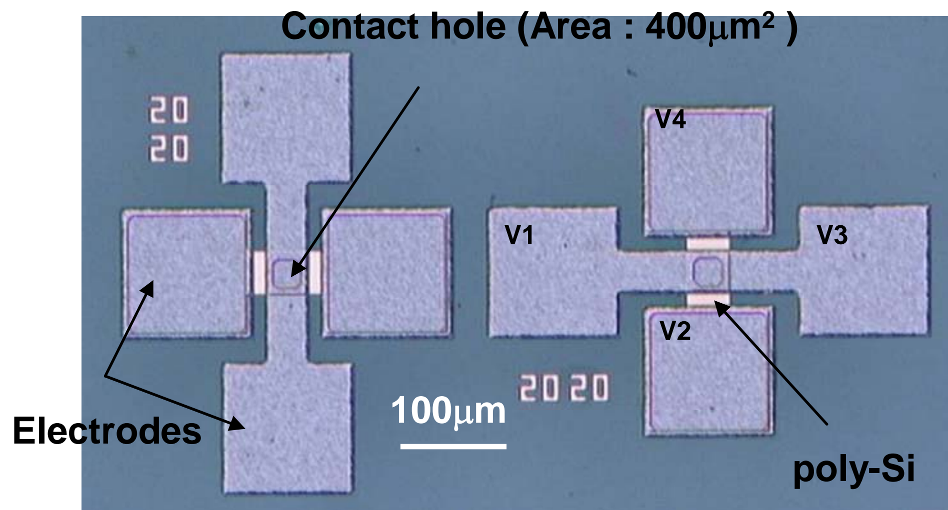


Figure 2.10: Test element group for the measurement of the contact resistance.

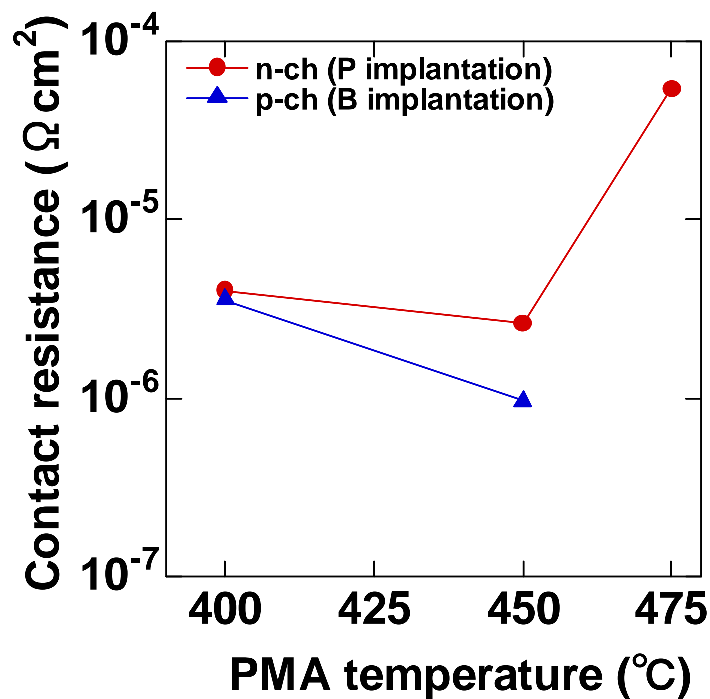


Figure 2.11: Relationship between the contact resistance and the PMA temperature.

2.5 Electrical measurement of ELA poly-Si TFTs

Figs. 2.12 show the typical transfer characteristics of n-ch TFTs of different PMA temperature, and Table 2.2 shows the transistor characteristics taken from the transfer curves of the TFTs in the liner region. The electrical measurement was performed by using Agilent 4156C precision semiconductor parameter analyzer. From these, the TFTs annealed at 450 ˚C showed the largest field effect mobility and the smallest sub-threshold swing. This is considered to be originated from the good contact characteristics obtained for PMA at 450 ˚C, as well as from the effective passivation of poly-Si / SiO_2 interface and the crystal grain boundaries in poly-Si by the hydrogen in the forming gas. The field effect mobility and the sub-threshold swing of the TFTs annealed at 475 ˚C were both degraded, which could be caused by the increase in the contact resistance and removal of the hydrogen from the poly-Si / gate SiO_2 inter face and poly-Si film. From these results, 450 ˚C was found to be suitable for the PMA temperature, and the P implantation condition and activation annealing condition were both considered to be within the optimized level because of the good contact and sub-threshold characteristics both in the liner and saturation region.

Figs. 2.13 show the typical transfer characteristics of p-ch TFTs of different PMA temperature ((a) and (b)), and with different Boron dose (1.2E15 /cm^2) (c). Table 2.3 shows the transistor characteristics taken from the transfer curves of the TFTs in the liner region. Owing to the fact that the mobility of hole in Si is smaller than that of electron, the p-ch TFTs show smaller field effect mobility than that of n-ch TFTs. However, to construct CMOS circuits by utilizing n-ch and p-ch TFTs, the field effect mobility of p-ch TFTs have to be within the range between one half and one third of that of n-ch TFTs, and the field effect mobility of p-ch TFTs ((a) and (b)) was smaller than one third of that of n-ch TFTs. This was considered to be originated from the insufficient

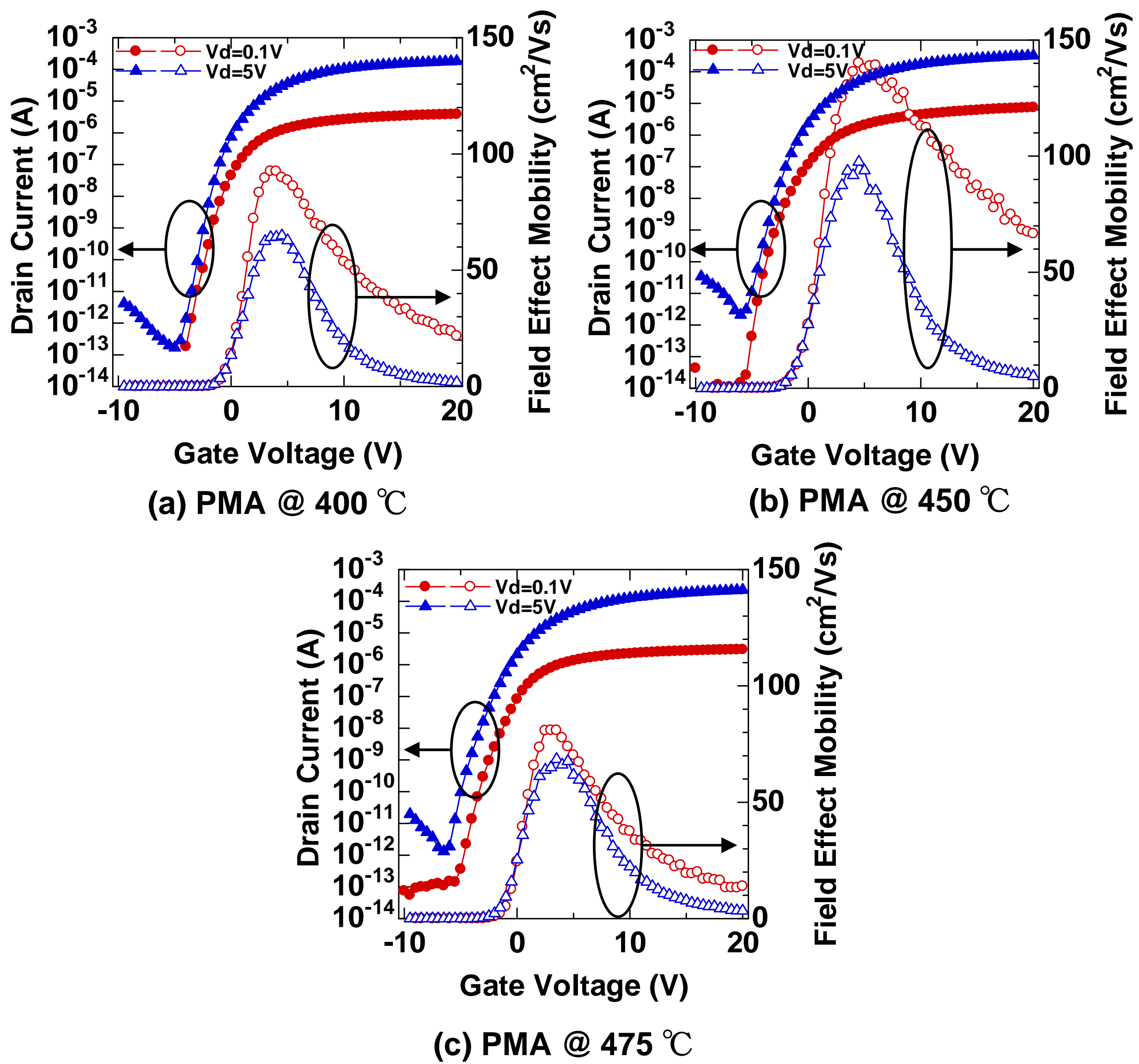


Figure 2.12: Transfer characteristics of n-ch TFTs with different PMA temperature (W/L = 5/5 [μm]).

Table 2.2: Characteristics of the n-ch TFTs shown in the Figure 2.12.

PMA temperature (℃)	400	450	475
Field effect mobility (cm^2/Vs)	92.6	140.2	80.9
Threshold voltage (V)	-0.8	-1.8	-1.2
Sub-threshold swing (V/decade)	0.56	0.41	0.63

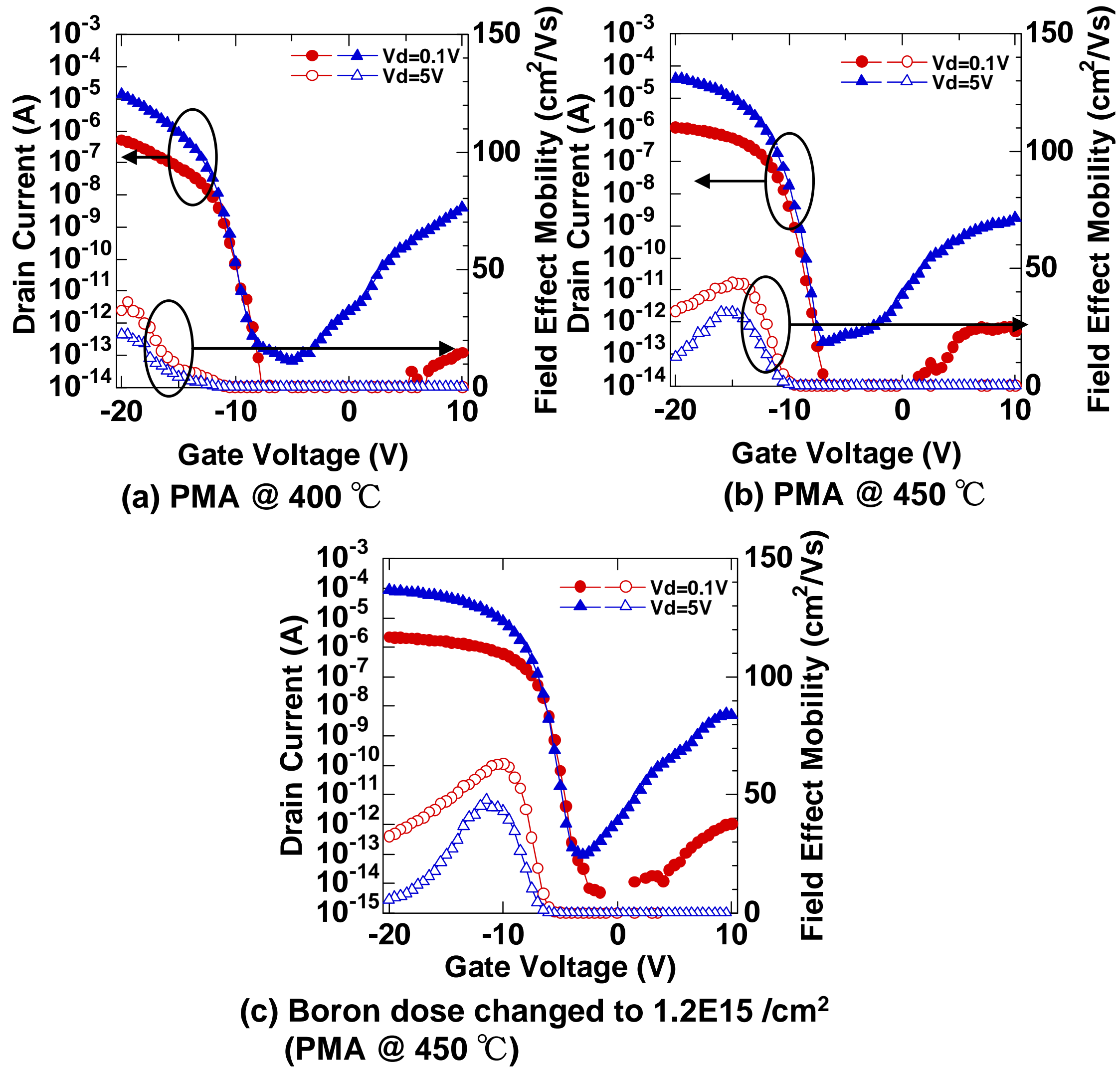


Figure 2.13: Transfer characteristics of p-ch TFTs with different PMA temperature (a) and (b), and with different Boron dose (1.2E15 /cm^2) (c) (W/L = 5/5 [μm]).

Table 2.3: Characteristics of the p-ch TFTs shown in the Figure 2.13.

PMA temperature (℃)	400	450	450
Field effect mobility (cm^2/Vs)	36.3	41.1	63.1
Threshold voltage (V)	-12.2	-10.4	-6.3
Sub-threshold swing (V/decade)	0.41	0.48	0.41

Boron dose changed to 1.2E15 /cm^2

activation of p+ regions, so the B implantation dose was reduced to the same amount as that of P implantation dose (1.2E15 /cm^2). As shown in Fig. 2.13 (c), the transfer characteristics of p-ch TFT was improved by the reduction of the B dose. The field effect mobility increased over 60 cm^2 / Vs and the threshold voltage was shifted to 0 V. Thus, to fabricate CMOS-compatible n-ch and p-ch poly-Si TFT, it was found that the impurity dose of P and B was set to be the same in this fabrication process. However, the threshold voltages of the fabricated n-ch and p-ch TFTs were slightly shifted to negative voltage. This was thought to be caused by the positive fixed charge in the gate SiO_2 and / or the interface of the gate SiO_2 and poly-Si film. This must be reduced by further optimization of SiO_2 deposition condition and poly-Si surface cleaning procedure, which will be the future works.

2.6 Summary

In this chapter, the development of the fabrication of LTPS TFTs using conventional two-dimensional substrate was treated. As a standard LTPS, excimer laser anneaing crystallized poly-Si was utilized. In the fabrication of n-ch TFTs, P was ion-implanted with the acceleration voltage of 90 keV and the doze amount of 1.2E15 /cm^2, and in the fabrication of p-ch TFTs, B was ion implanted with the acceleration voltage of 30 keV and the doze amount of 3.6E15 /cm^2. The activation annealing was performed at the temperature of 500 ˚C for 6 hours. n-ch TFTs and p-ch TFTs were fabricated under the PMA condition of 400, 450, 475 (only for n-ch TFTs) ˚C, and the contact characteristics and TFT characteristics were evaluated. As a result, at the PMA condition of 450 ˚C, TFTs with highest performance in the contact and transistor characteristics was fabricated, which showed the field effect mobility of around 150 cm^2 / Vs for n-ch TFTs and 50 cm^2 / Vs for p-ch TFTs taken in the liner region. Furthermore the

performance of the p-ch TFT was improved by employing the B implantation dose same as that of P implantation dose (1.2E15 /cm^2). From the literature, it can be said that the field effect mobility of the fabricated TFTs was in top-level characteristics compared to the poly-Si TFTs using the ELA poly-Si with the same size of crystal grains [7]. Although further process optimization for improvement of sub-threshold characteristics of the poly-Si TFTs is still needed, it is concluded that, in point of reflecting the poly-Si crystallinity to the TFT performance, the development of LTPS TFT fabrication process was successfully performed.

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Chapter 3

Laser crystallization and development of poly-Si TFT using one-dimensional fiber substrate

3.1 Introduction

Recently, both in the LSI industry and flat-panel active-matrix liquid crystal display (FPD) industry, the size of silicon wafers and glass substrates of a thin-film transistor (TFT) array has continuously increasing and now exceed 6 m^2 (Generation 10) for FPD; therefore, it is necessary to construct a huge fabrication apparatus for handling such wide substrates. Thus, the expansion of substrates has inevitably led to manufacturing factories of unprecedented scale, which require enormous amounts of capital investment. It is also important to construct and operate such a production system in an environmental friendly manner, which, with the process being of larger scale, imposes further technological demands [1].

From the concept opposite to the enlargement of these two-dimensional substrates, it can be said that it is possible for a new processing technology and product areas to be opened if a microelectronic device using semiconductor thin films can be made on a thin linear one-dimensional substrate such as a thin glass or a plastic fiber through high-speed, low-cost fabrication. The advantage of a fiber substrate lies on the fact that because of the one-dimensionality of its shape, which extends freely in only in

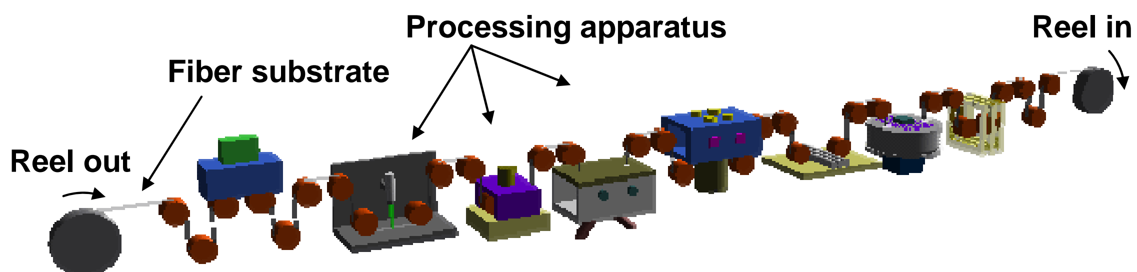

Figure 3.1: Schematic image of the reel-to-reel fabrication process using one-dimensional substrate.

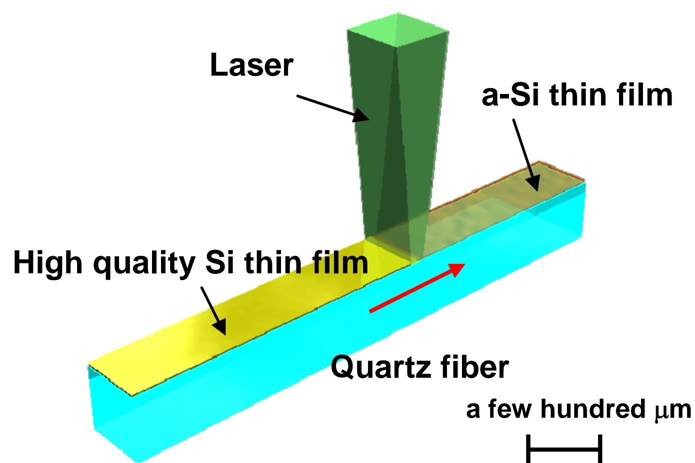

Figure 3.2: Schematic image of high quality Si crystallization by laser annealing of a-Si on a fiber.

one direction, it can be applied to a reel-to-reel process as shown in Fig. 3.1 for which fabrication systems are more compact than those in the case of using large two dimensional substrates. Thus, the characteristic shape of fibers is potentially applicable to various devices such as linear scanning heads of optical sensors, and by assembling many fibers, it is possible to fabricate flexible two dimensional active-matrix device [2]. Furthermore, because such device is fabricated as a compact substrate, its application in disposable biosensors is advantageous because it can be made to be low emitting [3].

According to this background, we propose the fabrication of poly-Si TFT on a quartz fiber, which we named as “Fiber-TFT”, as an example of the fabrication of microelectronic devices on a one-dimensional substrate. Quartz fibers have advantages such as those which can be prepared in any cross-sectional shape by conventional optical fiber fabrication, and also, they have good thermal endurance, which is convenient for high temperature treatment. Also, a-Si thin film on a quartz fiber can be considered to be suitable for the lateral crystallization processes by using such as laser annealing or RF zone melting. So far, there has been no experimental works on the lateral crystallization on a limited area such as on the surface of a fiber, not to mention on the fabrication of thin film devices using the Si films formed in such a way on the thin one-dimensional substrate. One of the possible advantages of this crystallization scheme is that by modulating the uniformities of the crystal growth on the fiber substrates a complete single crystallization of Si thin films can be expected as illustrated in Fig. 3.2, and by utilizing such a high quality Si thin films it is possible to fabricate high performance switching devices on the fibers.

Fig.3.3 shows a conceptual image of a Fiber-TFT for driving OLED devices as one example of Fiber-TFT application. This is the device utilizing a one dimensional substrate for driving each OLED device by combining it with a Fiber-OLED, which is an array of OLED devices on a fiber. Ultimately, by assembling many Fiber-TFTs and

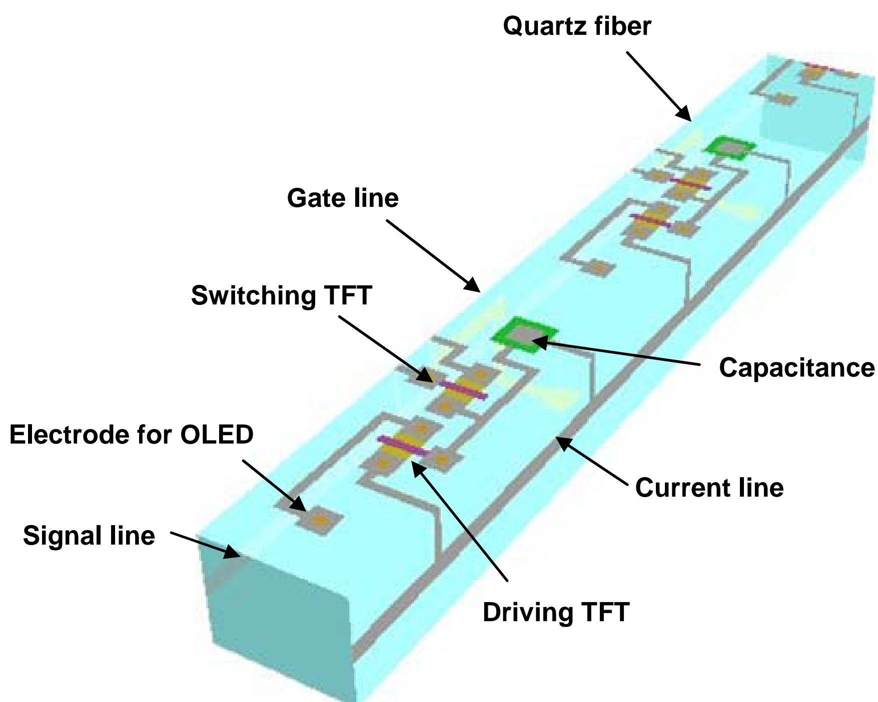

Figure 3.3: Schematic image of a Fiber-TFT for driving OLED.

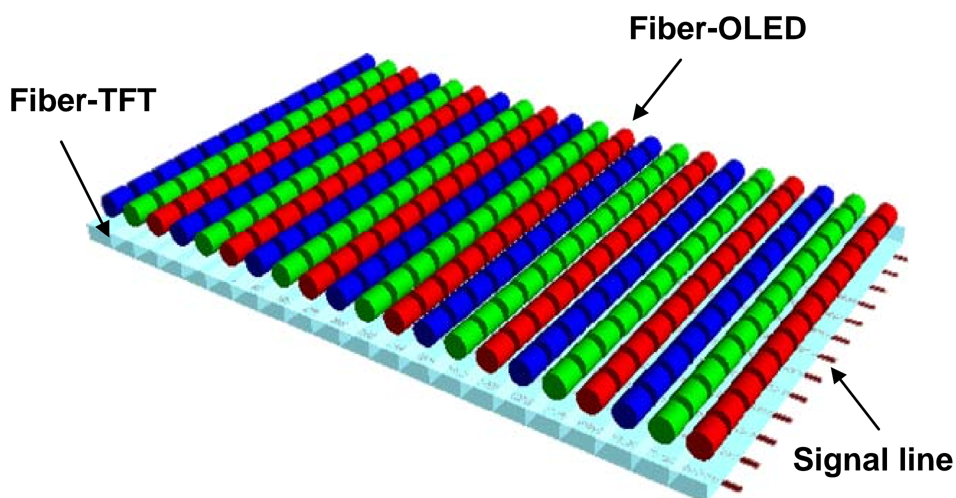

Figure 3.4: Schematic image of a TFT-OLED display assembled from Fiber-TFTs and Fiber-OLEDs.

Fiber-OLEDs with gate lines, a flexible TFT-OLED display of arbitrary size can be fabricated, as shown in Fig. 3.4. The fabrication method of flat panel displays like this is originated from a concept which fundamentally differs from that of current batch process. That is, as fibers can in practical be prepared to have unlimited length, wide area displays at any large size can be fabricated in principle through the assembly of each fiber devices. As mentioned above, this fiber-type device or module is well-fitted for the reel-to-reel fabrication process, which can be realized in small-sized manufacturing facilities. As the same time, device fabrication in low cost and low environmental load is expected.

In this study, the establishment of the peripheral process techniques needed for fabrication of poly-Si TFTs on such thin substrates was exclusively worked on. For the formation of poly-Si on the fibers, laser annealing crystallization of a-Si thin films deposited on the fiber substrate was demonstrated and the crystallinity of the resulted poly-Si was evaluated by comparing that crystallized on conventional flat glass substrates. Finally, LTPS TFTs were fabricated by the process scheme established in this study for the first time, and the electrical characteristics of the fabricated TFTs were evaluated.

3.2 Laser annealing crystallization using one-dimensional substrate

It is an important task to crystallize a-Si to form high quality poly-Si on the fiber in the fabrication of Si micro-electronic device using such one-dimensional substrate. This time, the excimer laser was irradiated to crystallize a-Si on fiber, and the crystallinity was evaluated.

Figs. 3.5 shows the quartz fiber used as the substrate, which was fabricated by

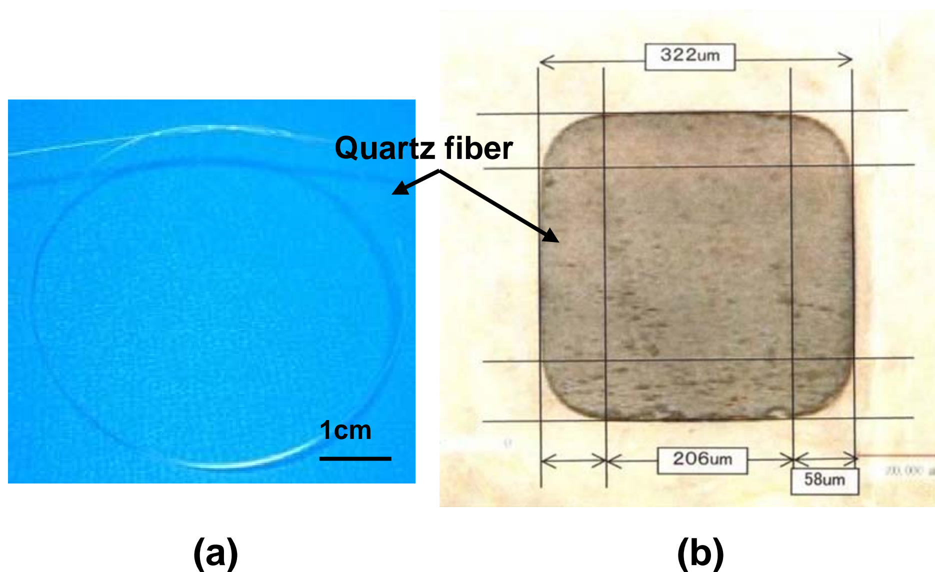

Figure 3.5: (a) Quartz fiber used as substrate of poly-Si TFT fabrication. When coated with plastic, it can be flexible. (b) Cross-sectional image of fiber after plastic coating is stripped. It has a square cross section with four flat faces on which poly-Si TFTs are to be fabricated.

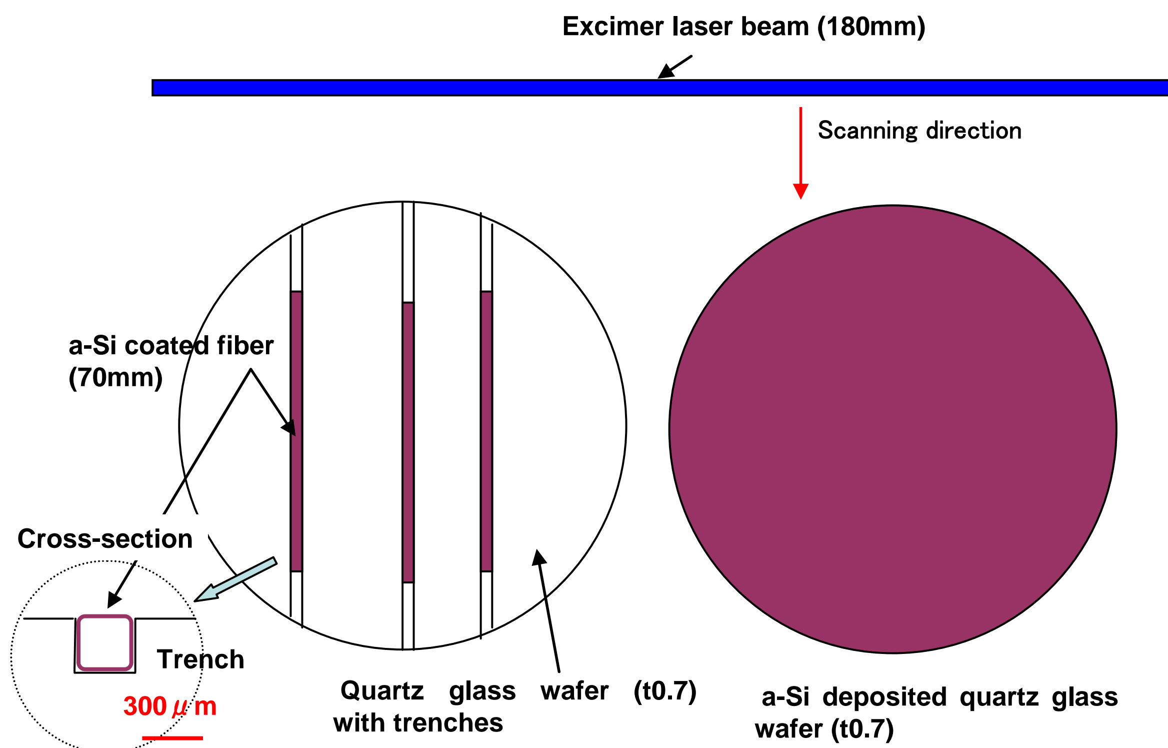

Figure 3.6: Configuration of the excimer laser annealing of a-Si on fiber and on wafer.

the same drawing process as that of typical optical fibers. When coated with plastic after the TFT fabrication, the fiber can be bent freely, as shown in (a), which makes it applicable to flexible devices. The cross section of the fiber is rectangular, as shown in (b), with four flat faces of widths approximately 200 μm. This kind of fiber can be prepared using a rectangular quartz glass preform, which is then placed in a drawing furnace as the seed material of the fiber.

Fig. 3.6 shows a schematic image of the procedure of the excimer laser annealing crystallization of a-Si on fibers. The a-Si coated fibers were embedded into the trenches with the width slightly larger than that of fibers formed in a 4-inch quartz glass wafer with the thickness of 0.7 mm. Then the wafer was loaded into the processing chamber of the excimer annealing system, and the excimer laser was irradiated on the a-Si on fibers. For comparison, the same a-Si was deposited a quarts wafer same as that used for the trench substrate, and the a-Si was laser crystallized at the same time as the fibers.

Fig. 3.7 shows the SEM observation of the poly-Si on fiber crystallized by ELA with the laser energy density of 370 mJ / cm^2. From the image, it was confirmed that the poly-Si with the crystal grain size of approximately 300 nm was successfully obtained. Fig. 3.8 shows SEM images of ELA poly-Si on fiber and on wafer with increasing laser energy density and Fig. 3.9 shows the relationship between average grain size of ELA poly-Si on fiber and on wafer. By increasing the energy density of the laser from 350 to 430 mJ / cm^2, it was observed that the crystal grains of the poly-Si grew in size from 70 to 500 nm. No anisotropy of the shape of the crystal grains with respect to the scanning direction of the laser was observed, as in the case of the crystallization of a-Si on a normal quartz glass substrate. Interestingly, the poly-Si on fiber exhibit larger crystal grains than that on wafer. The crystallization laser energy density reduction was estimated as 5 %. Though detailed mechanism of this still needs further investigation, it is strongly suggested that by using fiber, it can be possible to modulate the behavior of

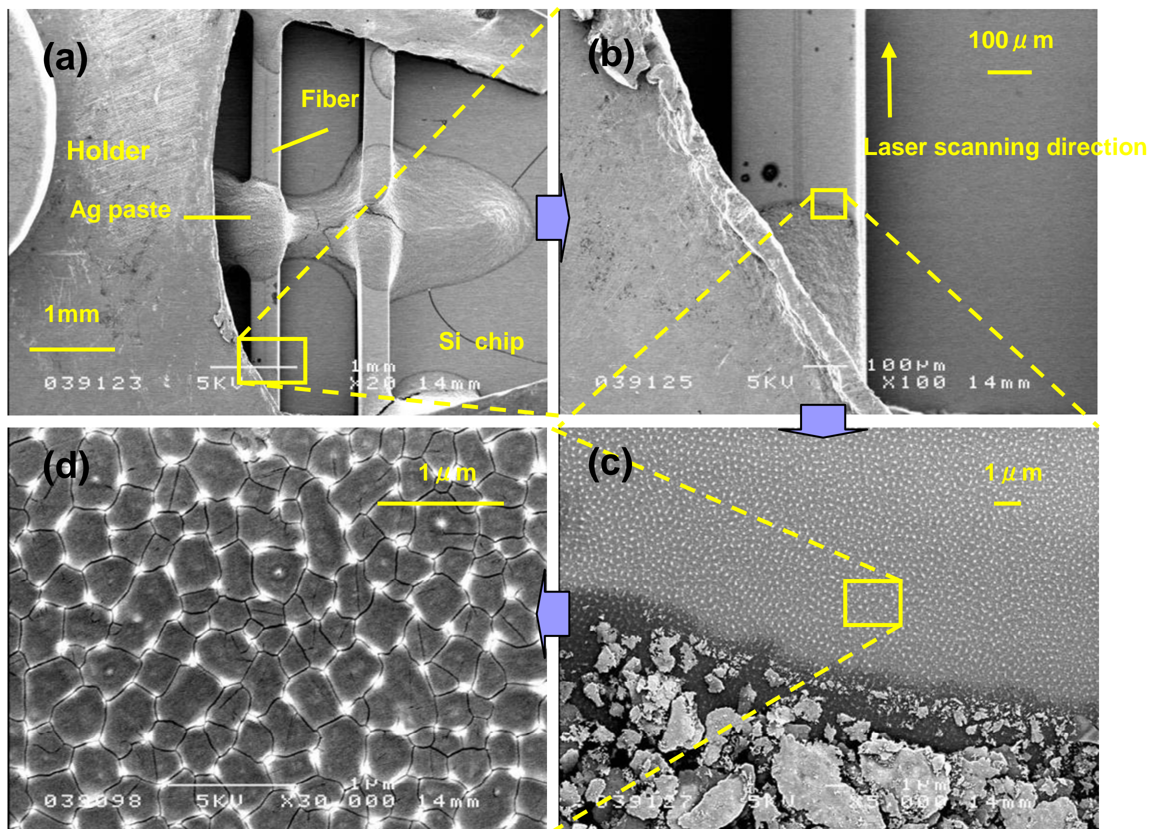

Figure 3.7: (a)–(d) Series of magnified SEM images of surface of ELA poly-Si on fiber.

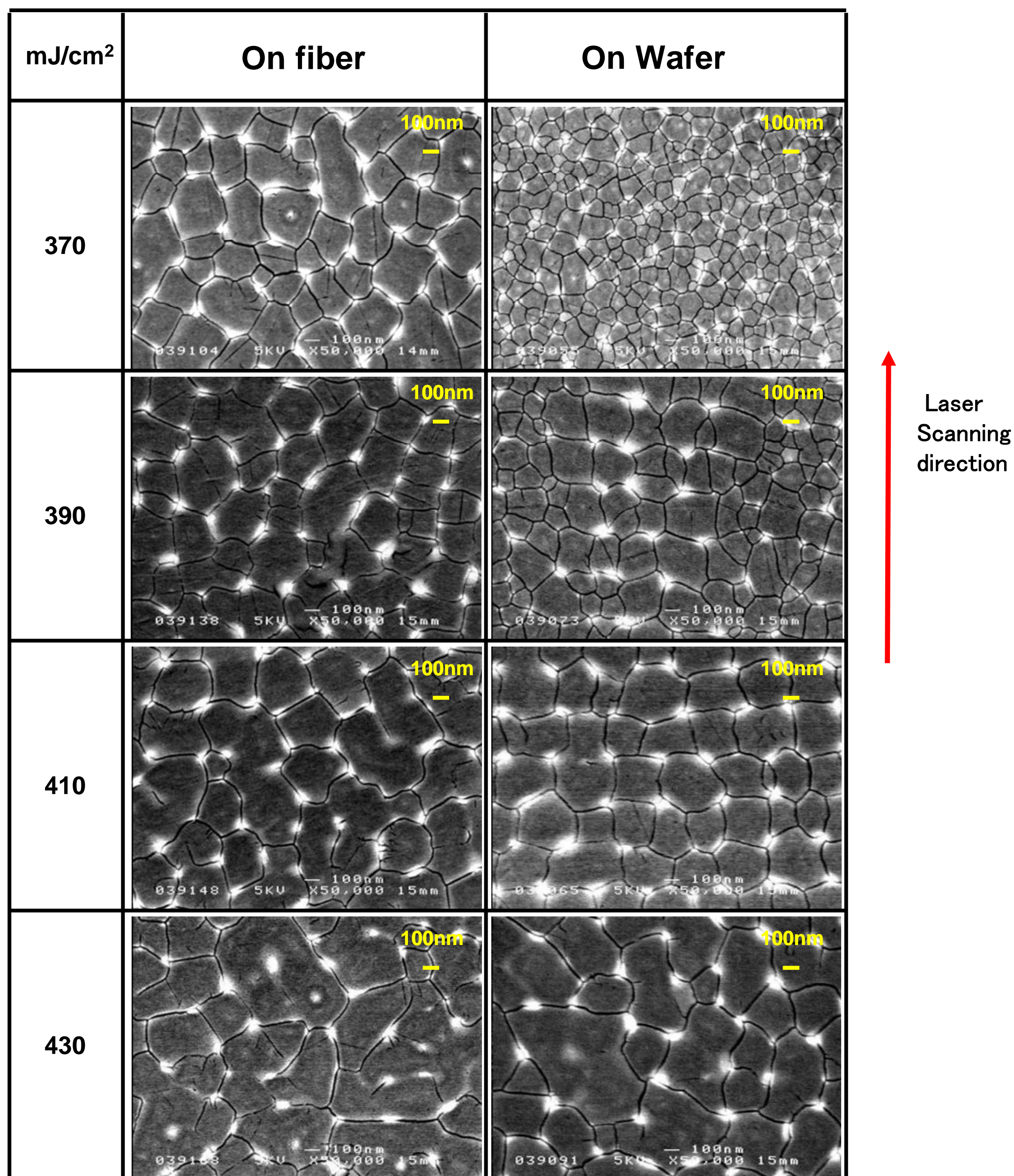

Figure 3.8: SEM images of ELA poly-Si on fiber and on wafer with increasing laser energy density.

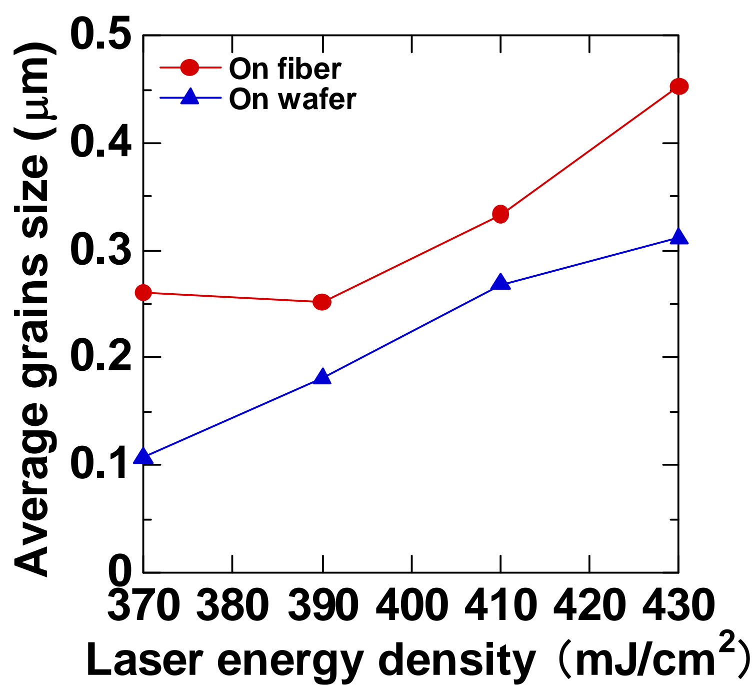

Figure 3.9: Relationship between average grain size of ELA poly-Si on fiber and the laser energy density.

laser crystallization of a-Si.

3.3 Development of Fiber-TFT

This work is regarded as a basic study of the development of thin film poly-Si devices utilizing one dimensional substrate such as fiber. As for the direction of the study, its ultimate goal is to leave off the batch process completely. However, at this early stage of the establishment of basic fabrication process it was aimed to develop a standard device fabrication process to which the batch process using flat substrates is applied.

A photo mask pattern was designed to fabricate TEG pattern of TFT on fiber as shown in Fig. 3.10 within a thin and long region of the flat face of the fiber. Fig. 3.11 shows a typical layout of the designed photo mask pattern.

The basic fabrication scheme of Fiber-TFTs is depicted in Fig. 3.12. First, fibers cut with the length about 50 mm were wet-cleaned. This was done by utilizing a tool made from teflon for the wet-cleaning of fibers. Next, to deposit a-Si thin film on the fibers, the cut fibers were inserted into the holes opened on the surface of a quartz substrate. Then the fibers were put into the LPCVD chamber together with the quartz substrate by handling it so as not to touch the cleaned fibers. A 50 nm thick a-Si thin film was deposited on the surface of fibers in a condition as follows; the gas flow of He-diluted (50 %) SiH_4 was 119 sccm, that of N_2 was 150 sccm, the pressure was 0.25 Torr, temperature of chamber was 520 ˚C degree and the deposition time was 60 min. Next, a special quartz substrate was prepared in which a rectangular trench with a width and a depth slightly larger than 300 μm, which are close to those of the fiber, is formed. The trench was formed by cutting the quartz substrate up to a depth of 300 μm using a dicing saw. Then the fiber was embedded in the trench, forming a nearly flat plane of the surface of the quartz substrate complemented by that of the fiber, which enables the whole substrate to be handled as a normal glass substrate through various processes of

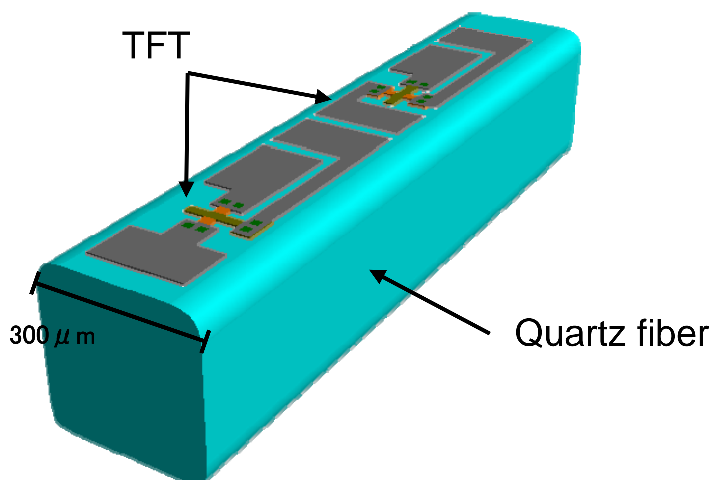

Figure 3.10: Schematic image of TFT TEG on the fiber.

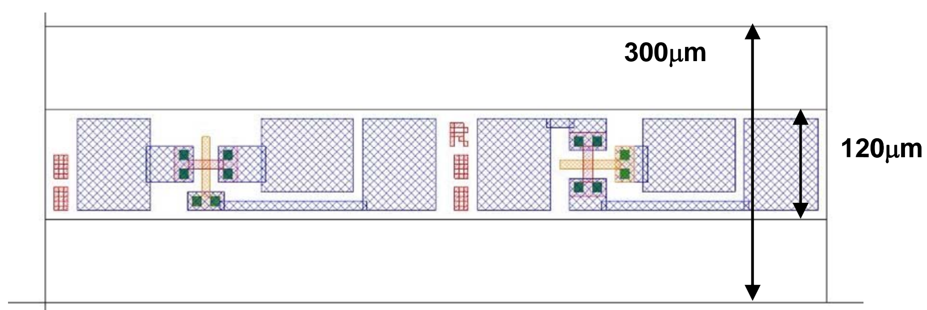

Figure 3.11: Designed photo mask pattern for the TFTs on the fiber.

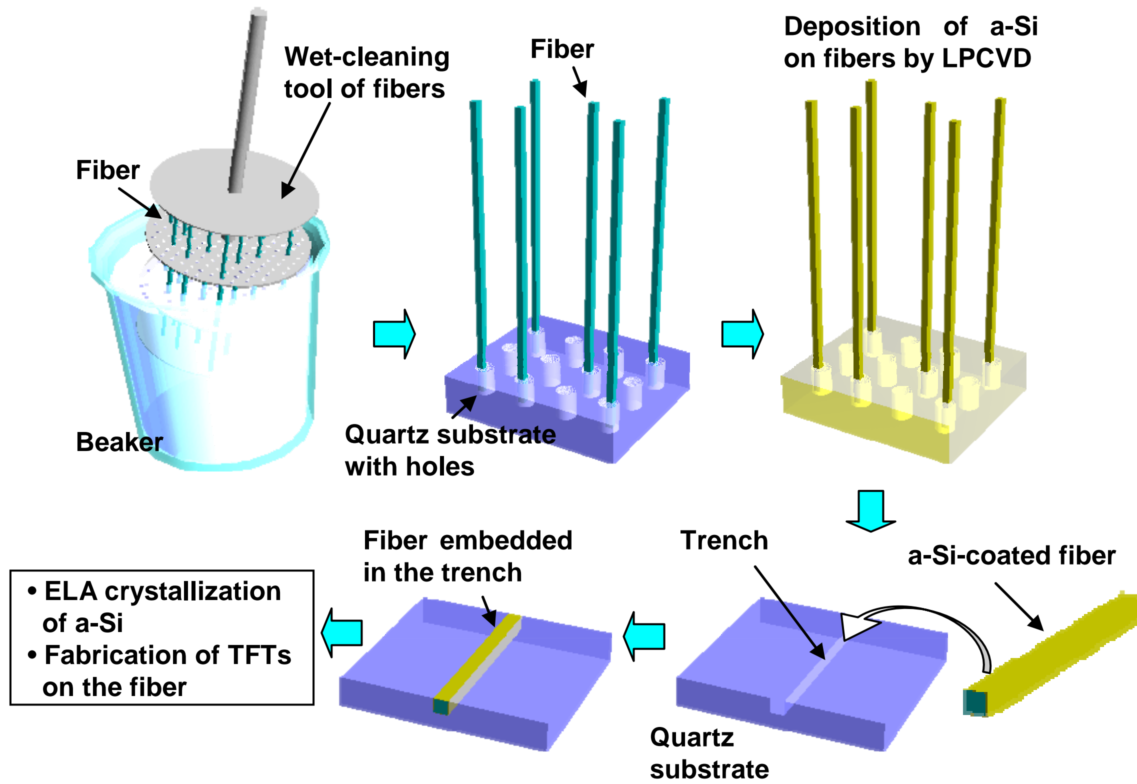

Figure 3.12: Basic scheme for the handling of fiber substrates.

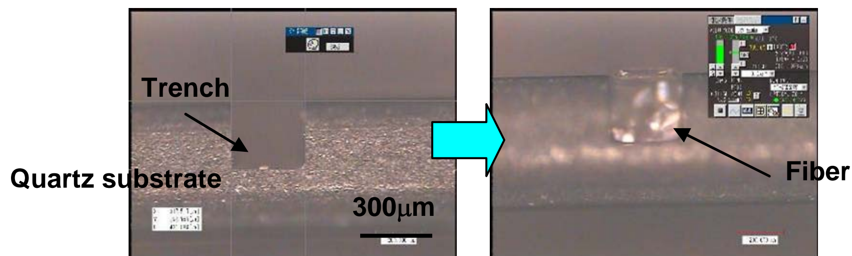

Figure 3.13: Cross-sectional microscope images of the fiber embedded into the trench formed in a quartz substrate.

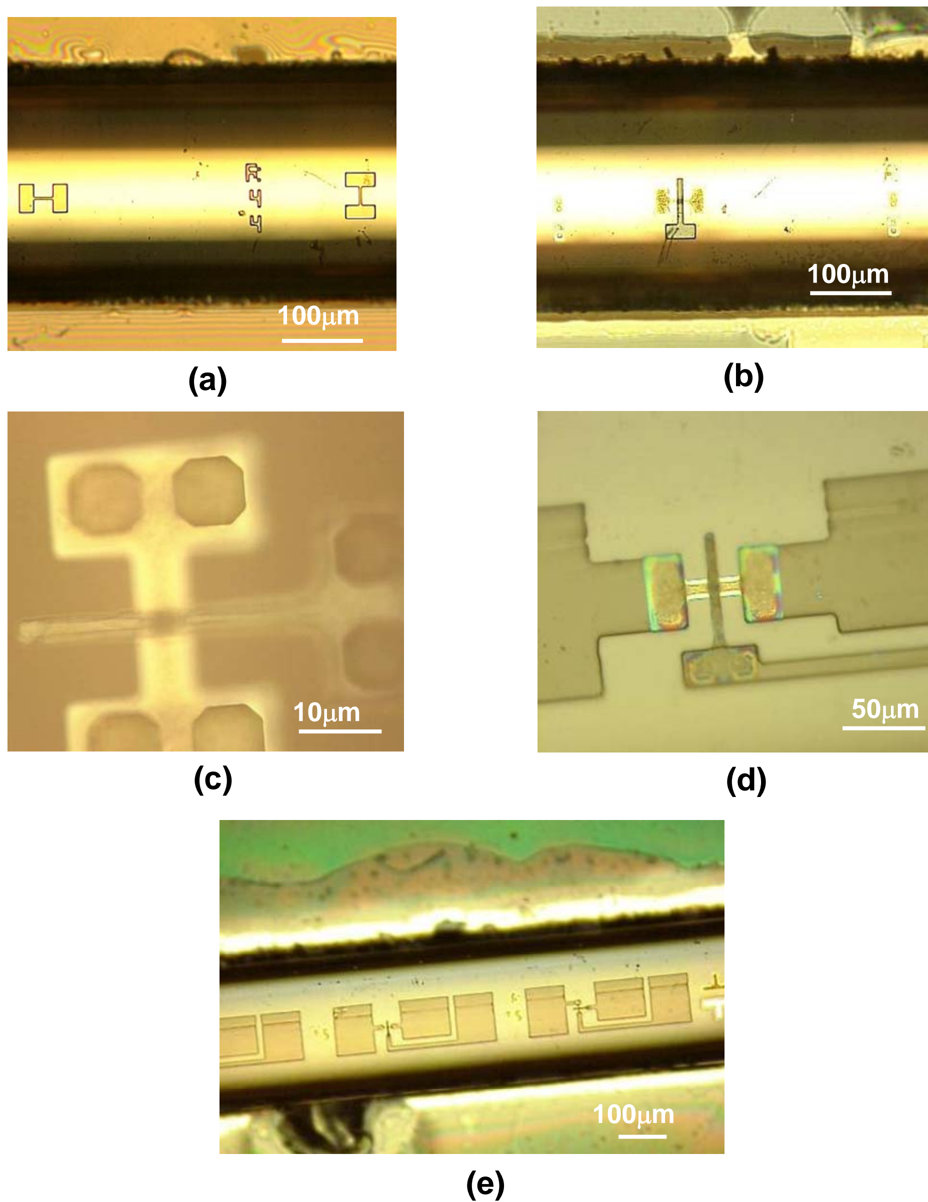

Figure 3.14: Microscope images of TFTs on fiber during fabrication.
(a) after Si island formation, (b) after gate electrode formation, (c) after contact hole opening, (d) after source / drain electrode formation, (e) overall view of the TFTs.

ELA crystallization of a-Si on fibers and the subsequent TFT fabrication. Fig. 3.13 shows the cross-sectional optical microscope images of the fiber embedded into the trench in the quartz substrate. It was confirmed before the actual process that the embedded fiber did not fall out from the trench during photo lithography process.

Figs. 3.14 show microscope images of the TFTs on a fiber during the fabrication by embedding the fiber into the trench on the quartz substrate. It was demonstrated that Si island etching, gate electrode formation, contact hole opening and source / drain electrode formation can be performed by employing the basic scheme described above.

3.4 Electrical evaluation of poly-Si TFTs on fiber

Top-gated TFTs were fabricated using the ELA crystallized poly-Si through conventional self-alignment process by employing the scheme described above. After the crystallization of *a*-Si on the fiber with the laser energy density of 370 mJ/cm^2, the surface of the poly-Si layer was wet cleaned, then a gate SiO_2 of 100 nm thickness was deposited by plasma-enhanced chemical vapor deposition using a tetraethoxysilane gas source. A 250 nm thick Mo film was deposited and patterned to form a gate electrode. Phosphorous was implanted to form source and drain regions. After a 400 nm thick SiO_2 layer was deposited, the samples were furnace annealed at 500 °C for impurity activation. After contact holes were formed, the source/drain electrode (Ti/Al/Mo) was formed. Finally, post metallization annealing was performed for 1 h at 450 °C in a forming gas atmosphere.

Figs. 3.15 show micrographs of the TFTs fabricated on the fiber, indicating that the patterning of the TFTs on the fiber was done through the fabrication scheme. The transfer and output characteristics of TFTs with a channel length of 6 μm and a channel width of 8 μm were evaluated using a semiconductor parameter analyzer and are shown

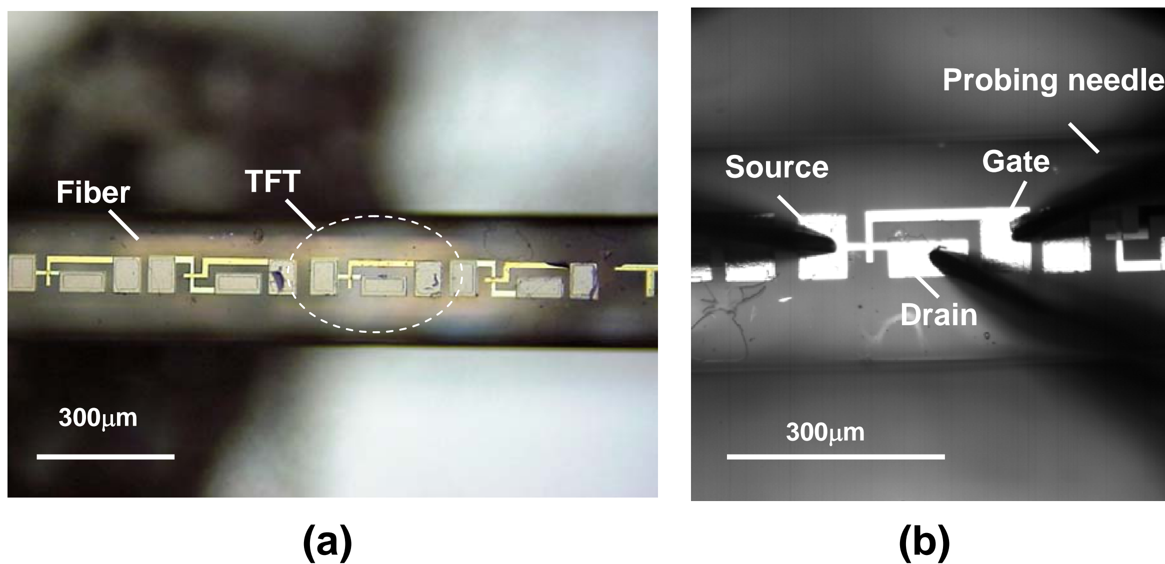

Figure 3.15: (a) Microscope image of TFTs fabricated on fiber, (b) Magnified image of measurement of the TFT.

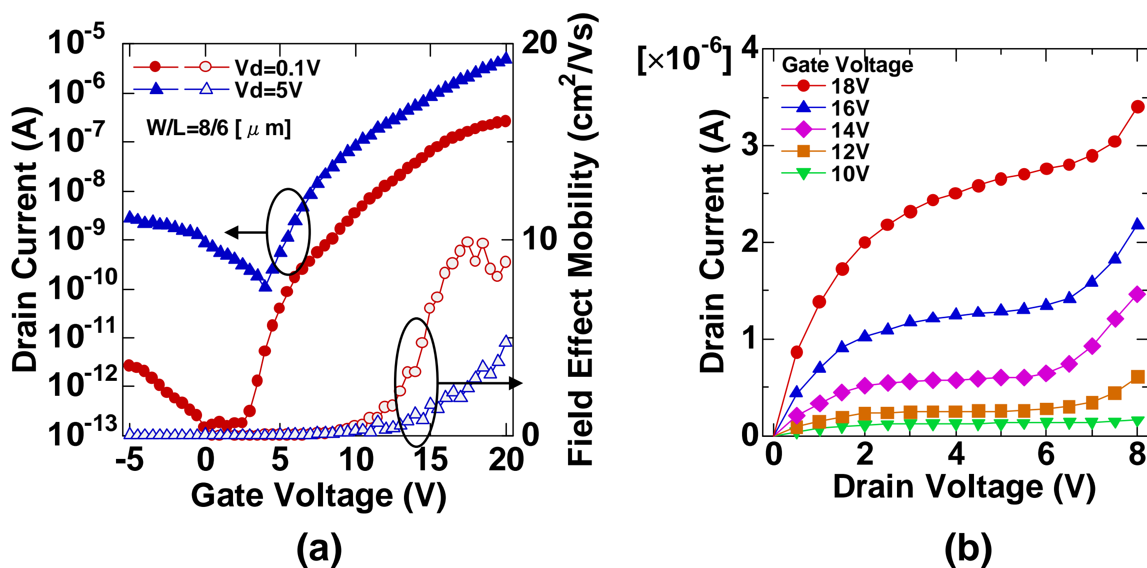

Figure 3.16: (a) Transfer curves and calculated field effect mobility curves for TFT, (b) Output characteristics of TFT.

in Figs. 3.16 (a) and (b), respectively. From the figures, the transistor operation of the fabricated TFT with a field effect mobility of 10 cm^2 /V s was confirmed. The lower mobility and higher V_{th} are considered to be due to the poor quality of the interface of poly-Si/gate SiO_2 and SiO_2 deposited on the fiber.

Considering that the fiber was handled when it was embedded in the trench formed in the quartz substrate, there might have been some contamination during the process. This can be prevented by adopting the reel-to-reel process of fiber handling. There have been reported poly-Si formation methods through high-speed scanning of a-Si film by using continuous wave (CW) laser, by which poly-Si with crystal grains elongated arbitrarily in the scanning direction can be produced. Thus, although the result presented here is preliminary, it can be considered that combining the high-speed reel-to-reel process with the irradiation of a continuous wave laser to *a*-Si on a thin quartz fiber can enhance not only the throughput but also the poly-Si crystallization on fiber.

3.5 Recent development of Fiber-TFT and remaining issue

Based on these results, recently, Mimura, et al. has advanced this Fiber-TFT concept still further [4, 5]. Figs. 3.17 show the developed OLEDs and TFTs on flexible quartz fibers, and a concept of ‘weaving’ of these fiber devices. As can be seen from these examples, not only the use of fiber for device fabrication is effective but also the function of the fiber (thin and flexible) is attractive for the creation of new device fabrication process. By lowering the process temperature, it can be also possible to utilize the flexible plastic fibers, which can only realized by laser annealing process and will leads to further reduction of fabrication cost and increase of the device functionality.

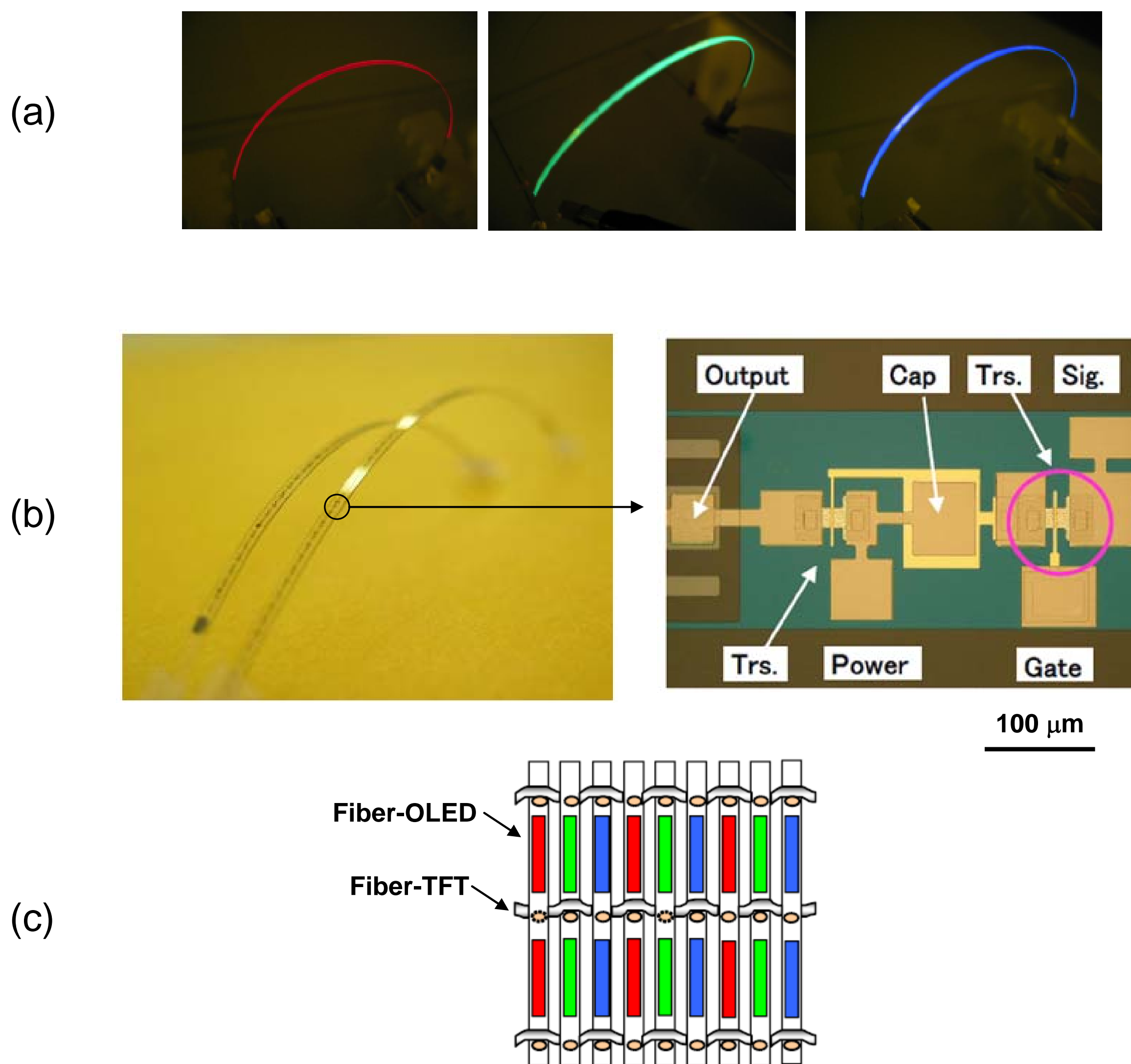

Figure 3.17: Recent development of Fiber-TFT;
(a) Fabricated OLED on flexible fiber (Fiber-OLED),
(b) Fabricated TFTs on flexible fiber,
(c) A concept of 'Weaving' of these fiber devices.

As for the formation of poly-Si thin film on the plastic fiber substrate, like on the two-dimensional plastic substrate, the reduction of thermal damage to the substrate itself during the melt and solidification of a-Si film becomes more strongly required, which can be realized by suitable choice of thermal buffer films. However, unlike the two-dimensional substrate, uniform formation of such buffer films on fiber plastic substrate in a very low temperature condition (below the glass transition temperature of the plastic) would require novel local processing scheme such as microplasma technology, by which the thin film deposition in room temperature and atmospheric ambient can be possible [6].

3.6 Summary

Poly-Si TFTs were fabricated on a one-dimensional quartz fiber. The excimer laser crystallization of a-Si on a quartz fiber was carried out, and a poly-Si layer with a crystal grain diameter of 300 nm was obtained. By using one-dimensional fiber substrate for laser annealing crystallization of a-Si thin film, possibility of modulation of the crystallization behavior of a-Si was suggested. The top-gated self-aligned TFTs obtained using the poly-Si layer showed a mobility of 10 cm^2 / Vs, indicating that TFTs can be fabricated on a one dimensional substrate. Although further development is still required, the demonstrated TFTs on a fiber, called fiber TFTs, are promising for the fabrication of silicon thin-film electronic devices on one-dimensional substrates.

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Chapter 4

Laser crystallization of three-dimensional silicon thin films for high performance LTPS TFT application

4.1 Introduction

LTPS TFTs have been utilized as active devices for the driving of high-resolution LCDs [1]. The electrical performance of LTPS TFTs is depended on the crystallinity of the poly-Si used as active layers of the TFTs, and for more high performance devices it is strongly needed to establish a method to crystallize a-Si to obtain poly-Si with high crystallinity [2]. For the application of LTPS to other than FPDs, recently, researches on advanced, low-cost image sensors composed of photo-sensing devices such as thin film photo diodes and thin film photo transistors utilizing LTPS thin films have attracted much attention because they can be integrated on the low-cost glass or plastic substrates together with the TFTs [3]. To improve the performances of such image sensors, high crystallinity LTPS is needed, and also, it is strongly desirable to make them have 3D structure in which the TFTs are stacked on the photo diodes (or vice versa) with an insulating film between them to achieve higher resolution and aperture ratio, as shown in Fig. 4.1 [4]. However, existing technology such as device transferring process to realize stacking of thin film devices has many complexities in the actual

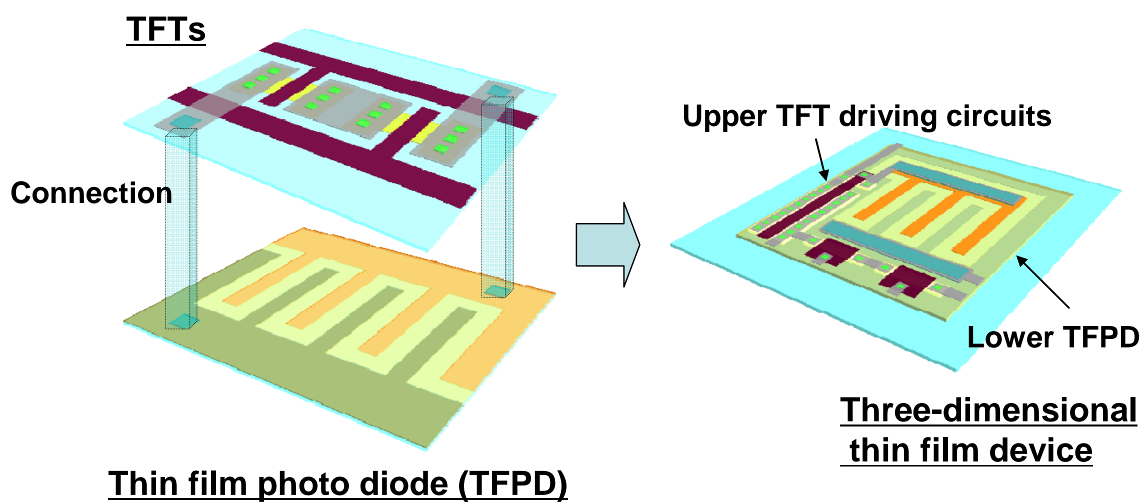


Figure 4.1: Concept of three-dimensional thin film device.

fabrication [5], so there needs a more straightforward fabrication process using laser annealing to make advanced 3D devices on low cost substrates.

As a new method for the fabrication of LTPS thin film devices with 3D structure, a laser crystallization method using doubly (or more) layered a-Si thin films substrate, that is to say, three-dimensional silicon substrate, was proposed [6]. For the laser to perform such crystallization of double-layered a-Si thin films, diode-pumped solid state (DPSS) pulsed green laser (λ = 532 nm) was employed because they have large transmissivity for a-Si, which makes it possible to heat all the layered a-Si thin films at a single irradiation of laser to crystallize them. In this chapter the experimental results from the crystallization of double-layered a-Si thin films using pulsed laser annealing system is presented. The method is named *GLADLAX*, standing for Green Laser Annealing Double-LAyered X'tallization [7]. In this experiment, a pulsed green laser annealing system for mass-production was used for the demonstration. Firstly, conventional single layer a-Si and double-layered a-Si thin films were annealed and crystallized by pulsed green laser annealing (PGLA, for the simplicity, GLA), and crystallinity of the obtained poly-Si was evaluated for comparison. The dependence of the crystal morphology of poly-Si on the laser energy was observed. Next, the double-layered poly-Si was applied to the fabrication of LTPS TFTs, and the electrical characteristics were evaluated and discussed with respect to the poly-Si electrical property and crystallinity. Finally, the mechanism of the crystallization of double-layered a-Si thin films is discussed.

4.2 Experimental

4.2.1 Pulsed green laser annealing crystallization

First, GLA crystallization method is briefly reviewed by comparing to the

conventional ELA crystallization method. GLA crystallization method was proposed to solve problems of ELA crystallization method. The problems are divided into the one on annealing system and the one on crystallization mechanism. Since conventional excimer lasers are using corrosive halogen gases, maintenance of gas tubes and other components are frequently required, which leads to the increase of operation cost. On the other hand, solid state lasers such as Nd:YAG laser exited by laser diode have several advantages over excimer lasers; excellent energy stability with output fluctuation less than 2 %, low operation cost owing to less frequent maintenance of system components, high coherency and compatibility to compact configuration. Thus, from a view point of constructing a laser annealing system, GLA system using all solid state laser is considered to be superior to ELA system.

The difference of the crystallization mechanism originates from the differences of the wavelength of each laser lights. Figs. 4.2 show the conceptual schematic diagrams of the each laser crystallization process. In the case of conventional XeCl excimer lasers (λ = 308 nm), the absorption coefficient of Si film is in the order of 10^6. Therefore, the irradiated laser light is totally absorbed in the surface of Si film within several nm, so that only the vicinity of the surface becomes heated, which creates sharp vertical temperature gradient in the molten Si. Due to this, the crystal grains grow from the interface of Si and the substrate to the Si surface, which consequently leads to the formation of poly-Si films consisted of small crystal grains with a few hundred nm in diameter (Fig. 4.2 (a)). On the other hand, in the case of green laser such as the second harmonics of Nd:YAG laser (λ = 532 nm), the absorption coefficient of Si film is in the order of 10^5. Therefore, the penetration length into silicon film is approximately 100 nm, so that the silicon film is uniformly heated to the bottom. In the result, the lateral temperature gradient is created near the edge of the laser irradiated part, which causes the crystal grain growth in the lateral direction rather than in the vertical direction. This

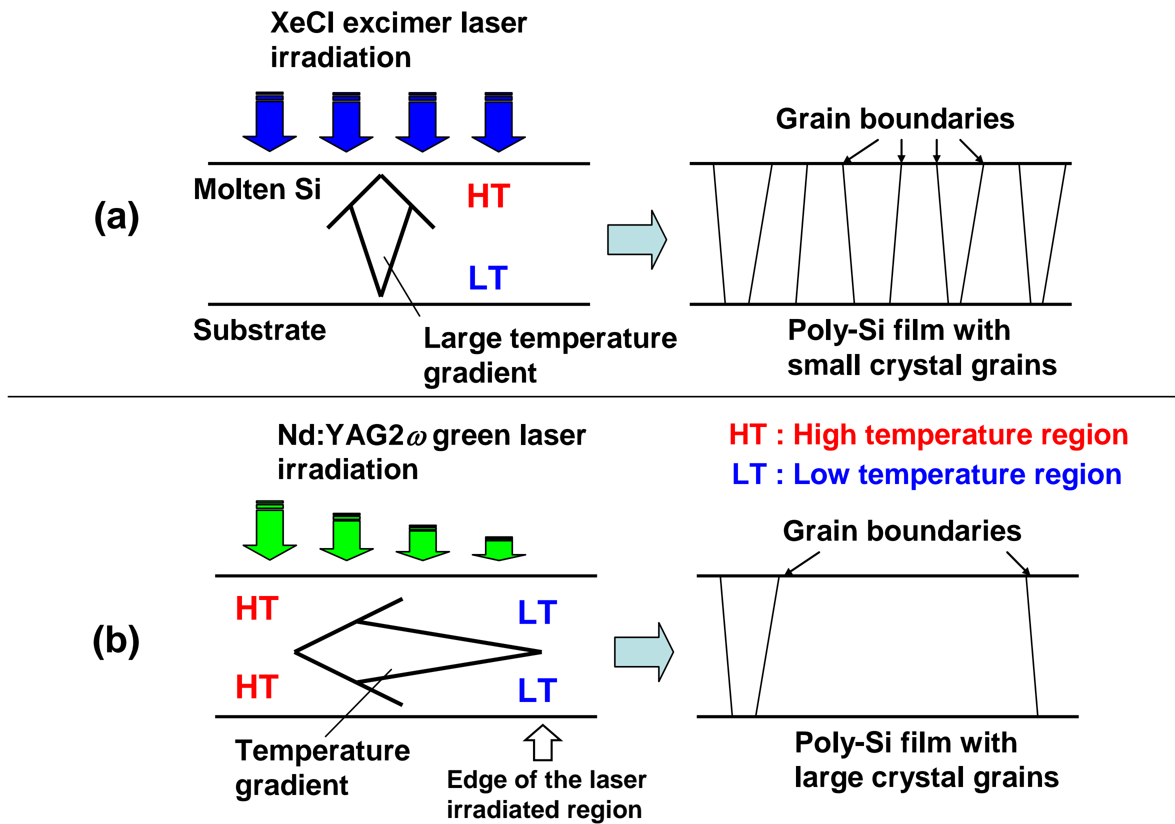


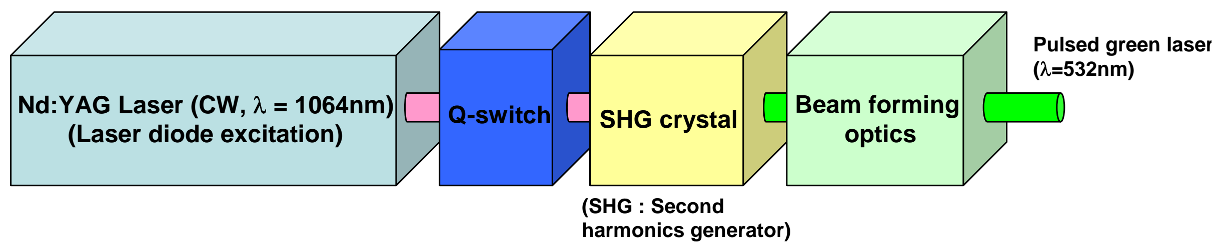
Figure 4.2: Schematics of crystallization mechanism of (a) ELA and (b) GLA.

results in larger crystal grain growth around the edge of the laser irradiated region (Fig. 4.2 (b)). These advantages of GLA crystallization method have attracted much attention these days, and a few companies have been developing GLA system for mass production of LTPS TFT-LCD.

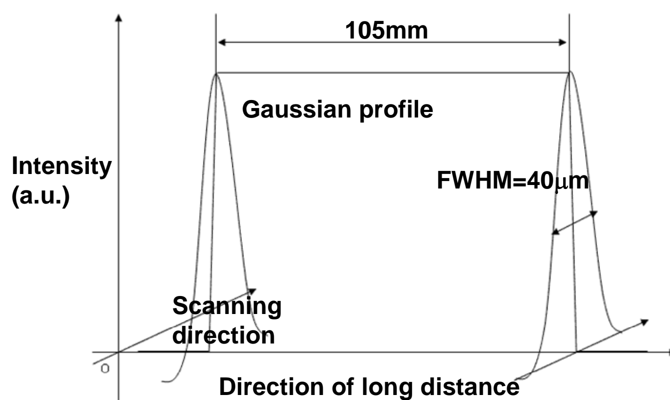
Next, the solid state pulsed green laser annealing system used to crystallize a-Si thin films in this experiment, and its configuration and laser annealing condition are explained. The system used has recently been developed by ULVAC, inc. (ULA-series), which employs the green laser of the second harmonics of Nd:YAG laser, wave length of 532 nm [8]. Beam intensity profile is Gaussian with its FWHM of approximately 40 μm, which equals the width of the beam spot of the laser irradiated on the surface of the substrate. As shown in Figs. 4.3, a line-shaped beam with the length of approximately 100 mm is scanned on the substrate to crystallize a-Si thin film. The generated laser beam was modulated by Q-switch to pulsed laser with the irradiation repletion frequency of 4 kHz, and the pulse duration time was 62 ns. The scanning speed was set to 8 mm / s, so that, the irradiation overlap ratio of 95 % and the laser irradiation pitch of 2 μm was achieved.

4.2.2 Crystallization of double-layered a-Si thin films

As precursor a-Si thin film substrates, double-layered a-Si thin films substrate as well as conventional single layer thin film substrate were prepared, as shown in Fig.4.4. All of the films were deposited by using plasma enhanced chemical vapor deposition (PECVD). On quartz grass substrate with thickness of 0.7 mm, first SiN_x and SiO_x were deposited as buffer layers. After that, for the double-layered substrate, lower layer a-Si, interlayer SiO_x and upper layer a-Si with 50 nm thickness were continuously deposited without breaking the vacuum. The gases used for the deposition of each film and its deposition rate were listed in Table 4.1. For the dehydrogenation, the whole substrates



(a)



(b)

Figure 4.3: Schematics of pulsed green laser irradiation;
(a) configuration of Q-switched DPSS pulsed green laser,
(b) beam intensity profile of the irradiated laser.

were heated at the temperature of 490 degree in N_2 ambient.

The a-Si films thus prepared were laser annealed by using the pulsed green laser annealing system. The laser irradiation condition was the same as noted before, and the output power was changed to 95, 100 and 105 W for the crystallization of the double-layered a-Si, and to 120, 125, 135 W for single layer a-Si.

Here, several definitions are made for later convenience;

・GLA crystallized double-layered Si thin films is defined as ‘GLADLAX poly-Si’

・The upper Si film of GLADLAX poly-Si is defined as ‘upper GLADLAX poly-Si’

・The lower Si film of GLADLAX poly-Si is defined as ‘lower GLADLAX poly-Si’

・GLA single layer poly-Si is defined as ‘GLA SL poly-Si’.

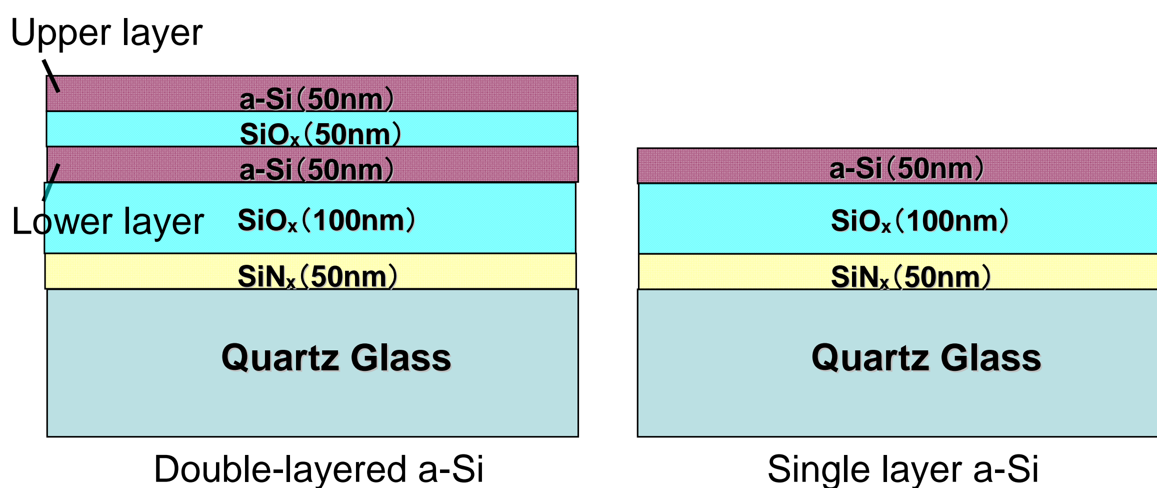


Figure 4.4: Structure of the double-layered a-Si (left), conventional single laser a-Si (right).

Table 4.1: Deposition condition of the films by PECVD

Film	Plasma power density(W/cm^2)	Gases	Deposition rate
SiN_x	0.8	$SiH_4/NH_3/N_2$	250 nm/min
SiO_x	0.3	$SiH_4/N_2O/Ar$	350 nm/min
a-Si	0.05	SiH_4/Ar	50 nm/min

(In all deposition, the temperature of substrate heater was 430°C)

4.3 Evaluation of GLA SL poly-Si

Crystal grains and surface morphology

The relationship of GLA crystallized poly-Si morphology between the laser energy was investigated both for the double-layered and single layer a-Si substrates. For the comparison, conventional GLA SL poly-Si was first investigated in this section. The crystal grain shape and size were observed by scanning electron microscopy (SEM). Before the observation, the poly-Si samples were dipped with Secco etching solution to etch the grain boundaries and other defects in the poly-Si film [9].

Fig. 4.5 shows the SEM images of the surfaces of the GLA SL poly-Si thin films crystallized by pulsed green laser annealing with elevated laser output power, which is indicated at upper left in each figure. The arrows indicate the scanning direction of the laser. From the images, it can be seen the crystal grains were becoming elongating toward the direction of the scanning direction of the laser. Also, at the lower energy condition, the grain boundaries there were forming themselves apparently randomly. However, at the higher energy condition, the grain boundaries were seen to be classified in to two groups: one running in the perpendicular direction from the scanning direction, the other running in parallel of the scanning direction.

Fig. 4.6 show atomic force microscopic (AFM) images of the above observed poly-Si surfaces. The arrows indicate the scanning direction of the laser. From the figure, it can be seen that the generation of “ridges” of Si with the height over 100 nm in the higher energy condition is distinctive from the lower energy condition. Also, it was observed that the interval of these ridges was approximately 2 μm, corresponding to the laser irradiation pitch.

Crystallization mechanism

It is now mentioned that the GLA SL poly-Si crystallized by this laser annealing

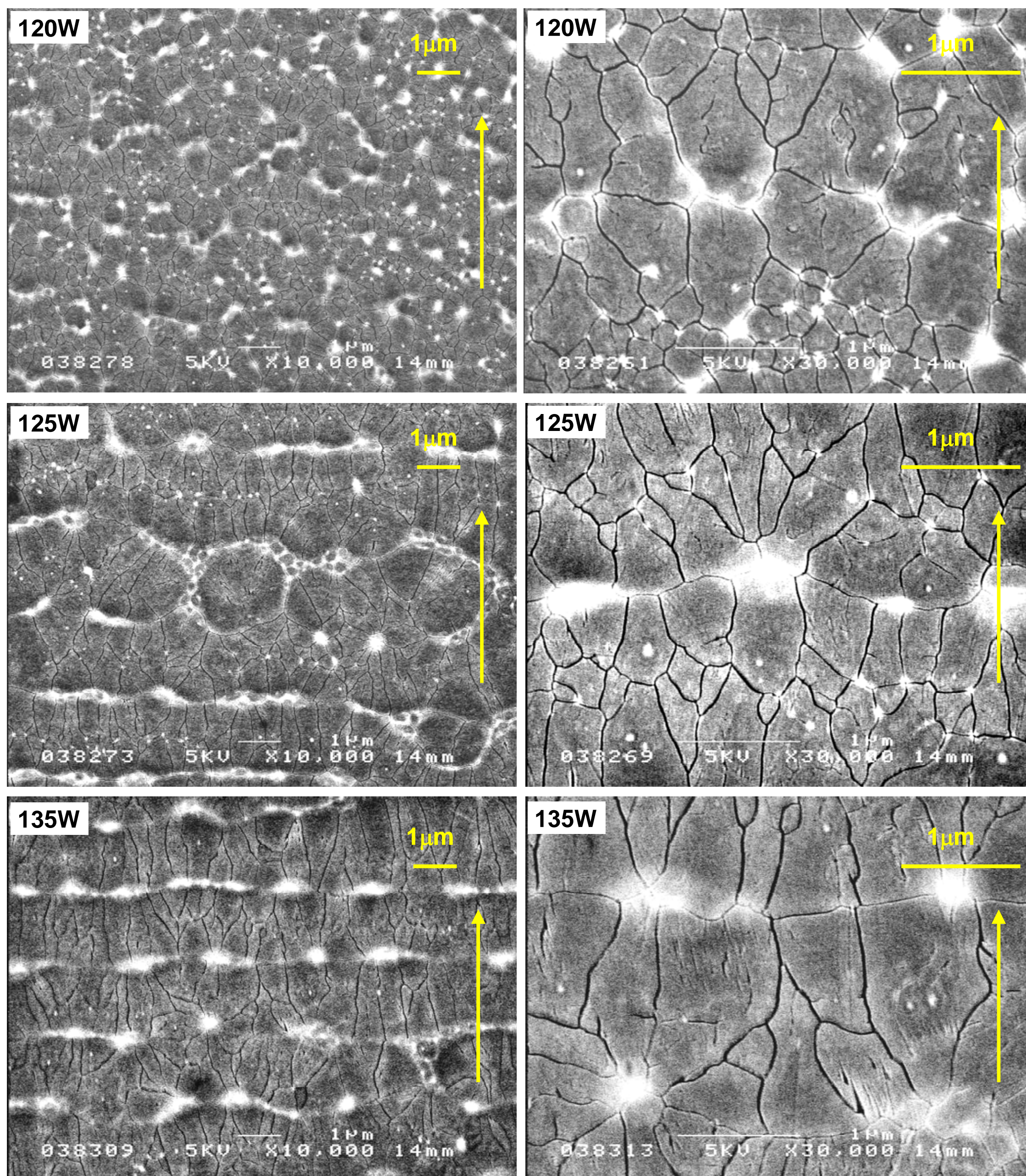


Figure 4.5: SEM images of the surface of the GLA SL poly-Si;
Left: ×10,000, Right: ×30,000. The laser power is indicated in each figure.
The arrow indicates the laser scanning direction.

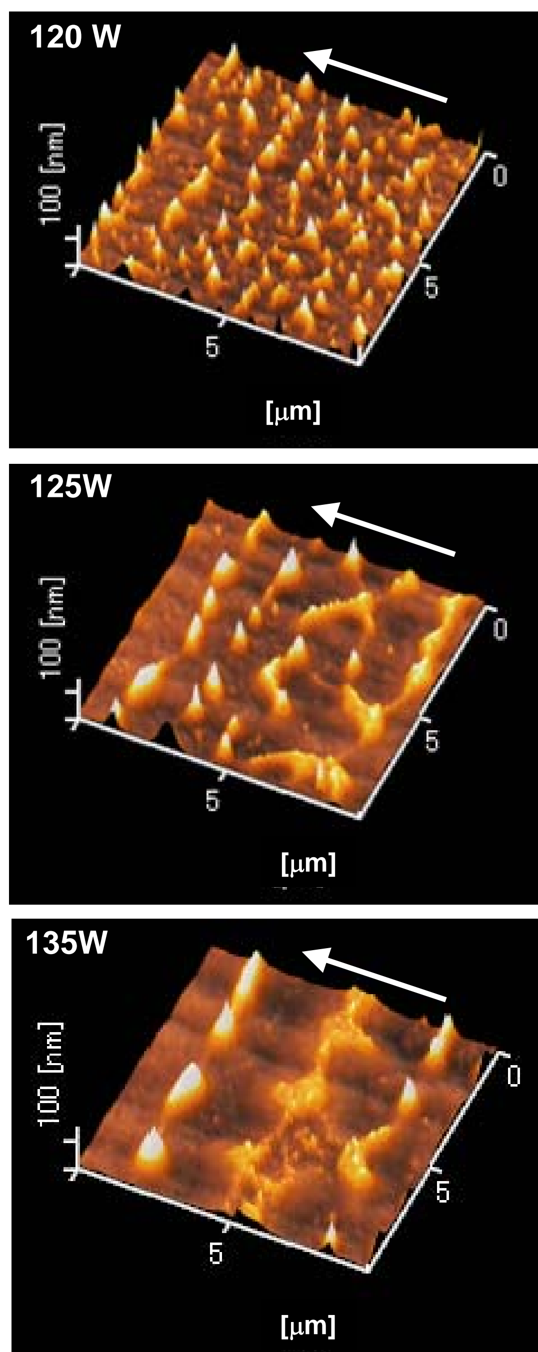


Figure 4.6: AFM images of the surface of the GLA SL poly-Si. The laser power is indicated in each figure. The arrow indicates the laser scanning direction.

condition have very different appearance from conventional ELA poly-Si, which was briefly described in Chapter 2. This originates from the different crystallization mechanism from that of ELA crystallization, and is now reviewed in detail [10]. Figs. 4.7 show the schematic of crystallization of a-Si by GLA after the 1st and 2nd irradiation of laser pulse. Since the absorption coefficient of a-Si for green laser light is much smaller than that for UV light such as excimer laser light, the irradiated green laser light penetrates the a-Si thin film, and with sufficient energy, melts the a-Si completely to the bottom, as depicted in Fig. 4.7 (a). In this experiment, the laser used has beam intensity with Gaussian profile in the scanning direction, which causes temperature gradient in the molten Si in that direction, with the center of the irradiated spot having much higher temperature. After the irradiation, the heat rapidly transmits into substrate, and the sufficiently molten Si cools down to the temperature below the melting point of Si. In this super cooled state, spontaneous generation of a dominant number of crystal nuclei occurs, and the crystallization starts explosively from the nuclei. This is so called the explosive crystallization [11], and the resulted poly-Si is micro-crystalline. At the point far from the irradiation center, where the a-Si temperature was increased but to below the melting point of Si, the solid phase crystallization of a-Si occurs forming small grain poly-Si.

Owing to the temperature gradient, the lateral crystallization of poly-Si occurs with the SPC poly-Si as nuclei of crystallization, as shown in Fig.4.7 (b). The lateral crystallization of poly-Si starting from the micro-crystalline Si formed by the explosive crystallization also occurs, and the two crystallization fronts collide with each other, forming Si ridges and grain boundaries. The formation of Si ridges is due to the 10% density change between solid and liquid phases of silicon, approximately 2.53 g/cm^3 for the liquid and 2.30 g/cm^3 for the solid, so that the solidifying silicon expands upward [12]. How much and which of the two laterally crystallized poly-Si grow further is

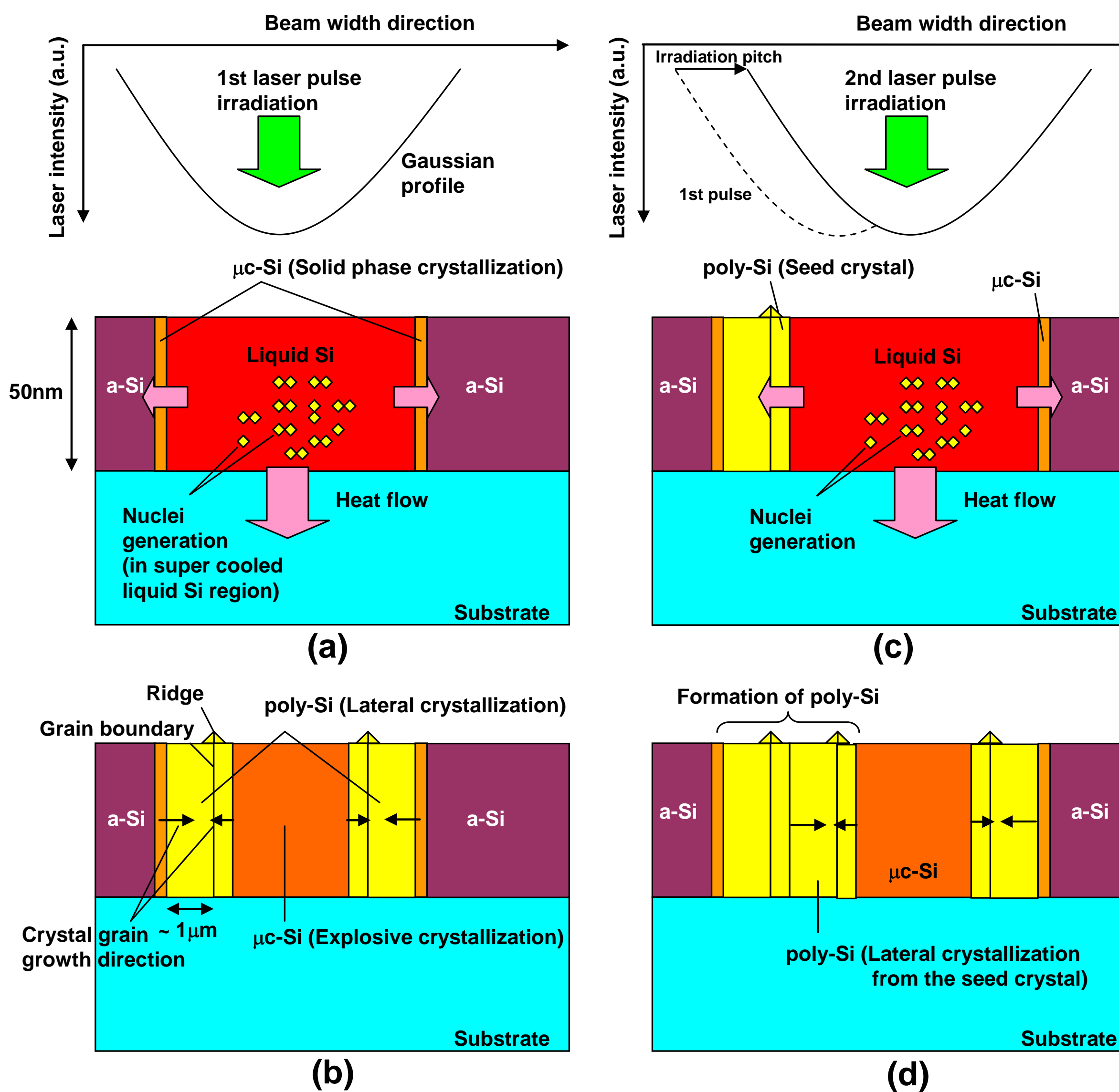


Figure 4.7: Schematic of crystallization mechanism of GLA SL poly-Si; (a) melt and (b) solidification of a-Si after the 1st laser pulse irradiation, (c) melt and (d) solidification of a-Si after 2nd laser pulse irradiation.

considered to be depended on the irradiation laser energy; for lower energy condition, both lateral crystallization will be suppressed, and the resulted poly-Si will have randomly formed grain boundaries, and for higher energy condition, the lateral crystallization from the SPC poly-Si will dominate because of the elongated melting time, and the resulted poly-Si will assume anisotropic morphology with the grain boundaries running in the scanning direction.

After the 2nd laser irradiation, in which the irradiated point is shifted by the irradiation pitch (in this experiment, 2 μm), the laterally grown poly-Si formed at the front side will melt (Fig. 4.7 (c)), and a new lateral crystallization process occurs, forming poly-Si laterally grown from the poly-Si formed in the previous laser irradiation (Fig. 4.7 (d)). It is clear that repeating these steps will produce the poly-Si on the entire substrate.

4.4 Evaluation of GLADLAX poly-Si

4.4.1 Dependence of poly-Si morphology on laser energy

Figs 4.8 show the SEM images of the surface of the upper GLADLAX double-layered poly-Si. The poly-Si shown in Figs. 4.8 was crystallized with the output power of 95 W, and seen to have a similar appearance of that crystallized by ELA, as shown in Fig. 2.4 (a). With a slight increase of the laser energy, when the output power was 100 W, however, the resulted poly-Si shows strikingly different appearance, as shown in Fig. 4.8 (b). A remarkable enlargement of crystal grains was observed, with the size of them increased from a few hundred nanometers to over 1 μm. With a more slight increase of the laser energy, when the output power was 105 W, the crystal grains of the resulted poly-Si became a mixed state of the very large grains exceeding 2 μm and smaller grains the diameter of which is around a few hundred nanometers.

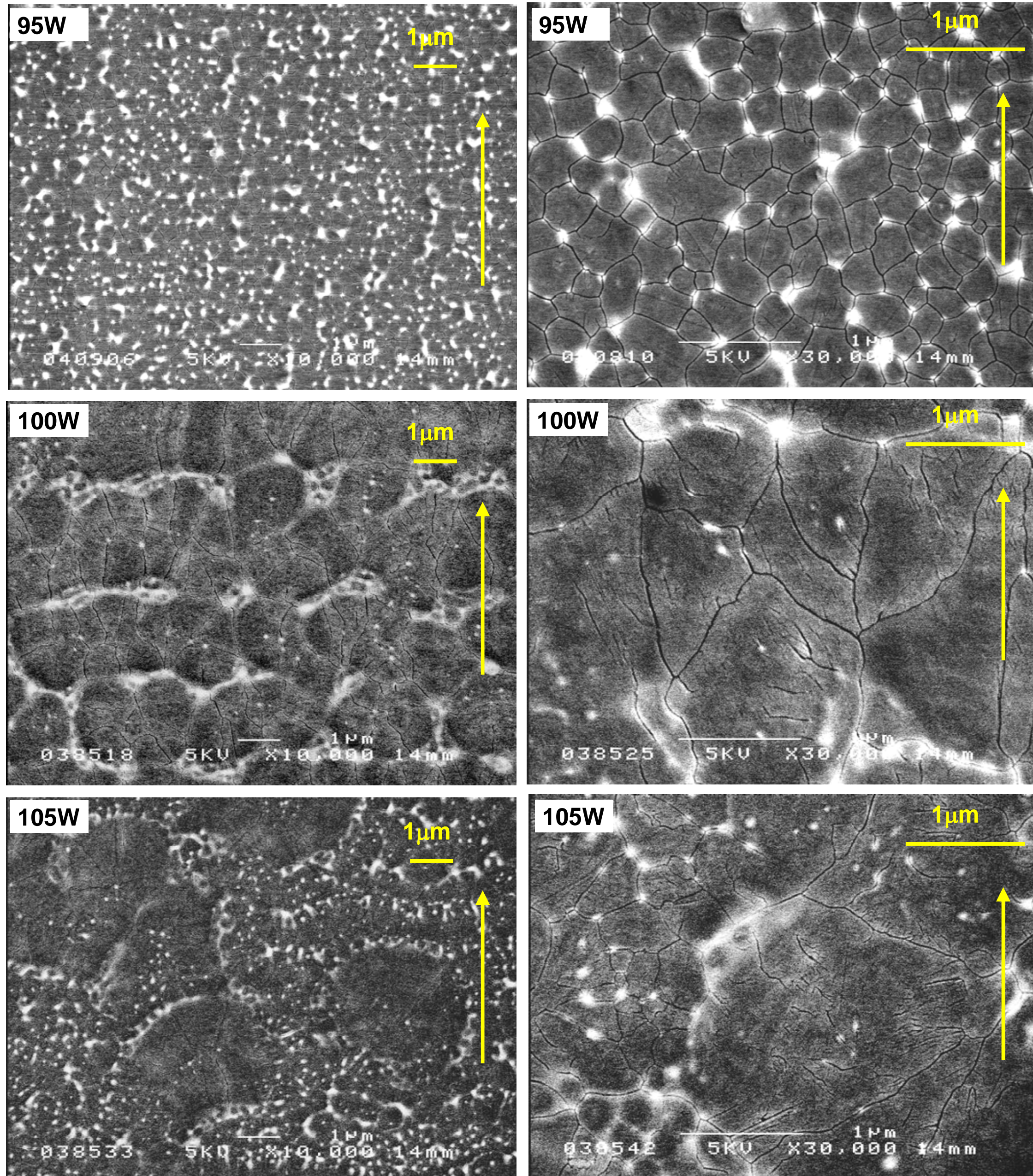


Figure 4.8: SEM images of surfaces of upper GLADLAX poly-Si;
Left: ×10,000, Right: ×30,000. The laser power is indicated in each figure.
The arrow indicates the laser scanning direction.

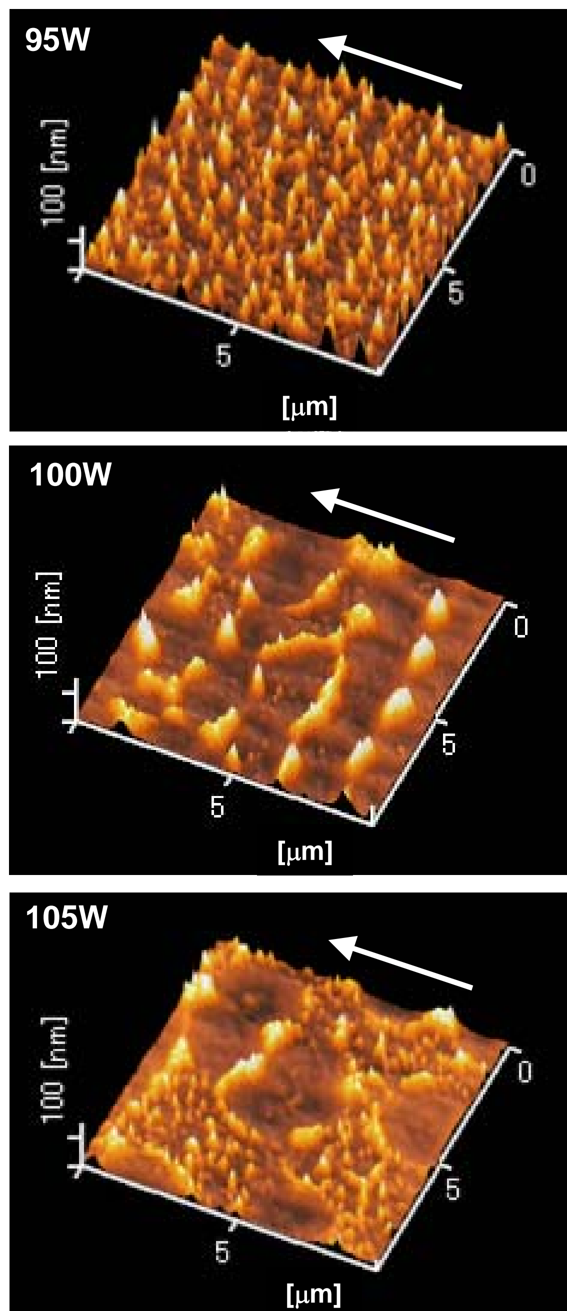


Figure 4.9: AFM images of surfaces of upper GLADLAX poly-Si. The laser power is indicated in each figure. The arrow indicates the laser scanning direction.

This phenomenon was observed more clearly from AFM images of the surfaces of the poly-Si films, as shown in Figs. 4.9. When the output power was increased to 100 W, Si ridges lining to the direction perpendicular to the scanning direction of the laser were appearing with the interval of 2 μm, as shown in Fig. 4.9 (b), which were not observed in the poly-Si crystallized with the lower energy condition, as shown in Fig 4.9 (a). When the output power was increased up to 105 W, those Si ridges characteristic of Fig. 4.9 (b) were becoming less prominent, as shown in Fig. 4.9 (c).

These results strongly suggests that the behavior of the crystallization changed drastically with the increase of the laser energy, into a state in that the laser irradiated a-Si melts for prolonged time. Note that these laser output levels were about 30 % less than that used in the GLA crystallization of conventional single layer a-Si thin films, indicating that by introducing one more a-Si layer under the single layer a-Si, the irradiated laser light became utilized more effectively to enhance the crystal growth of the upper poly-Si film.

4.4.2 Crystallinity of the lower GLADLAX poly-Si

Next the lower Si layer of GLA crystallized double-layered poly-Si was investigated. Figs. 4.10 show the SEM images of the lower GLADLAX poly-Si films investigated in the previous subsection. The observation was carried out after the upper poly-Si and the interlayer SiO_x films were wet-etched by a mixture of HF and HNO_3 solution and BHF solution, respectively. After Secco-etching of the surfaces the lower Si, the one crystallized with the laser output power of 95 W was suggested to be still amorphous or very weakly crystallized state because it melted away completely in Secco-etching solution. In contrast, the lower GLADLAX poly-Si with the irradiation conditions of the 100 W and 105 W did not melt in the Secco-etching solution and this means that they at least crystallized. So it was confirmed that at this

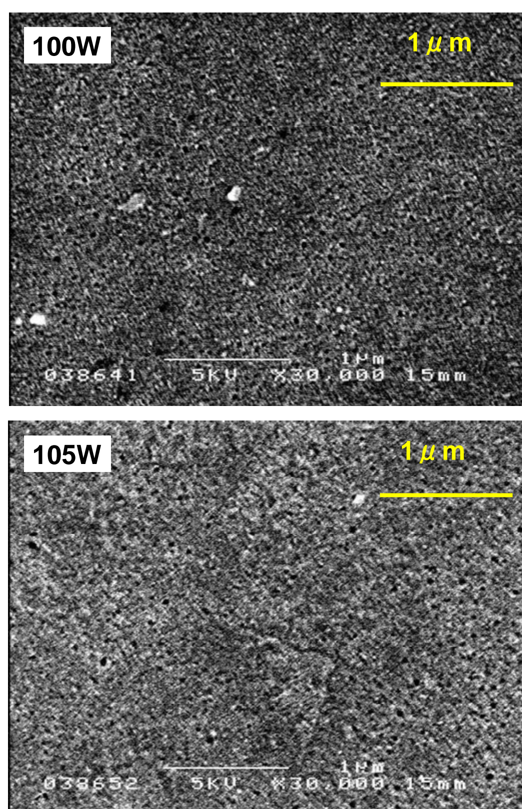


Figure 4.10: SEM images of lower layer GLADLAX poly-Si after the upper poly-Si and interlayer SiO_x were etched and the lower Si Secco etched. The laser power is indicated in each figure.

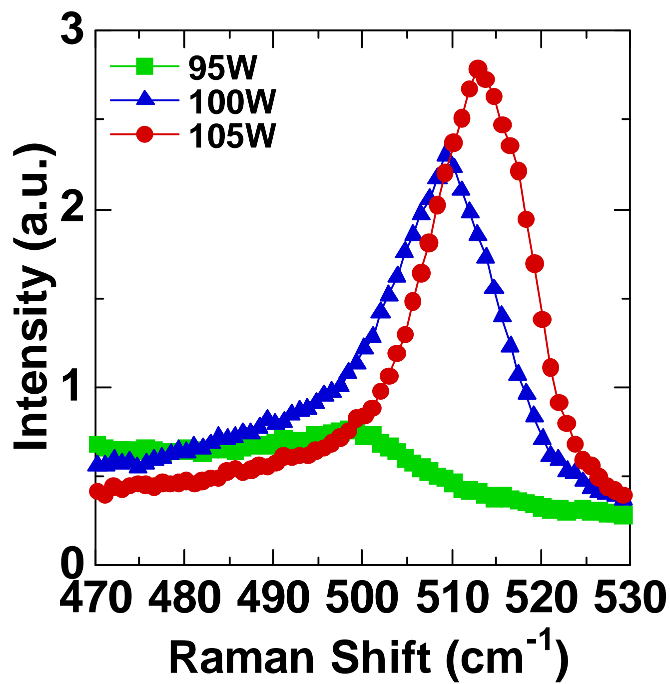


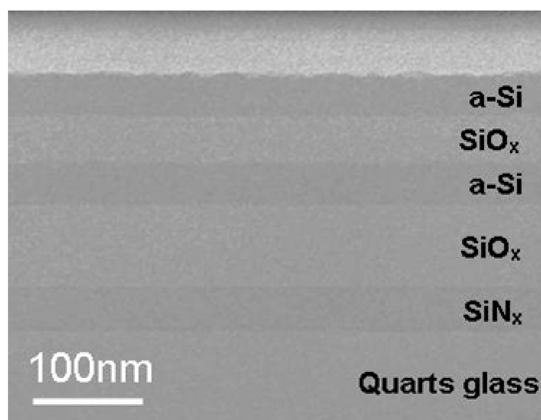
Figure 4.11: Raman spectra of the lower GLADLAX poly-Si films.

moment the crystallization of the both the upper and lower a-Si film by green laser annealing was successfully demonstrated. However, as seen from Figs. 4.10 (b) and (c), these lower films did not form clear crystal grains structure but crystallized to micro-crystalline state with the crystal grain size presumably of less than 10 nm.

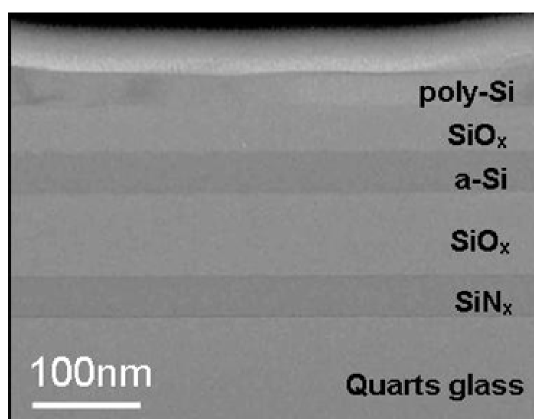
The crystallinity of these lower Si films was investigated by Raman spectroscopy. The upper poly-Si and the interlayer SiO_x were wet-etched as before, but the lower Si films were not treated by Secco etching. Figure 4.11 shows the Raman spectra of the films. As suggested above, no peak in the spectrum of the lower Si film with the laser output power of 95 W concludes its non-crystallization. Although peaks were appearing in the spectra of the lower Si films crystallized in the higher energy condition, their intensity level is low and their crystallinity leaves plenty of rooms of further improvement. However, it is interesting to note that the drastic enhancement of the crystal growth of the upper poly-Si was observed in the condition of the laser energy higher enough to crystallize the lower a-Si films too, strongly suggesting that the crystallization of the lower a-Si film is playing important role to such sudden enlargement of the crystal grains of the upper poly-Si, which is discussed in the next section.

4.4.3 Cross sectional TEM observation

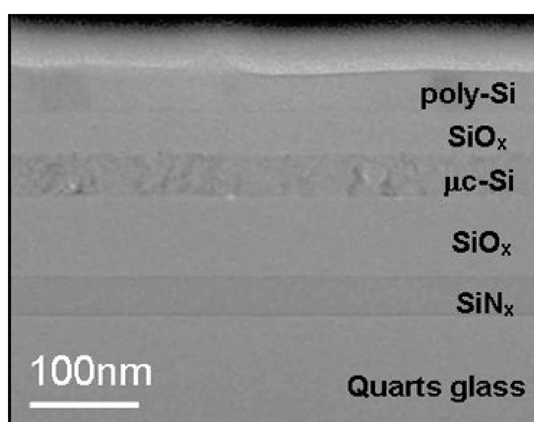
Now that the double-layered a-Si thin films can be crystallized into double-layered poly-Si, it is interesting to observe whether the interlayer SiO_2 suffers from any damage during the crystallization process, for in considering to the future application of double-layered poly-Si thin films to electronic devices its quality as an insulator is becoming important. Figures 4.12 show the cross-sectional TEM images of the double-layered Si substrates, (a) before laser irradiation and (b) and (c) are the GLA DLAX poly-Si observed in the previous subsections. From these figures, it can be



(a) Before annealing



(b) 95 W



(c) 100 W

Figure 4.12: Cross-sectional TEM images of (a) double-layered a-Si, (b) GLADLAX poly-Si crystallized with the laser output power of 95 W and (c) 100 W.

seen clearly that the lower a-Si was changing into crystallized state, with the interlayer SiO_x apparently unchanged, no sign of generation of voids or cracks. Thus, although in more detail the investigation of electrical properties of interlayer SiO_x films is undoubtedly needed, at least mechanically, durability of the interlayer SiO_x during the laser irradiation was confirmed.

4.4.4 SIMS measurement of double-layered poly-Si

Figs. 4.13 show the concentration profiles of atoms in the double-layered Si films measured by Secondary Ion-microprobe Mass Spectrometer (SIMS). In the double-layered a-Si films before crystallization, both the concentration levels of the impurity N and C atoms were low, as shown in Fig. 4.13 (a), and sharp increases and decreases of the concentrations of Si and O can be seen, indicating the thicknesses of the two a-Si films and the interlayer SiO_x. Even after the crystallization with the laser output power of 100 W, the concentration ratio of atoms in the upper poly-Si film was kept at nearly the same level as that before crystallization, as can be seen from Fig. 4.13 (b). However, the increase of the concentrations of O and N atoms in the lower Si became considerable. Especially the diffused oxygen atoms in the lower μc-Si film may degrade its electrical conductance.

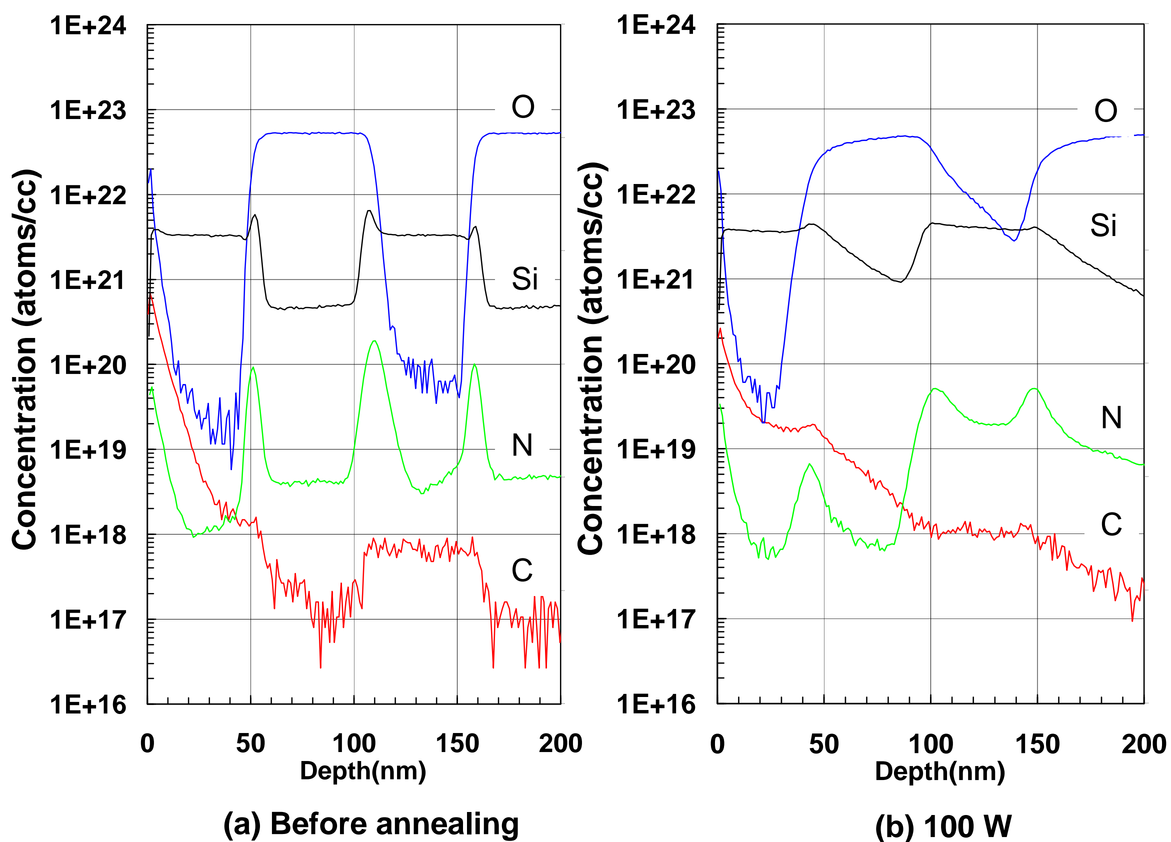


Figure 4.13: Concentration profiles of atoms in the double-layered poly-Si films; (a) Before annealing, (b) After annealing with the output power of 100 W.

4.5 Discussion on crystallization mechanism

4.5.1 Comparison of grain size

In this subsection, the evolution behavior of crystal grains upon increasing the laser output power is investigated in detail. Owing to that the crystal grains of GLA poly-Si thin films tend to have elongated shapes toward the laser scanning direction, it is convenient to define the crystal grain size in two directions as Grain Length measured in parallel with the scanning direction and as Grain Width measured in perpendicular to the scanning direction of laser, as depicted in Fig. 4.14. The average grain size was measured by the following procedure;

1. Place a line with arbitrary length (in parallel with the scanning direction for the measurement of Grain Length, in perpendicular to the scanning direction for the measurement of Grain Width) in a SEM image of Secco-etched poly-Si surface showing crystal grain boundaries.

2. Count the number of the crossing points of the line and grain boundaries.

3. Obtain the average grain size by dividing the length of the line by the crossing number plus 1.

In this evaluation, 5 lines in both directions respectively were placed. Fig. 4.15 shows the average grain size of upper GLADLAX poly-Si and GLA SL poly-Si. For GLA SL poly-Si, the Grain Length became strikingly large in increasing the laser output power, whereas the increase in the Grain Width was only around 100 nm. This indicates that the elongation of crystal grains in GLA SL poly-Si upon increasing crystallization laser energy is dominant. However, the situation changes drastically in GLADLAX poly-Si. From the figure, it can be seen that both the Grain Length and the Grain Width suddenly became large upon increasing of the laser output power over 100 W, meaning the growth of crystal grains was enhanced not only in the scanning direction but also in

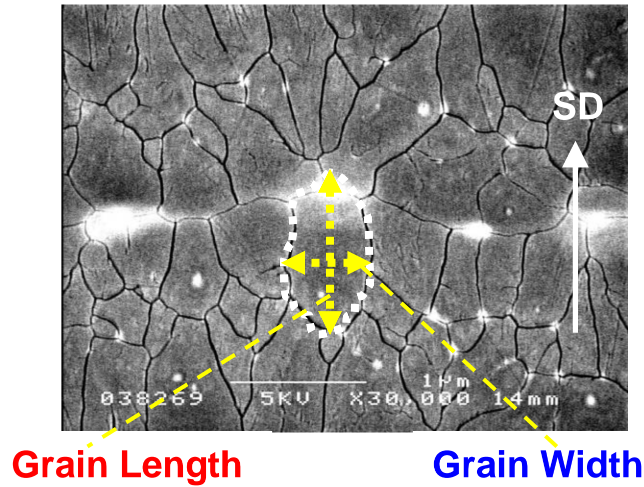


Figure 4.14: Definition of Grain Length and Grain Width. (The image is SEM image of the surface of the GLA SL poly-Si poly-Si crystallized with the laser output power of 125 W. The arrow indicates the scanning direction.

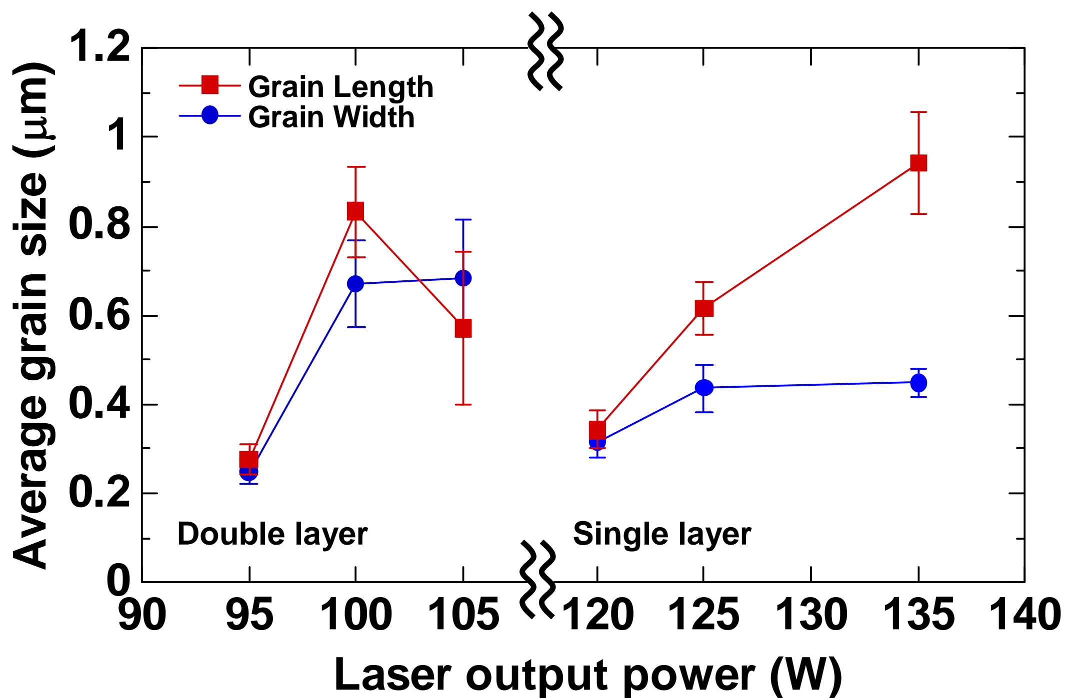


Figure 4.15: Average grain size of GLA double-layered poly-Si and single layer poly-Si. The error bars indicate the standard deviation.

the perpendicular direction of scanning direction. Remembering that the lower a-Si film was crystallized when the laser output power was over 100 W, it can be said that the sudden increase in the grain size is strongly related to the crystallization of lower a-Si films.

4.5.2 Crystallization mechanism of double-layered poly-Si

In this subsection, the crystallization mechanism of the double-layered a-Si thin films by pulsed green laser annealing is discussed in detail.

Energy density profile of the pulsed green laser beam

Fig. 4.16 shows the calculated energy density profile of the pulsed green laser beam with different output power. The calculation was done under the condition that the pulse repetition frequency is 4 kHz, the energy transmission efficiency is 72 %, the long axis of the laser beam is 10.1 cm, and the FWHM of the laser beam is 37.7 μm. The horizontal axis indicates the distance from the position at which the profile has a maximum intensity. The horizontal red line indicates 430 mJ / cm^2, which is the threshold energy density for lateral crystallization to occur in this experimental configuration [10]. From the figure, it can be seen that for the output power over 100 W, the energy density profiles are exceeding the 430 mJ / cm^2 line, and for the output power of 95 W, the energy density profile is less than 430 mJ / cm^2. Since the energy density profiles for the crystallization of single layer a-Si are greatly exceeding the threshold energy density for the lateral crystallization, the resulted single layer poly-Si film was composed of the poly-Si crystallized at the back of the irradiated beam, because the high energy intensity of the center part of the laser beam is enough to melt the poly-Si crystallized at the front of the laser beam, as illustrated in Fig. 4.5. On the contrary, the resulted upper poly-Si film of the double-layered poly-Si was considered to be constituted of the poly-Si crystallized at the front of the laser beam, because the center

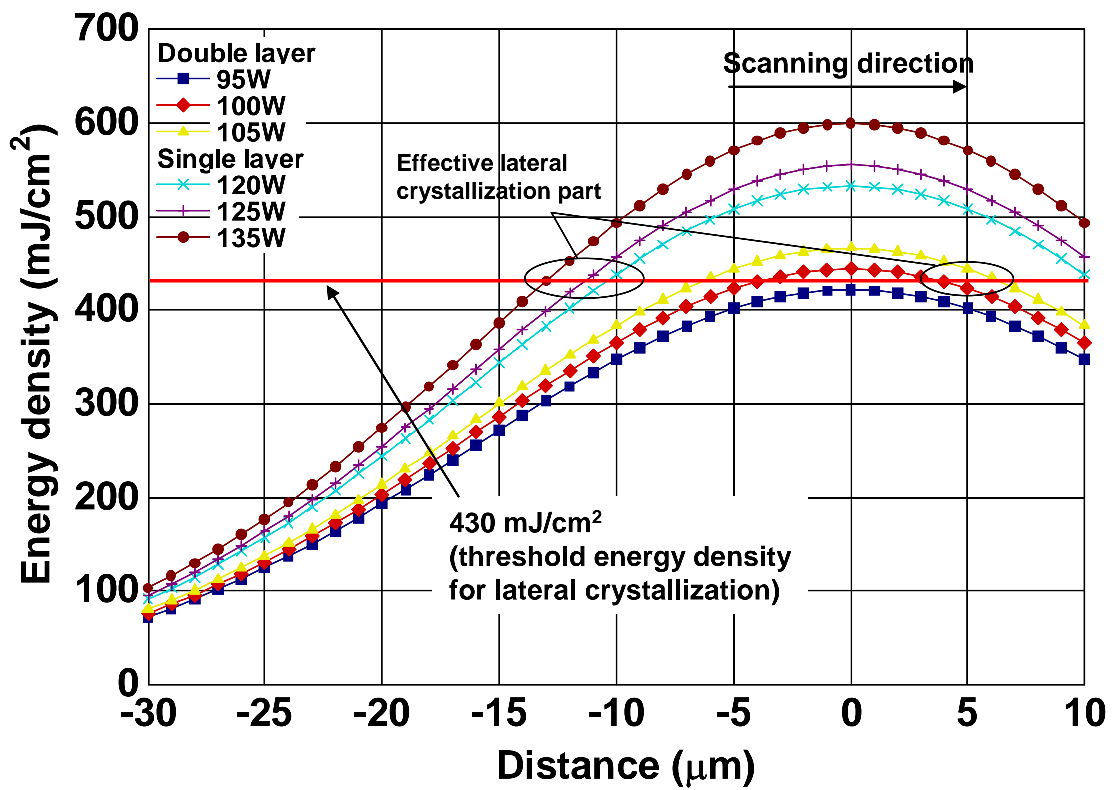


Figure 4.16: Calculated energy density profile of the pulsed green laser beam with different output power. The horizontal red line indicates 430 mJ/cm^2, which is the threshold energy density for lateral crystallization.

part of the laser beam is insufficient to melt the poly-Si, and simply transmits the upper poly-Si to the lower layers. Taking these consideration and some of the experimental results, the difference of the crystallization behavior of double-layered a-Si and single layer a-Si can be explained as follows.

Enlargement of crystal grains at lower laser output power

A marked feature of the upper GLADLAX poly-Si is the drastic enlargement of crystal grains at lower laser output power compared to the case of the crystallization of single layer a-Si. Figs. 4.17 show schematics of estimated temperature profile and crystallization behavior of double-layered a-Si thin films after irradiated by a laser pulse. When the laser output power was 95 W, the energy density of the laser beam did not reach the threshold for lateral crystallization. This means that the upper a-Si was incompletely molten, and the lower a-Si, though absorbed the laser light permeated from the upper a-Si, did not reach the temperature required to solid phase crystallization (SPC). Also, as seen from Fig. 4.16, approximately flat energy profile around the maximum intensity of the laser beam was participated in the crystallization of a-Si. Thus, temperature gradient along the scanning direction of the laser was considered to be negligible, and that along the vertical direction was dominant in this case. Therefore, the crystallization mechanism become similar to that of ELA crystallization of a-Si, that is, the crystal nuclei generate at the interface between upper a-Si and interlayer SiO_x, and the crystal grains grow upward from those nuclei resulting relatively small crystal grains, as depicted in Fig. 4.17 (a).

When the laser output power was increased over 100 W, the situation changed drastically. As seen from Fig. 4.16, the energy density profile curve slightly exceeds the threshold energy density for lateral crystallization and the laterally crystallized poly-Si at the front of the laser beam remained without suffering the re-crystallization by the following irradiation of laser pulses. Since the absorption coefficient of a-Si for the laser

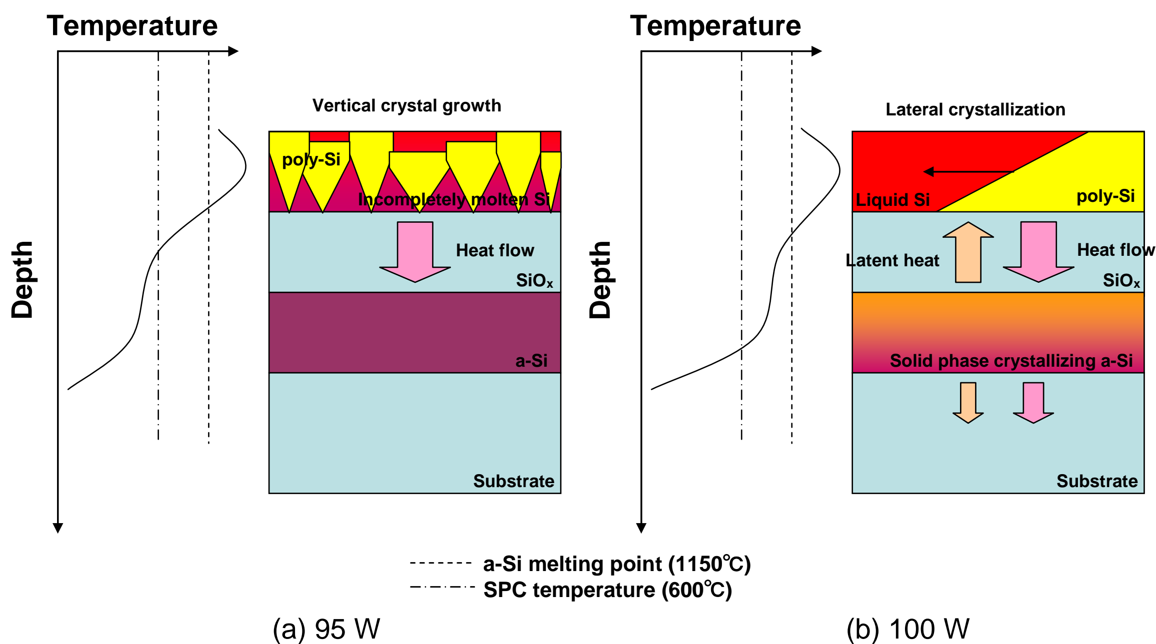


Figure 4.17: Schematics of estimated temperature profile and crystallization behavior of double-layered a-Si thin films after irradiated by a laser pulse; (a) the laser output power is 95 W, (b) 100 W.

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ight with the wavelength of 532 nm is the order of 1.0×10^5 cm^{-1} [13], the penetration length of the laser into a-Si film is estimated to 100 nm. So even if there was interlayer SiO_x film between the upper a-Si film and the lower a-Si film, both the films was thought to be wholly heated by the laser irradiation, with the temperature increase of the lower a-Si less than that of upper a-Si. Since the crystallization of lower a-Si was actually confirmed at this laser energy condition, it can be considered that the lower a-Si, upon absorbing the laser light permeated from the upper a-Si, crystallized in solid phase and generated heat. So the temperature gradient of the double-layered a-Si in this case is estimated as depicted in Fig. 4.17 (b). Owing to this heat generated from the solid phase crystallizing lower a-Si, the temperature gradient of the upper molten Si in the vertical direction is diminished due to the reduced net heat flow from the upper molten Si, which leads to the prolongation of melting time of the upper a-Si. As a result, poly-Si was growing fewer numbers of nuclei, forming larger-sized grains since they earn longer time to meet collisions of solidification fronts, which form the grain boundaries, from other grain growth [14].

When the laser output power was 105 W, the melting time was considered to become too prolonged. This can be caused by excessive laser energy and the thermal reservoir effect of the crystallizing lower a-Si. This not only leads to much enhanced crystal grain growth which would result in poly-Si with still larger crystal grains, but also produces poly-Si with small (a few hundred nm in diameter) crystal grains partially in the resulted poly-Si film. Which of the former or the later can occur depends whether the spontaneous generation of crystal nuclei in the molten Si will not occur or not, and the more the melting time of Si was increased, the more it is liable for such spontaneous generation of nuclei to occur.

Crystal grain growth in perpendicular to scanning direction

Another marked feature of the upper GLADLAX poly-Si is the enhancement of

crystal grain growth in perpendicular to scanning direction of laser. Two factors are considered to be related with this phenomenon; one is the prolongation of solidification time of upper molten Si due to the thermal reservoir effect of the lower a-Si, and the other is the moderate temperature gradient in the scanning direction, which was caused by the moderate energy density profile of the lower laser output power, as can be seen in Fig. 4.16. Fig. 4.18 shows schematics of estimated temperature profile in the scanning direction of laser and crystal grain growth of the GLA SL poly-Si and the upper GLADLAX poly-Si. In the case of GLA crystallization of single layer a-Si with high laser output power, the slope of the energy density profile at which the lateral crystallization occurs is steep, so that the resulted temperature gradient of a-Si in the scanning direction is also steep. This steep temperature gradient is considered to increase the solidification speed of the molten Si toward the scanning direction, which would prevent the crystal grains from growing the perpendicular direction to the scanning direction.

On the contrary, in the case of GLA crystallization of double-layered a-Si with low laser output power, the slope of the energy density profile at which the lateral crystallization occurs is moderate, so that the resulted temperature gradient of a-Si in the scanning direction is also moderate. Due to this moderate temperature gradient, and together with the increased melting time of the upper a-Si, the solidification speed in the direction opposite to the scanning direction is decreased, which gives the generated crystal grains the time to grow in the direction perpendicular to the scanning direction of laser. In short, it is thought that not only the increased melting time of the upper a-Si due to the thermal reservoir effect of lower a-Si but also the moderate energy density profile of the low laser output power participated in the lateral crystallization plays an important role in enhancement of crystal grain growth in the perpendicular direction to the scanning direction of laser.

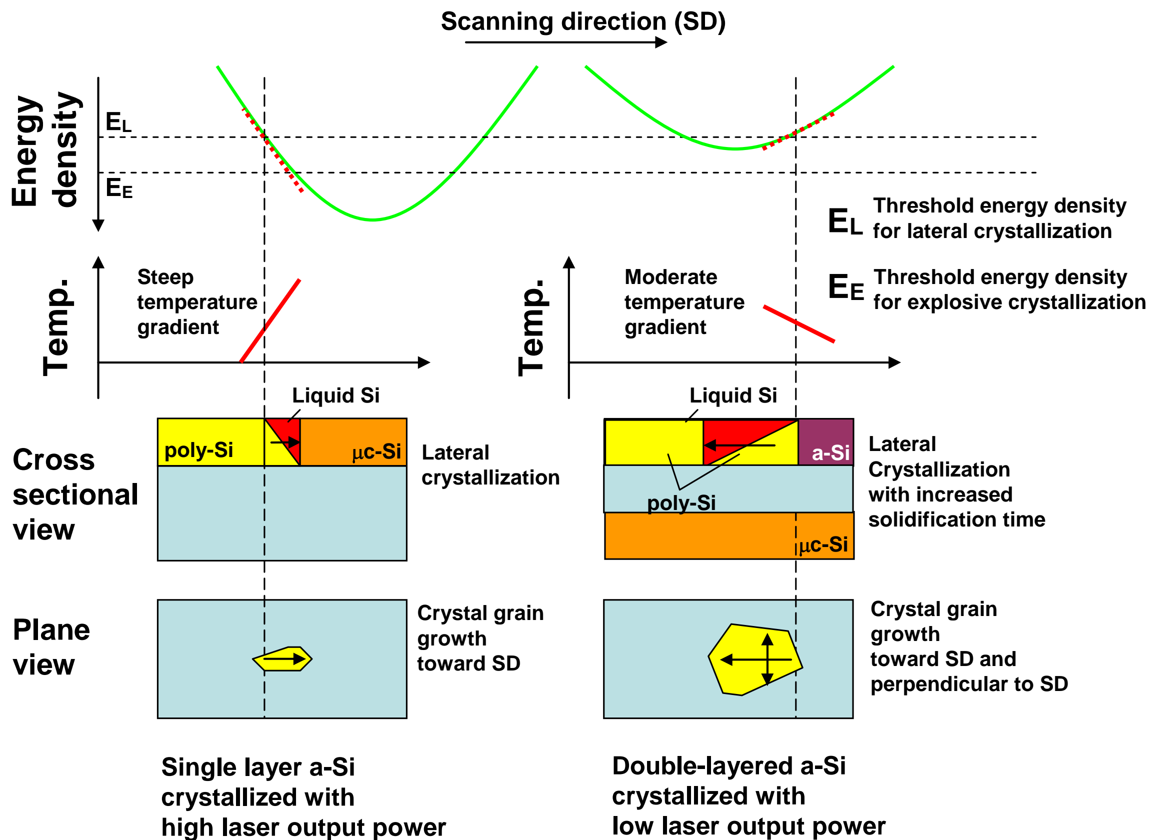


Figure 4.18: Schematics of estimated temperature profile in the scanning direction of laser and crystal grain growth of the single layer poly-Si (left) and the upper GLADLAX poly-Si (right) after irradiated by a laser pulse.

Summary

As elucidated above, in the GLA crystallization of double-layered a-Si thin films, the lower a-Si acts as a thermal reservoir in the optimum laser irradiation condition. The schematic of the crystallization mechanism is summarized in Fig. 4.19. In this experiment, only one structure of double-layered a-Si thin films was employed. Therefore, with different structure of double-layered a-Si (varying in the thickness of a-Si films and/or the interlayer SiO_x), the results of crystal grain evolution with respect to the laser output power will differ accordingly. That is also true with different laser irradiation configuration. From the consideration above, to get more enlarged crystal grains in the upper GLADLAX poly-Si, it would be appropriate to use the laser beam having more moderate energy density profile, ideally top flat, and employ longer irradiation pitch. By using different laser irradiation configuration and double-layered a-Si substrate with different structure, there would exist some condition which results in the lower poly-Si with more improved crystallinity. Although the detailed analysis needs numerical simulation of heat transfer between each film, in this subsection only qualitative discussion was presented. To get more information of the phase state of Si films during crystallization, the real-time observation of the crystallization is needed [15], which is one of future works

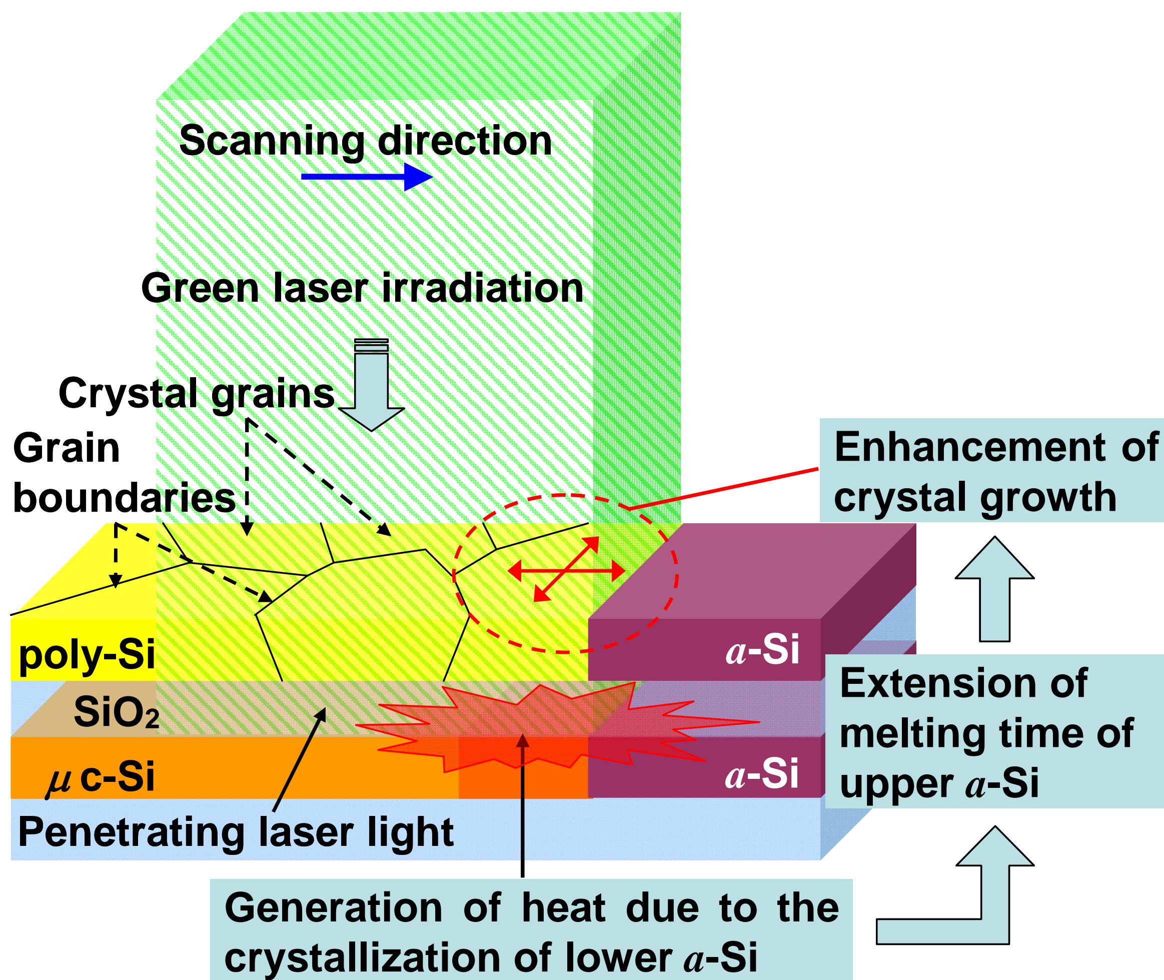


Figure 4.19: Model of the grain-enlargement of the upper GLADLAX poly-Si.

4.6 Electrical characteristics of GLA double-layered poly-Si TFTs

In the following two sections the GLA crystallized double-layered poly-Si films were applied to the fabrication of TFTs and their electrical characteristics were analyzed. In comparison, the characteristics of TFTs using GLA SL poly-Si were also evaluated. The relationship between their characteristics and the crystallinity of poly-Si films used was investigated in detail.

4.6.1 Fabrication and measurement of TFTs

The fabrication of TFTs was performed by employing the fabrication process established in Chapter 2. N-channel TFTs with their channel length and width of both 5 μm were fabricated in the maximum process temperature of 500 °C. Figs. 4.20 show schematics of the cross section of the TFTs and their microscope images. Here, TFTs using GLA SL poly-Si is defined as 'Single TFT', as shown in Fig. 4.20 (a), and TFTs using the upper GLADLAX poly-Si is defined as 'Double TFT', as shown in Fig. 4.20 (b).

The measurement of TFTs was carried out by using a semiconductor parameter analyzer. In the measurement of Double TFTs, the lower μc-Si layer was kept ungrounded. The field effect mobility (μ_{FE}) , subthreshold swing (S-value) and threshold voltage (V_{th}) of the each TFT characteristics were calculated. The detailed treatment is elucidated in the literature [16].

4.6.2 Electrical characteristics of TFTs

Channel directions of TFTs

In measuring the electric characteristics of GLA poly-Si TFTs, another classification of TFT is now defined. Since the GLA poly-Si films used possess

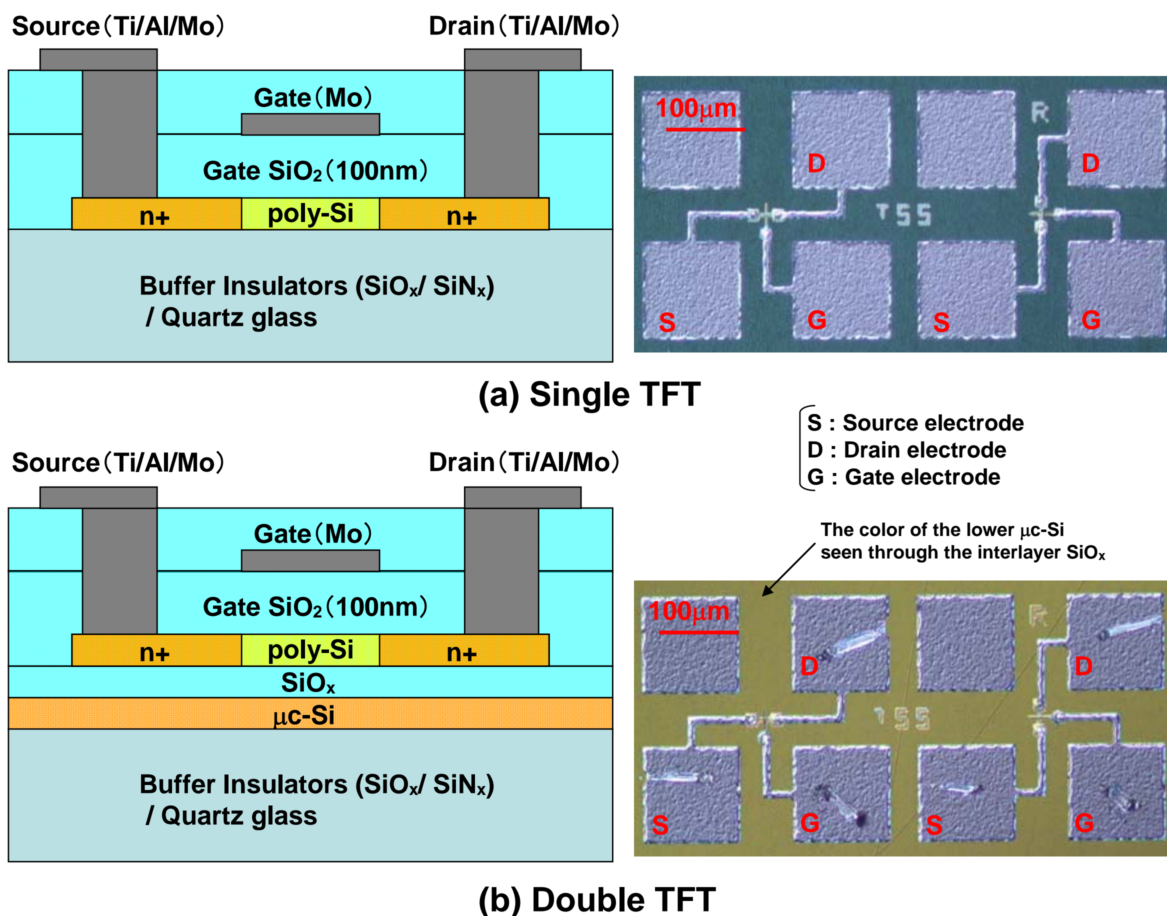


Figure 4.20: Schematics of the cross section of the TFTs (left) and their microscope images (right); (a) TFT using GLA SL poly-Si (Single TFT), (b) TFT using GLADLAX poly-Si (Double TFT).

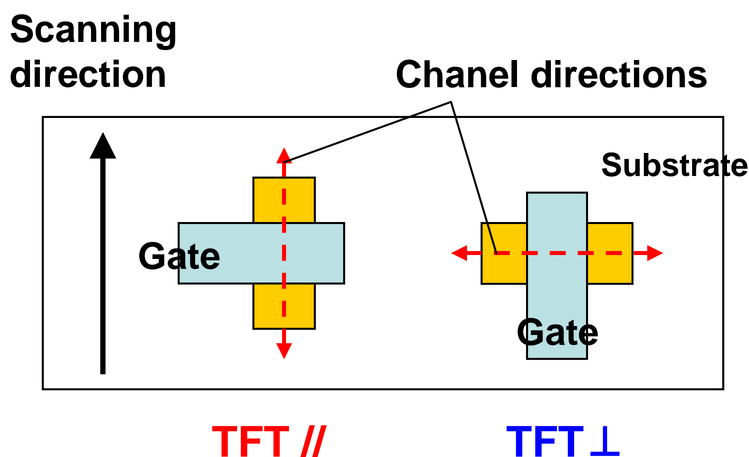


Figure 4.21: Two types of TFTs. TFT // is defined as that with its channel direction is parallel with the scanning direction of laser, while TFT⊥ is defined as that with its channel direction is perpendicular to the scanning direction of laser.

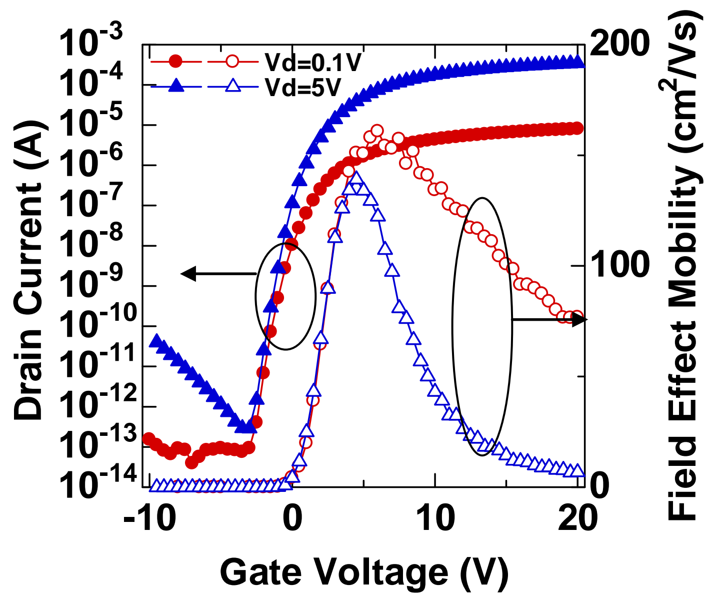
anisotropic morphology with respect to the laser scanning direction depending on the crystallization laser output power, the TFTs using the poly-Si films are expected to have the channel directional dependence of their electrical characteristics [17]. Therefore, TFTs with their channel direction in parallel with the scanning direction are defined as TFT //, whereas those with their channel direction perpendicular to the scanning direction are defined as TFT⊥, as shown in Fig. 4.21.

Single TFTs

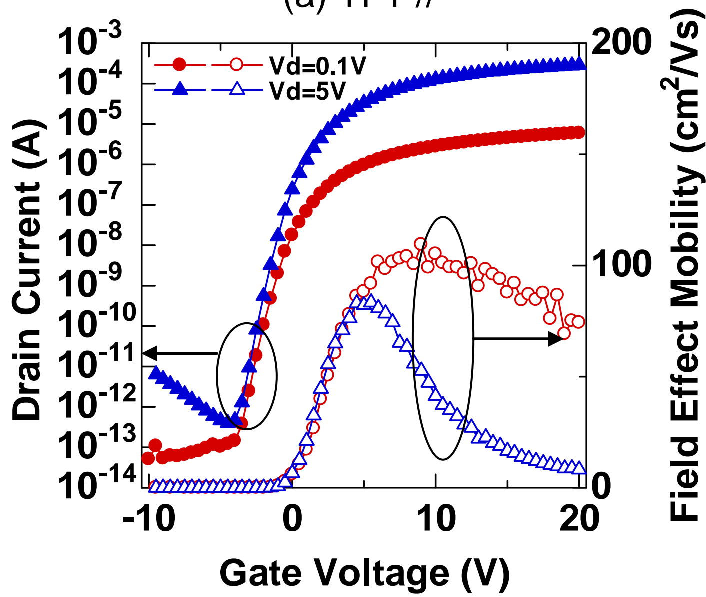
Figs. 4.22 show typical transfer characteristics of Single TFTs using GLA SL poly-Si crystallized with the laser output power of 125 W. The μ_{FE} in liner region of TFT // exceed over 150 cm^2 /Vs, whereas that of TFT⊥ reaches around 100 cm^2 / Vs. Reviewing the SEM image of the poly-Si film in Fig. 4.3, this decrease in μ_{FE} can be attributed to that the number of grain boundaries running mainly in parallel with the scanning direction is larger than that perpendicular to the scanning direction. That is, the carrier transport is more often interfered by the presence of grain boundaries in the channel of TFT⊥ than in the channel of TFT // [18].

Double TFTs

Figs. 4.23 show transfer characteristics of Double TFTs using upper GLADLAX poly-Si crystallized with the laser output power of 105 W. A remarkable upgrade of the electrical performance was observed, with the μ_{FE} in both channel directions of TFTs exceeding 350 cm^2 /Vs. This high field effect mobility was not observed in Single TFTs, the maximum of μ_{FE} of those was around 200 cm^2 / Vs, as seen later. Again reviewing the SEM image of the poly-Si film in Fig. 4.8, these TFTs with high μ_{FE} were considered to be fabricated at the point where the crystal grains were large enough to cover, but not entirely, the channel region of the TFTs. Figs. 4.24 show transfer and output characteristics of a Double TFT // using upper GLADLAX poly-Si crystallized with the laser output power of 100 W. The μ_{FE} of approximately 550 cm^2 / Vs was observed,



(a) TFT //



(b) TFT ⊥

Figure 4.22: Typical transfer characteristics of Single TFTs
(n-ch, W/L= 5/5 [mm], crystallization laser output power : 125 W).

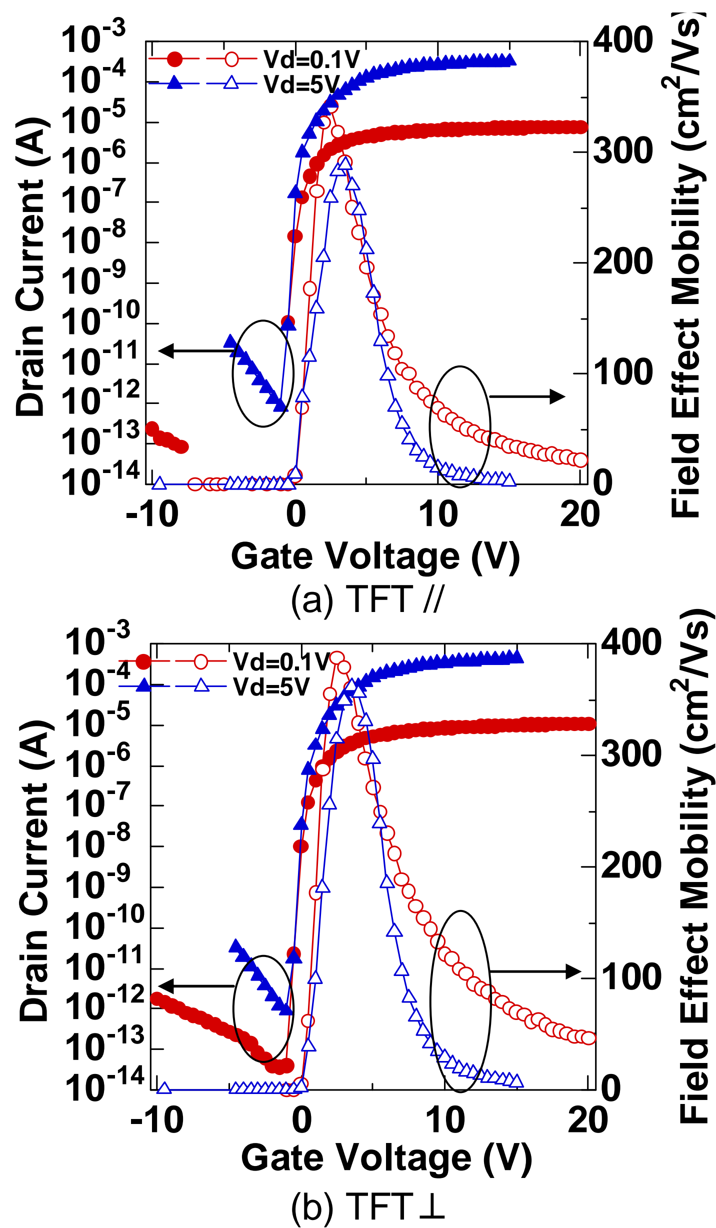
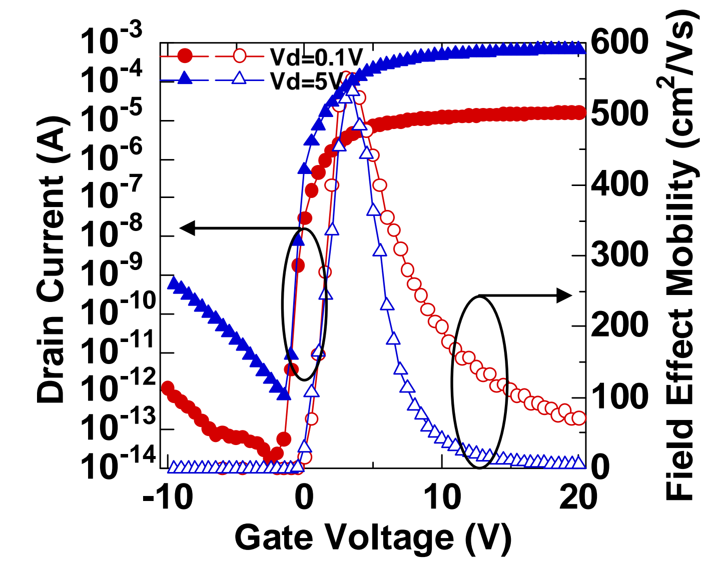
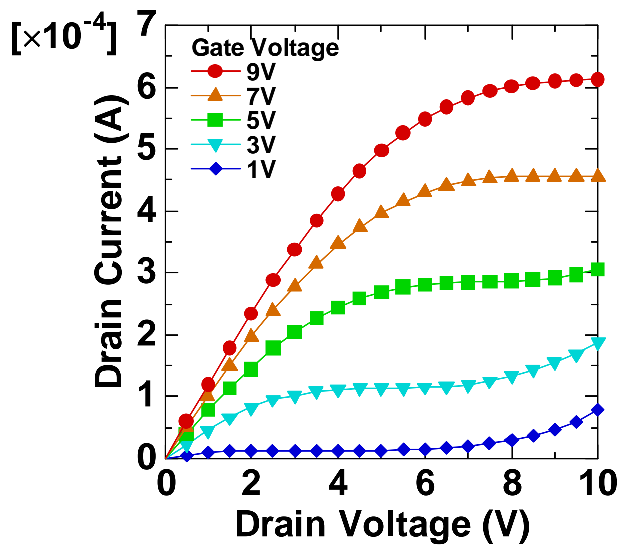


Figure 4.23: Transfer characteristics of the Double TFTs
(n-ch, W/L= 5/5 [mm], crystallization laser output power : 105 W).



(a) Transfer characteristics



(b) Output characteristics

Figure 4.24 (a) Transfer characteristics and (b) Output characteristics of Double TFT // (n-ch, W/L= 5/5 [mm], crystallization laser output power : 100 W).

which is a match for that of silicon on insulator (SOI) TFTs [19]. This suggests that this TFT was happened to be positioned at the crystal grains with the size comparable to the channel region. However, considering that the channel size of TFTs fabricated in this experiment is 5 × 5 μm, the crystal grain around that size is not identified in SEM observation. This issue is discussed in the next section.

Dependence on laser output power

Fig. 4.25 shows the crystallization laser output power dependence of field effect mobility of the TFTs. Over five TFTs in each laser output condition and in each channel direction were taken in the following figures. It can be seen that the magnitude level of μ_{FE} of Double TFTs is larger than that of Single TFTs on the whole. The average μ_{FE} of Single TFT⊥s was not improved with the increase of the laser output power, which can be attributed to that the Grain Width of GLA single layer poly-Si was not enlarged in higher laser output power. On the contrary, in accordance to the increase of Grain Width of the upper poly-Si of GLA double-layered poly-Si in increasing the laser output power, the upgrading of μ_{FE} of Double TFT⊥ was confirmed. However, by reviewing the laser output power dependence of the crystal grain size in Fig. 4.15, it can be seen that the two variations of μ_{FE} and the crystal grain size of poly-Si films with respect to the crystallization laser output power are not entirely correlated with each other.

Fig. 4.26 shows the crystallization laser output power dependence of subthreshold swing of the TFTs. It can be seen that the magnitude level of *S*-value of Double TFTs is larger than that of Single TFTs. For Single TFTs, *S*-value is decreasing with increasing laser output power. Since *S*-value is strongly related with the gate SiO_2 / poly-Si interface trap state density (D_{it}) and grain boundary trap state density (D_{gb}) [20], this result can be due to the decreasing number of grain boundaries in the channel region in accordance with the increasing crystal grain size of GLA single layer poly-Si.

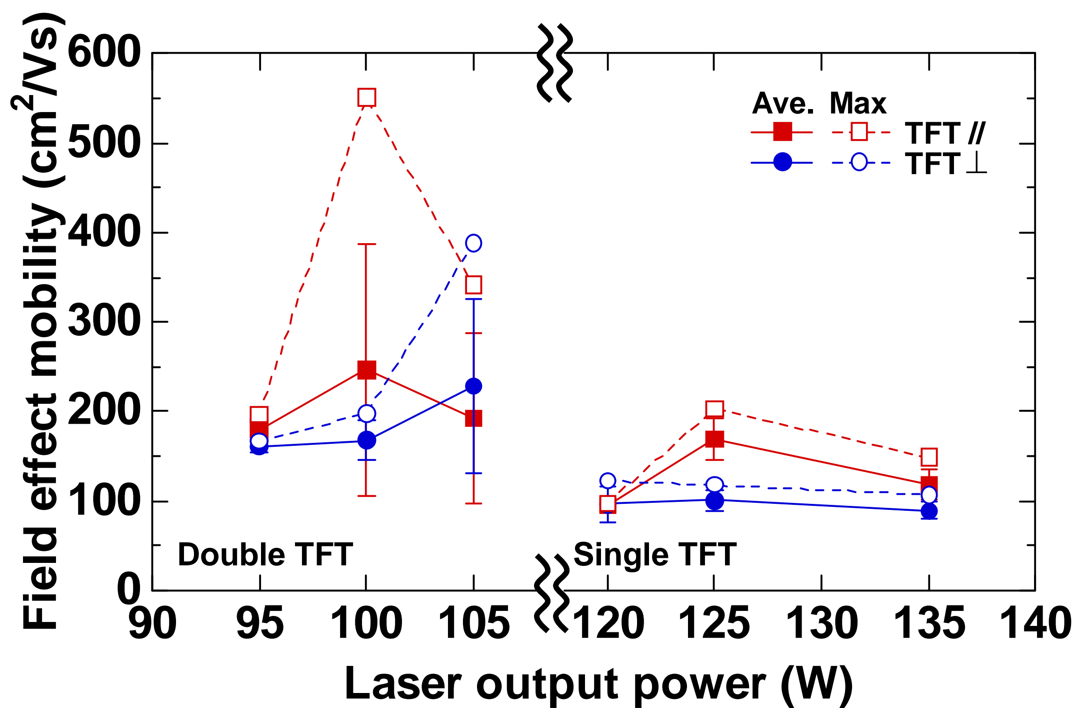


Figure 4.25: Crystallization laser output power dependence of field effect mobility of the TFTs.

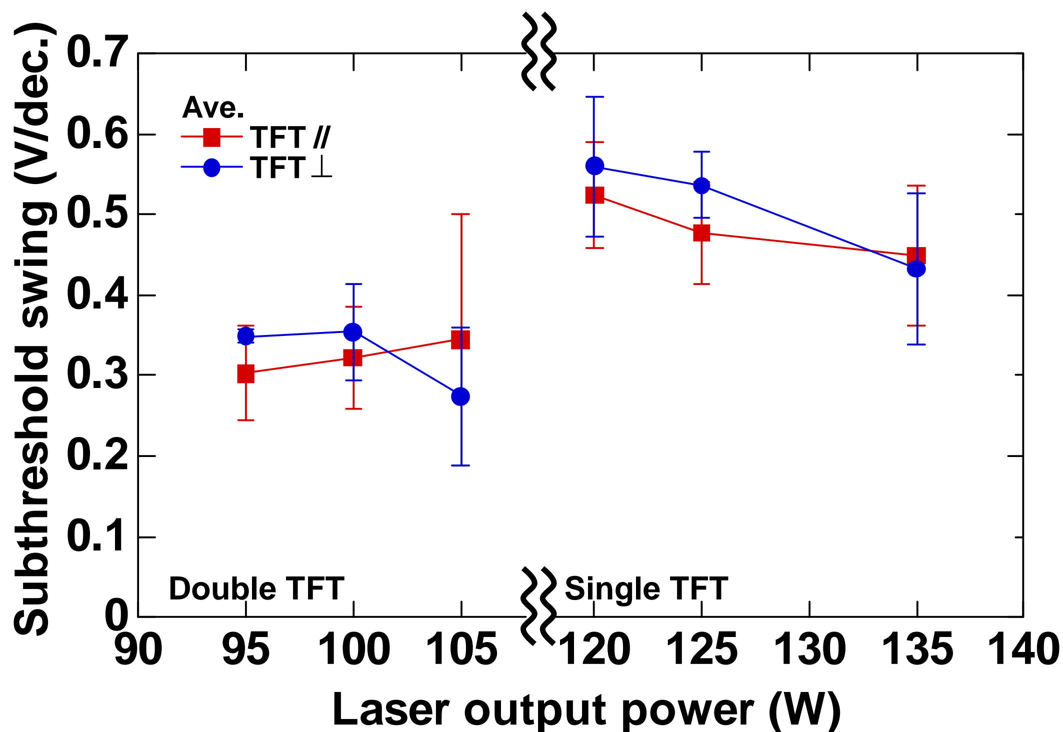


Figure 4.26: Crystallization laser output power dependence of subthreshold swing of the TFTs.

However, crystal grain size of GLA SL poly-Si crystallized with the laser output power of 120 is larger than that of the upper GLADLAX poly-Si crystallized with the laser output power of 95 W, but the *S*-value of TFTs using the former poly-Si film is larger than that of TFTs using the later. Thus, taking account of this phenomenon, it can be said that the *S*-value of Double TFTs is lower than that of Single TFTs is not totally explained by simple comparison of the size of crystal grains of GLA poly-Si.

Summary

In accordance to the enhanced crystal grain growth of the upper GLADLAX poly-Si, a dramatic improvement of the electrical performance of Double TFTs was confirmed. Some Double TFTs showed SOI-TFT like characteristics, meaning that the crystal grains of the upper poly-Si was increased to the size comparable to the TFT channel region. However, as seen above, there emerges one possibility that the characteristics of the Single and Double TFTs are not simply related by the crystal grain size of the poly-Si films used by those TFTs, the issue of which is treated in the next section.

4.7 Further analysis of GLA poly-Si films

4.7.1 μ-PCD analysis

To investigate the electrical property of upper GLADLAX poly-Si in comparing it with that of GLA SL poly-Si in more detail, evaluation of poly-Si by microwave photoconductive decay (μ-PCD) measurement was performed, and the results are examined to explain the relationship between crystallinity of poly-Si and TFT performance.

μ-PCD measurement of LTPS film

Here, the basic principle of the measurement is briefly explained [21]. μ-PCD is

a non-contact and nondestructive method of measuring the recombination lifetime of generated carriers by photo-excitation in a semiconducting material (in this study, poly-Si thin films), from the rate of decay of the reflectance of microwave irradiated on the sample. The recombination lifetime, in this case, is a measure of the crystallinity of the poly-Si. The light source for carrier excitation used in this measurement was a pulsed, frequency-tripled Nd:YLF ($LiYF_4$) laser with a wavelength of 349 nm, the laser spot diameter of approximately 1.5 mm, and a pulse duration of 15 ns. Since UV laser light was employed as the carrier-exciting light source, the penetration depth of the laser light in a poly-Si thin film was approximately 10 nm, as illustrated in Fig. 4.27. Thus, for poly-Si thin films with the double-layered structure used in this study, it is possible to evaluate the crystallinity of the upper poly-Si film without results being affected by the lower Si film, because the irradiated carrier excitation laser light is totally absorbed by the upper poly-Si film so that the generated carriers, which contribute to the reflection of the microwaves, are only from the surface of the upper poly-Si film.

Fig. 4.28 shows a schematic image of the change in the generated carrier density upon the irradiation of the carrier excitation laser. As shown in the figure, during irradiation by the laser, the density of generated carriers in the poly-Si attains a saturation value, which is well approximated by the product of the carrier injection velocity and the recombination lifetime of the poly-Si film under the condition of the recombination lifetime being sufficiently shorter than the pulse duration of the carrier-excitation laser. In response to the saturation value of the density of generated carriers, the reflection of the microwaves irradiated on the poly-Si thin film reaches a maximum value, hereafter called a reflectance-peak, which is proportional to the recombination lifetime. LPTS thin films have very short recombination lifetimes of approximately 100 ps; therefore, since the reflectance-peak of the microwave can be measured with much higher accuracy than the recombination lifetimes, the

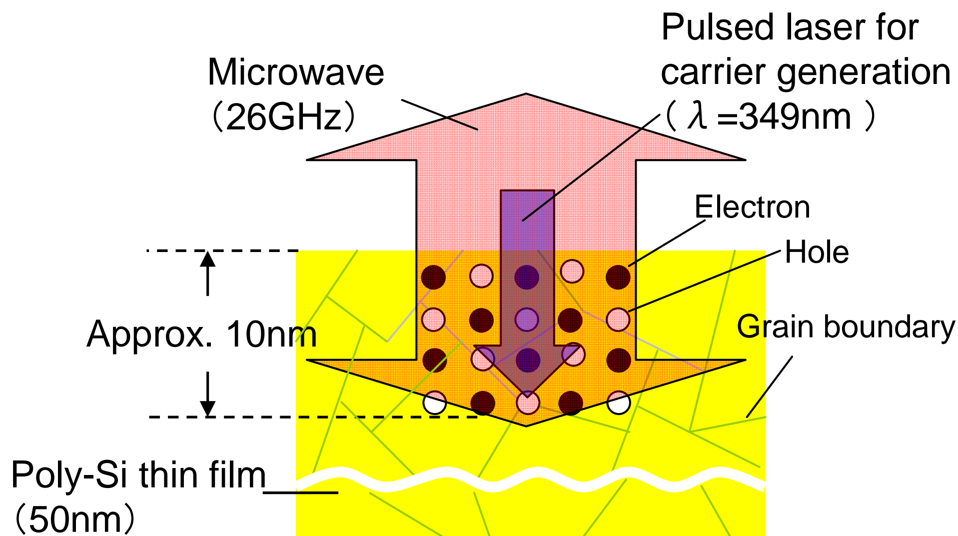


Figure 4.27: Schematic of carrier excitation in a poly-Si film by irradiation of pulsed UV laser.

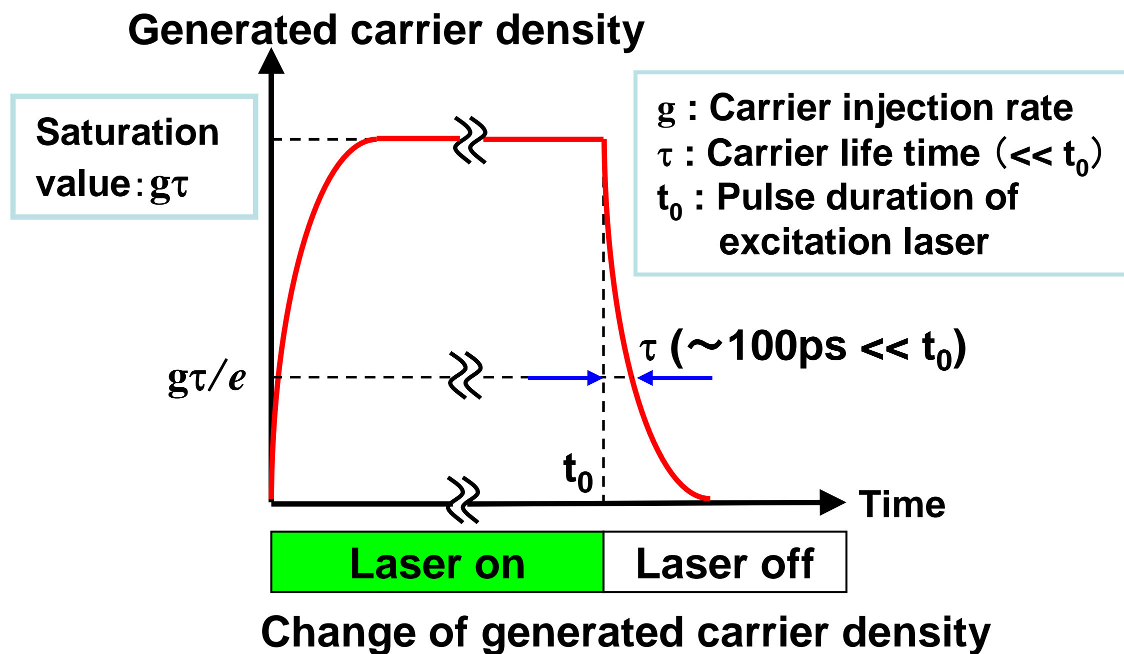


Figure 4.28: Schematic of the change in the generated carrier density upon the irradiation of the carrier excitation laser

reflectance-peak was adopted as the evaluation parameter of the crystllinity of poly-Si thin films in this study.

Dependence on electrical field direction

Figs 4.29 (a) shows a scanning electron microscopy (SEM) image of the surface of the GLA SL poly-Si crystallized with the laser output power of 125 W. The arrows in the figure indicate the scanning direction of the laser (SD). It can be seen that the poly-Si has distinct anisotropy, in which the grain boundaries mainly run parallel with SD. Figs 4.29 (b) and (c) show the reflectance-peak mapping images of the chip cut from the poly-Si substrate. The dotted polygon indicates the shape of the poly-Si substrate chip. The mapping image of the poly-Si measured with the microwave electric-field direction (EFD) parallel to SD is shown in (b), while that measured with EFD perpendicular to SD is shown in (c). The color-bar indicates the magnitude of the reflectance-peak, and the reddish part near the center of the mapping image (b) indicates a greater magnitude of the reflectance-peak.

Moreover, it can be seen that the magnitude of the reflectance-peak in mapping image (c) measured with EFD perpendicular to SD is lower than that in mapping image (b). This can be understood as follows. When EFD is perpendicular to SD in the reflectance-peak measurement of poly-Si with an anisotropic crystal morphology, the grain boundaries mostly extend parallel to SD, as a manifestation of the decrease in the recombination lifetime of the photo-excited carriers moving perpendicular to SD in response to the electric field of the microwave; thus, the carriers recombine more frequently when they cross the grain boundaries. It can be considered that this phenomenon corresponds to the considerable decrease in the mobility of the TFTs with the channel direction perpendicular to SD, compared with that of the TFTs with the channel direction parallel to SD, as can be seen in Figs. 4.22, since the carriers traveling in the channels are scattered more frequently in the former TFTs than in the latter.

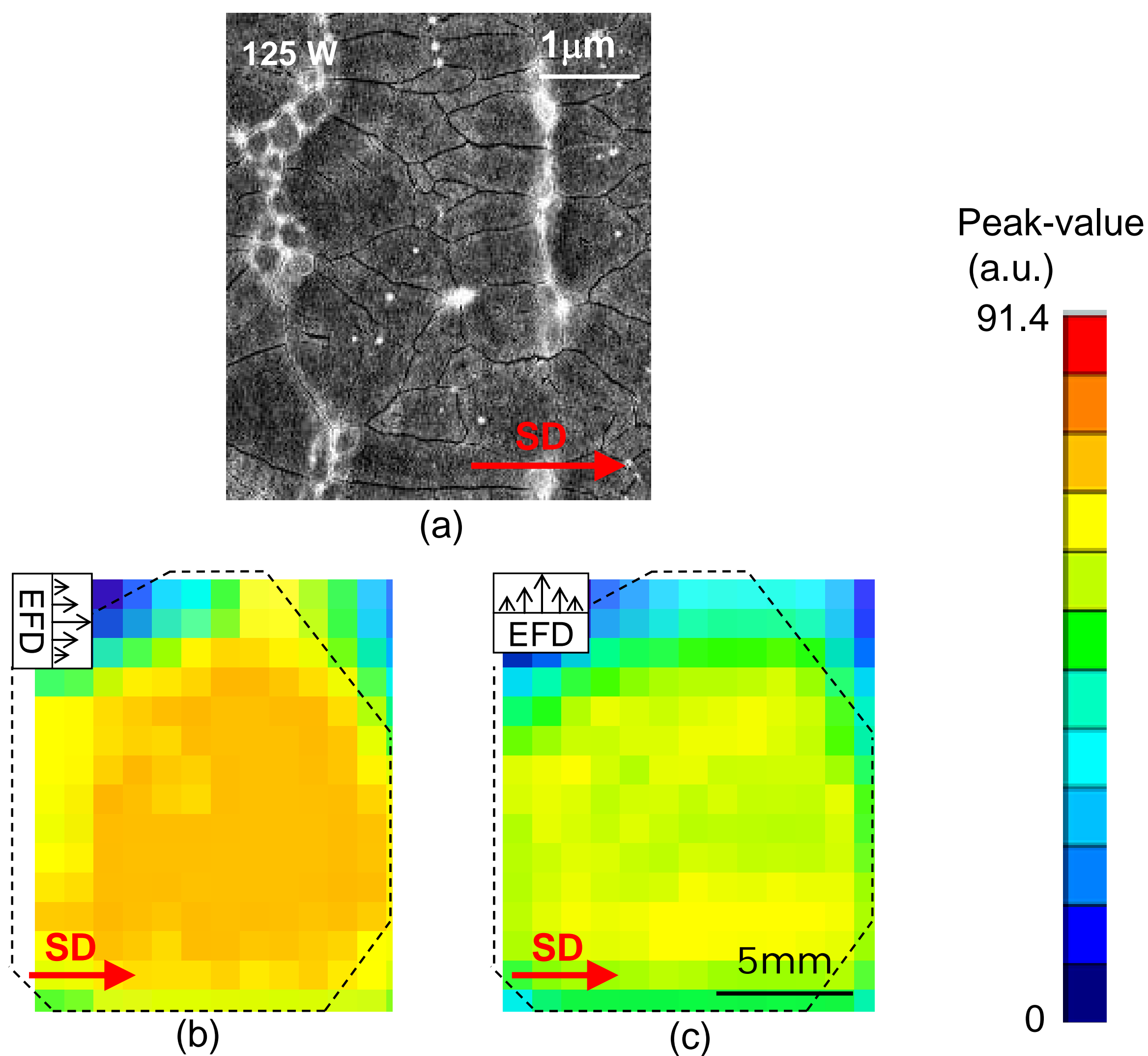


Figure 4.29: Observation of anisotropy of poly-Si crystal morphology by reflectance peak mapping measurement (EFD: electric-field direction of microwave, SD: scanning direction of laser). (a) SEM image of surface of a GLA SL poly-Si. (b, c) Mapping image of reflectance peak of the microwave for (b) EFD ∥ SD and (c) EFD ⊥ SD.

These results demonstrate that by μ-PCD measurement of the reflectance-peak mapping images of the microwaves irradiated on the poly-Si thin films, it is possible to nondestructively observe the anisotropy of poly-Si without observing the poly-Si surface directly, such as by SEM.

Correlation between reflectance peak level and TFT performance

Next, the relationship between the reflectance-peak of the poly-Si thin films and the mobility of the TFTs was investigated. Fig. 4.30 shows mapping images of reflectance-peak of the upper GLADLAX poly-Si and the GLA SL poly-Si. The same sample was measured with the electric field direction of microwave (EFD) in parallel with the scanning direction of laser annealing (SD), and EFD perpendicular to SD (lower side). The decrease in reflectance-peak of the poly-Si films measured with the EFD perpendicular is remarkable in GLA SL poly-Si films in higher laser output condition, whereas the reflectance-peak of the upper GLADLAX poly-Si films is apparently unchanged irrespective of the EFD. This suggests that the electrical property of grain boundaries in the upper GLADLAX poly-Si is different from that in the GLA SL poly-Si.

Fig. 4.31 shows the relationship between the average reflectance-peak near the center of the mapping image of each poly-Si chip (hereafter called the reflectance peak-level or simply, peak level) and the crystallization laser energy density of poly-Si. The left-hand side of the figure shows the reflectance-peak of the upper GLADLAX poly-Si, and the right-hand side shows that of GLA SL poly-Si. The reflectance-peak measured when EFD was parallel and perpendicular to SD is plotted in the figure. It can be seen that the reflectance-peak of upper GLADLAX poly-Si is larger than that of GLA SL poly-Si. When this graph is compared with the plot of the relationship between the mobility of the TFTs and the crystallization laser output power of the poly-Si used in the TFTs, as shown in Fig. 4.25, it is found that the degrees of mobility and the reflectance-peak correspond to each other in upper GLADLAX poly-Si and GLA SL

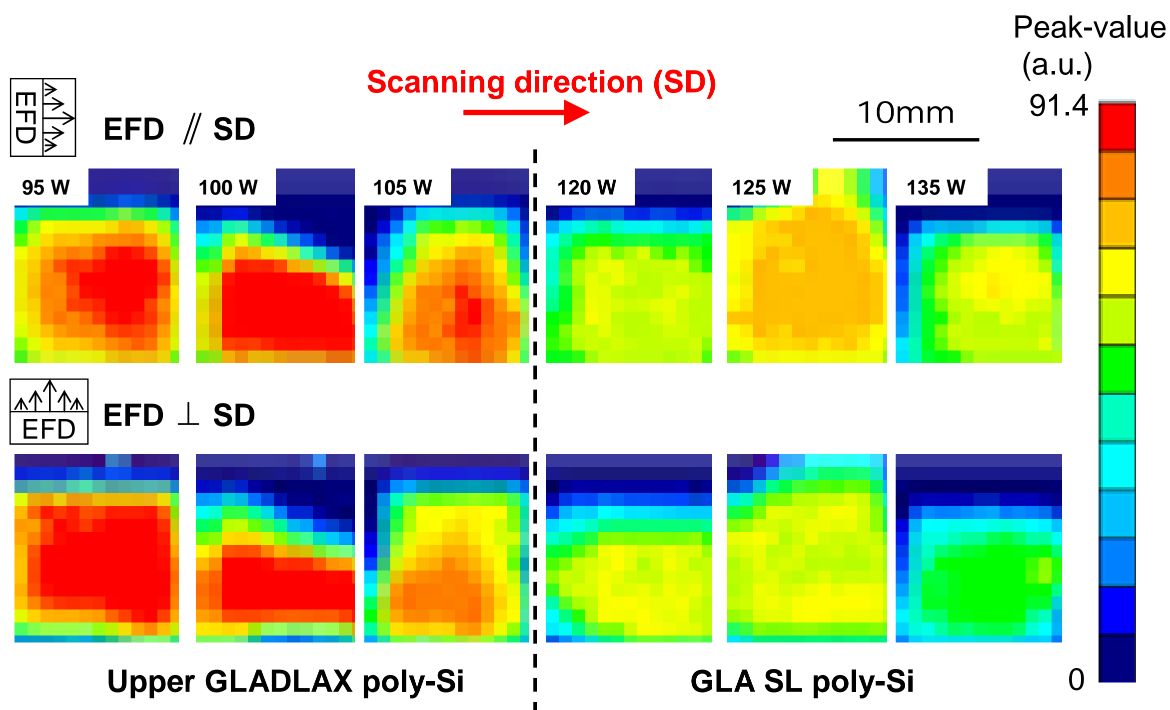


Figure 4.30: Mapping images of reflectance-peak of the upper GLADLAX poly-Si (left side) and the GLA SL poly-Si (right side). The same sample was measured with the electric field direction of microwave (EFD) in parallel with the scanning direction of laser annealing (SD) (upper side), and EFD perpendicular to SD (lower side). The figure shown in the each upper image is the crystallization laser output power.

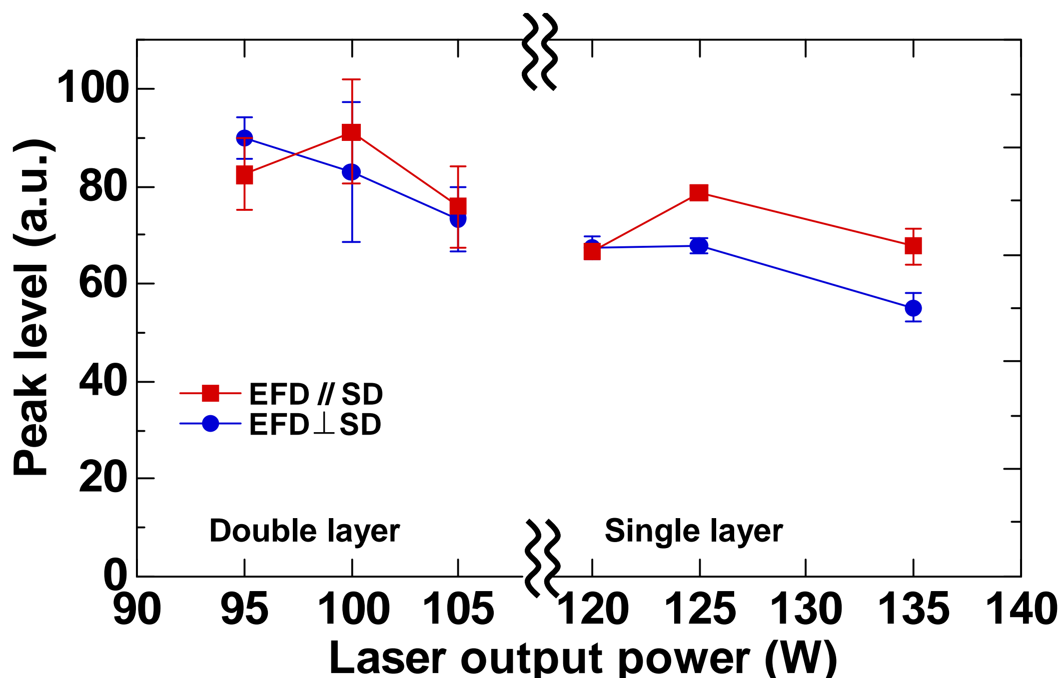


Figure 4.31: Relationship between reflectance peak level and crystallization laser energy density of upper GLADLAX poly-Si and GLA SL poly-Si (upper side), and crystallization laser energy dependence of averaged field effect mobilities of the upper GLADLAX poly-Si TFTs (lower side).

poly-Si.

On the basis of these results, the above mentioned graphs were re-plotted with the reflectance-peak along the horizontal axis and the mobility along the vertical axis. Figs 4.32 show the re-plotted graphs of the relationship between the field effect mobility of the TFTs and the reflectance-peak of the poly-Si measured with the direction of the TFTs channels and the electric field of the microwave (a) parallel to SD and (b) perpendicular to SD. Although there is variation in the data, there is a correlation between the mobility of the TFTs and the reflectance-peak of the microwave obtained by μ-PCD mapping measurement of the poly-Si. These results confirm superiority of the crystallinity of the upper layer of the GLADLAX poly-Si, which was not possible from only from the comparison of the grain sizes., and it is now clear that μ-PCD mapping measurement of the reflectance-peak is highly effective in evaluating the crystallinity of poly-Si formed by GLADLAX, as well as that of conventional LTPS thin films.

Likewise, Figs. 4.33 show the re-plotted graphs of the relationship between the *S*-value of the TFTs and the reflectance-peak of the poly-Si measured with the direction of the TFTs channels and the electric field of the microwave (a) parallel to SD and (b) perpendicular to SD. The *S*-value of Double TFTs are seen to be lower than that of Single TFTs and to be correlated with the peak level of the poly-Si films used in the TFTs. Together with Figs. 4.32, these results suggest not only that the grain boundary trap state density (D_{gb}) of the upper GLADLAX poly-Si is lower than that of GLA SL poly-Si, but also that the D_{gb} per grain boundary is lower than that of GLA SL poly-Si. It can be considered that, as the origin of the observed high crystallinity, there is the possibility of an improvement in the electrical property of defects in the crystal grain boundaries and/or in crystal grains of the upper GLADLAX poly-Si via an annealing effect due to the thermal storage of the lower a-Si film of the double-layered substrate.

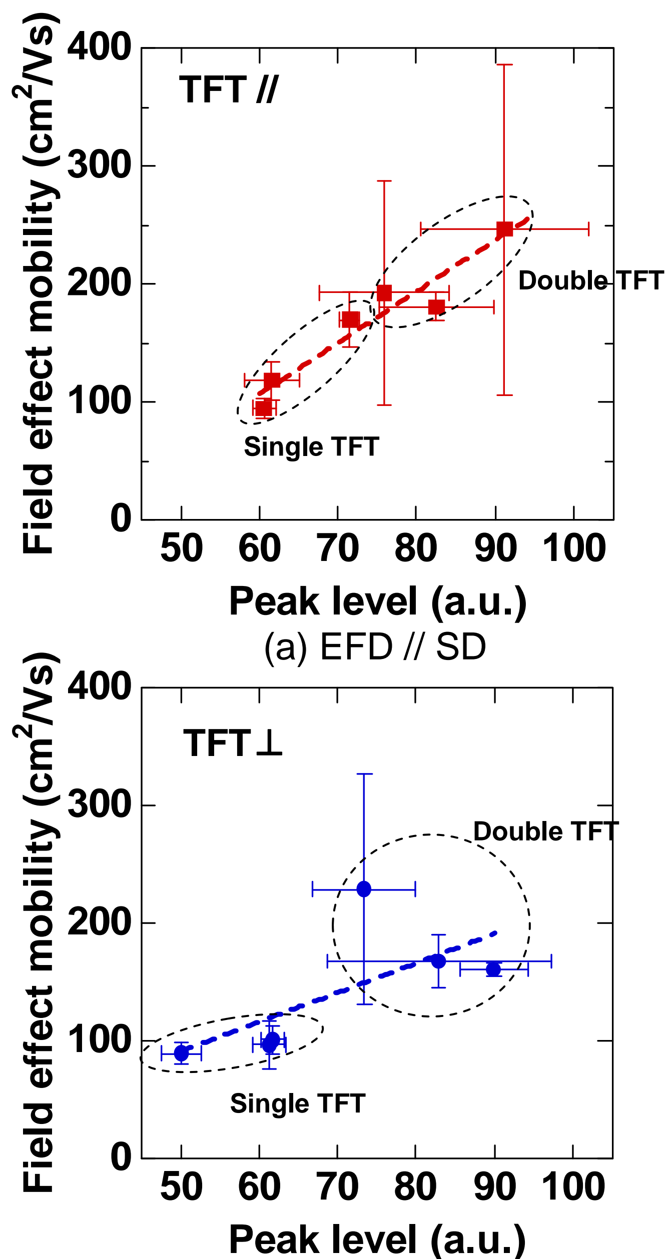
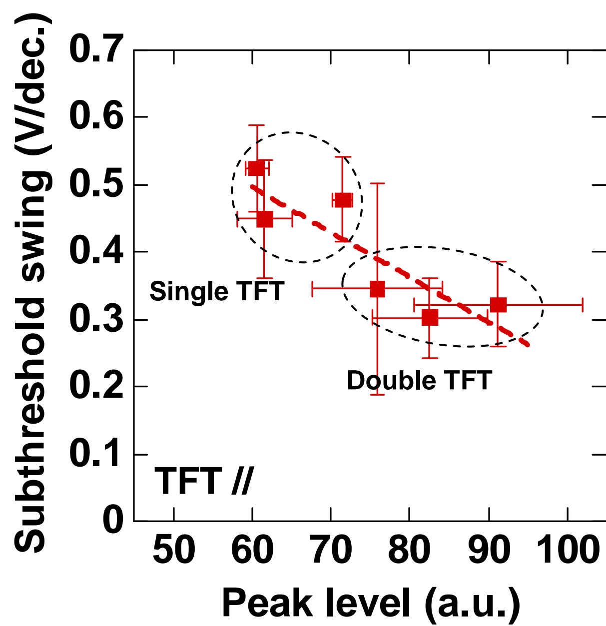
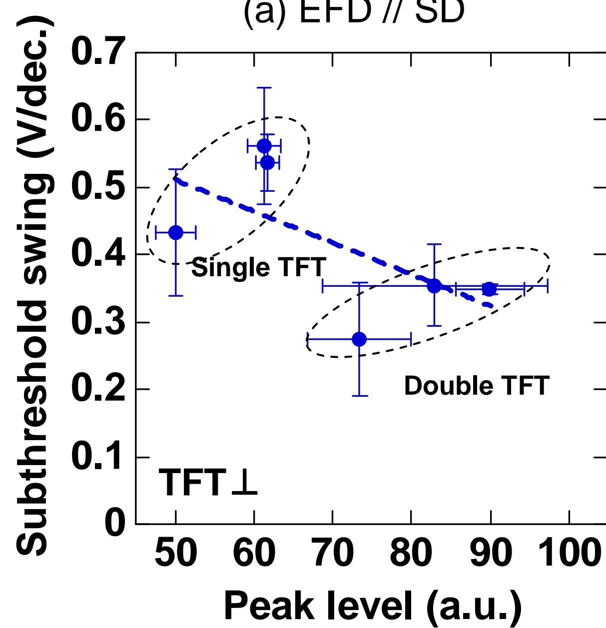


Figure 4.32: Relationship between mobility of upper GLADLAX poly-Si TFTs and GLA SL poly-Si TFTs and the peak level of the poly-Si films used in the TFTs.



(a) EFD // SD



(b) EFD ⊥ SD

Figure 4.33: Relationship between subthreshold swing of upper GLADLAX poly-Si TFTs and GLA SL poly-Si TFTs and the peak level of the poly-Si films used in the TFTs.

Summary

The crystallinity of double-layered poly-Si thin films crystallized by solid green laser annealing (upper GLADLAX poly-Si) was evaluated in comparison with that of the conventional green-laser annealed single-layer poly-Si (GLA SL poly-Si) by reflectance-peak mapping measurement by μ-PCD. As a result, the anisotropy of the poly-Si was observed as a difference in the reflectance-peak. Furthermore, the upper layer of the GLADLAX poly-Si had a larger microwave reflectance-peak than the GLA single-layer poly-Si, and correlation was confirmed between the reflectance-peak of the poly-Si and the electrical performance of the TFTs with poly-Si. From these results of the evaluation by μ-PCD measurement, it was clarified that the upper layer of the GLADLAX poly-Si had better crystallinity than that of the GLA SL poly-Si.

4.7.2 EBSD analysis

From the μ-PCD analysis of GLA poly-Si films, knowledge on the existence of crystal grain boundaries with improved electrical property in the upper GLADLAX poly-Si was obtained. Next, to investigate the microstructure of GLA poly-Si films more closely, the electron back scattering diffraction (EBSD) analysis of the upper GLADLAX poly-Si and GLA SL poly-Si was performed. By taking diffraction patterns (Kikuchi patterns) by using a back scattering electron diffraction pattern imager (slow scanning type CCD camera) installed to a scanning electron microscope, the information on crystal orientation and grain boundary of polycrystalline materials within fine scaled region [22]. The crystal orientation of the sample is analyzed through the diffraction pattern generated from the Bragg reflection of the inelastic scattering from specific lattice planes when the electron beam is irradiated into the sample.

Using this EBSD method, the micro structure of the GLA SL poly-Si crystallized with the laser output power of 125 W and the upper GLADLAX poly-Si

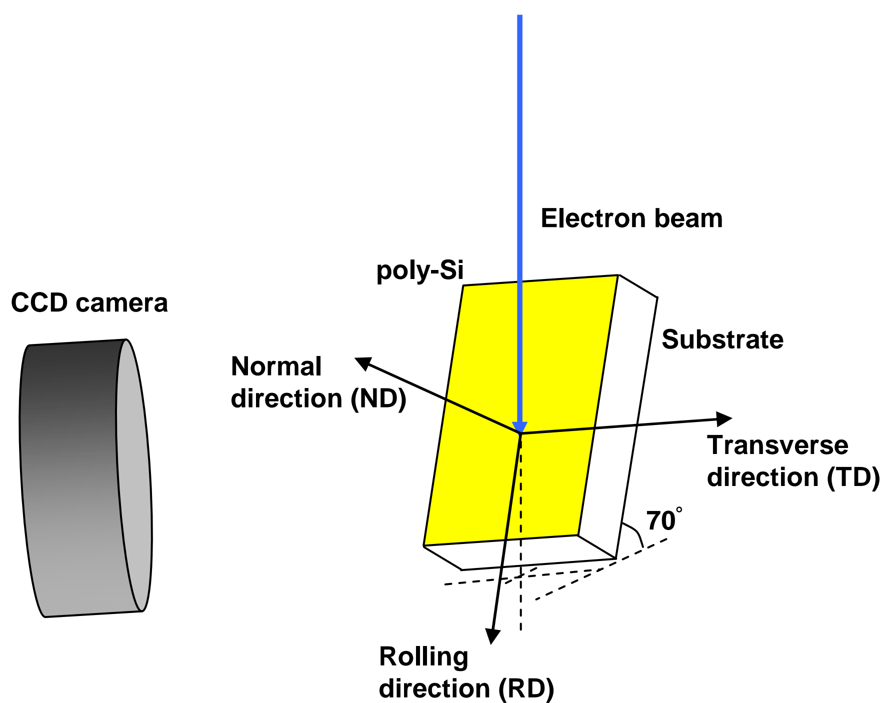


Figure 4.34: Configuration of the sample and the image detector.

crystallized with the laser output power of 100 W were evaluated (These two poly-Si films were chosen because the TFTs using these poly-Si showed higher electrical performance than other TFTs). The measurement conditions were as follows; the accelerated voltage was 15.0 kV, the current of incident electron beam was 1.5 nA, the tilting angle of the sample was 70 deg taken from the plane vertical to the direction of the electron beam, the magnification was 5,000 ×, the scanning region was 12 × 30 μm and the stepping interval was 50 nm. The measurement was done after the sample was fixed on to the sample holder by Ag paste and deposited with a carbon thin film to prevent charging up. Configuration of the sample and the image detector is shown in Fig. 4.34.

Crystal orientation

Fig. 4.35 shows the colored images of crystal orientation map of the GLA poly-Si films. These images illustrate the orientation of crystal domains which is indicated by neutral color of the three primary colors (Red, Green, Blue) each of which is assigned to the three apexes of unit stereo triangle in inverse pole figure (base orientation : <001>, <101>, <111>), respectively. These images were produced by the data taken when the detection orientation is normal to the substrate surface plane. As can be seen from the mapping images, the many crystal grains with shape elongating toward the scanning direction GLA SL poly-Si was observed, the extension of which is less than 2 μm. On the contrary, in the upper GLADLAX poly-Si, the crystal grains extending over 3 μm toward scanning direction, some extending as far as 5 μm, were observed. These large crystal grains were found to be elongating toward perpendicular to the scanning direction. However, in viewing the overall image, it was found that the orientation of crystal grains is not aligned to a particular direction.

Image Quality mapping

Fig. 4.36 Image Quality (IQ) mapping images of the GLA poly-Si films.

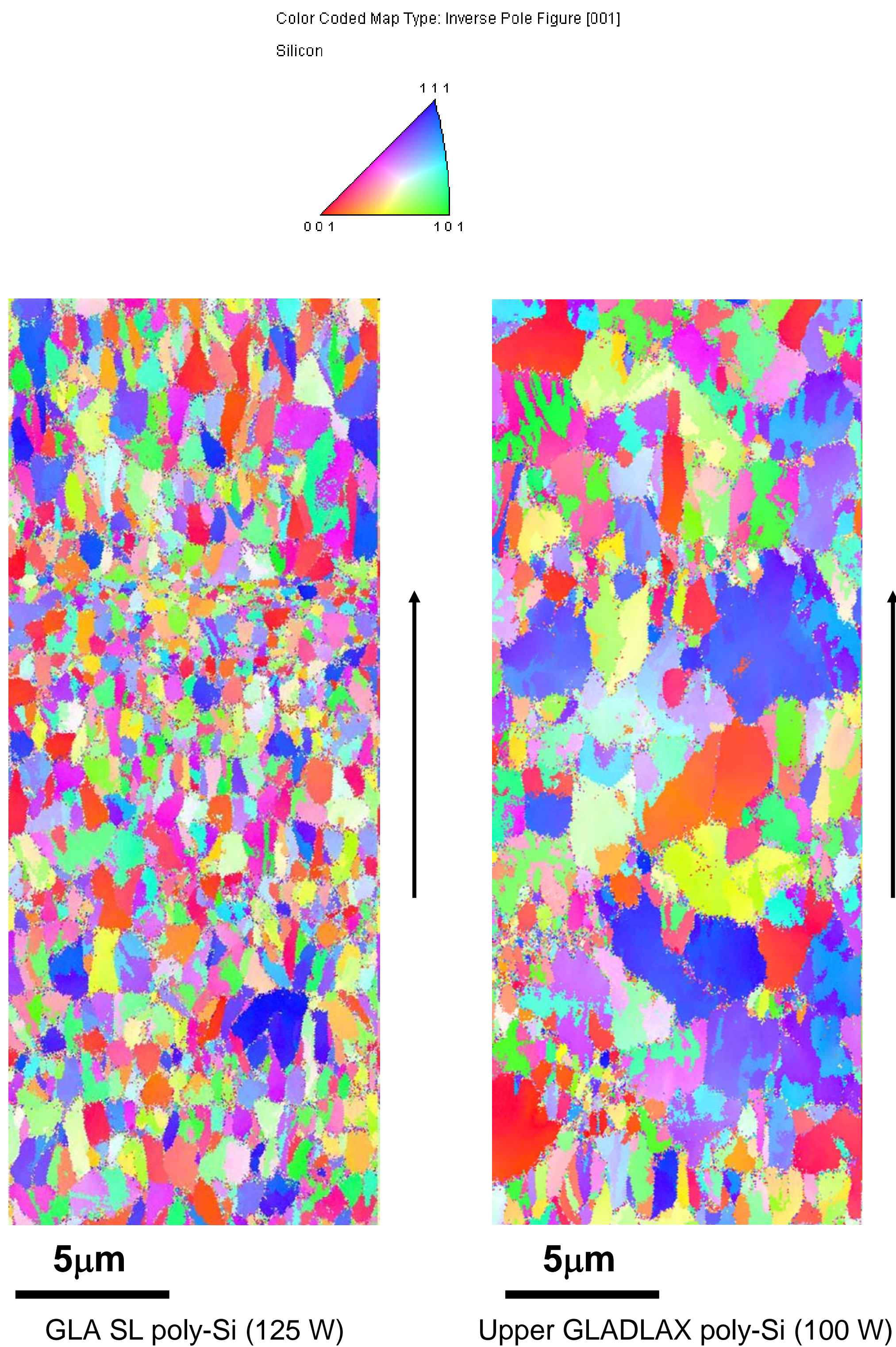


Figure 4.35: EBSD orientation mapping images of GLA SL poly-Si and upper GLADLAX poly-Si and color triangle coordinate indicating crystalline orientations. The arrows indicate laser scanning direction.

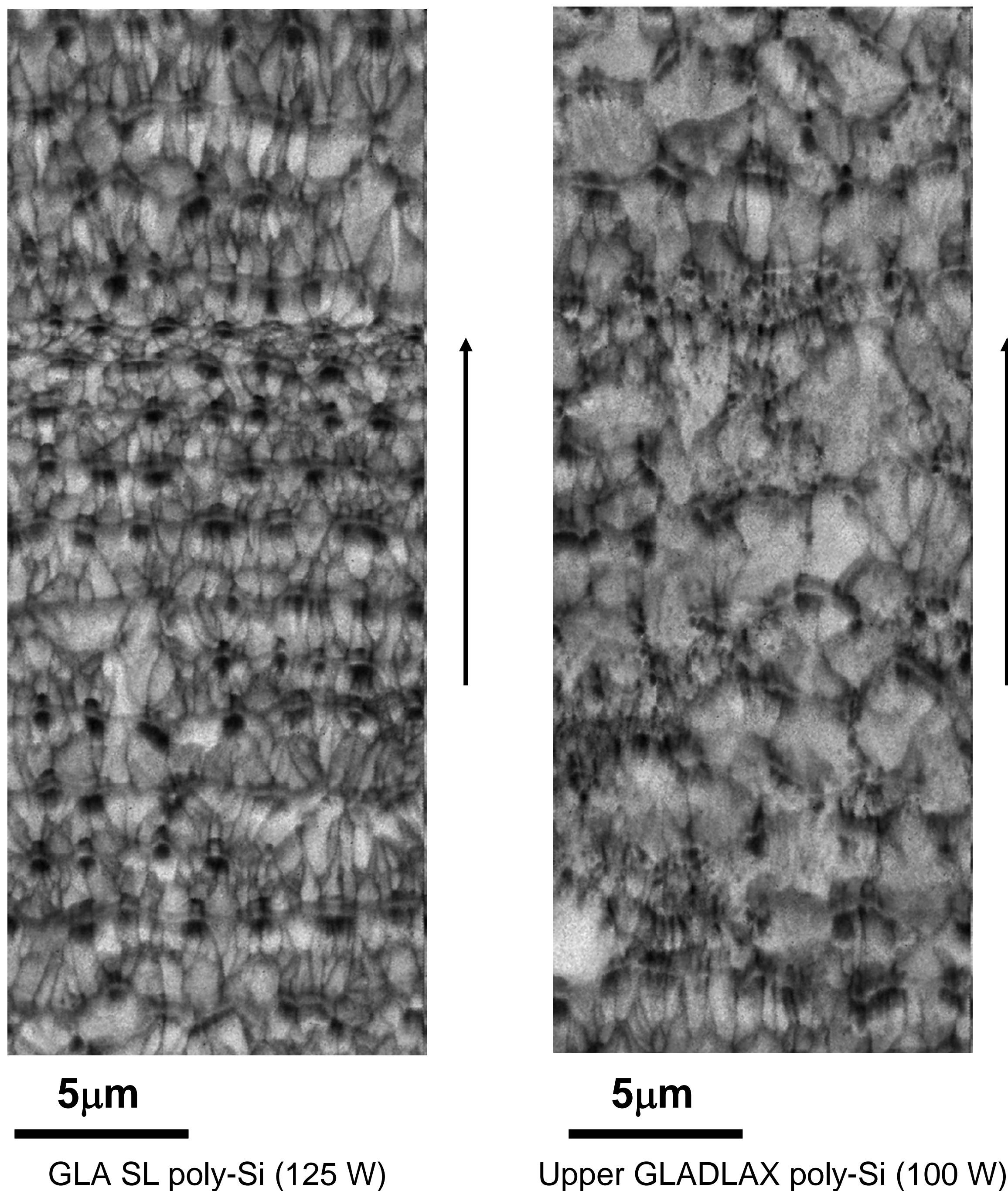


Figure 4.36: Image Quality (IQ) mapping images of GLA SL poly-Si and upper GLADLAX poly-Si. The arrows indicate laser scanning direction.

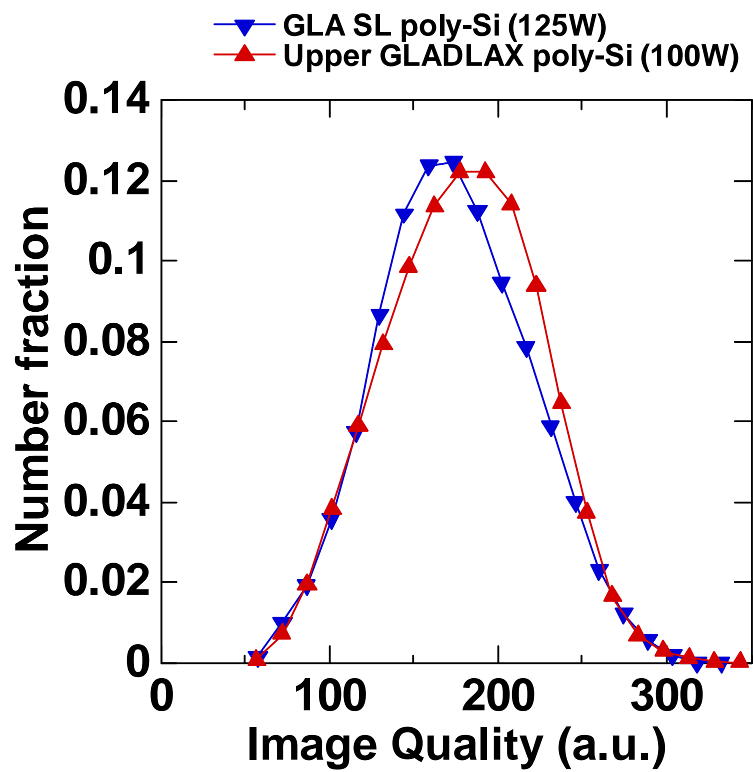


Figure 4.37: Distribution of grain average Image Quality of GLA poly-Si films.

IQ-value indicates the sharpness of EBSD pattern, which decreases at grain boundaries, surface distortion and surface contamination where the pattern becomes unclear. Thus, from the IQ-value it is possible to evaluate the crystallinity of the poly-Si films. In the IQ mapping image of GLA SL poly-Si, the grain boundaries indicated by dark lines running toward the scanning direction are clearly observed. Moreover, in the small crystal grain region the grain boundaries are not obscured. On the contrary, some grain boundaries in the upper GLADLAX poly-Si are observed to be unclear, especially in the small crystal grain regions and in the inner side of the enlarged crystal grains. This suggests that the there are grain boundaries in the upper GLADLAX poly-Si which differ with that in the GLA SL poly-Si in quality. Fig. 4.37 shows the distribution of Image Quality of GLA poly-Si films. It can be seen that the IQ-value distribution of the upper GLADLAX poly-Si is slightly sifted toward higher value, suggesting the crystallinity of the poly-Si is improved compared to the GLA SL poly-Si

Coincident site lattice and crystal grain size

Figs. 4.38 show number fraction of misorientation angle of GLA SL poly-Si and upper GLADLAX poly-Si. According to the histogram, the upper GLADLAX poly-Si includes many high angle grain boundaries at around 60 degrees in misorientation angle compared to that of GLA SL poly-Si.

The high angle grain boundaries are described by the misorientation between two adjacent grains. When these high angle grain boundaries are coincidence grain boundaries, there exists a lattice common to both adjacent grains. It is referred to as coincidence site lattice (CSL) and expressed by Σ parameter [23]. The Σ value is the reciprocal number of coincidence sites in the lattice that are occupied by the atoms of both grains. It is known that the symmetric Σ boundaries are the class of twin boundaries and these twin boundaries represent low energy configurations [24]. By EBSD analysis, it is able to separate these CSL boundaries from other random grain boundaries. Fig.

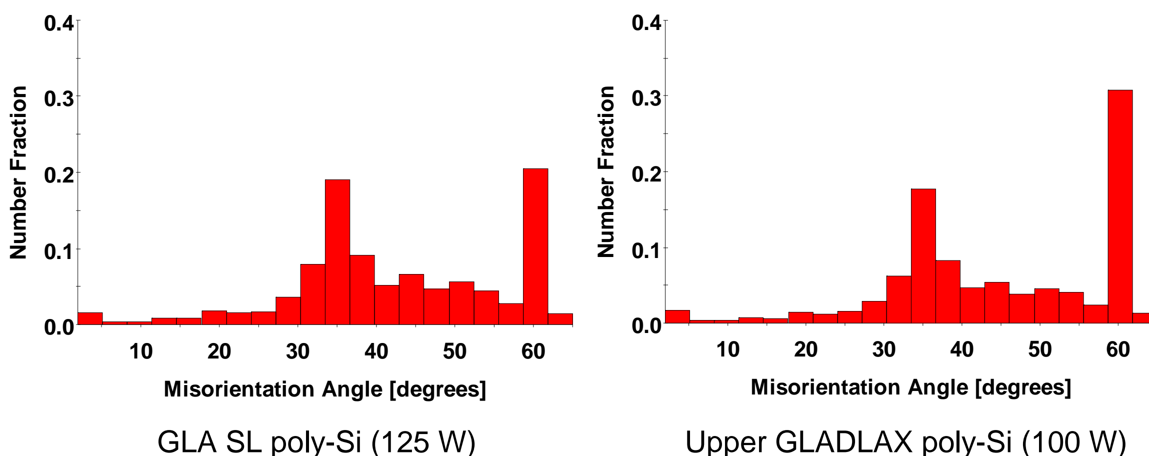


Figure 4.38: Number fraction of misorientation angle (upper) of GLA SL poly-Si and upper GLADLAX poly-Si.

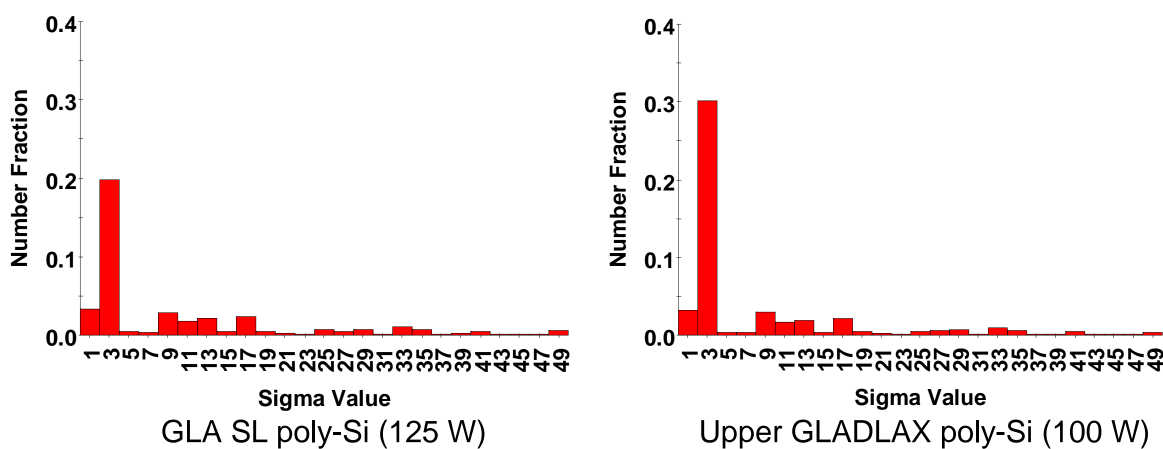


Figure 4.39: Number fraction of coincident site lattice of GLA SL poly-Si and upper GLADLAX poly-Si.

4.39 show number fraction of CSL boundaries. It can be seen that the number fraction of Σ3 CSL boundary in the upper GLADLAX poly-Si is larger than that of GLA SL poly-Si. The CSL boundaries most frequently observed in poly-Si are {111} Σ3 and {122} Σ9 [25]. The {111} Σ3 CSL boundary is known as coherent twin as well as electrically inactive.

Thus, in evaluating the crystal grains of the GLA poly-Si films, firstly the {111} Σ3 CSL boundary is considered, next the {111} Σ3 CSL boundary is excluded in the evaluation, and finally those two results from the different calculation treatments were compared. Fig. 4.40 shows EBSD crystal grain image of GLA SL poly-Si and the same image with the {111} Σ3 CSL boundaries were excluded. The crystal grains in the mapping images are determined by the grain boundary which is defined when the difference of angle of direction of adjacent measurement points is over 5° and expressed in grayscale. It can be seen that some of the crystal grains fused with the adjacent grains and they became larger grains. However, the overall difference is not considerable, and it appears that the grain boundaries running in the scanning direction are vanishing in the grain fusion.

Fig. 4.41 shows EBSD crystal grain image of upper GLADLAX poly-Si and the same image with the {111} Σ3 CSL boundaries were excluded. It can be seen that the resulted large crystal grains by the fusion of the two adjacent grains is notable. Not only the grain boundaries running in the scanning direction but also that running perpendicular to the scanning direction are participating the fusion of crystal grains. This result can be understood by that the fraction number of upper GLADLAX poly-Si is larger than that of GLA SL poly-Si. It can be observed that there is a crystal grain that spread as far as approximately 5 μm in both directions. If the TFT channel region is placed at this large crystal grain, the TFT would exhibit the electrical performance comparable to that of a SOI-TFT.

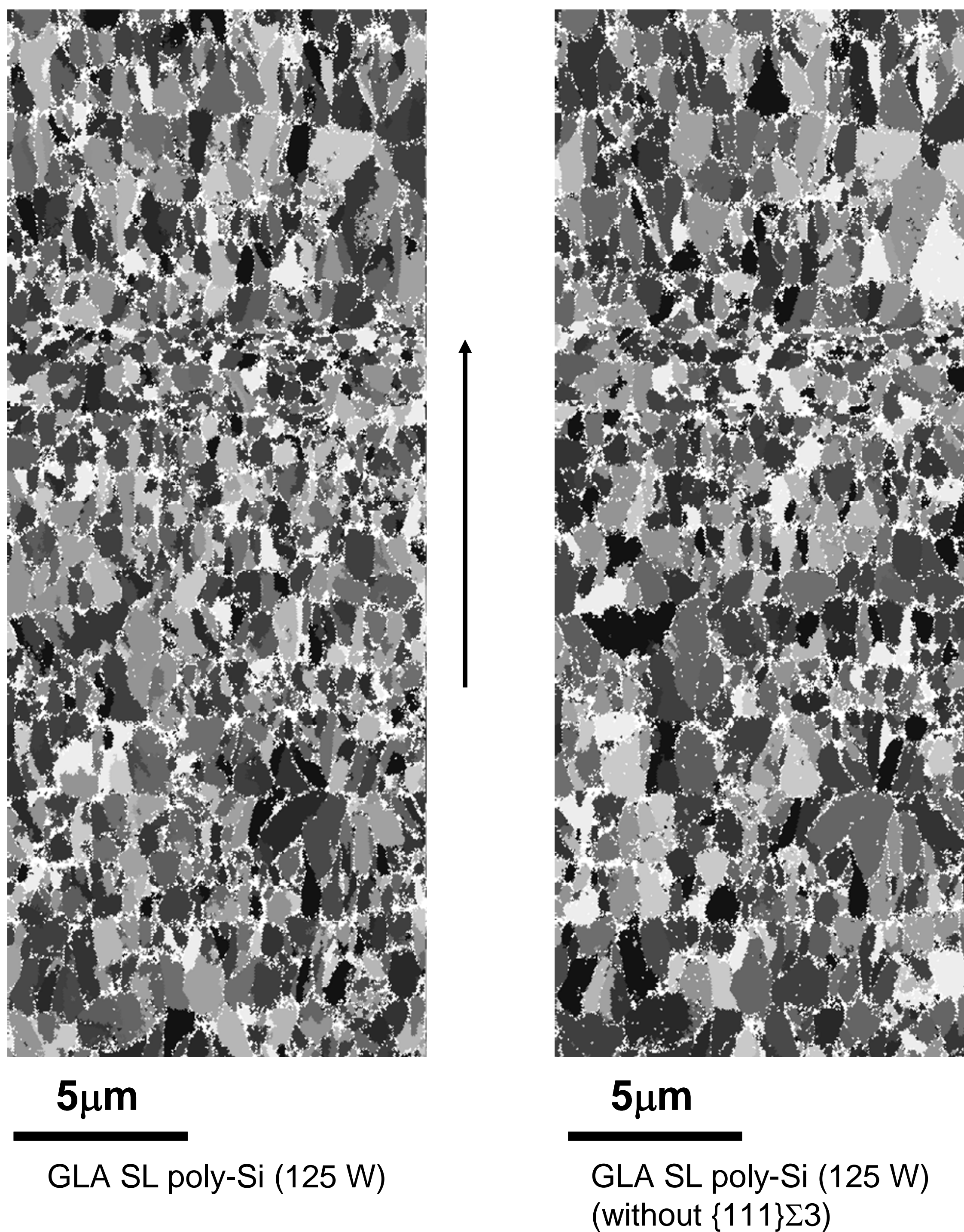


Figure 4.40: EBSD crystal grain image of GLA SL poly-Si (left) and the same image with the {111}Σ3 CSL boundaries were excluded (right). The arrows indicate laser scanning direction.

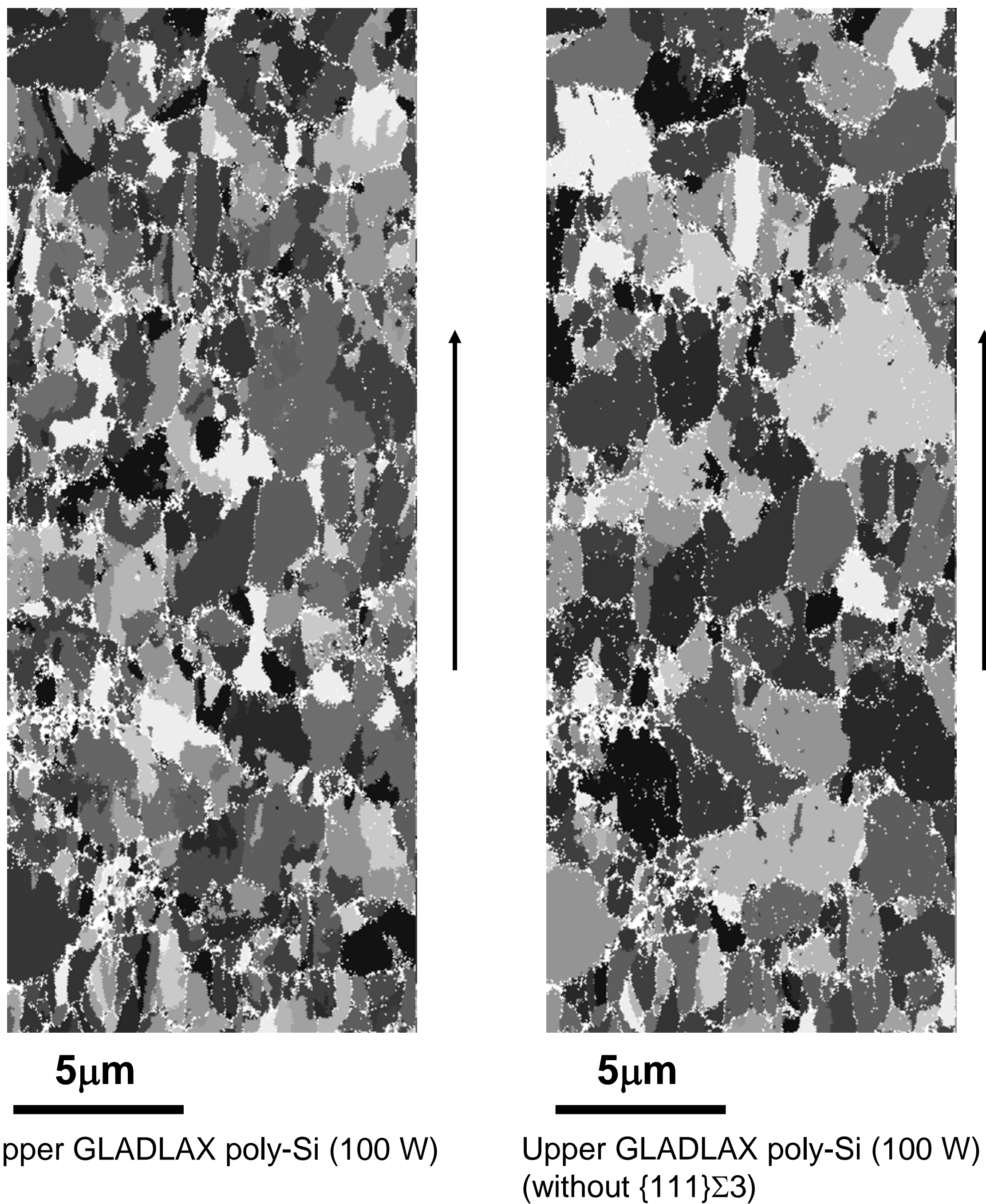


Figure 4.41: EBSD crystal grain image of upper GLADLAX poly-Si (left) and the same image with the {111}Σ3 CSL boundaries were excluded (right). The arrows indicate laser scanning direction.

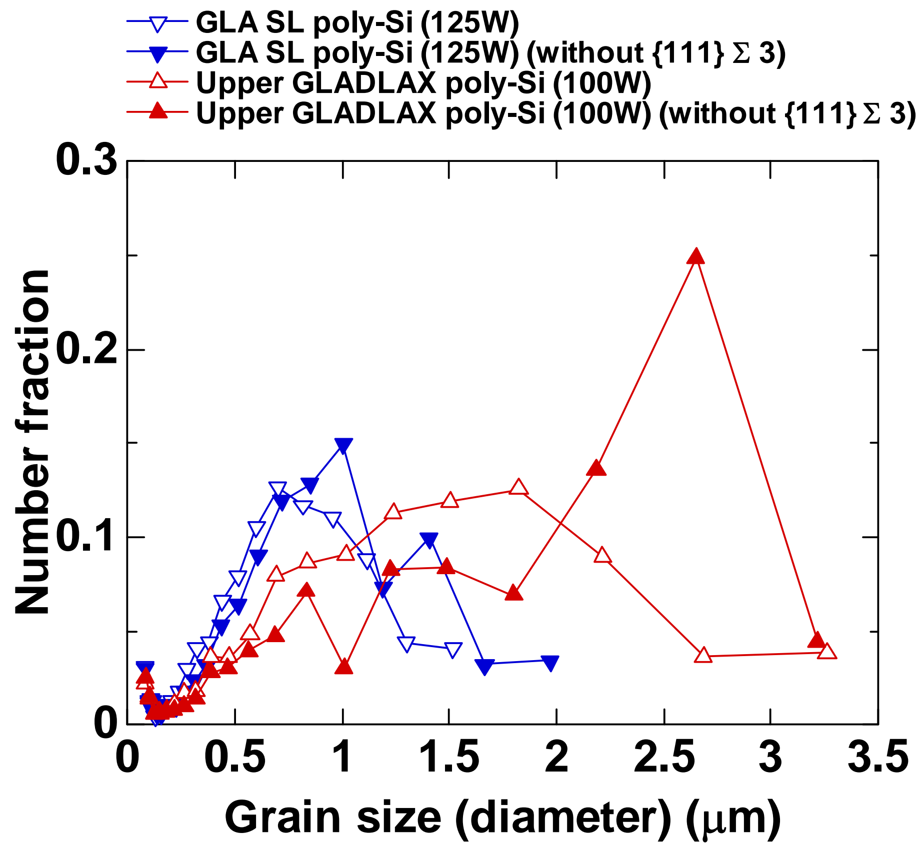


Figure 4.42: Distribution of grain size by EBSD analysis of the GLA poly-Si films Calculated with and without the {111} Σ3 CSL boundaries considered.

Fig. 4.42 shows the distribution of grain size by EBSD analysis of the GLA poly-Si films calculated with and without the {111} S3 CSL boundaries considered. The two distributions of GLA SL poly-Si before and after the {111} S3 CSL boundary is excluded differs with each other slightly, with the later shifting toward the larger crystal grains diameter. On the contrary, the overall increase of the crystal grain size of the upper GLADLAX poly-Si after the {111} S3 CLS boundary is excluded is remarkable. Also, the distribution shows the decrease of the number fraction of the smaller crystal grains, suggesting that the region containing the smaller crystal grains in the upper GLADLAX poly-Si possesses higher electrical conductivity than that in the GLA SL poly-Si has.

Summary

The EBSD analysis of GLA SL poly-Si and upper GLADLAX poly-Si was performed. From the crystal orientation mapping images, it was found that crystal grains orient apparently randomly. The investigation on the coincidence site lattice (CSL) boundary revealed that the upper GLADLAX poly-Si contains larger number fraction of Σ3 CSL boundary than the GLA SL poly-Si does. By considering this result, the crystal grain size of the GLA poly-Si was calculated by excluding the {111} S3 CSL boundary, which is electrically inactive, and it was confirmed that the distribution of the grain size of the upper GLADLAX poly-Si was greatly sifted to the larger value. Although further analysis of other GLA poly-Si films crystallized with different crystallization laser output power is needed, it is strongly suggested that the superiority of the TFT performance for the upper GLADLAX poly-Si is due not only to the enhanced crystal growth but also to large presence of the coherent twin such as {111} Σ3 CSL boundary compared to the GLA SL poly-Si.

4.8 GLADLAX for System on Panel Application

As one demonstration of device fabrication using both the upper and lower GLADLAX poly-Si thin films, System on Panel (SOP) application of GLADLAX poly-Si is proposed [26]. Fig.4.43 shows the schematic of the GLADLAX and how to apply it to SOP. First, double-layered poly-Si thin films were prepared by GLADLAX, with the upper poly-Si having excellent crystallinity while the lower one becoming micro-crystallized. Next, the upper poly-Si film is partially etched, so that the high-quality upper poly-Si film is utilized for the TFTs constituting the peripheral circuits of SOP, while the lower one with small-grains is used for the pixel driving TFTs of a display. The reason to use the less quality Si film for a display is that it could achieve better uniformity of the characteristics of the TFTs, which needs to be more severely required in the fabrication of organic light emitting diode (OLED) displays [27]. It is noted that this method in principle requires only an etching system and a green laser annealing system, which are both available in manufacturing use.

To demonstrate the above concept, both the upper and lower GLADLAX poly-Si thin films were applied to LTPS TFT fabrication simultaneously. This was done after the upper GLADLAX poly-Si, which was crystallized with the laser output power of 100 W, was partially etched. The fabrication process flow was described before. Figs. 4.44 show the schematics and the microscope image of actually fabricated TFTs using GLADLAX poly-Si films. Despite that there is step with 100 nm height at the edge of the partially etched upper poly-Si, the photolithography and other process were successfully carried out.

Figs. 4.45 show the typical transfer characteristics of the fabricated upper poly-Si TFT and lower μc-Si TFT. The upper poly-Si TFT showed the field effect mobility around 300 cm^2 /Vs, where as that of the lower mc-Si TFT calculated from the

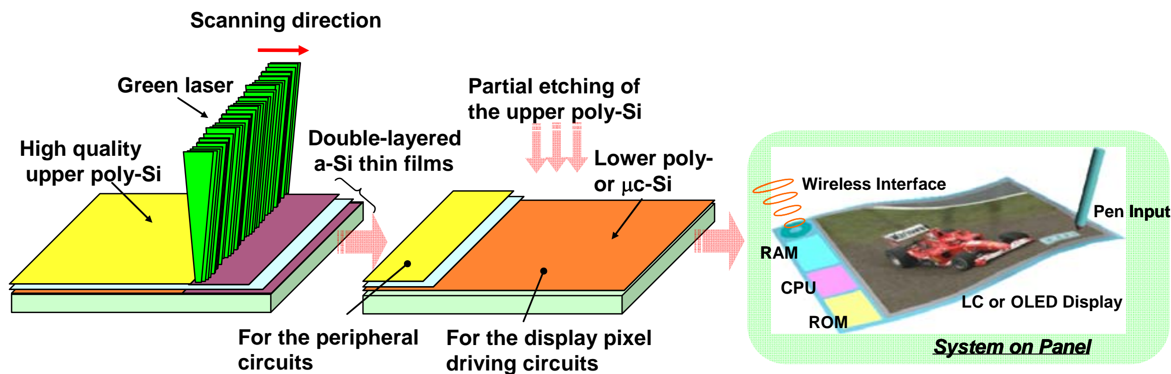


Figure 4.43: Schematic of GLADLAX and how to apply it for making of the SOP backplane.

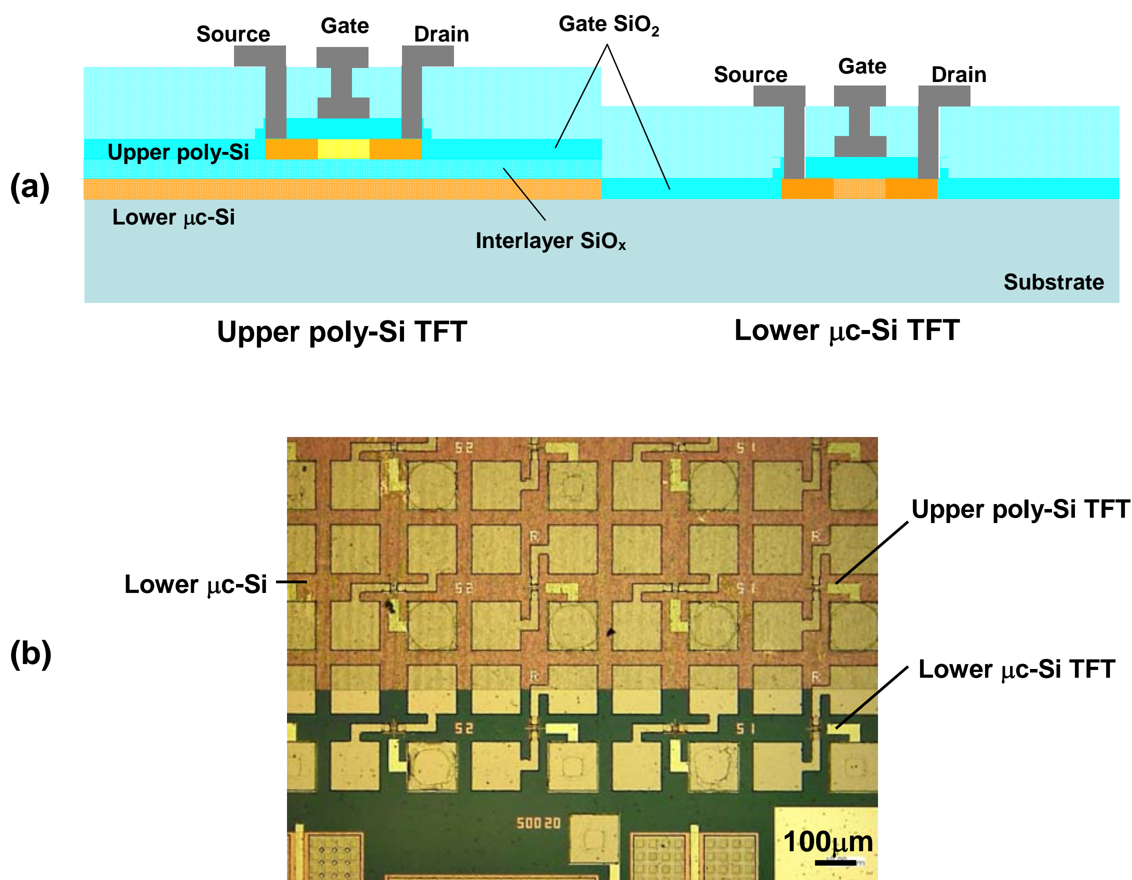


Figure 4.44: (a) Schematic of cross-section of GLADLAX poly-Si applied to TFT fabrication, (b) microscope image of the fabricated TFTs using GLADLAX poly-Si.

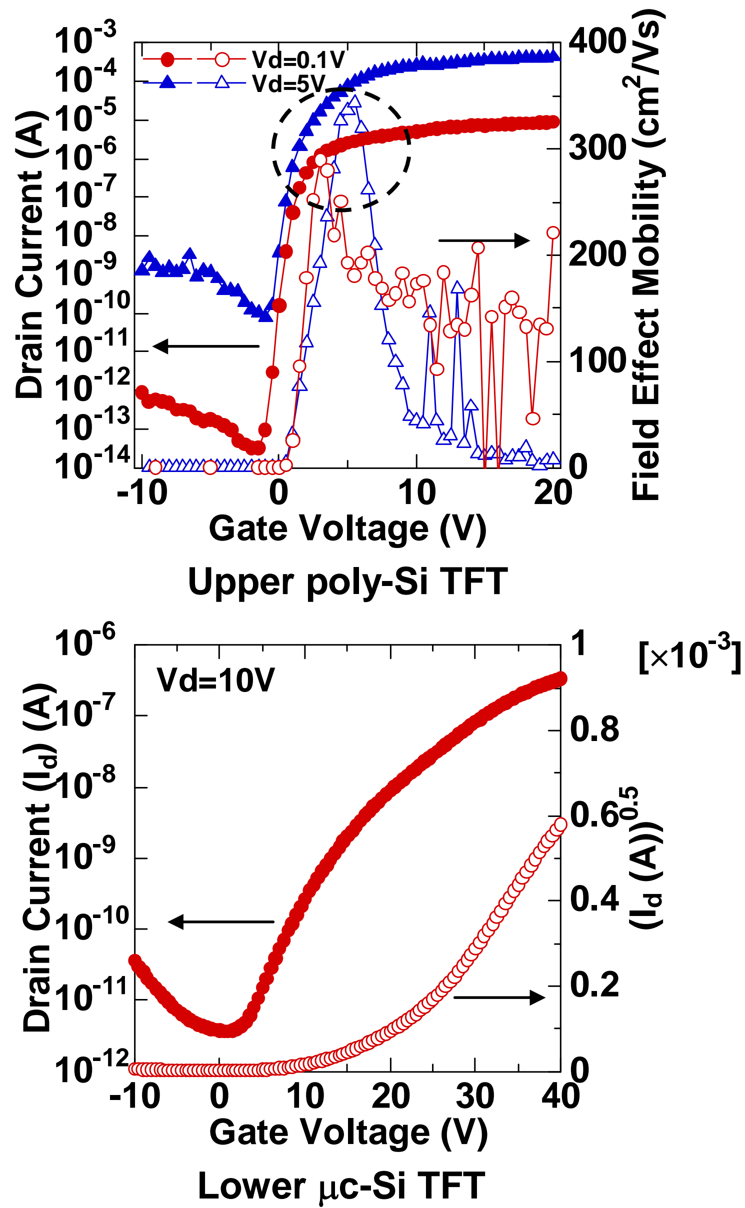


Figure 4.45: Transfer characteristics of the upper poly-Si TFT and lower μc-Si TFT.

transfer curve was 0.06 cm^2 /Vs. The performance of the lower μc-Si TFT was inferior to the a-Si TFT, the field effect mobility of which is typically 0.1 ~ 1 cm^2 /Vs. Taking account of that the fabrication process is totally different between poly-Si TFT and a-Si TFT; the former is top-gated self-aligned process and the later is bottom-gated process, the low mobility can be attributed to that the crystallinity of the lower Si is still not good enough to be processed into TFTs having sufficient performance to drive pixels, with the same fabrication condition as that of the TFTs using the upper poly-Si film. Although primitive, these results in principal demonstrate the applicability for fabrication of a SOP backplane.

4.9 Summary

Crystallization of double-layered a-Si thin films using solid state pulsed green laser annealing system was demonstrated for the first time. In the case of the double-layered structure of a-Si / SiO_x / a-Si = 50 / 50 / 50 (nm), it was found that the crystallization laser energy of the double-layered a-Si films was 30 % less than that of conventional single layer a-Si films with the a-Si thickness of 50 nm. That both the upper and lower a-Si films were successfully crystallized without damaging the interlayer SiO_x was confirmed by cross-sectional TEM observations. Furthermore, in the condition of the crystallization of the lower a-Si film, a drastic enhancement of crystal grows was observed. It can be considered that crystallizing lower a-Si was playing a role of thermal storage, which causes the extension of the melting time of the upper a-Si and reduces the thermal gradient around the interface of the molten Si and interlayer SiO_x.

The upper poly-Si of GLA double-layered poly-Si (upper GLADLAX poly-Si) was applied to the fabrication of LTPS TFTs. They were found to possess superior performance over the TFTs using GLA single layer poly-Si. The silicon on insulator like

performance was observed in the upper GLADLAX poly-Si TFTs. However, the transistor characteristics of the TFTs were not correlated with the size of crystal grains of the GLA poly-Si films.

To investigate that more closely, μ-PCD analysis and EBSD analysis of the GLA poly-Si films were performed. The μ-PCD results revealed that the crystallinity of the upper GLADLAX poly-Si is better than that of GLA SL poly-Si, which correlated with the TFT characteristics. The EBSD analysis of the microstructure of the GLA poly-Si clarified that the upper GLADLAX poly-Si contains larger number fraction of coincidence site lattice (CSL) boundaries, especially $\Sigma 3$ CSL boundary. The exclusion of {111} $\Sigma 3$ CSL boundary, which is electrically inactive, in the calculation of crystal grain size showed that the upper GLADLAX poly-Si have effectively large crystal grains comparable to the channel size of TFTs, thus confirming the superiority of the upper GLADLAX poly-Si. Considering these results, the GLADALX method can be said to be promising for the 3D thin film application.

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Chapter 5
Conclusions

5.1 Conclusions

This study developed a new work on the laser annealing crystallization of silicon thin films by introducing one-dimensional, and three-dimensional substrates, that is to say, non two-dimensional substrates which have not hitherto been employed. It aimed not only for the enhancement of the poly-Si crystallinity by making use of crystallization mechanism originating from each silicon substrate structure, but also for the creation of a efficient fabrication method of high-performance device by applying the substrate structure itself.

In Chapter 2, a basic fabrication process of LTPS TFTs was developed. Excimer laser anneaing crystallized poly-Si was used as a standard LTPS substrate. Top-gated self-aligned n-ch, and p-ch TFTs with the channel length and width of 5 μm were fabricated under the process temperature of 550 °C. Post metallization annealing condition of 400, 450, 475 (only for n-ch TFTs) °C, and the contact characteristics and TFT characteristics were evaluated. As a result, at the PMA condition of 450 °C, TFTs with highest performance in the contact and transistor characteristics was fabricated, which showed the field effect mobility of around 150 cm^2/Vs for n-ch TFTs and 50 cm^2/Vs for p-ch TFTs taken in the liner region. From the literature, it can be said that the field effect mobility of the fabricated TFTs was in top-level characteristics compared to the poly-Si TFTs using the ELA poly-Si with the same size of crystal

grains.

In Chapter 3, development of poly-Si TFTs on a quartz fiber was demonstrated. The fiber was embedded into the trench formed in a quartz substrate, and handled as a whole through the TFT fabrication. The excimer laser crystallization of a-Si deposited on a quartz fiber was carried out, and a poly-Si layer with a crystal grain diameter of 300 nm was obtained. The top-gated self-aligned TFTs fabricated on the fiber using the poly-Si film showed a mobility of 10 cm^2 /Vs, The lower mobility is considered to be due to the poor quality of the interface of poly-Si / gate SiO_2 deposited on the fiber. Although further development is still required, the demonstrated TFTs on a fiber, called fiber TFTs, are promising for the fabrication of silicon thin-film electronic devices on one-dimensional substrates.

In Chapter 4, crystallization of double-layered a-Si thin films using solid state pulsed green laser annealing system was demonstrated. In the case of the double-layered structure of a-Si / SiO_x / a-Si = 50 / 50 / 50 (nm), it was found that the crystallization laser energy of the double-layered a-Si films was 30 % less than that of conventional single layer a-Si films with the a-Si thickness of 50 nm. That both the upper and lower a-Si films were successfully crystallized without damaging the interlayer SiO_x was confirmed by cross-sectional TEM observations. Furthermore, in the condition of the crystallization of the lower a-Si film, a drastic enhancement of crystal growth over 2 μm was observed. It can be considered that crystallizing lower a-Si was playing a role of thermal storage, which causes the extension of the melting time of the upper a-Si and reduces the thermal gradient around the interface of the molten Si and interlayer SiO_x. TFTs using the large grained double-layered poly-Si were confirmed to possess superior electrical performance with the field effect mobility of up to 550 cm^2 / Vs.

To investigate that more closely, μ-PCD analysis and EBSD analysis of the

GLA poly-Si films were performed. The μ-PCD results revealed that the crystallinity of the upper GLADLAX poly-Si is better than that of GLA SL poly-Si, which correlated with the TFT characteristics. The EBSD analysis of the microstructure of the GLA poly-Si clarified that the upper GLADLAX poly-Si contains larger number fraction of coincidence site lattice (CSL) boundaries, especially Σ3 CSL boundary. The exclusion of {111} Σ3 CSL boundary, which is electrically inactive, in the calculation of crystal grain size showed that the upper GLADLAX poly-Si have effectively large crystal grains comparable to the channel size of TFTs, thus confirming the superiority of the upper GLADLAX poly-Si. Considering these results, the GLADALX method can be said to be promising for the 3D thin film application.

5.2 For the future work

In this thesis, new scientific knowledge was obtained from the device fabrication and evaluations employing the new processing technology. However, there still remain a lot of issues from scientific and engineering view as follows.

1. **CW laser crystallization of a-Si thin film on flexible glass or plastic fiber substrate**

To obtain poly-Si thin film with more improved crystallinity on fibers, use of continuous wave (CW) laser annealing crystallization of a-Si on such restricted regions is proporsed. Since many studies have been reported on high-speed scanning of CW laser beam on a-Si films to obtain single-crystalline poly-Si, the use of one-dimensional substrate for CW crystallization is promising from the viewpoint of large through-put fabrication of poly-Si with high crystallinity. Also, it is interesting to investigate the crystallization behavior difference compared to the case of using conventional flat substrate.

2. Investigation of the relationship between the double-layered a-Si structure and the GLADLAX poly-Si crystallinity, real-time observation of solidification of a-Si and simulation of crystallization process

By using different structure of double-layered a-Si (varying in the thickness of a-Si films and/or the interlayer SiO_x), the results of crystal grain evolution with respect to the laser output power will differ accordingly. That is also true with different laser irradiation configuration. From the consideration above, to get more enlarged crystal grains in the upper GLADLAX poly-Si, it would be appropriate to use the laser beam having more moderate energy density profile, ideally top flat, and employ longer irradiation pitch. By using different laser irradiation configuration and double-layered a-Si substrate with different structure, there would exist some condition which results in the lower poly-Si with more improved crystallinity. To get more information of the phase state of Si films during crystallization, the real-time observation of the crystallization is needed and confirmed by numerical simulation of heat transfer between each film.

VITA

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List of Publications

I. Academic journal

1. Yuta Sugawara, Yukiharu Uraoka, Hiroshi Yano, Tomoaki Hatayama, Takashi Fuyuki, Toshihiro Nakamura, Sadayuki Toda, Hisashi Koaizawa, Akio Mimura and Kenkichi Suzuki
   "Polycrystalline silicon thin-film transistors on quartz fiber"
   Applied Physics Letters, **91**, 203518 (2007).

2. Yuta Sugawara, Yukiharu Uraoka, Hiroshi Yano, Tomoaki Hatayama, Takashi Fuyuki and Akio Mimura
   "Crystallization of Double-Layered Silicon Thin Films by Solid Green Laser Annealing"
   Japanese Journal of Applied Physics, **46**, L164 (2007)
.

3. Yuta Sugawara, Yukiharu Uraoka, Hiroshi Yano, Tomoaki Hatayama, Takashi Fuyuki and Akio Mimura
   "Crystallization of Double-Layered Silicon Thin Films by Solid Green Laser Annealing for High-Performance Thin Film Transistors"
   IEEE Electron Device Letters, **28**, 395 (2007)

4. Yuta Sugawara, Yukiharu Uraoka, Hiroshi Yano, Tomoaki Hatayama, Takashi Fuyuki and Akio Mimura
   "Crystallinity Evaluation by Microwave Photoconductivity Decay in Double-Layered Polycrystalline Silicon Thin Films Crystallized by Solid Green Laser Annealing"
   Japanese Journal of Applied Physics, **46**, 7607 (2007).

II. Conference

1. Yuta Sugawara, Yukiharu Uraoka, Hiroshi Yano, Tomoaki Hatayama and Takashi Fuyuki
   "Reliability of Low Temperature poly-Si Thin Film Transistors Comparing with High Temperature poly-Si TFT and SOI TFT"
   12th International Workshops on Active-Matrix Liquid Crystal Displays 2006, 269 (2005). (Kanazawa, Japan)

2. Yuta Sugawara, Yukiharu Uraoka, Hiroshi Yano, Tomoaki Hatayama, Takashi Fuyuki and Akio Mimura
   "Crystallization of Double-Layered Silicon Thin Films by Solid Green Laser Annealing"
   13th International Workshops on Active-Matrix Flat Panel Displays and Devices 2006, 317 (2006). (Tokyo, Japan)
   (Best Paper Award)

3. Yuta Sugawara, Yukiharu Uraoka, Hiroshi Yano, Tomoaki Hatayama, Takashi Fuyuki and Akio Mimura
   "Crystallization of Double-Layered Silicon Thin Films by Solid Green Laser Annealing and Its Application to Low Temperature poly-Si Thin Film Transistors"
   Thin Film Transistors 8, 210th Meeting of The Electrochemical Society, 1569 (2006). (Cancun, Mexico)

4. Yuta Sugawara, Yukiharu Uraoka, Hiroshi Yano, Tomoaki Hatayama, Takashi Fuyuki and Akio Mimura
   "Crystallization of Double-Layered Silicon Thin Films by Solid Green Laser Annealing and Its Application to LTPS-TFTs"
   3rd Thin Film Materials and Device Meeting (2006). (Nara, Japan)
   (Lamp Session)

5. Yuta Sugawara, Yukiharu Uraoka, Hiroshi Yano, Tomoaki Hatayama, Takashi Fuyuki and Akio Mimura
   "Crystallization of Double-Layered Silicon Thin Films by Solid Green Laser Annealing and Its Application to LTPS-TFTs"
   6th GIST-NAIST joint international symposium (2006). (Nara, Japan)
   (Best Poster Award)

6. Yuta Sugawara, Yukiharu Uraoka, Hiroshi Yano, Tomoaki Hatayama, Takashi Fuyuki and Akio Mimura
"μ-PCD Measurement of Double-Layered poly-Si Thin Films Crystallized by Solid Green Laser Annealing"
2007 International Thin Film Transistors Conference, 208 (2007). (Roma, Italy)

7. Yuta Sugawara, Yukiharu Uraoka, Hiroshi Yano, Tomoaki Hatayama, Takashi Fuyuki and Akio Mimura
"Crystallization of Double-Layered Silicon Thin Films by Solid Green Laser Annealing for High Performance Thin Film Transistors"
14th International Workshops on Active-Matrix Flat Panel Displays and Devices 2007, 25 (2007). (Hyogo, Japan)
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"Pulsed Green Laser Annealing Crystallization of Double-Layered Silicon Thin Films"
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III. Related Paper

1. A. Mimura, Y. Sugawara*, M. Hiroshima, T. Ikehara, R. Maeda, K. Suzuki, K. Yase, I. Shuu**, A. Nakajima**, S. Toda**, H. Koaizawa** (AIST, Japan, *NAIST, Japan, **Furukawa Elec., Japan)
"Fabrication of Poly-Si TFTs on Fine Quartz Fibers for Display Applications"
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(Outstanding Poster Paper Award)

2. M. Ochi, Y. Sugawara, A. Miura, Y. Uraoka, T. Fuyuki and I. Yamashita
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   2008 International Thin Film Transistors Conference, 169 (2008). (Seoul, Korea)
   (Outstanding Poster Paper Award)

3. Patent: **JPA2007-258234**