Development of Single Crystalline Silicon Foil Solar Cells toward High Efficiency

(高効率化を目指した単結晶シリコンホイル太陽電池の開発)

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To my parents

and

Fiancee

Phoebus III

In the middle of difficulty, lies opportunity.

Albert Einstein

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Abstract

The purpose of this thesis is to develop the single crystalline silicon (c-Si) foil solar cells with active layer thickness as thin as 15 μm grown epitaxially on porous silicon layer after hydrogen annealing using Sintered Porous Silicon (SPS) process. In order to obtain high efficiency c-Si foil solar cells, the following three points were to be considered, (1): High quality c-Si layer, (2): Uniform separation technique from the Mother silicon substrate. (3): High quality silicon surface passivation layer.

Author has paid special attention on two things equaling the goal of this thesis. Firstly, the high quality epitaxial silicon layer was produced by evaluation of minority carrier lifetime. Because the minority carrier lifetime is a barometer in the view point of a characterization of crystalline silicon solar cells. There are not so much reports about evaluation of c-Si quality as factor of porous-Si fabrication parameter and hydrogen annealing.

Secondly, the low temperature fabrication process of rear side was developed. Since the c-Si foil solar cell is deposited epitaxially on a silicon substrate wafer, from which the cell has to be transferred to a glass superstrate by high transparency glue before the rear side is processed. The limitation of this process is the maximum process temperature for fabrication of passivation layer and contacting the rear side to below 200 ℃ in the SPS process. We proposed NH_3 plasma-treatment for silicon surface modification and fabrication of rear side contact using LFC at low temperature. The structure of SPS cell with LFC developed in this study (so, call it LFC-SPS cell). In our proposed structure, highest process temperature is below 200 ℃ after separation. There are not so much papers about specific policy of achieving high efficiency in previous reports.

The following five chapters of this thesis consider in detail the development of c-Si foil solar cells for high efficiency.

In Chapter 2, we found out the required electrical properties, which are especially bulk carrier lifetime and surface recombination velocity in c-Si foil, and the structure of c-Si foil solar cell using device simulation. These bulk carrier lifetime and surface recombination velocity became the target for the development of LFC-SPS cell.

In Chapter 3, Layer Transfer using SPS process was demonstrated and optimized. The quality of epitaxial silicon layer dependence on anodization and hydrogen annealing conditions was discussed through the evaluation of carrier lifetime. On the quality of epitaxial growth silicon layer dependence on anodization and hydrogen annealing conditions, accompanying the anodization current of forming third porous-Si layer increase was a decrease in the crystal quality and minority carrier lifetime, accompanying the annealing temperature increase was an increase the quality of crystal and minority carrier lifetime.

In Chapter 4, NH_3 plasma-treatment for interface modification was performed at low temperature. For applied SiN_X layer passivation to 15 μm c-Si foils, NH_3 plasma-treatment condition was investigated. The p-type c-Si material was exposed to the NH_3 plasma before depositing the SiN_X layer in a PECVD system. The effective lifetimes of the samples with NH_3 plasma-treatment were superior to the samples without NH_3 plasma-treatment. Moreover, the SIMS measurement results indicated that the mechanism of NH_3 plasma-treatment affected hydrogenation and carbon cleaning. By NH_3 plasma-treatment, passivation layer/c-Si interface was modified and passivation effect increased even when the passivation layer was deposited at 200 ℃ Finally, we obtained effective recombination velocity of SiN_X pssivation as 20 cm/s.

In Chapter 5, 15 μm c-Si foil solar cell fabrication process was produced. The optimized LFC process condition for bulk type LFC cell was applied. After adjusted the lower pulse energy condition, 3.90 % efficiency was obtained for LFC-SPS cell and 5.54 % for SPS

cell. The LFC-SPS cell was expected to achieve 10 % efficiency after the improvement of rear contact.

Contents

Chapter 3. Optimization and characterization of c-Si foils fabricated by Sintered Porous Silicon process

Chapter 4. NH_3 plasma-treatment interface modification for SiN_X passivation at below 200 ℃

Chapter 5. Development of rear passivated type c-Si foil solar cells with Laser Fired Contact

Chapter 6. Conclusion

Chapter 1

Introduction

1.1 High efficiency and thin single crystalline silicon solar cells

In 1954, a crystalline silicon solar cell with diffused pn junction having a conversion efficiency of 6% was developed [1]. Since the solar cell technology has made a dramatic development with the silicon technology. In 1998, a high efficiency single crystalline silicon (c-Si) solar cell showed a conversion efficiency of 24.7 % on Floating-zone (Fz) c-Si substrate (Fig.1.1) [2]. It was named PERL (Passivated Emitter and Rear Locally diffused) cell. This world record has not been broken yet. The PERL cell indicated guidance and showed the key techniques for the achieving high efficiency. One is the using Fz c-Si material which has the long carrier lifetime. The long carrier lifetime lead to increase efficiency for solar cell which is minority carrier device. Another one is the excellent passivation of the front and rear side. The very small areas of the Ag･Pd･Ti/c-Si front contact and c-Si/Al rear contact which shows great big surface recombination are fabricated by photolithography technique. The decreasing extinction of carrier on the surface of front and rear side is leads to increase directly short circuit current density and open circuit voltage, furthermore efficiency increase. Influence of front and rear surface recombination increase with thinner wafer. Another one is effective light trapping structure. The PERL cell has the inverted pyramid structure on front surface for the increasing light absorption. The PERL cell obtains high short circuit current density of 42.9 mA/cm^2.

Recently, further reductions of the cost of silicon which required for solar cells, are likely to be achieved with a thin c-Si solar cell (<100μm). The same group that developed PERL cell proposed 47 μm-thick PERL cell of 21.5 % [3]. Fraunhofer ISE published 21.5 % thin c-Si solar cell with 40 μm and flexible wafers (Fig.1.2) [4]. This cell was produced with Laser Fired Contact (LFC) technique and conventional laboratory processing. In the LFC process, an aluminum layer for rear side contact is evaporated directly onto the passivation layer and fires through the passivation layer with a laser into the underlying silicon to form the local contacts. It is possible that rear side contact fabricate at room temperature. It also shows that rear side passivation is a key technique for achieving high efficiency. These cells are base on single crystalline silicon wafer with conventional laboratory processing for high efficiency.

1.2 Layer Transfer technique base on the porous silicon [5]

The production of solar cell achieved 2521 MW in the entire world (2006) [6]. Most of these solar cells are crystalline silicon solar cell. The shortage of silicon material is caused by exponential growth of solar cell production.

Recently, the Layer Transfer techniques gather much attention on the view points of thin thickness and high efficiency. Especially sintered porous silicon (porous-Si) layer is used for separation layer. In the transfer technique, a thin c-Si layer is transferred from a c-Si wafer ("Mother c-Si substrate") to a different substrate (e.g. glass) and the c-Si wafer can be reused several times. (in Fig. 1.3) Ott et.al. published evaluation of the microstructure during annealing of porous-Si multilayer. The low porosity porous-Si layer (<20 %) restructures in hydrogen annealing [7]. The surface of porous-Si changed to a closure surface (in Fig1.4). This surface is single crystalline. A c-Si layer can be epitaxially growth on annealed porous-Si. All transfer technique using porous-Si is based on this physical reaction.

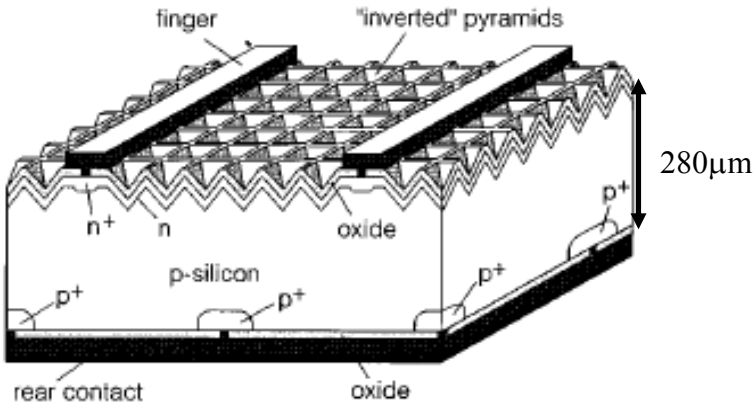
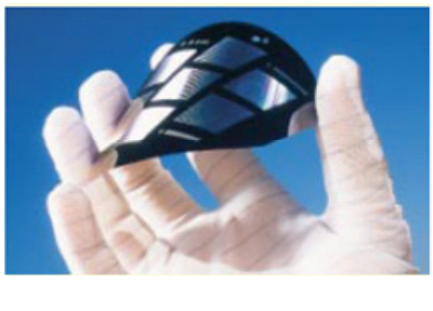
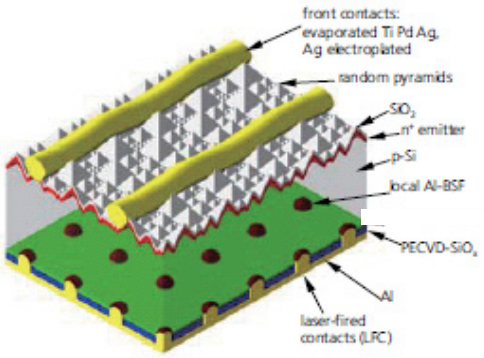


Fig 1.1 World record conversion efficiency solar cell of single crystalline silicon solar cell using Passivated Emitter Rear Locally diffused (PERL) structure.





Refer to Fraunhofer ISE, *Annual Report 2003*, (2003) p.36.

Figure 1.2 40 µm thin monocrystalline silicon solar cell based on wafer technology with LFC technique.

The successful transfer of a c-Si film using sintered porous silicon was first published by Yonehara et al. using Epitaxial Layer Transfer (ELTRAN) process developed at Canon Corporation [8]. However, they developed ELTRAN process for the fabrication of Silicon on Insulator (SOI) substrate.

The Quasai-Monocrystalline Silicon process (QMS) was introduced and developed by Rinke et al. [9] at the University of Stuttgart. Their device results include independently world record efficiency for thin film silicon solar cells on glass, demonstrating the outstanding electrical quality of the epitaxial silicon thin films grown on sintered porous silicon double layers. An efficiency of 12.7 % was achieved with small transferred cell (1 cm^2) [10]. This cell thickness was 14.5 μm.

Kim et al. published Free-standing Monocrystalline Silicon (FMS) solar cells by Layer Transfer process using porous-Si. The highest cell efficiency achieved for a 1 cm^2. FMS solar cell is 13.5%. The large-area FMS solar cells gave the best efficiency of 11.4% with an area of 11.1 cm^2. However this FMS cell has 20 μm active layer (p-type) and 50 μm QMS layer for high rear side reflector [11].

The Porous Silicon (PSI) process was introduced by Brendel et al. This cell achieved 12.2 % with 4 cm^2 and 15.5 μm-tick transferred cell [12]. They also publish 24 μm-thick big size PSI cell. The efficiency is 14.1 % with an area of 95.5 cm^2 [13].

The Sintered Porous Silicon (SPS) process was developed by Tayanaka et al. at Sony Co. (Fig. 1.5). Using photolithography and high efficiency fabrication process, they reported with a 12 μm-tick transferred cell achieving an efficiency of 12.5 % [14]. This result is currently the highest efficiency of all thin film solar cells using transfer technique. These repots showed the achievements of separation and cell fabrication. There are not so much papers about specific policy of achieving high efficiency and also are not so much reports about evaluation of c-Si quality as factor of porous-Si fabrication parameter and hydrogen annealing. All previous studies are cell thickness of over 20 μm, and Layer Transfer technique

and high efficiency in detail were not discussed.

1.3 Sintered Porous Silicon (SPS) process

In this thesis, Development and evaluation of c-Si foil solar cell using SPS process for high efficiency was been studied. In many cases, thin film silicon solar cells indicate the meaning of amorphous silicon or microcrystalline silicon solar cell. Therefore, the c-Si thin film will be called the c-Si foil in this thesis. This SPS cell has 15 μm-thick. In the view point of reducing cost of solar cell, 15 μm-thick is most thinnest thickness using SPS process safely.

The SPS process was developing by Sony Co. [14]. Similarly to ELTRAN, annealing in hydrogen closes the surface of the porous-Si layer system prior to epitaxy, a porous multi-layer system with a low surface porosity and a high porosity at depth permits high-quality epitaxial growth and a subsequent detachment of epitaxial layer. SPS process can supply high quality c-Si foil compared with other transfer technique (PSI, QMS, FMS).

Figure 1.5 illustrated the schematic of solar cell fabrication process using SPS process. Anodizing of the c-Si substrate forms porous-Si layers (Fig.1.5 (1)). This porous-Si layers has firstly low porosity layer (<10 %), secondly middle porosity layer (<30 %) and thirdly high porosity layer (>50 %) from surface of the Mother c-Si substrate. In the next process, this porous-Si layers is treat hydrogen annealing in high temperature (>1000 ℃). The porous-Si layers restructure, the closure of porous-Si surface is caused and high porosity layer change to separation layer which is big cavity (Fig. 1.5 (2)). This restructured surface is single crystalline silicon. 15 μm-thick silicon layer is epitaxially grown on the annealed porous-Si (Fig. 1.5 (3)) and a solar cell is fabricated (Fig. 1.5 (4)). An inexpensive transparent glass superstrate is adhered on the surface of the solar cell (Fig. 1.5 (5)) and the cell on the glass superstrate is separated from the c-Si substrate and formed backside contact and then the solar cell is completed.

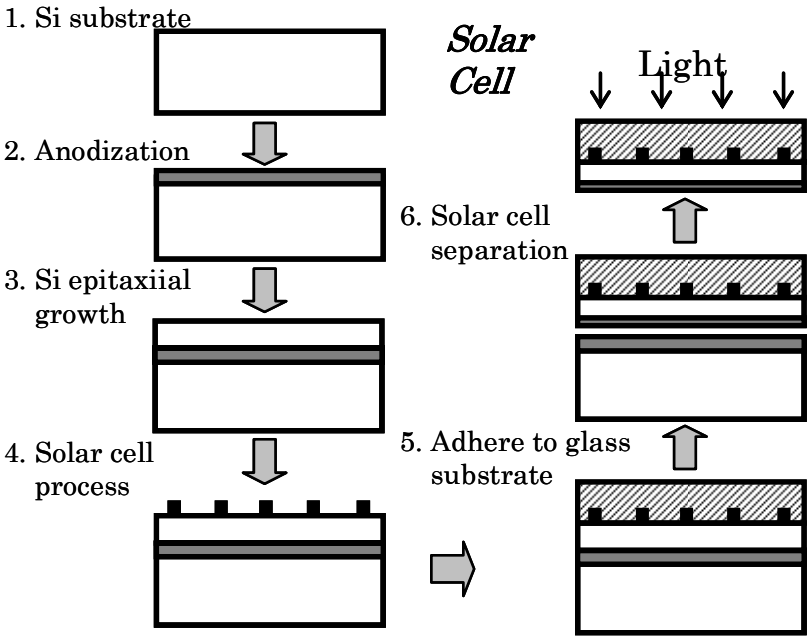


Figure 1.3 Transfer technique process using Porous-Si

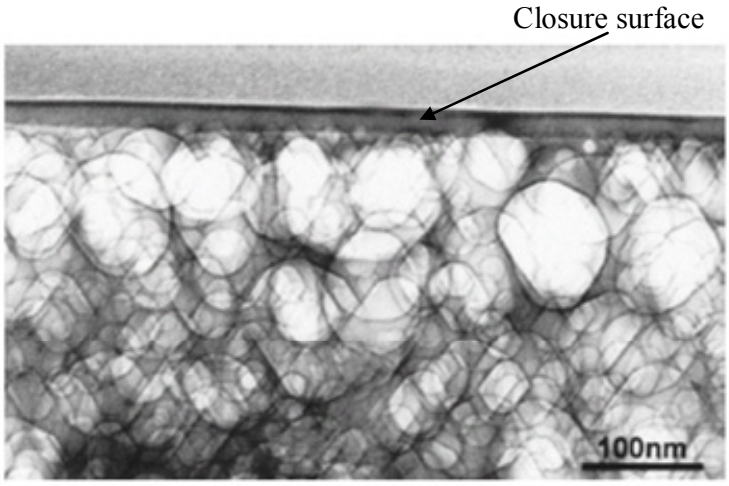


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Figure 1.4 TEM cross-section micrograph of porous-Si after hydrogen annealing

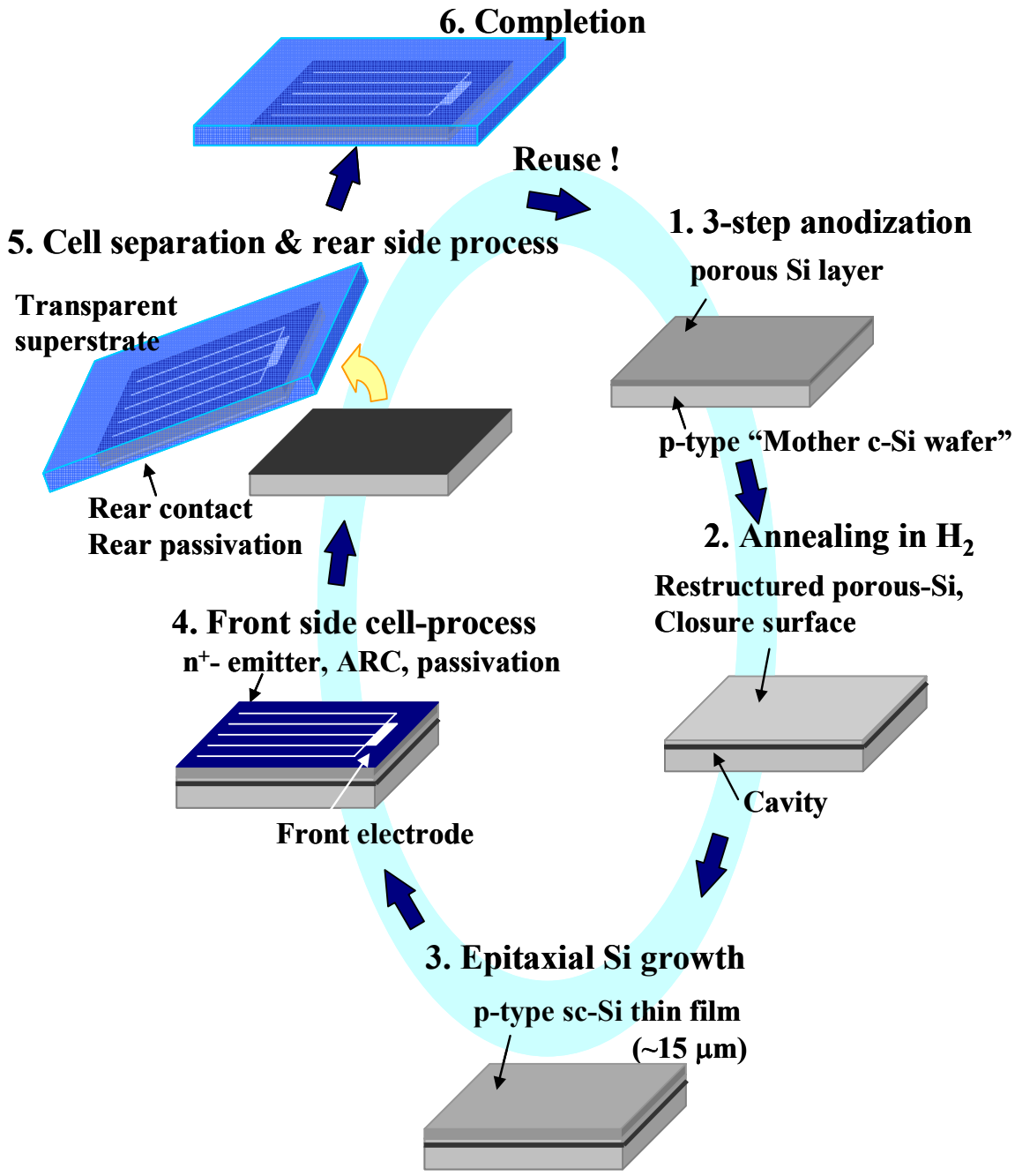

Figure 1.5 Schematic of the SPS process

1.3 Objective of this work

The target of this thesis is to develop the c-Si foil solar cells with active layer thickness as thin as 15μm grown epitaxially on porous-Si layer after hydrogen annealing using SPS process. In order to obtain high efficiency single crystalline foil silicon solar cells, the following three points were to be considered, (1): High quality c-Si layer, (2): Uniform separation technique from the Mother silicon substrate. (3): High quality silicon surface passivation layer.

Author has paid special attention on two things equaling the goal of this thesis. Firstly, the epitaxial silicon layer was produced high quality by evaluation of minority carrier lifetime. Because the minority carrier lifetime is a barometer in the view point of a characterization of crystalline silicon solar cells. There are not so much reports about evaluation of c-Si quality as factor of porous-Si fabrication parameter and hydrogen annealing.

Secondly, the low temperature fabrication process of rear side was developed. Because the c-Si foil solar cell is deposited epitaxially on a silicon substrate wafer, from which the cell has to be transferred to a glass superstrate by high transparency glue before the rear side is processed. The limitation of this process is the maximum process temperature for fabrication of passivation layer and contacting the rear side to below 200 ℃ in the SPS process. We proposed NH_3 plasma-treatment for silicon surface modification and fabrication of rear side contact using LFC at low temperature.

Figure 1.6 shows the structure of SPS cell with LFC developed in this study (so, call it LFC-SPS cell). In our proposed structure, highest process temperature is below 200 ℃ after separation. There are not so much papers about specific policy of achieving high efficiency in previous reports. However, I didn’t discus about effective light trapping technique for c-Si foil solar cell in this thesis because of becoming involved problem.

The following five chapters of this thesis consider in detail the development of c-Si foil solar cells for high efficiency.

In Chapter 2, the dependence of solar cell performance on electrical properties at silicon material was analyzed by two-dimensional numerical simulation. Not only the required electrical properties, which were especially minority carrier lifetime and surface recombination velocity in c-Si foil, but also the structure of c-Si foil solar cell using device simulation for achieving high efficiency were found out in this Chapter.

In Chapter 3, Layer Transfer using SPS process was demonstrated and optimized. The epitaxial silicon layer was produced high quality. The quality of epitaxial silicon layer dependence on anodization and hydrogen anneal conditions was discussed through the evaluation of carrier lifetime and crystallinity. The making of higher quality epitaxial silicon layer for getting required electrical properties calculated by device simulation in Chapter 2 is also discussed.

In Chapter 4, the optimization of interface modification using NH_3 plasma-treatment for SiN_X layer passivation on rear side of c-Si foil solar cell is studied. SPS process requires the rear side processing of solar cell at low temperature. We proposed that NH_3 plasma-treatment for interface modification is performed at low temperature. For applied SiN layer passivation to 15 μm c-Si foil solar cell, NH_3 plasma-treatment condition is investigated through the evaluation of carrier lifetime. Thus, the effective surface recombination velocity at SiN_X/c-Si interface is calculated.

In Chapter 5, a 15 μm c-Si foil solar cell fabrication process was developed and LFC-SPS cell is demonstrated and optimized. Appling LFC process to bulk type (300 μm) c-Si solar cell, LFC process was established. LFC-SPS cell is fabricated by optimized LFC condition. SPS cell and LFC-SPS cell were analyzed and discussed.

In the final Chapter, conclusions obtained through this study were summarized. Remaining issues for fabrication of high efficiency c-Si foil solar cells are mentioned.

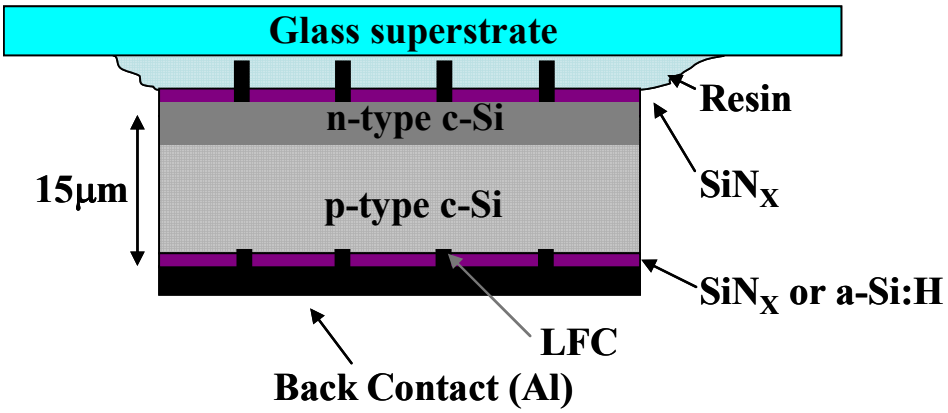

Figure 1.6 LFC-SPS cell (This thesis proposed solar cell structure).

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Chapter 2

Numerical analyses for c-Si foil solar cells using 2-dimensional device simulation

2.1 Introduction

Single crystalline silicon (c-Si) foil solar cells have many advantages such as reduction of c-Si material, a possibility of high conversion efficiency, lower light induced degradation. However, in the development of c-Si foil solar cell, we need to allow for the carriers diffusing to lateral direction in c-Si foil solar cell compared with the case of bulk type (300 μm-thick) c-Si solar cells. In addition to high carrier lifetime and very low rear surface recombination are needed for achieving high efficiency of c-Si solar cell. Additionally, the c-Si foil solar cells require the optimum designing of solar cell structure and evaluate the required electrical properties for high efficiency. Especially, I proposed the rear passivated type cell through this thesis, the design of rear side contact is very important. It needs to investigate for the achieving c-Si foil solar cell.

In this chapter, the required electrical properties, which are especially minority carrier lifetime and surface recombination velocity in c-Si foil, and the structure of c-Si foil solar cell can be calculated by the device simulation. The requirements of minority carrier lifetime and rear surface recombination velocity for high efficiency are also investigated. Therefore, actual device sizes and physical parameters in this calculation using device simulation were used. Moreover, Photoconductance decay (PCD) and Quasi-Steady-State

Photoconductance method (QSSPC) were used for the evaluation of minority carrier lifetime and surface recombination velocity. In this chapter, the measurement technique for minority carrier lifetime and surface recombination are also introduced and discussed.

2.2 Numerical analysis using 2-dementional simulation

In the numerical analysis of thin c-Si solar cells, one-dimensional approximation is insufficient, because thickness of the active layer is too small compared with the electrode interval. Therefore, the numerical analysis in two dimensions is necessary.

For the simulation of thin c-Si solar cells, we used the commercially available software of ATLAS (SILVACO Co.). This simulation is based on the solution of the set of semiconductor equations represents a math description of semiconductor device operation under non-equilibrium and steady-state conditions. ATLAS includes the physics model of recombination lifetime such as Radiative, Auger, SRH and surface recombination [1]. Bulk lifetime consists of the three main recombination mechanisms. These recombinations determine the recombination lifetimes:

1) Radiative recombination, characterized by τ_{rad},
2) Auger recombination characterized by τ_{Auger},
3) Shockley–Read–Hall (SRH) recombination, characterized by τ_{SRH}.

The bulk lifetime is determined by the three processes according to the relationship,

$$\tau_{bulk} = \frac{1}{\tau_{SRH}^{-1} + \tau_{rad}^{-1} + \tau_{Auger}^{-1}} \tag{2-1}$$

These recombination mechanize is very famous. For details, refer to Rein's textbook [2]. These three recombinations are physical phenomenon inside bulk silicon. For

improvement of bulk lifetime, the decrease of the defects formed by impurities or crystallographic imperfections such as dislocations is required. The relationship between carrier lifetime and characterization of crystal structure is discussed in the Chapter 3

The surfaces or interfaces of a silicon substrate represent a severe discontinuity in their crystalline structure. A large number of partially bonded silicon atoms gives rise to many dangling bonds, and therefore a large density of defect levels are found within the bandgap near the semiconductor. The surface recombination rate U_S is a rate per unit area. And U_S can be expressed as

$$U_S = S\Delta n \tag{2-2}$$

Where *S* is defined surface recombination velocity. And so the surface recombination velocity can be related to the fundamental properties of the surface defects. It is the surface recombination velocity, *S*, that is typically used for quantifying surface recombination processes. In the ATLAS simulator, the recombination process via the single-level states located at the intrinsic Felmi level is assumed in accordance with the SRH statistics. Front and rear surface recombination velocity was decided.

2.3 Device modeling of rear passivated type c-Si foil solar cells

Figure 2.1 shows a schematic view of a 15 μm-thick c-Si foil solar cell. Table II-I and II-II give fixed and variable parameters used for the simulation, respectively. The model is assumed as an n^+p junction simple device which consists of a 0.2 μm thin emitter layer with uniform doping concentration of 10^{19} cm^{-3}, a 14.8 μm active layer with the fixed doping concentration of 10^{16} cm^{-3}. This reason is accurate doping concentration for getting high

carrier lifetime because the carrier lifetimes decrease with higher doping concentration over 10^{16} cm^{-3} [3]. In this thesis, Base layer is p-type silicon and carrier lifetime indicates the carrier lifetime of electron as minority carrier in p-type silicon. Front surface recombination velocity and c-Si/Al contact interface recombination velocity are fixed with 4000 cm/s and 10^6 cm/s, respectively [3,4]. 15 μm-thick c-Si foil solar cell is characterized by three important parameters, i.e., the bulk carrier lifetime (τ_{bulk}), rear surface recombination velocity and the ratio of rear contact area. The value of τ_{bulk} was varied in the range from 0.0069 to 7.5 μs. This τ_{bulk} can be used to obtain the value of carrier diffusion length (L_{bulk}) as the range from 5 to 150 μm by [5]

$$L_{bulk} = \sqrt{D_n \tau_{bulk}} \tag{2-3}$$

The diffusion constant, D_n, is 0.003m^2/s. A rear side structure was local contact with SiN layer passivation. This layer had a refractive index of 2.0 and a thickness of 70 nm. The values of contact area ratio and c-Si/SiN interface recombination velocity were varied in the ranges from 1 to 100 % and 10 to 1000 cm/s, respectively. An emitter electrode covered 5 % of the surface and the other part of the surface was covered with an antireflective (AR) coating. This layer had a refractive index of 2.0 and a thickness of 70 nm. This structure doesn't have surface texturing. In this thesis, we don't discuss about light trapping structure.

Irradiation spectrum was AM 1.5 with the total power of 100 mW/cm^2 in the wavelength region from 200 to 1500 nm. The light was illuminated vertically onto the solar cell. The illuminated light was refracted and reflected on the basis of continuous boundary condition. Some of incident light were absorbed in the solar cell and the other permeated the solar cell. The unabsorbed light was reflected totally at the Back Surface Reflector (BSR), and reflected light was returned and, then, was absorbed in the solar cell.

In order to investigate the solar cell performance, the current-voltage characteristics

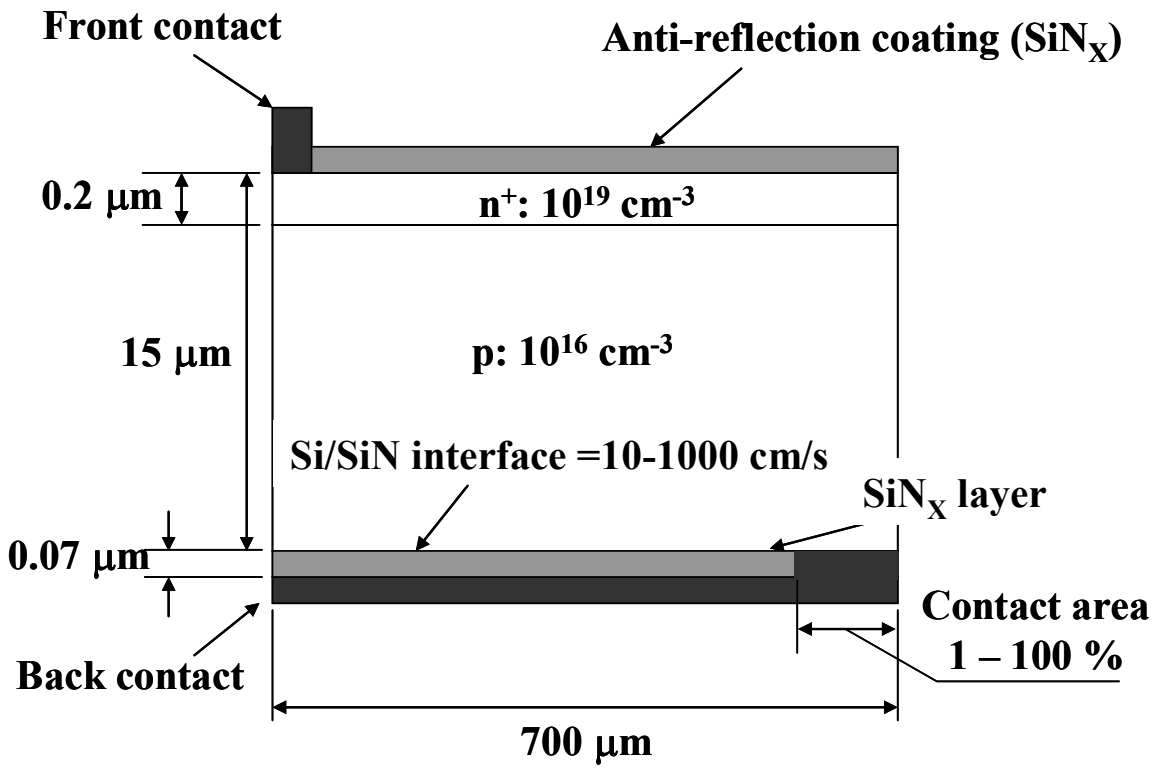

Figure 2.1 Structure of simulation model
(LFC-SPS cell)

Table II-I Fixed parameters in simulation model
(LFC-SPS cell = Rear passivated type)

Parameters	Values
n^+ layer thickness (μm)	0.2
Max doping in n^+ layer (cm^{-3})	10^{19}
p layer thickness (μm)	14.8
Doping concentration in p layer (cm^{-3})	10^{16}
c-Si/Al interface recombination velocity (cm/s)	10^6
Front surface recombination velocity (cm/s)	4000

were calculated. A typical current density-voltage and power-voltage curve of a solar cell under illumination is shown in Fig. 2.2. The short circuit current density (J_{sc}), the open circuit voltage (V_{oc}) and the maximum power point P_{max} (V_m, J_m) were indicated in the figure. The conversion efficiency η is the ratio of the incident power P_{in} and P_{max}, and given by,

$$\eta = \frac{P_{max}}{P_{in}} \times 100 = \frac{J_{sc} \cdot V_{oc} \cdot FF}{P_{in}} \times 100 . \quad (2\text{-}4)$$

where FF is the fill factor and defined as $FF = (J_m \cdot V_m)/(J_{sc} \cdot V_{oc})$.

2.4 Effect of electrical properties on solar cell performance

2.4.1 Efficiency of solar cells depending on bulk lifetime

Figure 2.3 shows the efficiency of SPS (non rear passivatied type) and LFC-SPS cells (rear passivated type; rear contact area ratio: 10 %, S_{rear}: 100 cm/s) dependence on the τ_{bulk}. The S_{rear} as 100 cm/s is equal to one of the high efficiency bulk c-Si solar cells. In the region of lower τ_{bulk}, of course, efficiency is very low. In the region of below 0.03 μs (L_{bulk}=9.4 μm), the efficiency of LFC-SPS cells was low on comparison of SPS cells. This reason is that carriers are not possible to move lateral direction of cell due to low τ_{bulk} in LFC-SPS cells. In the higher τ_{bulk} (0.3 μs), SPS cell have saturation of efficiency as 8%. SPS cells don't have rear passivation layer and the recombination in rear surface caused by high S_{rear} as 10^6 cm/s of c-Si/Al contact. In contrast, LFC-SPS cells increase efficiency with higher τ_{bulk} due to the good rear passivation layer (100 cm/s), τ_{bulk} leads to increase efficiency. However, LFC-SPS cells also have the saturation of efficiency in the region of over 4.8 μs. In this region of over 4.8 μs, J_{SC} increase slightly with higher τ_{bulk} while V_{OC} and F.F. slightly increase.

TableII-II Variable parameters in simulation model
(LFC-SPS cell = Rear passivated type)

Parameters	Values
Carrier lifetime (μs)	**0.0069 ~ 7.5**
c-Si/SiN surface recombination velocity (cm/s)	**10 ~ 1000**
Contact area on backside (%)	**1 ~ 100**

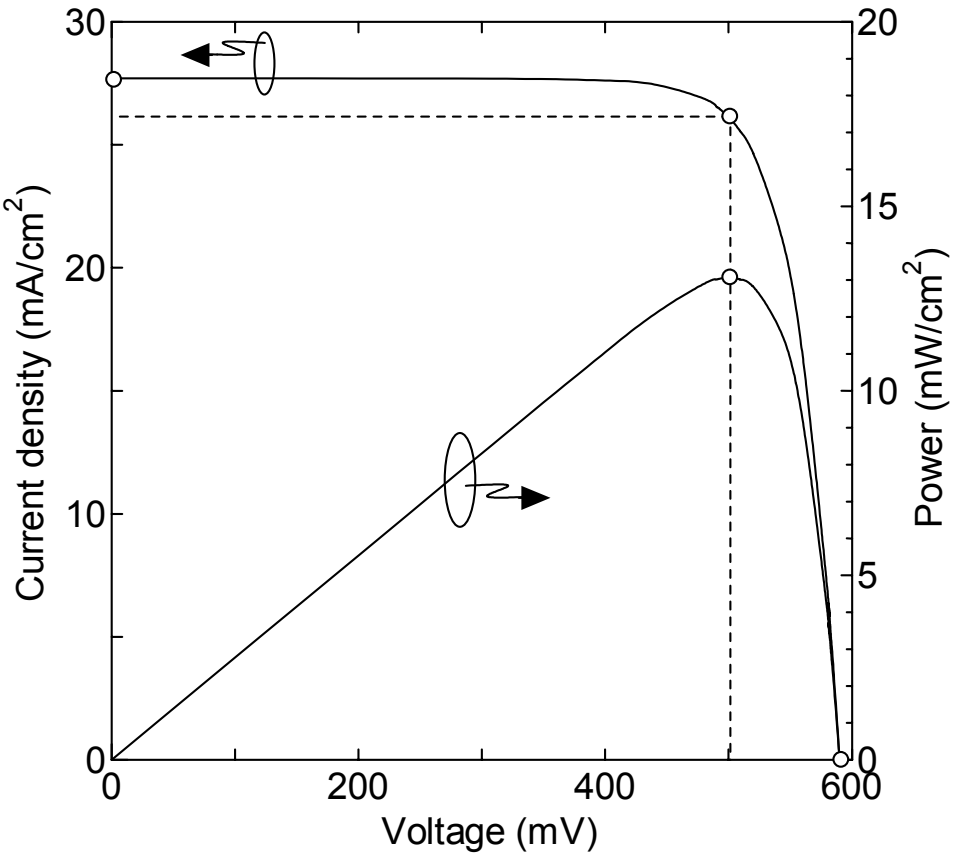

Figure 2.2 Current density-voltage and power-voltage curves of a solar cell under illumination (A.M 1.5, 100 mW/cm2)

2.4.2 Efficiency of solar calls depending on rear surface recombination

Figure 2.4 shows the efficiency of LFC-SPS cells depending on rear surface recombination (rear side contact ratio: 5 %). We calculated two bulk carrier lifetimes which are 0.075 μs (L_{bulk}=15μm) and 4.8 μs (L_{bulk}=120 μm). The value of 0.075 μs means that carrier diffusion length is equal to cell thickness. The value of 4.8 μs means that carrier diffusion length is enough longer than cell thickness and showed the saturation of efficiency in the section 2.4.1. High τ_{bulk} (4.8 μs) kept the constant efficiency with rear surface recombination increase. It is possible that the efficiency with High τ_{bulk} is affected by rear surface recombination in the region of S_{rear} from 10 to 1000 cm/s. The recombination in silicon surface was occurred by the high S_{rear} (from 10 to 1000 cm/s), the carrier generated in the silicon can enough diffuse around pn junction. However, the low τ_{bulk} (0.075 μs) decreased the efficiency with rear surface recombination increase, especially in the region of over 100 cm/s. This reason is that the carrier generated in the silicon can't enough arrive around pn junction. Additionally, the recombination in silicon surface was occurred by the high S_{rear} (from 10 to 1000 cm/s), and a lot of carriers disappear. This decreasing efficiency with higher S_{rear} is caused mainly by J_{SC} decreasing.

2.4.3 Efficiency of solar calls depending on the rear contact area

Figure 2.5 shows the efficiency and F.F. of LFC-SPS cells depending on rear contact area ratio (rear surface recombination velocity: 100 cm/s, τ_{bulk}: 4.8 μs). In the efficiency, the smaller rear contact area ratio achieved higher efficiency. This means that the decreasing area of c-Si/Al contacts which have the high S_{rear} effectively lead to decrease carrier recombination in rear surface. However, F.F had the peak (10%) of rear contact ratio. This reason is that the small rear contact area ratio leads to high series resistance. The value of 10% rear contact

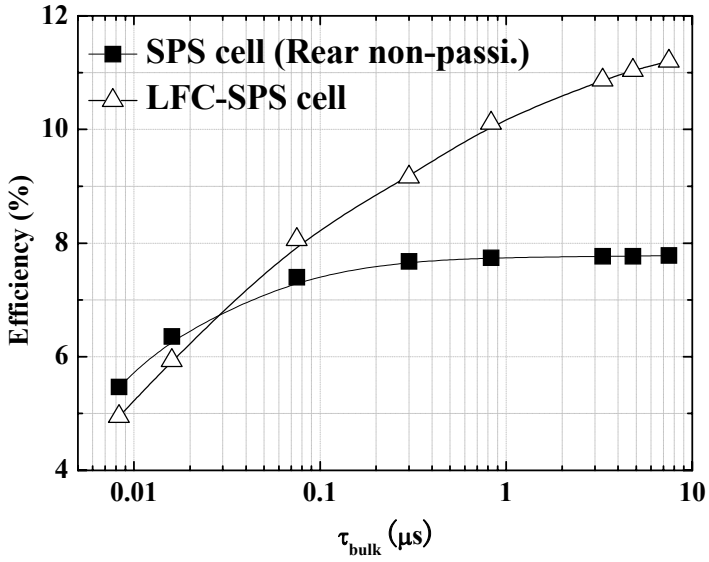

Figure 2.3 Efficiency of SPS and LFC-SPS cell obtained by the variation of minority carrier lifetime

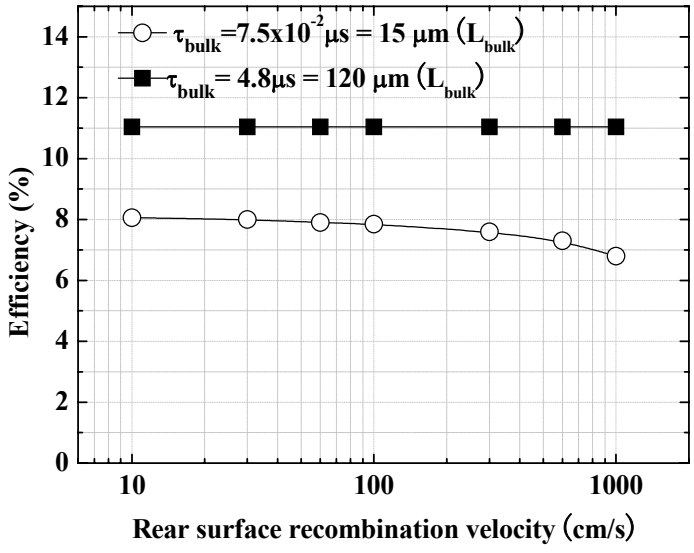

Figure 2.4 Efficiency of LFC-SPS cell obtained by the variation of rear surface recombination

ratio is a well balance of the series resistance factor and rear surface recombination factor. In this case (15 μm c-Si foil solar cell with LFC-SPS cell type), blow the rear 10 % contact area indicated high solar cell performance.

Finally, we got the result of calculation using 2D-dimensional simulation. For the improvement of efficiency, τ_{bulk} is over 4.8 μs, S_{rear} is below 100 cm/s and rear contact ratio is below 10 %.

2.5 Effective carrier lifetime and evaluation technique

2.5.1 Bulk carrier lifetime

Figure 2.6 shows lifetime curves for a 2 Ωcm p-type silicon wafer for SRH recombination (deep defect, τ_{n0} = 2.5 ms and τ_{p0}= 25 ms), radiative recombination and Auger recombination. This lifetime were calculated using Eq. (2-1) and the parameters obtained from Karsten Bothe [6]. It can be seen that recombination through deep defects results in a distinctly different excess carrier density dependence than the intrinsic recombination processes (radiative and Auger), and that SRH recombination normally dominates at low injection levels. In contrast, Auger recombination strongly dominates at very high injection levels. The bulk lifetime in Fig. 2.6 is showed with the excess carrier density dependence. The lifetime evaluation of silicon material for solar cell has very important. Because the carrier injection level is changed in the operation from J_{sc} condition to V_{oc} condition which is a current density-voltage curve of a solar cell under illumination (in Fig.2.2).

We used 300 μm-thick Fz (100) 2 Ωcm p-type silicon wafer for passivation effect and the calculation of effective surface recombination velocity in chapter 4. We assumed that this wafer was the same level bulk carrier lifetime as 2.5 ms compared to other researchers used wafer [8, 9].

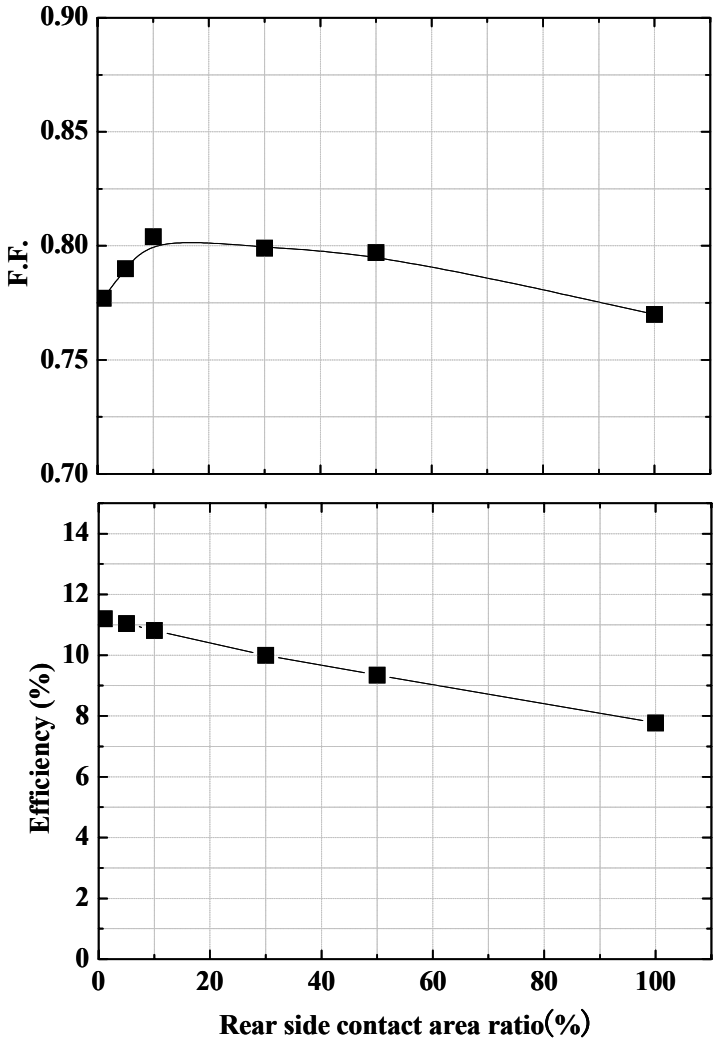

Figure 2.5 Efficiency and F.F. of LFC-SPS cell obtained by the variation of rear side contact ratio

2.5.2 Effective carrier lifetime

The effective lifetime (τ_{eff}) is the sum of three main recombination lifetimes and surface recombination. According to Eq. (2-1), the bulk carrier lifetime is the sum of the radiative, Auger and SRH recombination lifetimes. When measuring the recombination lifetime, the measured quantity strongly depends on the surface condition, in other word, depends on the effective surface recombination velocity, S_{eff}. By assuming no injection-level dependence of S_{eff}, the effective lifetime can be given by:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \alpha^2 D_n \tag{2-5}$$

where D_n is the electron diffusion constant and α is given by:

$$\tan\left(\frac{\alpha W}{2}\right) = \frac{S_{eff}}{\alpha D_n}. \tag{2-6}$$

where W is silicon thickness. The effective surface recombination velocity can be given by [7]

$$S_{eff} = \sqrt{D_n\left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_{bulk}}\right)}\tan\left[\frac{W}{2}\sqrt{\frac{1}{D_n}\left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_{bulk}}\right)}\right]. \tag{2-7}$$

and also, the effective carrier lifetime is expressed

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \left(\frac{W}{2S_{eff}} + \frac{1}{D_n}\left(\frac{W}{\pi}\right)^2\right)^{-1} \tag{2-8}$$

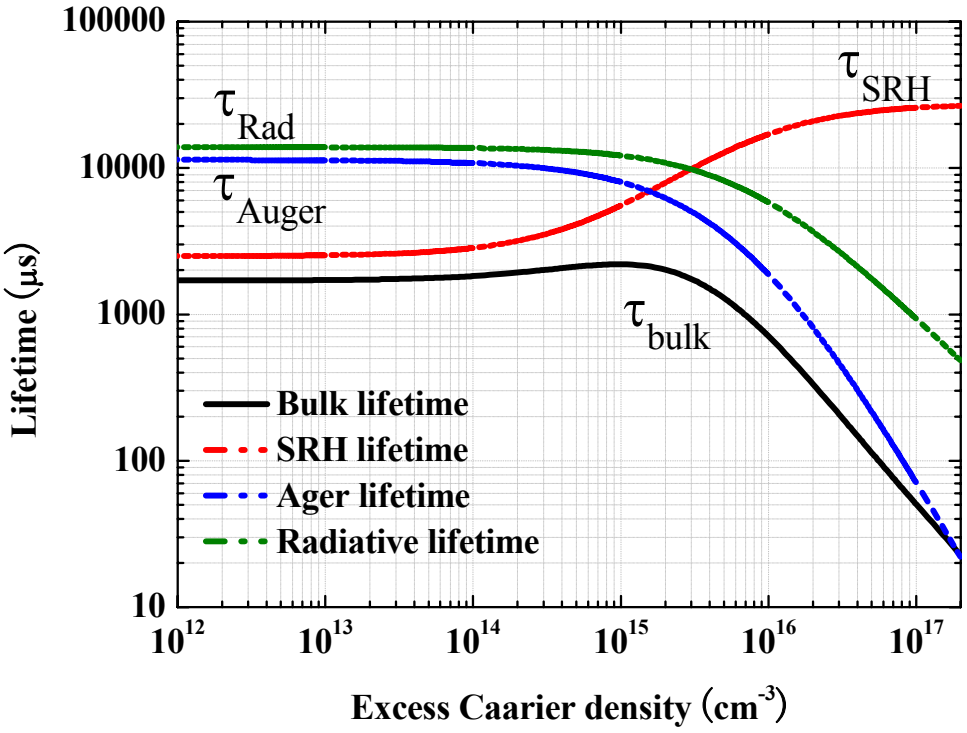

Figure 2.6 Lifetime curve of SRH recombination, radiative recombination and Auger recombination

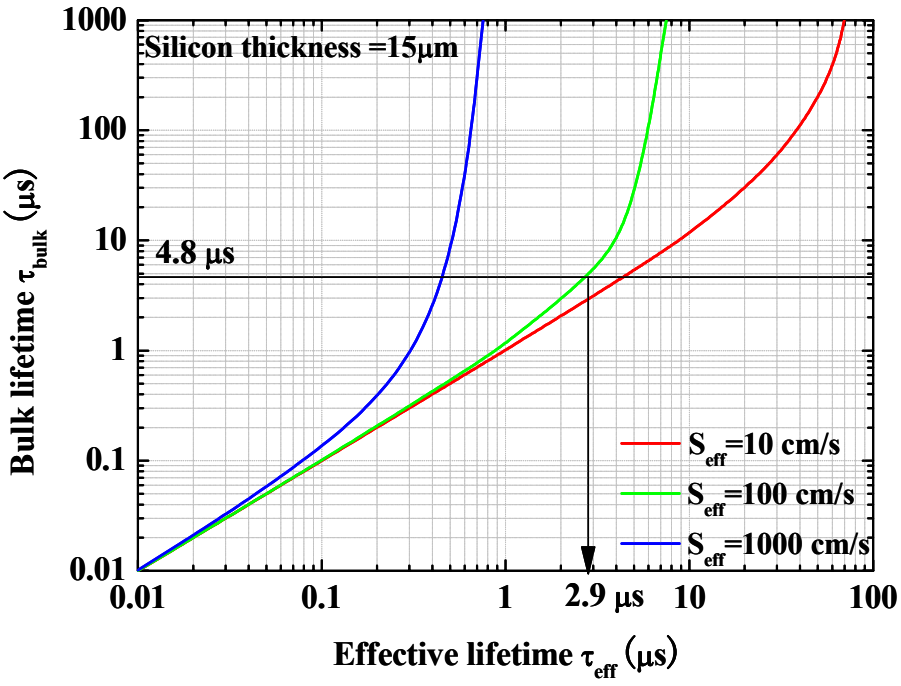

Figure 2.7 The relationship between the effective lifetime and bulk lifetime due to the surface recombination velocities

Figure 2.7 shows the relationship between the τ_{eff} and the τ_{bulk} due to surface recombination velocities using numerical calculations. The τ_{eff} is equal to the τ_{bulk} only if the S_{eff} near or being equal to 0. At high S_{eff}, the measured the τ_{eff} are no longer equal to the τ_{bulk} and therefore, the extracting of the τ_{bulk} is needed. Thinner wafer for instance, provided big difference between the τ_{bulk} and the τ_{eff}. No matter how high τ_{bulk} the silicon wafer had, we could only measure the low τ_{eff} in the case of the extremely high S_{eff}. It means that the lower S_{eff}. (below 1000 cm/s) is needed for the accurate evaluation of τ_{eff}. Thus, passivation technique is very important for the evaluation of surface recombination. It needs to obtain over the τ_{eff} of 2.9 μs for the achieving τ_{bulk} of 4.8 μs which was got from the result of device simulation in the S_{eff} of 100 cm/s.

2.5.3 Evaluation technique of effective carrier lifetime

The carrier lifetime is the most important electrical characterization in silicon solar cells which are minority carrier device. The carrier lifetime indicates material quality and check of device fabrication process in silicon. Photoconductance decay (PCD) and Quasi-Steady-State PhotoConductance method (QSSPC) are discussed in detail. In the both methods, surface passivation on front and rear side of samples is needed. Bare bulk type c-Si wafer (300 μm) without surface passivation indicate carrier lifetime below 5 μs in both methods. We can't measure correctly bulk lifetime by too big influence of surface recombination. We can measure the carrier lifetime, which is not the effective lifetime and the bulk lifetime, using PCD and QSSPC.

2.5.4 Micro-wave Photoconductance decay method

PCD involves the generation of excess carriers by a brief, sharp pulse of illumination

that is rapidly turned off [10]. The resulting decay of carriers back to their equilibrium concentrations is monitored via the photoconductance, and the recombination lifetime calculated. In the absence of significant trapping, the excess carrier densities are equal, and the net excess conductance $\Delta\sigma$ will be given by:

$$\Delta\sigma = q\Delta n_{av}\left(\mu_n + \mu_p\right)W \tag{2-9}$$

where Δn_{av} is the average excess carrier density, μ_n and μ_p are the electron and hole mobilities and W the sample thickness. In conjunction with a carrier density dependent mobility model, this expression allows Δn_{av} to be calculated for each measured value of $\Delta\sigma$. The effective lifetime is then calculated by differentiating this time-dependent trace:

$$\tau_{eff} = -\frac{\Delta n_{av}}{d\Delta n_{av}/dt} \tag{2-10}$$

Other researchers widely used PCD method is micro wave PCD (μ-PCD), in which the photoconductance is measured by means of the reflectivity of microwaves directed at the sample surface.

Figure 2.8 shows a schematic illustration of μ-PCD apparatus in our laboratory (WT-85XT Life Time scanner, SemiLab. Co). Excess carriers are generated by laser diode and photoconductivity is monitored by micro wave reflection. Microwaves from Gunn diode are irradiated onto the wafer, reflected microwaves are detected and then displayed. The frequency of microwave is the range of 10.043 GHz to 10.558 GHz which has enough penetration depth in silicon wafer thickness of the rage from 15 μm to 300 μm. And the wavelengths of laser diode can be selected to 532 nm and 904 nm. It means that the position of two points can be measured by the effect of light penetration depth in silicon. Especially, μ-PCD can measure the τ_{eff} of c-Si foils (15 μm). μ-PCD was mainly used for the τ_{eff}

measurement in Chapter 3 and 4. Compared with QSSPC method, there is one potential advantage of μ-PCD and that is the ability to 'mapping' lifetimes with high resolution, down to a spot size of around 0.25mm. However, μ -PCD can't measure in the wide range of carrier injection level as the solar cell operation under illumination.

2.5.5 Quasai-Steady-State Photoconductance

QSSPC technique was introduced by R. Sinton and a schematic is given in Figure 2.9 [11]. This method is relatively new technique of the evaluation of lifetime. The experimental apparatus (WT-120) used in this thesis was fabricated by Sinton Consulting. An instrument was available that applies inductive coupling and illumination with a photo flash lamp. The QSSPC is a large signal technique and covers a wide and well defined injection range in a single measurement. The sample of interest is inductively coupled by the coil to an rf-bridge circuit, which senses changes in the sample's permeability and therefore its conductance. A steady-state analysis can be used to determine the effective lifetime from the absolute values of the photoconductance and photogeneration. Under the steady-state illumination, generation and recombination of electron-hole pairs are in balance and expressing generation (J_{ph}) and recombination (J_{rec}) in terms of current densities will lead to

$$J_{ph} = J_{rec} \tag{2-11}$$

One can use the effective lifetime to give the total recombination in the sample of known thickness by:

$$J_{ph} = \Delta n q W / \tau_{eff} \tag{2-12}$$

where Δn is the excess carrier concentration, q is the electron charge , W is the sample thickness and τ_{eff} is the effective lifetime. The excess photoconductance, σ_L is given by

$$\sigma_L = q\Delta n_{av}(\mu_n + \mu_p)W \tag{2-13}$$

and the effective minority carrier lifetime can then be determined from Eqs. 2-12 and 2-13,

$$\tau_{eff} = \sigma_L / \left[J_{ph}\left(\mu_n + \mu_p\right)\right] \tag{2-14}$$

The conductance and light intensity can be measured using a calibrated instrument and a reference solar cell and the collected data can be processed using a computer. In this thesis, The QSSPC technique is used intensively to measure the injection level dependant τ_{eff} for accurate evaluation of surface recombination in Chapter 4.

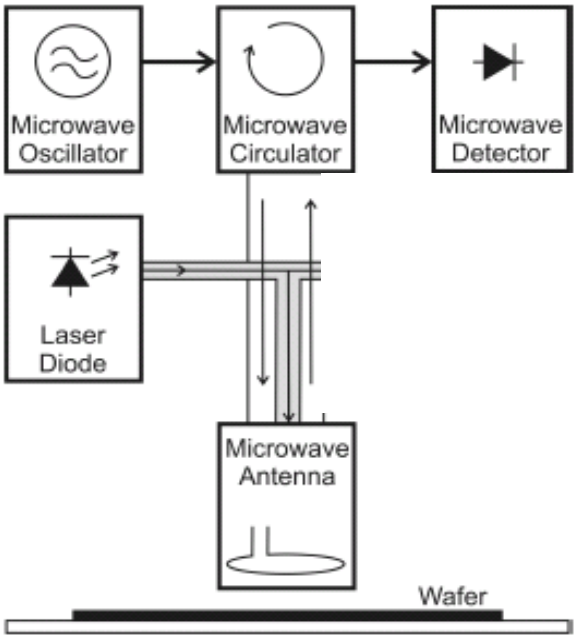

Figure 2.8 A schematic illustration of μ-PCD apparatus

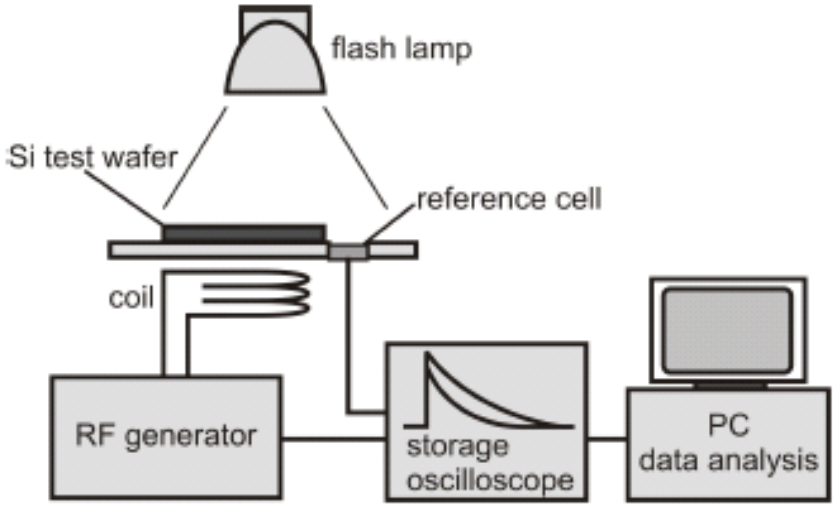

Figure 2.9 A schematic illustration of QSSPC apparatus

2.6 Summary

For the development of high efficiency c-Si foil solar cells, the required electrical properties, which are especially bulk carrier lifetime and surface recombination velocity in c-Si foil, and the structure of c-Si foil solar cell can be found using device simulation. The practical theories and measurement technique for minority carrier lifetime and surface recombination were obtained. In the 15 μm c-Si foil solar cells, the required electrical properties which are bulk carrier lifetime: over 4.8 μs and rear surface recombination velocity: below 100 cm/s were obtained by device simulation. The rear contact ratio of below 10% was obtained for high efficiency. If these electrical properties have been achieved, 10 % efficiency could be obtained without light trapping. It needs to obtain over the τ_{eff} of 2.9 μs to the achieving τ_{bulk} of 4.8 μs which was noticed from the result of device simulation in case of the S_{eff} =100 cm/s. These bulk carrier lifetime and surface recombination velocity became the target for the development of LFC-SPS cell through this thesis.

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Chapter 3

Optimization and characterization of c-Si foils fabricated by Sintered Porous Silicon process

3.1 Introduction

Layer Transfer technique based on restructured porous silicon (porous-Si) used the distinction that the surface closure of porous-Si is caused by hydrogen annealing. The anodization condition and hydrogen annealing condition have a strong influence on the quality of silicon crystalline. For improvement of high efficiency solar cell (over 10 % conversion efficiency), bulk minority carrier lifetime (τ_{bulk}) was found to be over 2.9 μs by device simulation in Chapter 2. For getting excellent epitaxial growth silicon layer as active layer of c-Si foil solar cell, we require to know the influence of anodization condition and hydrogen annealing. However, a few studies have been reported on the influence of dependence on anodization and hydrogen annealing.

In this Chapter, Layer Transfer using SPS process is demonstrated and optimized through many experiment. The quality of epitaxial growth silicon layer dependence on anodization and hydrogen anneal conditions is discussed through the evaluation of carrier lifetime and Raman spectra. We propose and discuss the making higher quality of epitaxial growth silicon layer.

3.2 Formation of porous silicon layer

3.2.1 Porous silicon

A lot of researches about porous-Si had been reported. These were mainly experimental observation, formation of porous silicon, and electronic and optical properties and applications. Uhlir first reported on the formation of porous-Si in 1956 [1]. However, the mechanism of formation and properties of porous-Si are still not completely understood until now. One layer of porous-Si is easy to fabricate. It forms electrochemical etching of silicon in fluoride atoms including etchants.

Figure 3.1 shows that the setup of anodization apparatus consists of a container filled with HF including electrolyte. The silicon wafer is use as an anode and the platinum plate is used as a cathode. The porous silicon is formed on the surface of silicon by the current flows. This reaction is made by the supply of positive charge carriers from the surface of silicon and negative fluoride ions from the etchants. In this reaction, it bore pores on the surface of silicon. A variation of current flow leads to the variations of the porosity of porous-Si layer.

A lot of researchers currently discuss about reaction paths during the formation of porous-Si layer. Unagami reported one of reaction paths during the formation of porous-Si [2]. First reaction path is

$$Si + 2HF + (2-\lambda)e^{+} \rightarrow SiF_2 + 2H^{+} + \lambda e^{-} (\lambda < 2) \quad (3\text{-}1)$$

$$SiF_2 + 2HF \rightarrow SiF_4 + H_2 \quad (3\text{-}2)$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6 \quad (3\text{-}3)$$

$$(\lambda < 2)$$

Second reaction path is

$$Si + 4HF + (4-\lambda)e^{+} \rightarrow SiF_4 + 4H^{+} + \lambda e^{-} (\lambda < 4) \quad (3\text{-}4)$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6 \quad (3\text{-}5)$$

where e^{+} is hole, e^{-} is electron. In the empirical rule formed by many experiment of formation porous-Si, we can predict the properties of a porous-Si layer formed by varied formation parameters (Table III-I.) [3].

3.2.2 Anodization apparatus

When we make a porous-Si in aqueous HF etchants, there are three important things: (i) The contact of the wafer surface with the fluoride-containing etchant, (ii) A homogeneous current flow through the wafer for electrochemical dissolution reactions, and (iii) No leakage current to allow control of the etching current by control of the current flowing from the anode to the cathode.

Figure 3.2 shows two-chamber anodiziation etching apparatus for 2 inch silicon wafer. Figure 3.3 shows a cross section sketch of two-chamber anodiziation etching apparatus. This apparatus was made of vinyl chloride (for (i)). The two chambers were separated by a 2 inch silicon wafer mounted on the wall. A 2 inch silicon wafer was pressed by a wafer cover with eight screws. The distance between the wafer and the wall, the cover and the wafer were sealed by Viton O-ring (for (ii)). Anodiziation etchants are poured into both chambers and filled. The anode and cathode electrodes, consisting of circular Pt plats with a diameter of 3.5cm are mounted 1cm from the wafer. Porous-Si is formed in a circular pattern with diameter 3.8cm by Viton O-ring sealing. One porous-Si formation needs 540 ml etchants. The etching procedure was controlling by control of the current flow from the anode to the cathode using the computer (for (iii)).

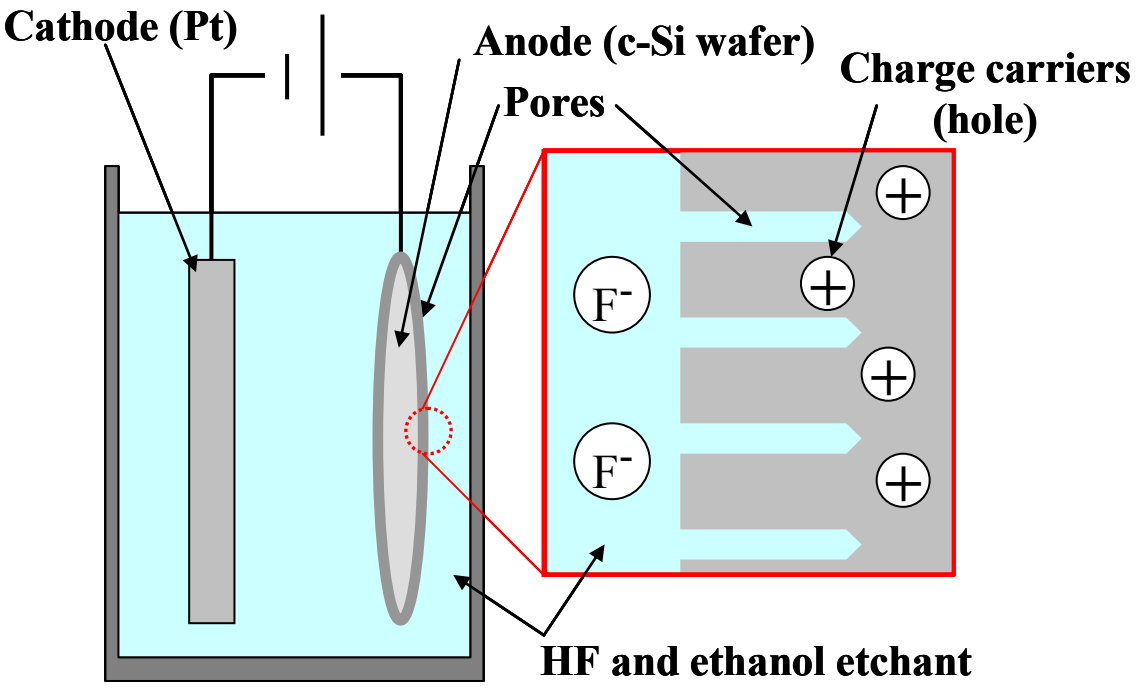


Figure 3.1 Porous silicon formation by electrochemical etching in HF and ethanol.

Table III-I. Dependence of porous silicon layer thickness, porosity and growth rate on etching current and HF concentration.

An increase of …	cause…	and leads to…
anodization current	flooding of the space charge region with carriers	increased pore size increased porosity increased layer growth rate
HF concentration	Increased dissolution velocity	decreased pore size decreased porosity increased layer growth rate

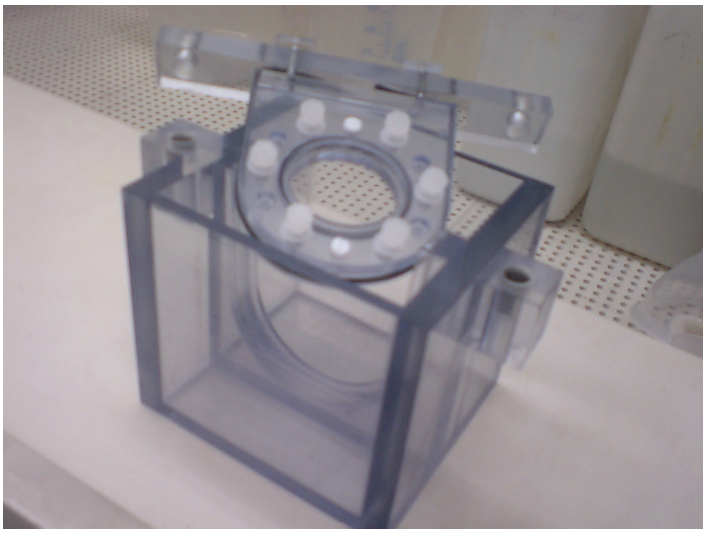


Figure 3.2 Photograph of two-chamber anodiziation etching apparatus.

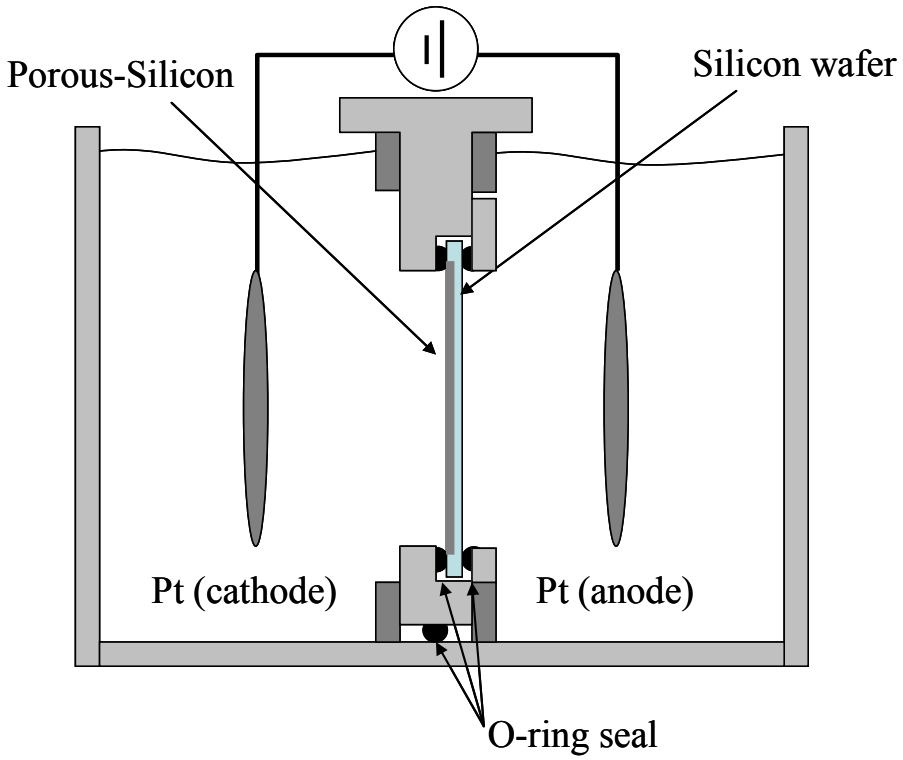


Figure 3.3 A cross section sketch of two-chamber anodiziation etching apparatus

3.2.3 Processing sequences for anodization porous silicon

A 15 μm c-Si foil sample was prepared. 2 inch p-type Cz c-Si (100) wafers were used as substrates. The resistivity of the wafer was 0.01-0.02 Ω cm. 15 μm c-Si foil samples were prepared by the following procedure using the porous-Si process

1. Cleaning before the formation of porous-Si
   1.) The Si wafers were dipped in acetone for 5min. Next the wafers were dipped in diluted HF (1%) to remove an oxide layer.
   2) The wafers were rinsed in de-ionized water.
   3) Drying of the wafers with nitrogen.
2. The electrochemical porous-Si formation

The anodization current is very important for deciding the characteristics of multi porous-Si layer. The target anodization current steps are decided before the porous-Si formation. The computer-controlled power supply operates in constant current mode. For three porous-Si layers formation, the anodization current profile consists of three constant current steps. The current controlling programs make constant current and linear ramping of anodization current.

3. Removing of native oxide and anodization oxide
   1) The wafers were rinsed in de-ionized water in several times. Next the wafers were dipped in diluted HF (5%) for 15 min.
   2) The wafers were rinsed in de-ionized water five times.
   3) Drying of the wafers with nitrogen.
   4) The wafers were sealed in low pressure desiccators, transport hydrogen anneal process.

Figure 3.4 (a) and (b) show the SEM cross section image of porous-Si formed by 50 mA/cm^2 anodization current using our anodization apparatus for conventional result. In the 50

mA/cm^2 anodization current, the porosity is approximately 35 % and the porous-Si layer uniformly was formed.

In the empirical rule formed by many experiment of formation porous-Si, we can predict the properties of a porous-Si layer formed can be predicted by varied formation parameters (Table III-I.) [2].

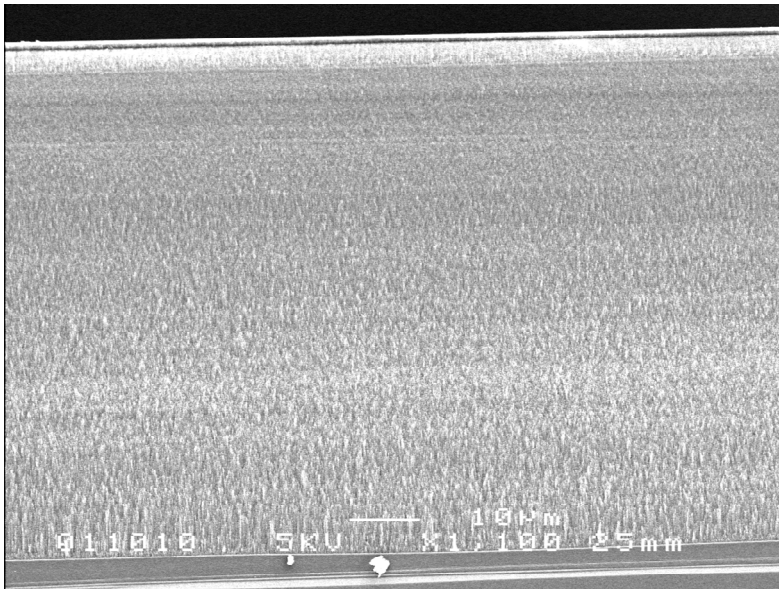
3.2.4 Three porous-Si layers formation

Three porous-Si layers were used for separation and anodization etchants, while consists of HF and ethanol =3:1. The silicon atoms are dissolved from the top of the silicon surface and micro pores are formed.

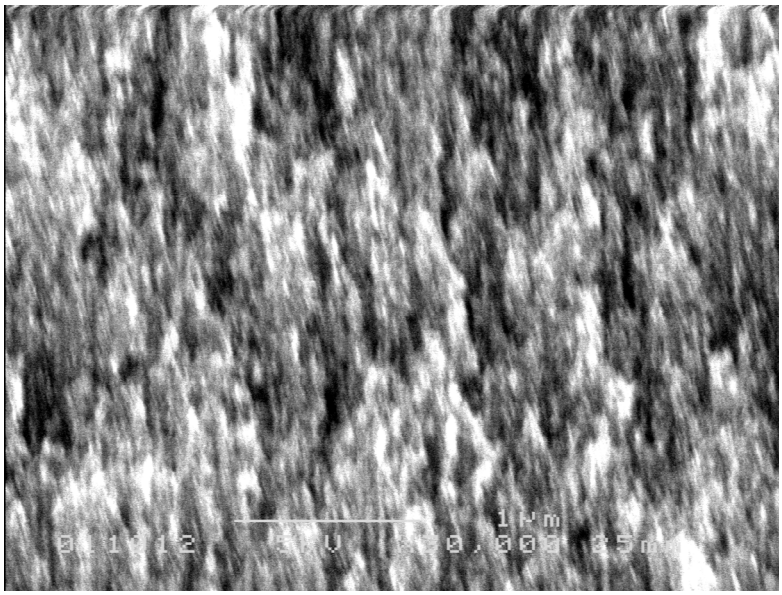
The c-Si wafer is anodized to a few microns from the surface of silicon wafer for low current density (1-10 mA/cm^2) of the first steps and middle current density (10-50 mA/cm^2) of the second step. Then, high current density (200-350 mA/cm^2) in the third step was flowed in the already formed middle porosity silicon layer with middle current density (in Fig. 3.5). This mechanism was proposed by Tayanaka et al. [4]. This high porosity silicon layer was approximately 50-80% and may have beeen due to the shortage of F^- atoms deep inside the micro pores in the low porosity layer. HF-based solution is provided through the micro pores from the top surface of porous-Si. With the low current density as in step 1 and step 2, anodization is preformed at the interface between the silicon substrate and HF-base solution because the resistivity of porous-Si R_{HF0} is smaller than the resistivity of R_{Si} (Fig.3.6 a).

However, if high current density flows in the already formed low-porosity layer, some electrochemical reaction to reduce F^- atoms occurred in the process. In this way, the resistivity of the HF-based solution R_{HF1} became higher than the resistivity of the porous-Si R_{Si} underneath the already formed low-porosity silicon layer. (Fig.3.6 b).

Figure 3.7 shows the cross section of a SEM image of poorly multi different



(a)



(b)

Figure 3.4 The SEM cross section image of porous silicon formed
(a) Porous silicon layer were formed by 50mA/cm^2 anodization current
(b) The magnified figure of (a)

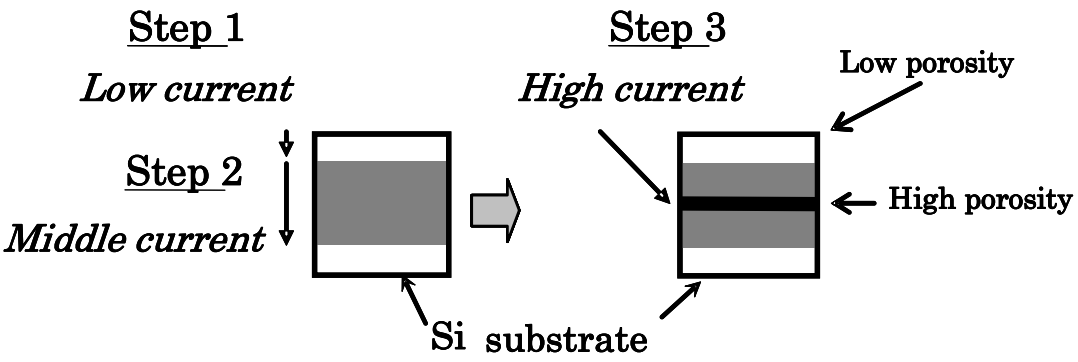


Figure 3.5 Three different porous silicon layers fabrication sequence

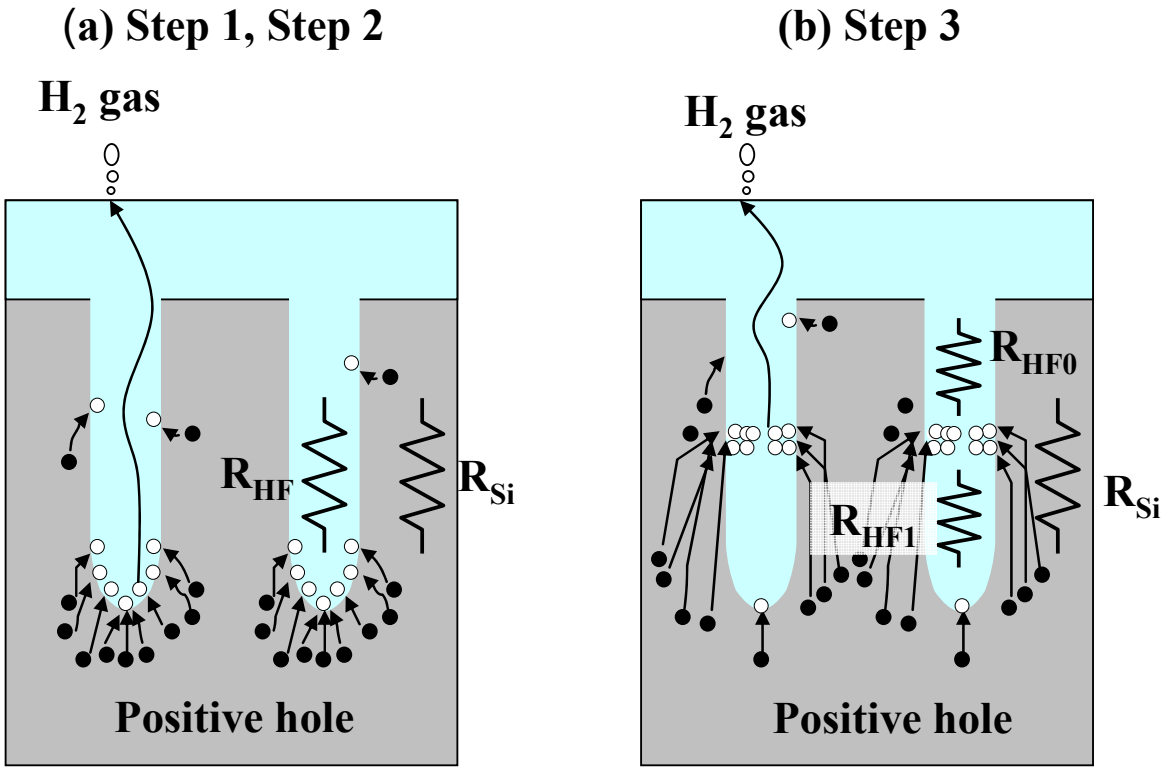


Figure 3.6 Three porous silicon layers fabrication mechanism.

porous-Si layer formation. This poorly multi porous-Si layers indicates an inhomogeneous third layer as the separation layer was formed. The unhomogeneous third layer leads to cracks in the separation. The inhomogeneous porous-Si layer formation was caused by unhomogeneous anodization current.

The anodization apparatus was developed in order to obtain porous-Si layers. Figure 3.8 shows separated porous-Si layers just after anodization. The third porous-Si layer as a separation layer of this sample was formed by anodization current of 400mA/cm^2.

The anodization condition that made the possible separation are list as follow, Step 1: 1-5 mA/cm^2 for 4 min, Step 2: 15-30 mA/cm^2 for 4 min and Step 3: 200-350 mA/cm^2 for 4 sec (in Fig.3.9). Figure 3.10 shows one of homogeneous porous-Si layer of possible separation. The approximately 4.5 μm low porosity silicon layer and approximately 5.5 μm middle porosity silicon layers were formed by Step 1 and Step 2 respectively. Finally, the current density region of Step 3. The approximately 0.4 μm high porosity silicon layer was formed in the center of middle porosity layer by Step 3.

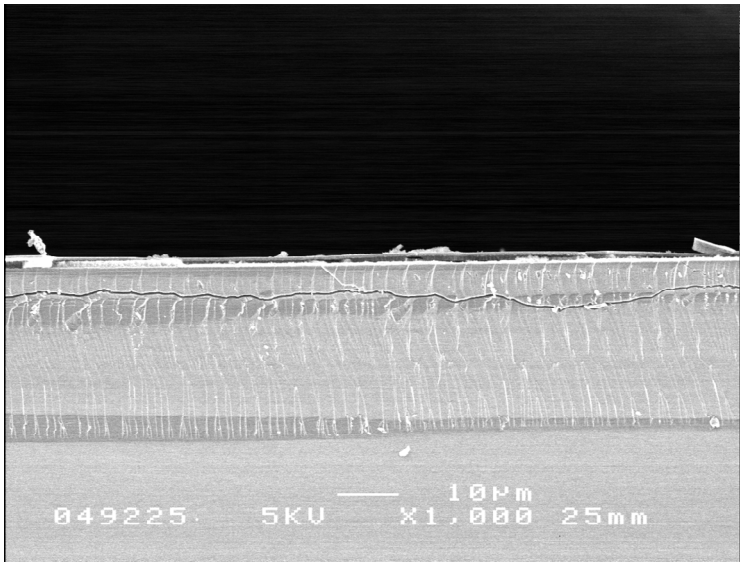


Figure 3.7 The cross section SEM image of poorly porous-Si layer formation

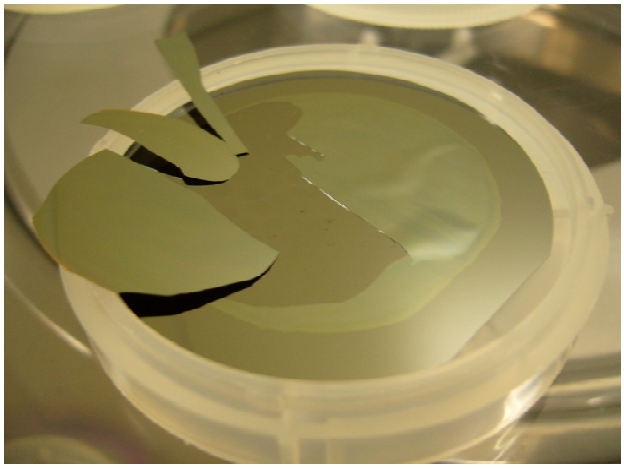


Figure 3.8 Photograph of separated porous silicon foil after anodization

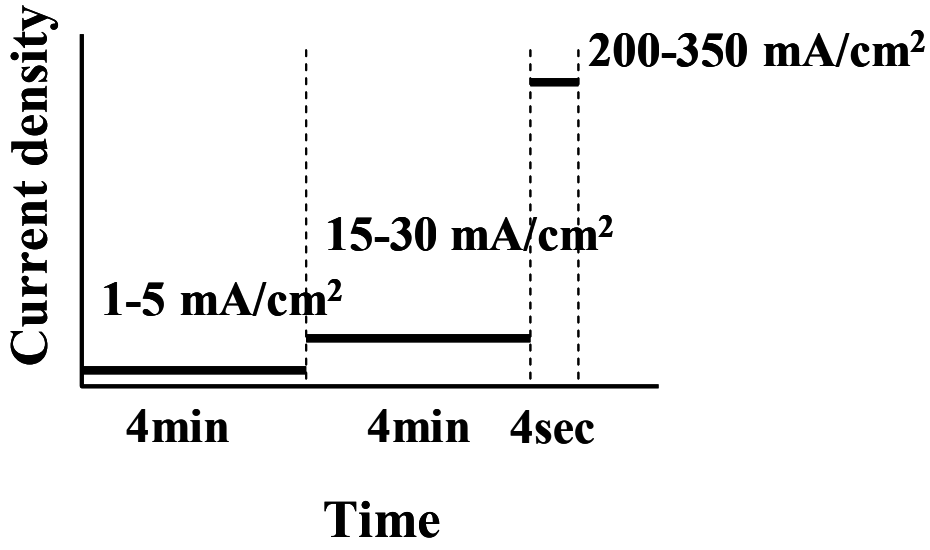


Figure 3.9 Anodization current density sequence for separation.

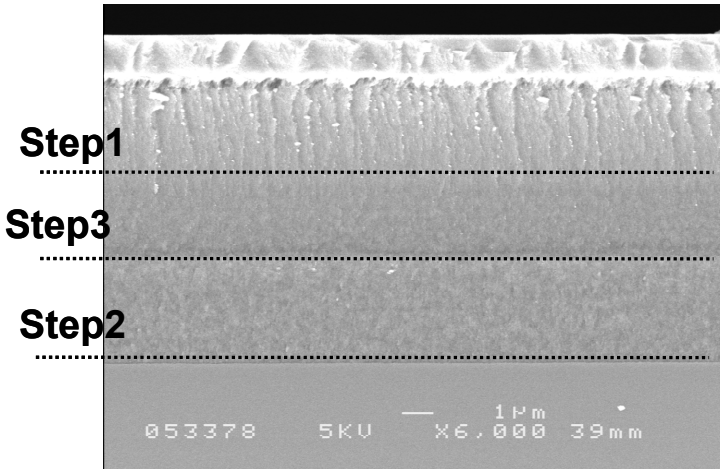


Figure 3.10 The cross section SEM image of homogeneous three porous silicon layers formation.

3.3 Atmospheric hydrogen annealing and epitaxial growth

3.3.1 Atmospheric pressure chemical vapor deposition apparatus

After anodization, the wafer was carried in an Atmospheric Pressure Chemical Vapor Deposition (APCVD) apparatus for structural change of the separation layer and deposition of 15 μm c-Si foils. An overview of the CVD apparatus is shown in Fig. 3.11, and the schematic is shown in Fig. 3.12. The 1200 W high-frequency induction heating and a 900 mm long quartz tube were used as reactors. The Induction coil made an eddy current in SiC coated carbon susceptor and a carbon susceptor was heated. The wafer put on this susceptor was the one for the growth reaction whose maximum temperature was 1250 ˚C. The growth temperature was 1050 ˚C and controlled by high-frequency current with a PID system and measured outside of the quartz tube by the radiation thermometer. The inner diameter of the tube was 150 mm. In the epitaxial growth, SiH_2Cl_2 (DCS) was used as a Si gas source and purified H_2 gas was used as the carrier gas. BCl_3 of 99.8 ppm diluted with Ar was used for the p-type doping. These gas flows were controlled by mass flow controllers. The chlorine ingredient in the gas after a crystal growth was removed with the cleaning unit.

3.3.2 Atmospheric hydrogen annealing

In the hydrogen annealing, APCVD apparatus (Fig.3.12 and Fig.3.13) was used and the annealing condition was 900 - 1100 ˚C with pure H_2 at atmospheric pressure. The hydrogen annealing temperature and time varied from 900 ˚C to 1100 ˚C and 20 to 50 min, respectively.

Figure 3.13 shows separated porous-Si layers in the hydrogen annealing. After anodization, the porous-Si layers of this sample were stabilized on c-Si wafer. However the

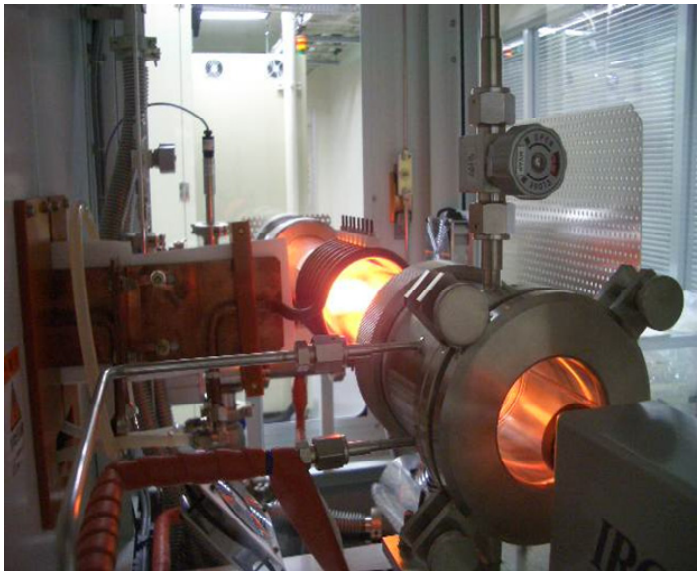


Figure 3.11 Photograph of CVD apparatus

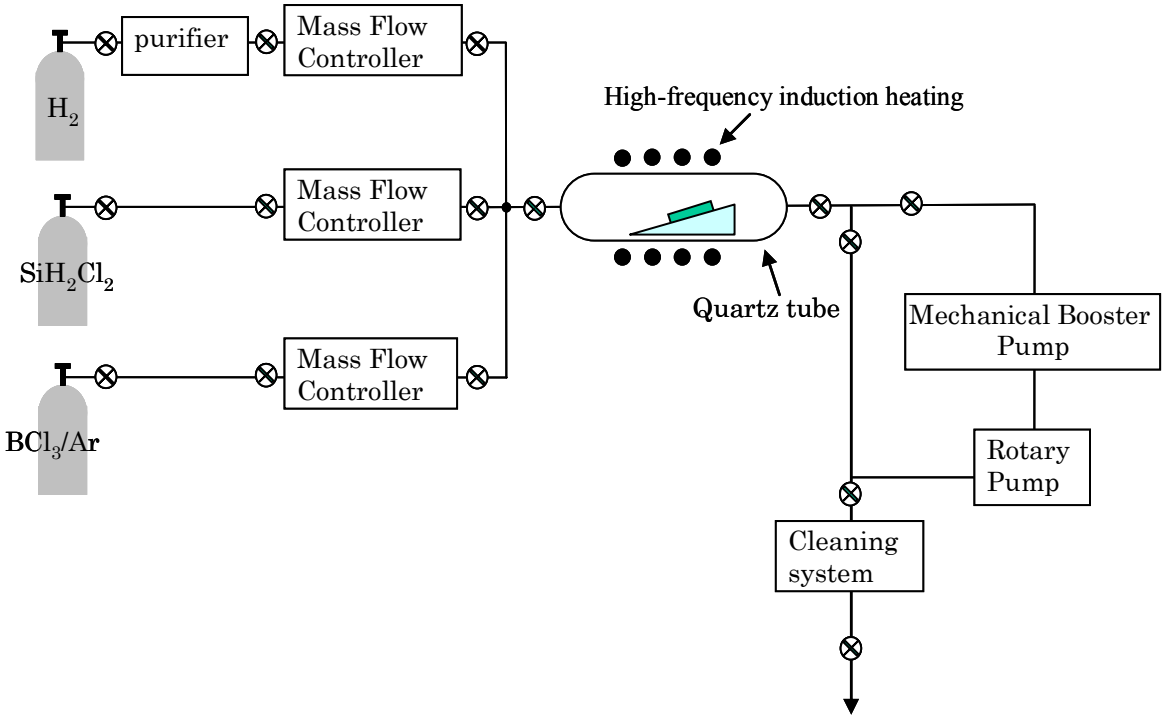


Figure 3.12 Schematic diagram of CVD

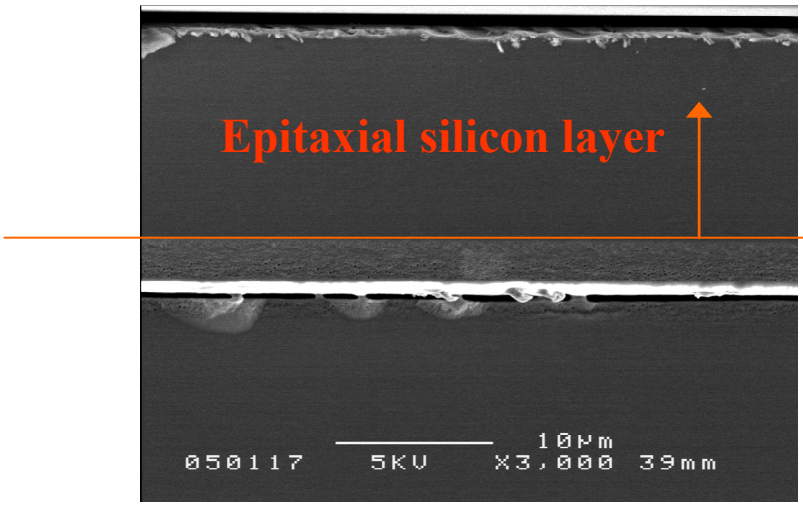
Figure 3.13 Photograph of separated porous silicon in process of hydrogen annealing

separation layer grew greater by adjacent voids agglutinated and porous-Si layers separated in the hydrogen annealing. Figure 3.14 shows a cross section of a SEM image of 15 μm c-Si foils (Fig. 3.14(a)) and separation layer (Fig. 3.14(b)) after hydrogen annealing and epitaxial growth. The annealing temperature was 1050˚C for 20 min and epitaxially crystalline was grown at 1050 ˚C for 20min. After hydrogen annealing, the wafer surface, which is low porosity porous-Si layer became to c-Si. The void of surface close by surface diffusion of silicon atoms. The voids in hydrogen annealing explained by the free surface energy that depends on the orientation of the crystal surface.

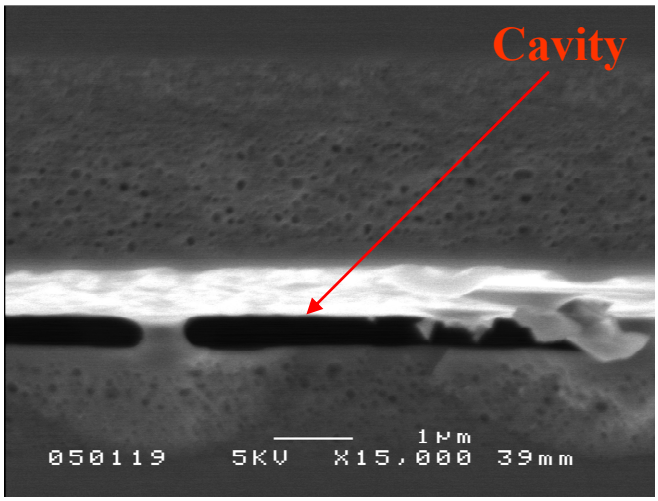
3.3.3 Epitaxial growth of 15 μm c-Si foil on separation layer

15 μm c-Si foils are deposited on the wafer of surface closure after hydrogen annealing. The epitaxially growth temperature was 1050˚C for 20 min with boron doping density of 5.8×10^{15} cm^{-3} and a growth rate of 0.75 μm/min. In order to transfer to 15mm× 15mm, 1.5 mm thickness glass superstrates, Polyene-polythiol UV cure adhesive (Denka Kagaku Kogyo) was used [5].

Figure 3.15 shows 15 μm c-Si foil adhered on glass superstrate after separation. Figure 3.16 shows the X-ray diffraction (XRD) spectrum measured with the $Cu_{K\alpha}$ lines for a 15 μm c-Si foil on glass superstrate. Only the large (400) peak originates from 15 μm c-Si foil. This peak indicates at 69.14^{o}, corresponding to a lattice constant of 542.991 pm. The silicon lattice constant is 543.095 pm [6]. Our result is same result of Brendel et al. [7]. They tried to record Laue images of epitaxial film and c-Si substrate. The Laue images of the epitaxial film showed spots at same position as for the c-Si substrate. They explained that the x-ray diffraction spectrum does not strictly prove monocrystalinity because the epitaxial film could consist of many (100)-oriented crystallites being rotated by various angle around (100) direction.



(a)



(b)

Figure 3.14 The cross section SEM image of 15 μm c-Si layer after epitaxial growth
(a) 15 μm c-Si layer and separation layer
(b) magnified figure of separation layer

Figure 3.15 Photograph of 15 μm c-Si foil adhered on glass superstrate after separation

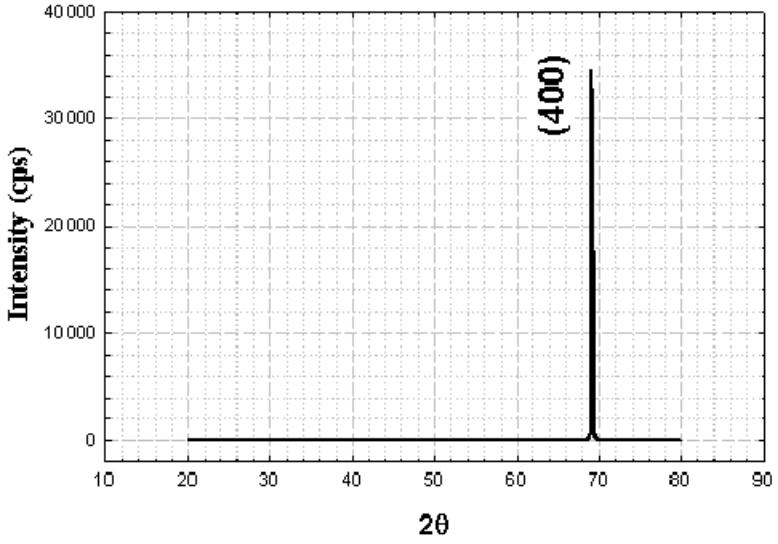


Figure 3.16 X-ray diffraction spectrum of 15 μm c-Si layer after separation

Figure 3.17 shows the SIMS profiles of 15 μm c-Si foil about Si, H, O, B and Cu. These profiles are from restructured porous-Si surface to15 μm c-Si foil. It shows two things which are porous-Si surface becoming high B doped layer, which is called BSF (Back Surface Field) layer, and the metal impurities exist in porous-Si layer. After hydrogen annealing, the surface of porous-Si is changed to close to c-Si. This layer has approximately 1-1.5 μm and high B doping diffuse from Mother c-Si substrate. The porous-Si layer is polluted by copper as metal impurities. Other literature published gathering effect of porous-Si [8].

The iron impurities were also measured by SIMS. However, the iron profile couldn't get this clearly because the masses of silicon and iron are similar. We predicted iron impurities were also gathered in restructured porous-Si like copper refer to [9]. Oxygen atoms in 15 μm c-Si foil were also very low. In particular, iron and oxygen create recombination centers and lead to the degradation of lifetime in silicon [10]. It is important to minimize iron and oxide contamination by the gathering effect of porous-Si. It is possible that porous-Si after separation include many impurities. The restructured porous-Si layers were removed from the rear side of 15 μm c-Si foil through this thesis.

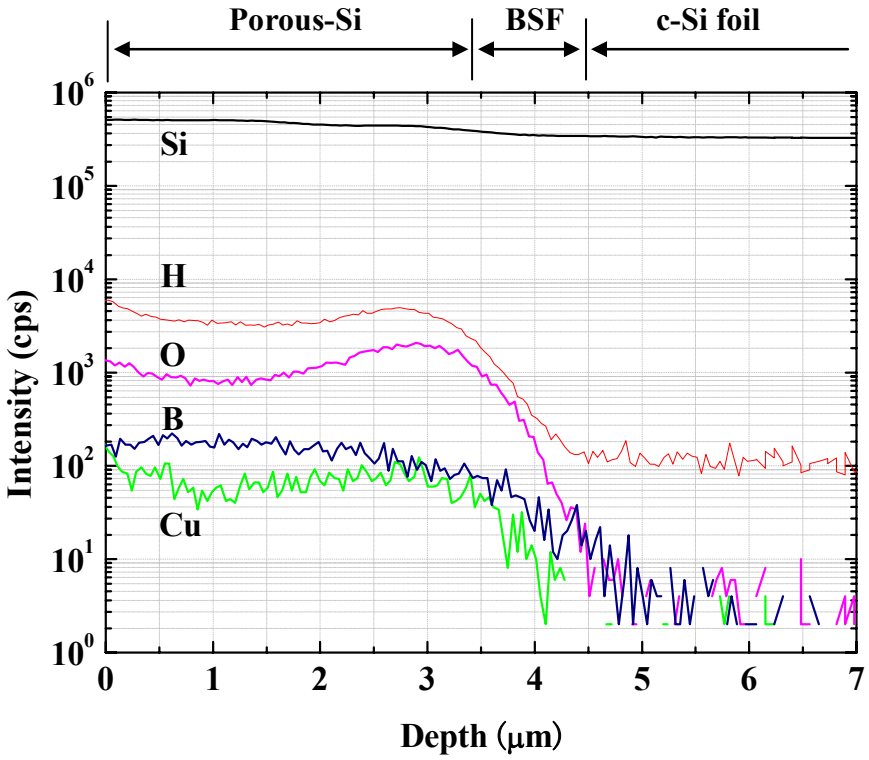


Figure 3.17 The SIMS profiles of 15 μm c-Si foil after separation

3.4 Characterization of c-Si foil depending on anodization and hydrogen annealing

To achieve the high efficiency, the requirement of getting the high effective carrier lifetime (τ_{eff}) in 15 μm c-Si foil was derived from Chapter 2. In this section, we analyzed that crystallization and minority carrier lifetime of 15 μm c-Si foil depending on various anodization conditions. The epitaxial growth condition of all samples were the same condition which is 1050 ˚C for 20 min with boron doping density of 5.8×10^{15} cm^{-3} and the growth rate of 0.75 μm/min. Table III-II. shows varied anodization conditions and hydrogen annealing condition, the anodization current density of Step 1 and Step 3 were changed. The Step 2 anodization current density was fixed at 20mA/cm^2.

3.4.1 Crystal characterization analysis of c-Si foils

We investigated 15 μm c-Si foils by Raman scattering spectroscopy. Figure 3.18 shows sample structures of 15 μm c-Si foils on the silicon wafer before separation. The Ar laser (wavelength: 514.53 nm) was used in Raman scattering spectroscopy apparatus. We could just get the information from 15 μm c-Si foil because of the penetration depth of Ar in silicon (approximately 0.1 μm).

Figure 3.19 shows the FWHM and peak position of the TO-LO phonon band (520.5 cm^{-1} in c-Si) as a function of the third step anodization current density. With a decrease of the third step current density, FWHM of the TO-LO phonon band became narrower, becoming close to that of epitaxial growth on Fz c-Si substrate (non-doped >1000 Ω cm (100) 400 μm thick) due to improvement of crystallization. At the 300 mA/cm^2 third step anodization current, Raman band is much wider, which means the resulting Si lattice contained higher disorder for which higher crystal defect density was expected. In the peak position of TO-LO

phonon band, with higher third anodization current density, peak position much shifted. In the result of XRD, Only the large (400) peak originates from 15 μm c-Si foil. This peak indicates at 69.14^{o}, corresponding to a lattice constant of 542.991 pm. This result showed shorter than the lattice constant of (100) silicon surface. The epitaxial film could consist of many (100)-oriented crystallites being rotated by various angle around (100) direction. This influence is increase with lower crystallinity.

Third step anodization current is role on formation of separation. High current density is much better for easy to separation. However, High third anodization current density causes low crystallization of 15 μm c-Si foil. And first step anodization current also strongly affect crystallization of 15 μm c-Si foils (in Fig. 3.19 red square symbol). With the lower Step1 anodization current density (3 mA/cm^2), Step 2: 20 mA/cm^2, Step 3: 250 mA/cm^2, FWHM of the TO-LO phonon band became narrower and the crystallization became higher. However this condition (red square symbol condition) got inhomogeneous separation. The yield ratio of separation is low.

Figure 3.20 shows the FWHM of the TO-LO phonon band as a function of the hydrogen annealing time and temperature. While anodization condition, which is Step 1: 3mA/cm^2, Step 2: 20mA/cm^2, and Step 3: 250 mA/cm^2, was fixed.

These results in Fig. 3.20 have not peak sift of Raman spectral and also indicate quality of crystal increasing with increase temperature and annealing time. In the hydrogen annealing at 1000 ˚C, FWHM of the TO-LO phonon band became much wider. This sample always couldn't separate 15 μm c-Si foils from Mother c-Si substrate in this condition.

Table III-II. The varied anodization conditions and hydrogen annealing condition

Parameters	Values
Anodization current density (mA/cm^2)	
1st step for 4 min	**3 – 5**
2nd step for 4 min	**40**
3rd step for 4s	**200 – 300**
Etchants (HF:ethanol)	**3 : 1**
Hydrogen annealing time (min)	**20 - 50**
Hydrogen annealing temperature (℃)	**1000 – 1100**

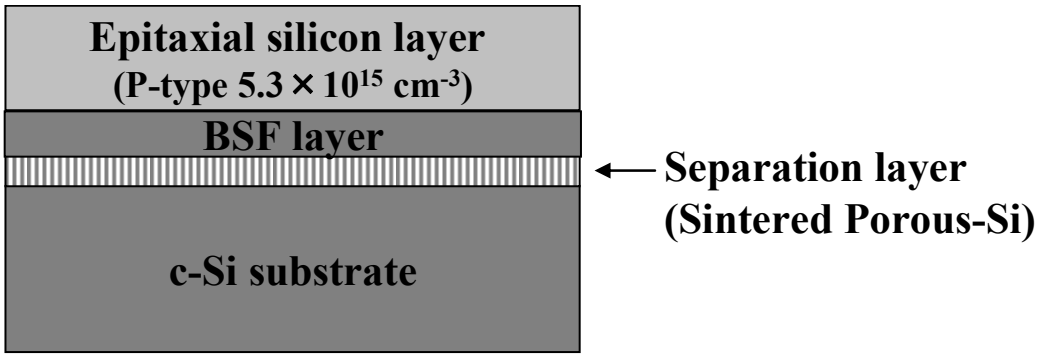


Figure 3.18 The sample structure of Raman scattering spectroscopy.

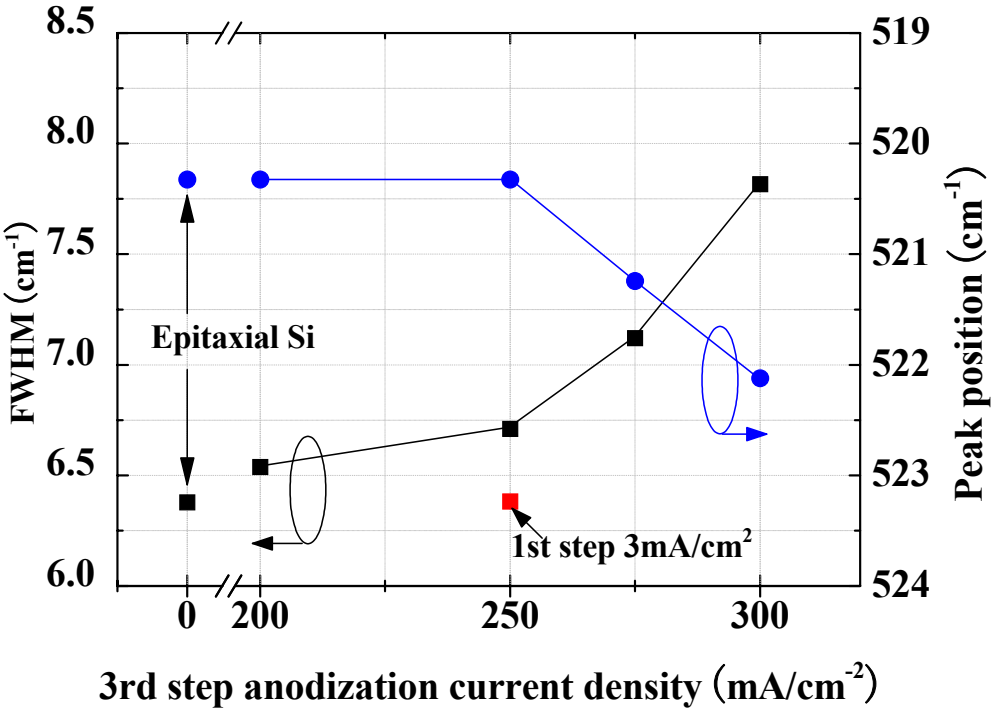


Figure 3.19 The FWHM and peak position of the TO-LO phonon band as a function of the third step anodization current density.

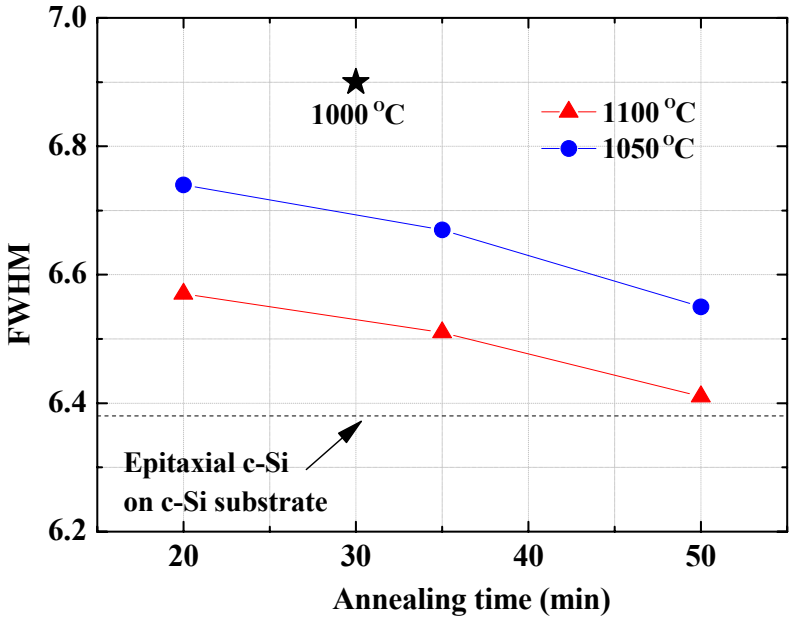


Figure 3.20 The FWHM of the TO-LO phonon band as a function of the hydrogen annealing time and temperature.

3.4.2 Effective carrier lifetime of c-Si foils

To develop high-efficiency solar cells, effective carrier lifetime is the key parameter. We investigated effective carrier lifetime in 15μm c-Si foil by μ-PCD. The excited light wavelength was 532 nm in μ-PCD. We could just get the information from 15 μm c-Si foil because laser beam was almost absorbed in 15 μm c-Si silicon foil.

Figure 3.21 shows the structure of lifetime measurement sample. SiN_X layer were deposited on both side of 15μm c-Si foil for surface passivation. The deposition condition of SiN_X was as follows: the substrate temperature was 200 ˚C, the RF-power with an excitation frequency of 13.56 MHz was 40 W, the pressure was 80 Pa, the flow rate of SiH_4/H_2 and NH_3 were 50 and 80 sccm respectively. The thickness was about 70 nm. The NH_3 plasma-treatment was used to increase passivation effect at low temperature refer to Chapter 4.

Table III-III shows effective carrier lifetime of 15 μm c-Si foil as a function of anodization current density and hydrogen annealing conditions.

For the reference lifetime sample which is directly 15 μm silicon epitaxial growth on c-Si substrate at 1050 ˚C and 1100 ˚C for 35 min was measured. These show 9.0 μs and 9.1 μs for crystal growth at 1050 ˚C and 1100 ˚C, respectively. All samples of 15 μm c-Si foil indicated below 9.0 μs.

However, Similar to the previous experiment in crystal analysis, with a decrease of the third step current density and first step current density, minority carrier lifetime indicated higher value. However, the τ_{eff} didn't depend on hydrogen annealing temperature like previous experiment in crystal analysis.

Figure 3.22 shows the relationship between the yield rate of successful separation and anodization and hydrogen annealing temperature. The sample conditions: (a) - (f) corresponded to sample conditions indicated in Table III-III. 10 samples in each condition were prepared. The (a) and (b), represent low anodization current in Step 1 and Step 3,

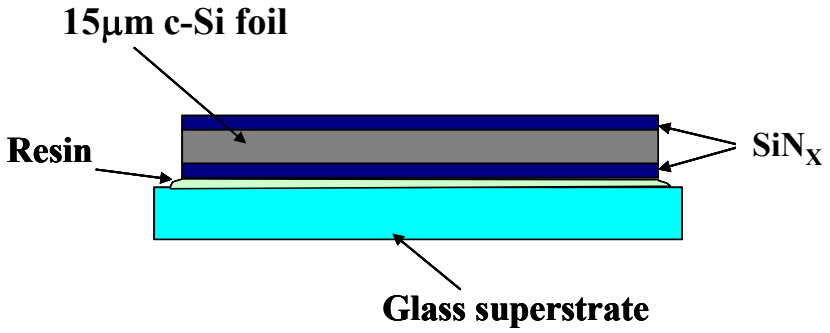


Figure 3.21 The sample structure of 15μm single crystalline silicon foil for effective lifetime measurement.

Table III-III. Effective lifetime of dependence of anodization current density condition

	Hydrogen annealing temperature (35min)	Epitaxial c-Si on c-Si substrate	15μm c-Si foil		
			Anodixation current density (mA/cm^2)		
			1st : 3 2nd : 20 3rd : 200	1st : 5 2nd : 20 3rd : 250	1st : 5 2nd : 20 3rd : 300
τ_{eff} Effective lifetime (μs)	1050℃	9.0	5.3 (a)	4.1 (c)	2.0 (e)
	1100℃	9.1	5.5 (b)	4.6 (d)	Separated (f)

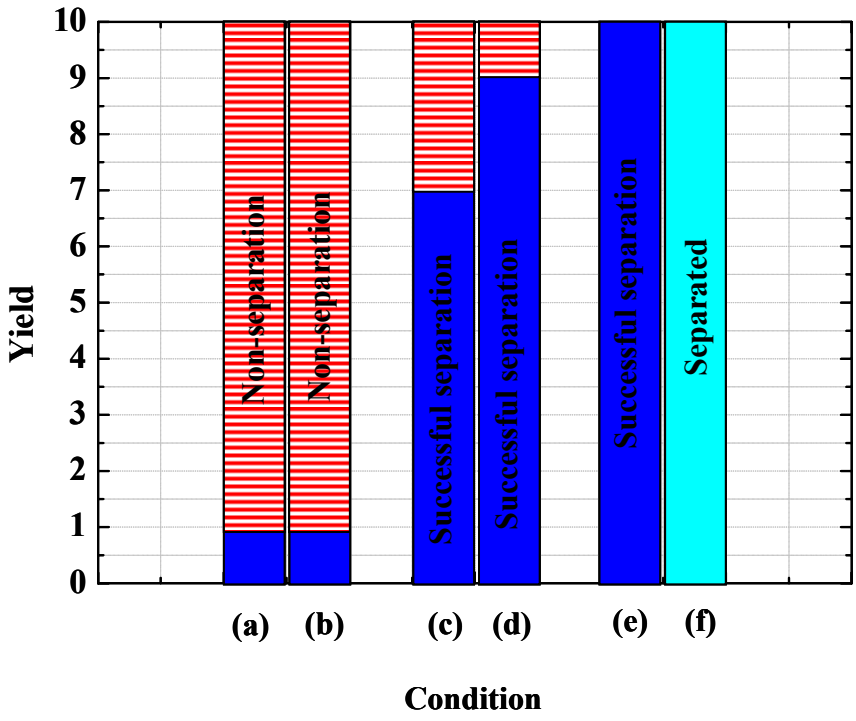


Figure 3.22 The relationship between the yield rate of separation and anodization and hydrogen annealing temperature

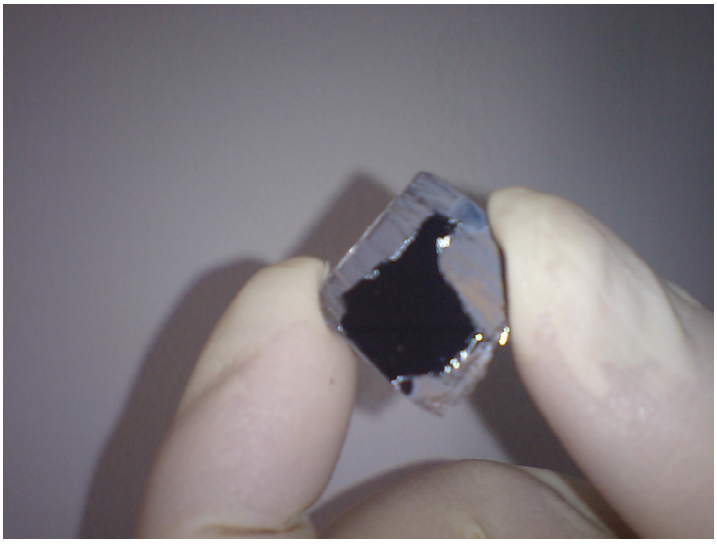


Figure 3. 23 Photograph of non-separated samples

showed high τ_{eff} as over 5 μs. However, these samples couldn't be separated from Mother silicon substrate at a rate of 90 %. Figure 3.23 shows the photograph of non-separated samples. In contrast, the (e) and (f) represent high anodization current in Step 3 and showed low effective carrier lifetime as (below 2 μs). Especially, (f) separated from Mother c-Si substrate before Layer Transfer. The (c) and (d) showed effective carrier lifetime as 4.1 μs 4.6 μs, respectively and these samples were successfully separated from Mother c-Si substrate.

The (d) was obtained as best condition through these experiments. Step 1: 5 mA/cm^2, Step 2: 20 mA/cm^2, Step 3: 250 mA/cm^2 at 1100 ˚C hydrogen annealing temperature. We calculated a value of the L_{eff} as 117 μm from the τ_{eff} as 4.6 μs using Eq. (2-7). This value of L_{eff} was enough longer than thickness of 15 μm c-Si foil. We could exceed calculated τ_{eff} as 2.9 μs in Chapter 2.

3.5 Discussion about the mechanism of SPS process conditions and characterization of c-Si foils

Figure 3.24 shows the mechanism of relationship between SPS process conditions and characterization of c-Si foils.

In case of high anodization current density in Step 1, lack of silicon atoms on the surface of Mother c-Si substrate are caused by high anodization current. This lack of silicon leads to crystal defects in the hydrogen annealing. This mechanism could be explained by small Raman peak sift in low anodization current density of Step 1.

In case of high anodization current density in Step 3, greater separation layer was caused by high anodization current density in Step 3. The reaction of closure porous-Si surface is caused by porous-Si as high potential energy condition moved to c-Si as low potential energy condition. Thus, migration of Si atoms is very important. The greater

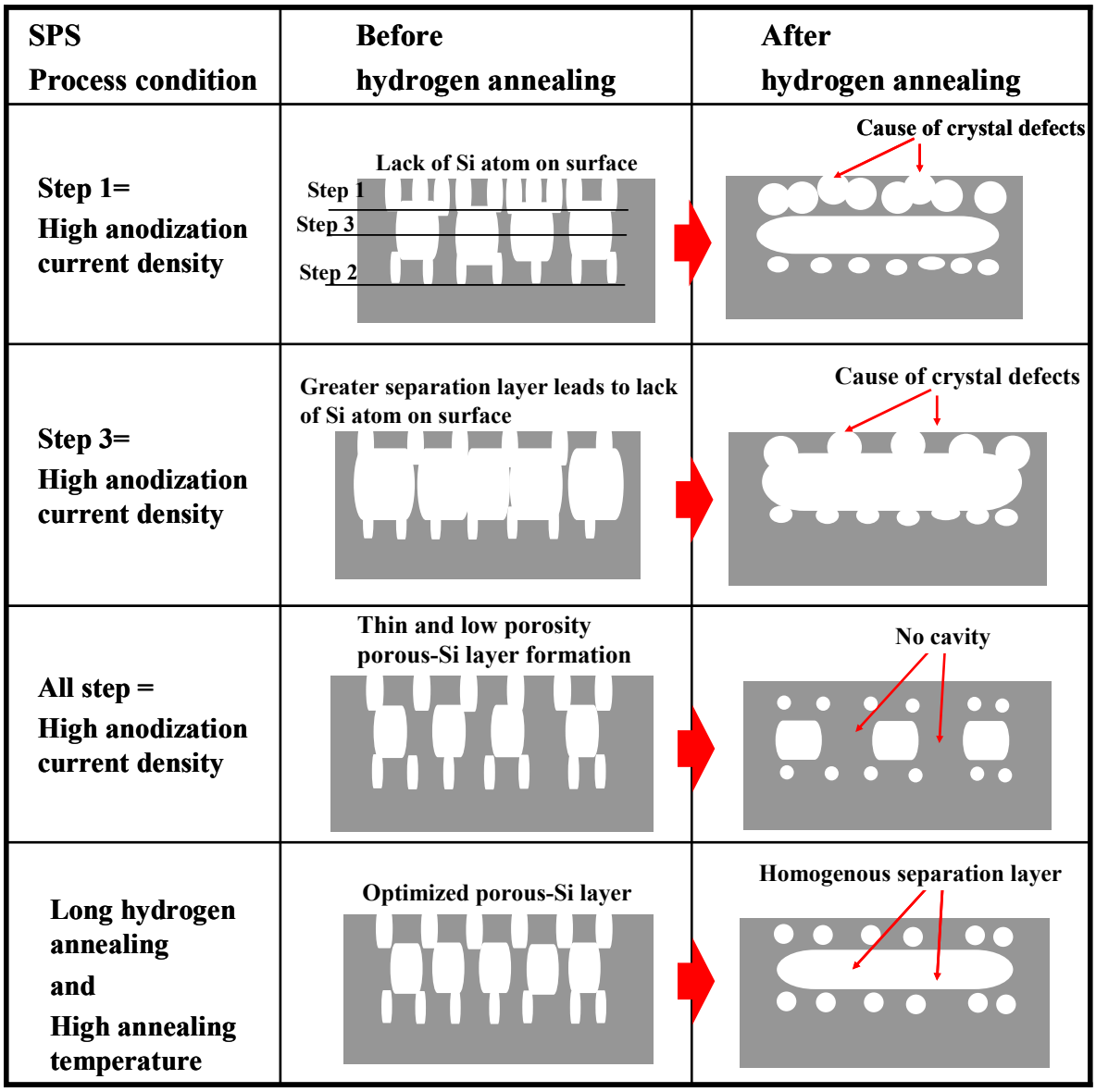


Figure 3.24 Mechanism of the relationship between SPS process conditions and characterization of c-Si foils

separation layer leads to the block of Si atoms migration on the surface of Mother c-Si substrate. The crystal defects are caused by greater separation. This mechanism could be explained by big Raman peak sift and low carrier lifetime in high anodization current density of Step 3.

In case of low current anodization current density in all step, thin and low porosity porous-Si layers are formed. Separation layer couldn't be formed enough, and epitaxially crystalline was grown on the most of Mother c-Si substrate. This mechanism could be explained by the close epitaxial c-Si layer in the Raman spectra and high carrier lifetime in low anodization current density condition. Additionally, under this condition, c-Si foils couldn't be separated from Mother c-Si substrate.

In case of long hydrogen annealing and high annealing temperature, Acceleration of migration of Si atom is caused by long hydrogen annealing and high annealing temperature. Too long hydrogen annealing time or too high annealing temperature is leads to perfect recrystallization or separation, respectively [11].

The characterization of epitaxial growth silicon layer depends on anodization and hydrogen annealing conditions. Thus, the characterization of epitaxial silicon layer is decided on the condition of restructured porous-Si surface after hydrogen annealing.

3.6 Summary

Layer Transfer using SPS process was demonstrated and optimized in this chapter. We got homogeneous three different porous-Si layers by improvement of anodization apparatus. On the quality of epitaxial growth silicon layer dependence on anodization and hydrogen annealing conditions, accompanying the anodization current of forming third porous-Si layer increase was a decrease in the crystal quality and effective carrier lifetime. And accompanying the annealing temperature increase was an increase in crystal quality and

minority carrier lifetime. However, we had to notice the yield rate of successful separation. We achieved minority carrier lifetime: 4.6 μs, which is over the required effective carrier lifetime (2.9 μs) in the chapter 2.

In chapter 5, 15 μm c-Si foil solar cell is produced by best condition of forming c-Si foils (first step: 5 mA/cm^2, second step: 20 mA/cm^2, third step 250 mA/cm^2 at 1100 ˚C). We used this condition for the formation of solar cell.

References Chapter 3

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Chapter 4

NH_3 plasma-treatment interface modification for SiN_X passivation at below 200 ℃

4.1 Introduction

To increase the efficiency the c-Si foil solar cell is needed to decrease the surface recombination, especially rear surface recombination, (in Chapter 2). In this thesis, c-Si foil solar cells using the SPS process are deposited epitaxialy on a silicon substrate wafer, from which the cell has to be transferred to a glass superstrate by high transparency glue before the rear side is processed. After separation, rear side passivation and contact fabrication process limits the maximum process temperature for fabrication of passivation layer and contacting the rear side to low temperature. For using plastic surperstrate in the future, I have to keep below 200 ℃ in the cell fabrication process after separation. In general, however, the surface passivation layer is deposited at around 400 ℃ for excellent passivation [1]. The improving conversion efficiency of c-Si foil solar cell is needed to suppress the effect of surface recombination by SiN_X passivation at 200 ℃ .

Other researchers reported that a metal-insulator-semiconductor field effect transistor (MISFEF) with SiN_X gate insulator had high field-effect mobility when the gate insulator was made by Plasma Enhanced Chemical Vapor Deposition (PECVD) after exposing the silicon surface to the NH_3 plasma [2]. However, nobody reported detailed analysis and evaluation of modified SiN_X/c-Si interface by NH_3 plasma-treatment. Especially, the report of the surface recombination velocity at modified SiN_X/c-Si interface for solar cell application has not been

investigated. I proposed NH_3 plasma-treatment technique before passivation layer deposition at low temperature. I thought that NH_3 plasma-treatment was applied to the deposition of SiN_X layer passivation at low temperature, and evaluated including surface recombination velocity at SiN_X/c-Si.

In this chapter, to modify the interfacial state by NH_3 plasma-treatment with SiN_X layer passivation at low temperatures (<200 ℃) and optimized NH_3 plasma-treatment conditions. In order to consider interface modification mechanism, the samples were measured by means of Fourier Transform Infrared Spectroscopy (FT-IR), Secondary Ion-microprobe Mass Spectrometer (SIMS) and X-ray photoemission spectroscopy (XPS). Furthermore, effective surface recombination velocity as a function of excess carrier density was investigated for p-type c-Si substrates passivated by SiN_X layer at low temperature [2], and I proposed new evaluation technique of effective surface recombination using Electroluminescence (EL) and analyzed the effect of NH_3 plasma-treatment.

4.2 Optimum NH_3 plasma-treatment conditions

2 Ωcm 150 μm and p-type Cz (100) c-Si wafer was used as substrate material. The wafers received a standard RCA clean. Prior to the deposition of passivation layer, we tried to modify interfacial state by NH_3 plasma (Table IV-I.). As the passivation layer, we applied SiN_X layer deposited by PECVD of plasma ratio frequency 13.56 MHz at a relative low temperature (100 – 300 ℃). In the SiN_X layer deposition, SiH_4 and NH_3 were used as source gas (Table IV-II.)[3]. The SiN_X layer deposition condition was same condition through this study are identical. Finally, silicon surface was modified by NH_3 plasma-treatment and deposited SiN_X layer on both sides of the samples (Fig.4.1). The temperature of NH_3 plasma-treatment is equal to the temperature of SiN_X deposition. The samples were characterized using μ-PCD and QSSPC τ_{eff} measurement techniques. Then in order to

consider interface modification mechanism, the samples were measured by means of FT-IR, XPS and SIMS.

μ-PCD measurements were carried out on each samples when the excess carrier density was 1.67×10^{16} cm^{-3}. The excess carriers are generated by 200 ns light pulse from a 904 nm diode laser with a pulse rate 1.6 kHz. 150 μm-thick c-Si wafers were used in order to increasing influence of surface recombination. The surface recombination becomes dominant recombination in c-Si wafer. The effect of passivation indicates sensitive.

Figure 4.2 shows the results of the SiN_X passivated samples in the temperature range from 27 to 300 ℃. In this result, at lower deposition temperatures (27 – 150 ℃) gave the τ_{eff} smaller than the sample deposited at 300 ℃. The reason would be that the samples were damaged by plasma and the SiN_X films were low quality due to low substrate temperature. As results shown in Fig. 4.2, NH_3 plasma-treatment increased the τ_{eff} dramatically (3 - 18 times) even the sample deposited at 100 ℃. In this time, NH_3 plasma-treatment conditions were the following : RF Power = 40 W, Gas Pressure = 80 Pa, Treatment Time = 5.0 min.

For the further investigations, NH_3 plasma-treatment was optimized through varied treatment conditions. Figure 4.3 shows the relationship between τ_{eff} and RF Power at 100 ℃, 80 Pa, and 5.0 min treatment condition. In the lower region, the τ_{eff} increased with the increase of RF Power and reached the maximum when RF Power was set at 80 W. In contrast, the τ_{eff} drastically decreased when the RF Power greater than 100 W which probably due to the plasma damage.

Figure 4.4 shows the relationship between τ_{eff} and Gas Pressure at 100 ℃, 40 W, and 5.0 min treatment condition. The results illustrated that higher τ_{eff} were obtained when the Gas Pressure was more than 60 Pa. The τ_{eff} was lower with the lower gas pressure (40 Pa) because of the effect of interface modification fell off at the low NH_3 density and the higher plasma damage.

Table IV-I. Interface modification NH_3 plasma-treatment condition

Parameters	Values
NH_3 flow rate [sccm]	200
RF Power [W]	20 - 150
Gas Pressure [Pa]	40 - 120
Treatment Time [min]	0 - 10.0
Substrate Temperature [℃]	100 - 300

Table IV-II. SiN_X passivation layer deposition parameters

Parameters	Values
SiH_4 flow rate [sccm]	50
NH_3 flow rate [sccm]	80
RF Power [W]	40
Gas Pressure [Pa]	80
Thickness [nm]	200
Substrate Temperature [℃]	27-300

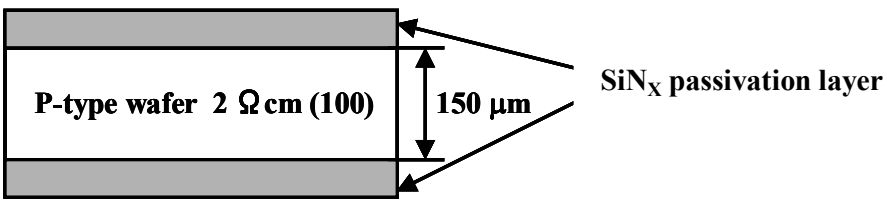

Figure 4.1 Schematic of deposited sample for lifetime measurement

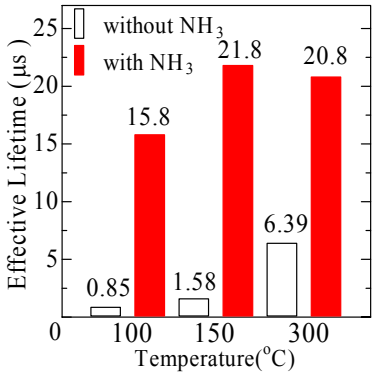

Figure 4.2 Effective lifetime of SiN_X passivated samples with and without NH_3 plasma-treatment

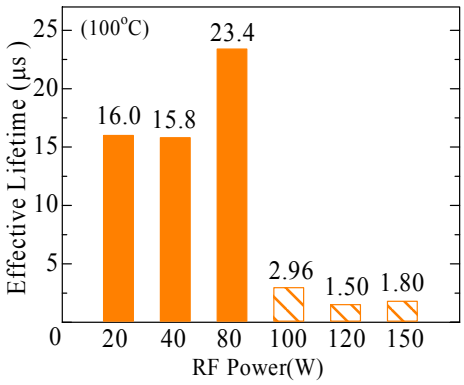

Figure 4.3 Effective lifetime as a dependence of the RF power

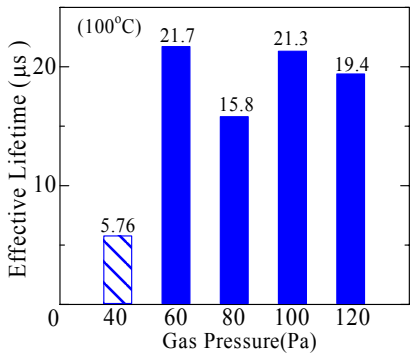

Figure 4.4 Effective lifetime as a dependence of the gas pressure

Figure 4.5 illustrates the relationship between the τ_{eff} and Treatment Time 100 ℃, 40 W, and 80 Pa treatment condition. The results indicate that the τ_{eff} increased with the increase of Treatment Time and got saturated at Treatment Time = 8.0 min.

In the previous results, only one parameter was varied, while the others were kept constant. Generally, it is possible to improve the τ_{eff} when more than two parameters are varied. From the results shown in Fig. 4.3, if the plasma damage could be prevented, the τ_{eff} should increase with the increase of RF Power. However when they are low gas pressure and high RF power, superfluous RF power for the formation of NH_3 plasma induce bigger plasma damage. Thus, the high gas pressure which has higher amount of NH_3 molecules could protects c-Si substrate from plasma damage.

The relationship between τ_{eff} and Gas pressure at high RF powers was shown in Fig. 4.6. In this result, the effect of NH_3 plasma-treatment improved the τ_{eff} dramatically and obtained the maximum value = 32.4 μs when the parameters were following: RF Power = 120 W, Gas Pressure = 100 Pa, Treatment Time = 8.0 min, Substrate Temperature =100 ℃. The optimized condition exhibits about 38 times improvement when compared to the standard condition without NH_3 plasma-treatment. From these results, optimize condition is decided by the balance of plasma damage and interface modification (nitriding reaction or hydrogenation). Thus, the improvement of τ_{eff} is caused when the reaction of interface modification is superior condition.

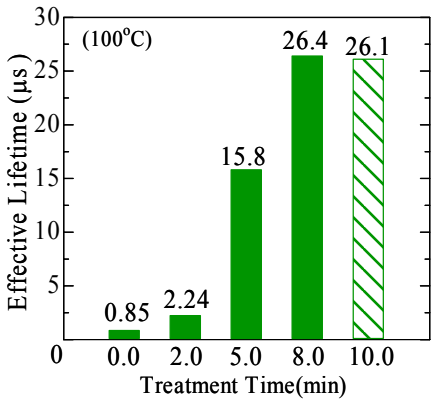

Figure 4.5 Effective lifetime as a dependence of treatment time

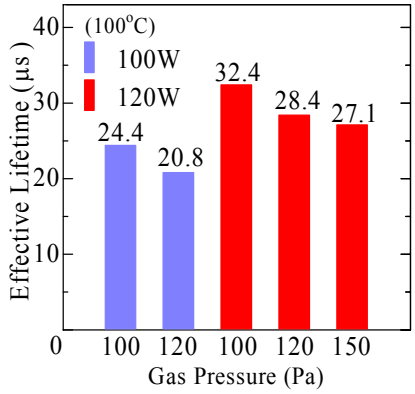

Figure 4.6 Effective lifetime when the higher RF power and Gas pressure

4.3 Analysis of NH_3 plasma-treatment modified interface

In order to verify the NH_3 plasma-treatment mechanism, the samples were analyzed by the FT-IR, SIMS and XPS measurements. Figure 4.7 shows FT-IR spectra with or without NH_3 plasma-treatment for various temperatures. There was difference of SiN_X layer quality depending on temperature. However there was no significant difference of SiN_X layer quality between with and without NH_3 plasma-treatment at each temperature. These spectra reflect layer properties. NH_3 plasma-treatment doesn't effect a change of SiN_X layer quality.

Then, we analyzed passivation layer/c-Si interface. Since there are much hydrogen and nitrogen contents in the SiN_X layer. For sensitive SIMS and XPS measurement, the SiO_X was used for passivation layer when the measurement of hydrogen content at the interface was performed. SiO_X layer deposition conditions were the following : SiH_4 flow rate = 30 sccm, N_2O flow rate = 300 sccm, N_2 flow rate = 300 sccm, RF Power = 50 W, Gas Pressure = 66.5 Pa, Thickness = 50nm, Substrate Temperature = 100 ℃. The SIMS spectra with or without NH_3 plasma-treatment were illustrated in Fig. 4.8 and 4.9. From the result of Fig. 4.8, the higher hydrogen content obtained from the NH_3 plasma-treatment samples. This is probably due to this hydrogen passivated Silicon dangling bond sites. In contrast, as shown in Fig. 4.9, the tremendous decrease of carbon content with NH_3 plasma-treatment indicates that this treatment has the effect of carbon cleaning [4]. These results of SIMS and FT-IR indicated the interface of passivation layer and c-Si was hydrogenated and cleaned by NH_3 plasma-treatment. SiO_X layer passivated sample with NH_3 plasma-treatment also showed high τ_{eff} (16.1 μs) compared with τ_{eff} (0.45 μs) of SiO_X layer passivated sample without NH_3 plasma-treatment. Thus, this could be said that the τ_{eff} improvement would be caused by the change of interfacial state resulted from the NH_3 plasma-treatment.

Figure 4.10 shows the XPS spectra in SiO_X layer passivated samples. The XPS spectra results confirmed that nitrogen atom existed on SiO_X/c-Si interface by NH_3

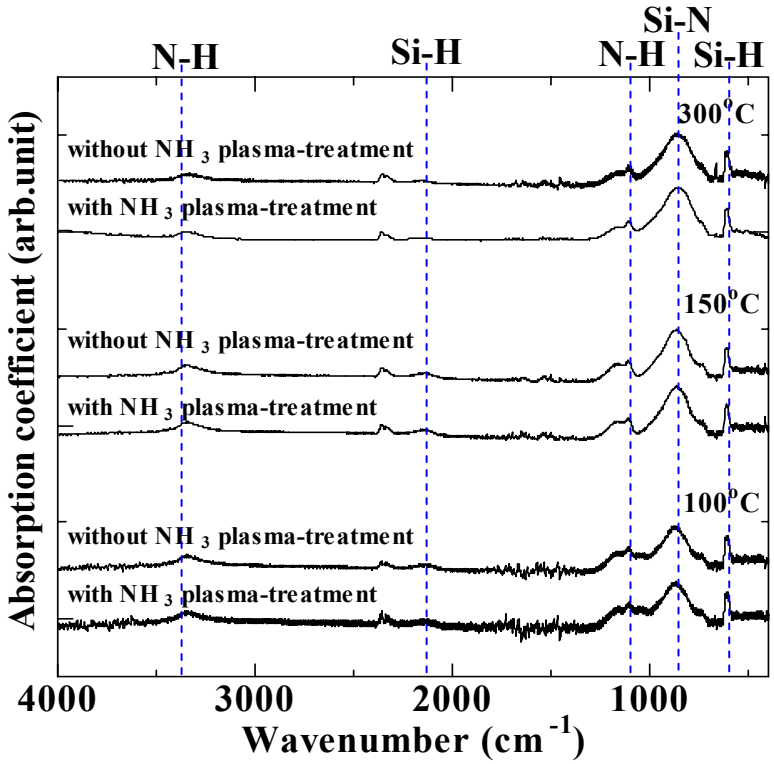

Figure 4.7 FT-IR spectra with or without NH_3 plasma-treatment SiN_X layer

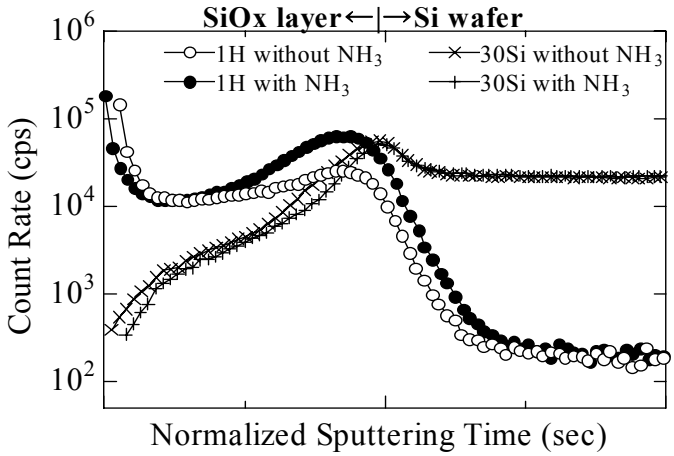

Figure 4.8 SIMS profiles of hydrogen content analysis

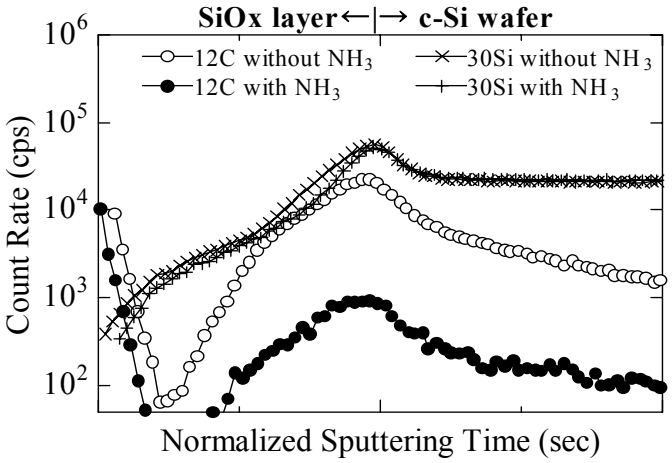

Figure 4.9 SIMS profiles of carbon content analysis

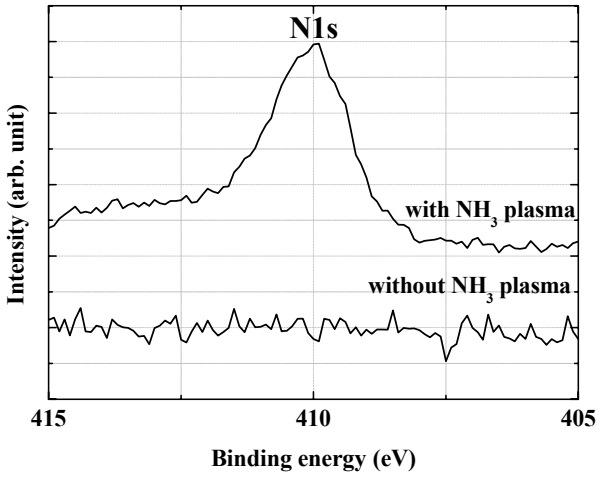

Figure 4.10 N1s XPS spectra in SiO_X layer samples

plasma-treatment. It is possible that nitrogen leads to nitride the silicon surface. Interface modification would be caused by the collaboration of nitriding, hydrogenation and carbon cleaning.

4.4 Surface recombination velocity at SiN_X/c-Si interface

For further study, NH_3 plasma-treatment technique was applied to SiN_X passivation. 2 Ωcm 300μm and p-type Fz (100) c-Si wafer was used as the substrate material for SiN_X passivation samples. QSSPC measurements were carried out on SiN_X passivation samples of the optimized plasma-treatment conditions (the parameters were the following: RF Power = 120 W, Gas Pressure = 100 Pa, Treatment Time = 8.0 min, Substrate Temperature =200 ℃) and non plasma-treatment conditions. Figure 4.11 shows τ_{eff} of SiN_X layer passivation in the dependence on excess carrier density. In these results, the τ_{eff} improved dramatically with Cz silicon material and Fz silicon material. In order to determine the surface passivation quality, the effective surface recombination velocity at the SiN_X/c-Si interfaces was calculated according to Eq.(2-7). Figure 4.12 shows S_{eff} of SiN_X layer passivation in the dependence on excess carrier density. In Fig. 4.12, SiN_X passivated sample with NH_3 plasma-treatment showed below 100 cm/s in the region of excess carrier density from 10^{14} to 10^{16}, especially, 20 cm/s as the excess carrier density of $1.0\times10^{15}cm^{-3}$ In contrast, SiN_X passivation without NH_3 plasma-treatment showed over 5000 cm/s as the excess carrier density of $1.0\times10^{15}cm^{-3}$. The S_{eff} could be reduced to below 100 cm/s using Fz c-Si wafers. Kerr and Cuevas [5] or Dawe [6] reported the S_{eff} as below 10 cm/s (Δn :$1.0\times10^{15}cm^{-3}$) of excellent SiN passivation with the deposition temperature at over 300 ℃ In spite of low temperature as 200 ℃, S_{eff} = 20 cm/s can be obtained which proved a good passivation.

Finally, SiN_X layer was deposited on 15 μm c-Si foil with NH_3 plasma-treatment in section 3.6.2. Figure 4.13 shows effective carrier lifetime of SiN_X passivated 15 μm c-Si foil.

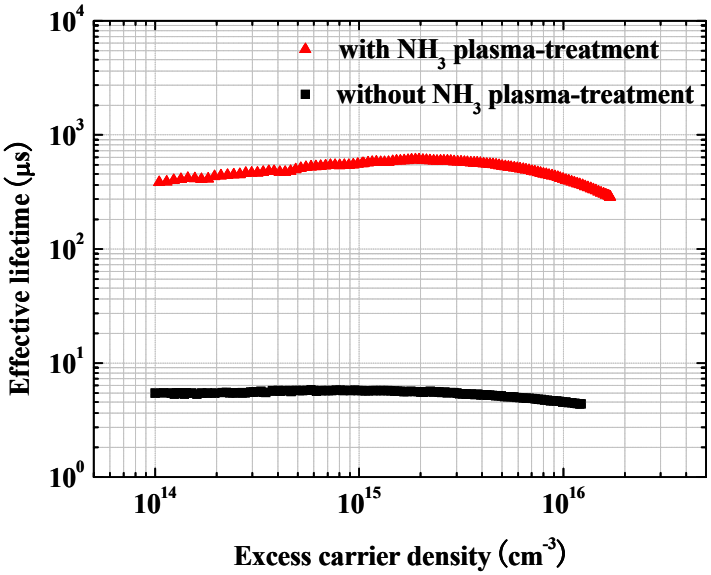

Figure. 4.11 Effective lifetime of SiN_X passivation samples dependence on excess carrier density.

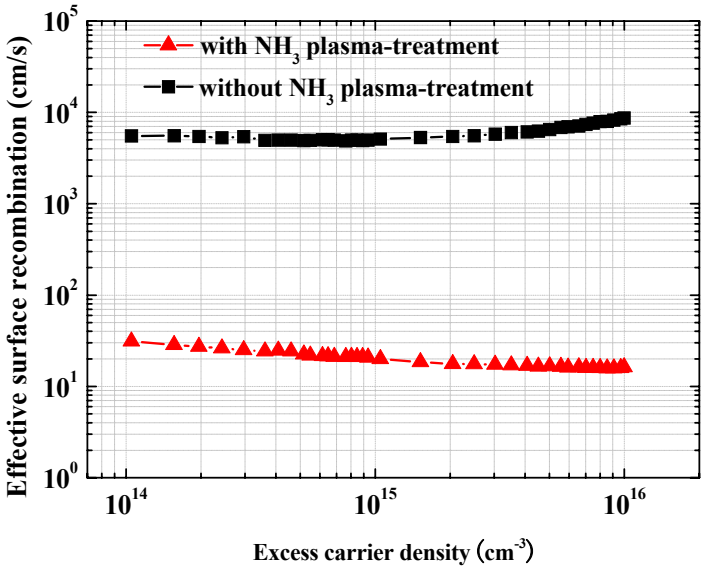

Figure. 4.12 Effective surface recombination velocity of SiN_X passivation samples dependence on excess carrier density.

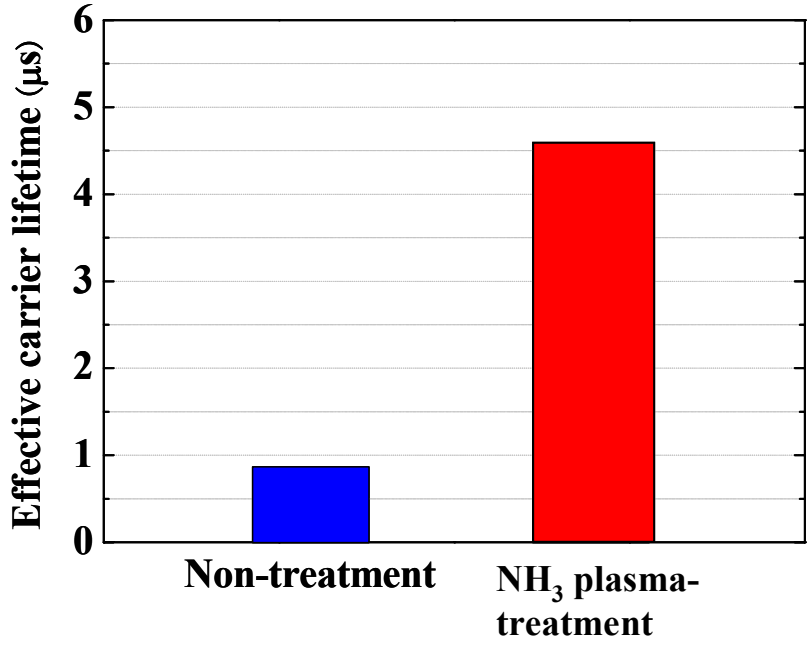

Figure. 4.13 Effective lifetime of SiN passivated 15 μm c-Si foils measured by μ-PCD

This illustrated that NH_3 plasma-treatment was also particularly useful for c-Si foils.

4.5 Evaluation of Surface recombination using EL

The reduction of surface recombination is essentially important and the precise evaluation of surface recombination velocity is needed to develop high efficiency cells. Conventional analysis technique using the spectral response [7] needs long measuring time, and is hard to achieve spatial distribution. Thus, The EL technique a new evaluation technique of surface recombination in c-Si cells, was proposed and demonstrate that the analysis of EL intensity can reveal the surface recombination velocity quantitatively since the minority carrier number in base region is sensitively affected by the rear surface recombination.

The schematic measurement setup is shown in Fig. 4.14, and explained in detail elsewhere [8]. A sample cell biased at an appropriate forward voltage emitted infrared light (λ= 900 to 1300 nm) which was collected by the cooled (at around -50 ℃) c-Si CCD camera using a selected objective lens. The CCD had 512 x 512 pixels. The spatial resolution depended upon optical lens system, and the resolution limit became about 10μm in length.

The photographic measurement of EL has been proposed a new evaluation technique of S_{rear} on base layer surfaces of cells. If we assume that the bulk minority carrier diffusion length (L_b) is constant in single crystalline c-Si solar cells and much longer than cell thickness, the number of minority carriers is considered to be sensitively affected by S_{rear}. The EL intensity is proportional to the total number of the minority carriers in base layers [8], then, EL intensity should has strong correlation with S_{rear}.

I demonstrate the validity of evaluation method of S_{rear} using EL for several kinds of passivation techniques experimentally. Figure 4.15 shows the structure of sample c-Si solar cell especially configured to measure the surface recombination velocity, S_{rear}, (the top surface in Fig.4.15). It should be noted that the structure was devised to measure the surface

recombination velocity on p base layer, and so, the ohmic electrode (Ti/Ag) fully covered emitter layer (the bottom n^+ c-Si layer in Fig.4.15) for homogeneous excess carrier injection without the influence of series resistance. The substrate was c-Si (Cz) p-type (2 Ω cm) wafer, and the cell thickness was 110μm. The value of bulk diffusion length L_b was around 800 μm and much longer than the cell thickness, so, the effective diffusion length L_{eff} depended markedly on S_{rear}. The cell area was 1.0 cm^2. The grid contact was fabricated on p base layer to detect the emitted light.

The surface of p-type base layer was passivated by the conventional methods which practically used in the present cell fabrication processes as shown below;

(i) 10 nm thin thermal SiO_2 covered by plasma PECVD-SiO_X

(ii) PECVD-SiO_X

(iii) PECVD-SiN_X

(iv) Non passivation as a reference

The deposition temperature by PECVD was 200 − 300 ℃, and 10nm thermal SiO_2 was grown at 800℃. Thickness of each passivation layer was 200 nm.

Figure 4.17 shows the typical distribution of the EL intensity in the case of the cell with thin thermal SiO_2 /PECVD-SiO_X under forward current density of 20mA/cm^2. The EL intensity was expressed with gray scale in the range of 0 - 3250 in an arbitrary unit. The EL intensity was uniform as expected in c-Si substrate, and finger electrodes were clearly shown in black stripes.

The obtained average EL intensity of each cell ((i) – (iv)) at the same forward current (25 mA/cm^2) was as follows. (i) Thin thermal SiO^2 /PECVD-SiO_X : 2000. (ii) PECVD-SiO_X : 1400. (iii) PECVD-SiN_X : 1800. (iv) non-passivation : 1200.

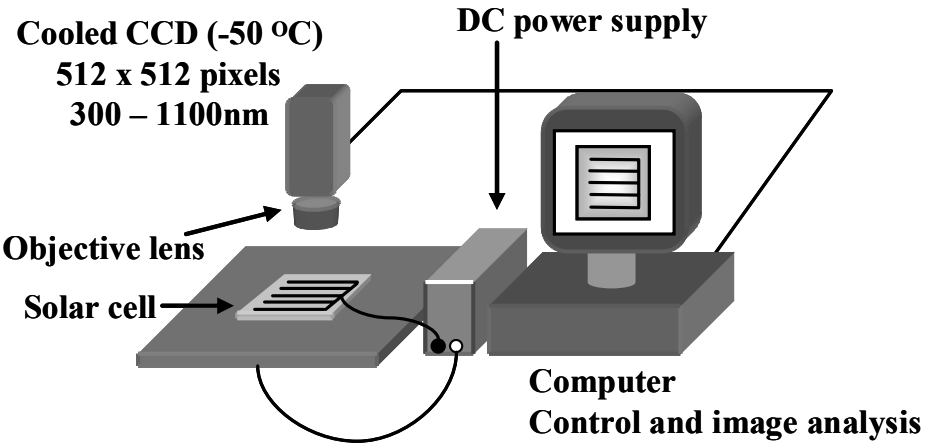

Figure 4.14 Schematic viewgraph of experimental apparatus.

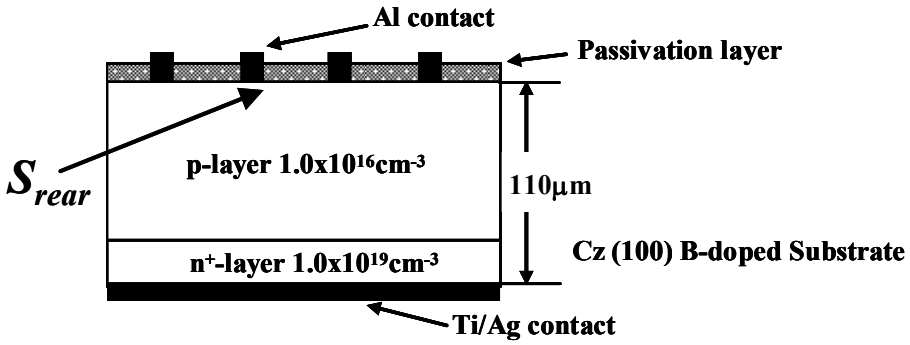

Figure 4.15 Test cell structure configured for the analysis
of surface recombination velocity on p base layer of cell.

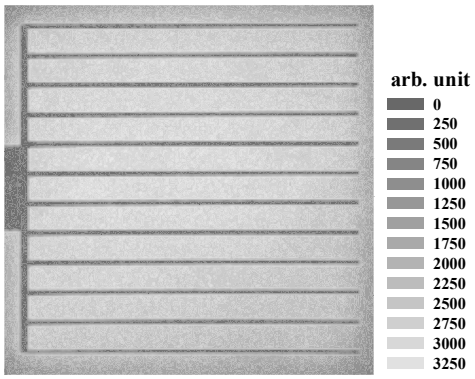

Figure. 4.16 Emission intensity distribution of EL for the cell with a passivation layer of thermally grown SiO_2/PECVD SiO_X

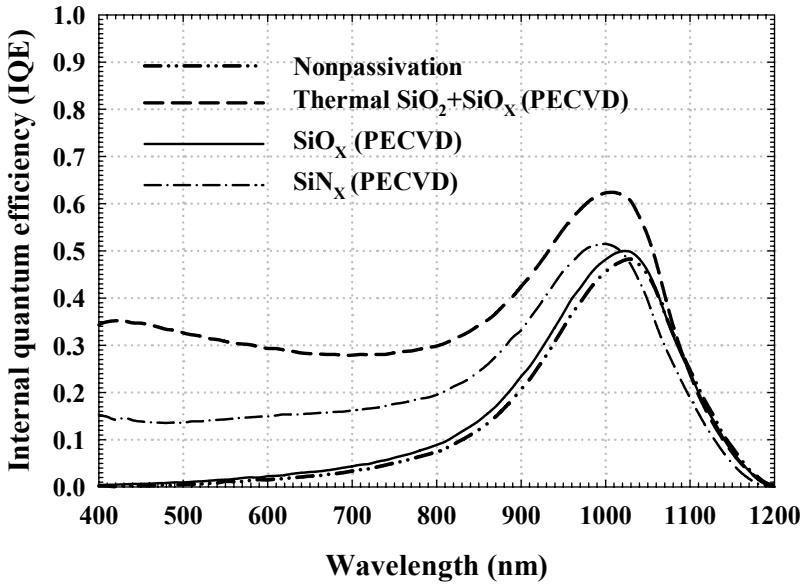

Figure. 4.17 Internal quantum efficiency (IQE) spectra for the cells with different passivation layers.

The forward current (25 mA/cm^2) to measure EL was set at almost the same value of short circuit current density under 1 sun irradiation for the typical n^+/p Si structure cell fabricated using the same process.

Figure 4.17 shows the internal quantum efficiency (IQE) spectra for the four types ((i) − (iv)) of cells. IQE in the wavelength region of 400 ～ 900 nm was considered to be affected by S_{rear} on p base layers since the light was irradiated through the top surface as shown in Fig. 4.15. The L_{eff} was derived by plotting IQE against the penetration depth α [9],

$$IQE^{-1} = 1 + \frac{1}{\alpha \cdot L_{eff}} \tag{4–1}$$

$$L_{eff} = L_{bulk} \cdot \frac{1 + \left(\frac{S_{rear} L_{bulk}}{D}\right) \tanh\left(\frac{W}{L_{bulk}}\right)}{\left(\frac{S_{rear} L_{bulk}}{D}\right) + \tanh\left(\frac{W}{L_{bulk}}\right)} \tag{4–2}$$

The values of S_{rear} and L_{eff} were calculated by fitting the experimental data using equations (1) and (2).[10-12] The values of cell thickness, W, diffusion constant, D, and L_{bulk} were 110 μm, 0.003 m^2/s and 800 μm, respectively, for each cell since the sample cells were fabricated using the same Si wafers. The value of τ_{bulk} was measured by the μ-PCD. The value of L_{bulk} is 800 μm which can be calculated from the τ_{bulk} = 180 μs by Eq. (2-3)

Table IV-III shows L_{eff} and S_{rear} of four types of cells. The longest L_{eff} of 770μm was achieved in the (i): thermal SiO_2 /PECVD-SiO_X case compared with the minimum value of 470 μm for the (iv): Non-passivation case. The experimentally derived L_{eff} was much longer than the cell thickness (110 μm) for every sample, which reflected that the obtained L_{eff} was related directly with S_{rear} following the Eq.(4-2).

The relationship between EL intensity and S_{rear} was analyzed quantitatively as shown in Fig. 4.18. The EL intensity had one to one dependence upon the value of S_{rear}. The value of

S_{rear} increased with decreasing the EL intensity. The EL intensity was proportional to the number of minority carriers in p-type c-Si base layer.[8] The number of minority carrier decreased with increasing S_{rear}, then the EL intensity decreased with increasing S_{rear}. When the samples of thin thermal SiO_2/PECVD-SiO_X cell and PECVD-SiN_X were compared, the difference in S_{rear} was only 10 cm/s. However, the difference in EL intensity was 200, which proved that EL method was very sensitive to evaluate the surface recombination velocity quantitatively. In c-Si solar cells with L_{eff} larger than cell thickness, the number of minority carriers was sensitively affected by S_{rear}. Therefore, S_{rear} could be estimated from the EL intensity quantitatively. The proposed technique was very useful to evaluate surface passivation effect, especially for very thin c-Si cell.

SiN_X passivated c-Si solar cell samples (in Fig 4.16) with and without NH_3 plasma-treatment could be analyzed using this EL image evaluation. S_{rear} were obtained from IQE. In the samples without NH_3 plasma-treatment, the value of S_{rear} showed 2380 cm/s and EL intensity indicated 1350. In contrast, the value of S_{rear} showed 127 cm/s and EL intensity indicated 4300 in the samples with NH_3 plasma-treatment.

Table IV-III. Effective diffusion length and surface recombination velocity for the cells passivated using different methods.

Passivation layer	L_{eff} (μm)	S_{rear} (cm/s)
Nonpassivation	470	1100
Thermal SiO_2	780	490
SiO_2 (PECVD)	540	780
SiN (PECVD)	770	500

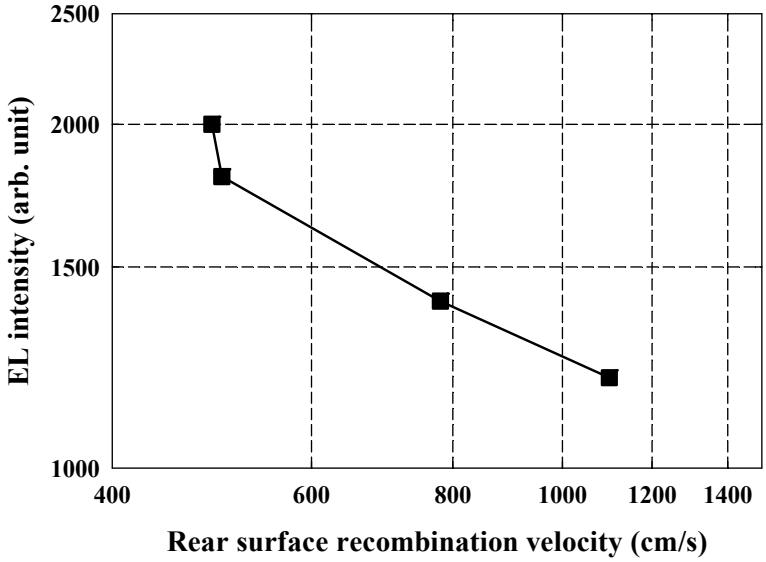

Figure. 4.18 Emission intensity of EL as a function of S_{rear} on p base layer.

4.6 Summary

The p-type c-Si material was exposed to the NH_3 plasma before depositing the SiN_X, and SiO_X passivation layer in a PECVD system, respectively. The τ_{eff} of the samples with NH_3 plasma-treatment was superior to the samples without NH_3 plasma-treatment regardless of the low deposition temperature. Moreover, the SIMS measurement results indicated the change of Hydrogen and Carbon on silicon surface with and without NH_3 plasma-treatment. It is possible that NH_3 plasma-treatment cause hydrogenation and carbon cleaning on silicon surface. And the XPS spectra results confirmed that nitrogen atom existed on passivation layer/c-Si interface by NH_3 plasma-treatment. Interface modification would be caused by the collaboration of nitriding, hydrogenation and carbon cleaning.

Finally, SiN_X pasivated sample with NH_3 plasma-treatment at 200 ℃ showed below 100 cm/s in the region of excess carrier density from 10^{14} to 10^{16} cm^{-3},especially, 20 cm/s as the excess carrier density of $1.0 \times 10^{15} cm^{-3}$

The EL technique has been proposed as a new evaluation technique of surface recombination velocity in c-Si solar cells. The S_{rear} could be estimated from the EL intensity quantitatively. Thus, the EL intensity had a tight one to one correlation with S_{rear}. The proposed technique was very useful to evaluate surface passivation effect, especially for very thin c-Si cell.

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Chapter 5

Development of rear passivated type c-Si foil solar cells with Laser Fired Contact

5.1 Introduction

The important key issues for high efficiency c-Si foil solar cells are front and rear surface passivation. However c-Si foil solar cells based on transfer technique have not been strongly studied about the passivation of rear surface because the difficulty of processing on rear side after separation. This process limitation is the maximum process temperature for fabrication of passivation layer and contacting the rear side to below 200 ℃. Only Plagwitz et al. demonstrated Symmetric-COSIMA PSI process. They applied COSIMA process as a-Si:H passivation and front and rear side contacting at around 300 ℃ to PSI cell [1].

For improvement of high efficiency c-Si foil solar cell, we have to solve two issues on the view point of solar cell structure and fabrication process. They are passivation technique and rear contact fabrication at below 200 ℃.

In previous chapter, we developed passivation effects of SiN_X increased by NH_3 plasma-treatment before passivation layer deposition. We solved one of the issues in high quality passivation at below 200 °C. And so, recently, Schneiderlochner et al. developed LFC process gathers mach attention in the view of low temperature process for passivated rear side contact fabrication [2]. In LFC process, aluminum layer for rear side contact is evaporated directly onto the passivation layer and then fire it through the passivation layer with a laser

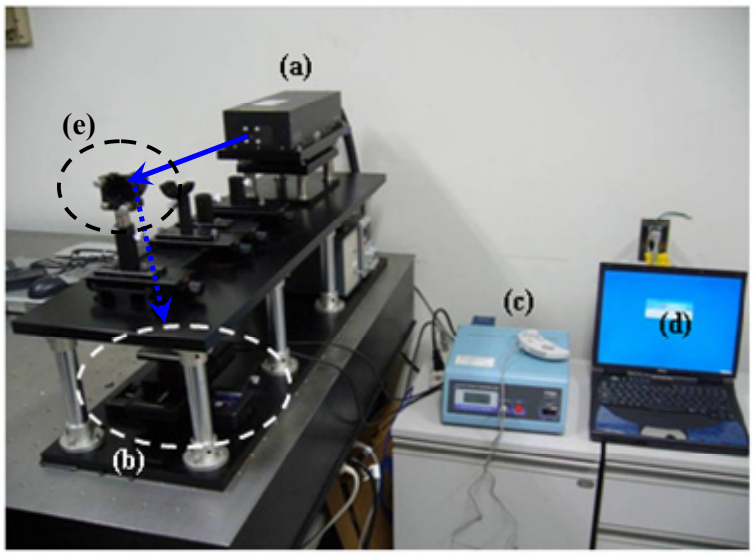
into the underlying silicon to form the local contacts. Thus the rear side contact could possibly be fabricated at room temperature.

In this chapter, we proposed LFC-SPS cell (Fig.1.6), and applied LFC to c-Si foil solar cell to solve the other issue as the processing rear side contact at below 200 ℃. Consequently, the fabrication process of c-Si foil solar cell using SPS process developed and optimized. All solar cells have SiN_X layer on the front surface without texturing in this chapter.

5.2 Optimization of LFC process

5.2.1 Laser system for LFC process

Figure 5.1 illustrated photograph of laser system used in this study which consists of 355nm pulsed Nd^{3+}: YAG laser (AVIA Ultra 355, Coherent Co.), automatic controlling X-Y stage (Sigma Koki Co.), X-Y stage controller (Mark-202, Sigma Koki Co.), reflect mirrors (Sigma Koki Co.) and a computer for automatic controlling. The c-Si foil solar cells as 15 μm-thick is very thin. Thus the short wavelength laser was used for shorter penetration depth. Figure 5.2 shows the simple sketch of laser system used in this study. The repetition frequency of the laser can be varied from 1k Hz to 50k Hz. Laser spot diameter and move speed of X-Y stage were 50μm and 10 mm/s respectively. Schneiderlochner et al. used 1064 nm YAG laser with q-switch in LFC process. However we used 355 nm Nd^{3+} YAG laser which is shorter penetration depth in the Silicon than 1064 nm YAG laser.



→ Laser beam path

(a) : Nd^{3+}:YAG laser

(b) : x-y stage

(c) : x-y stage controller

(d) : computer of control

(e) : reflecting mirror

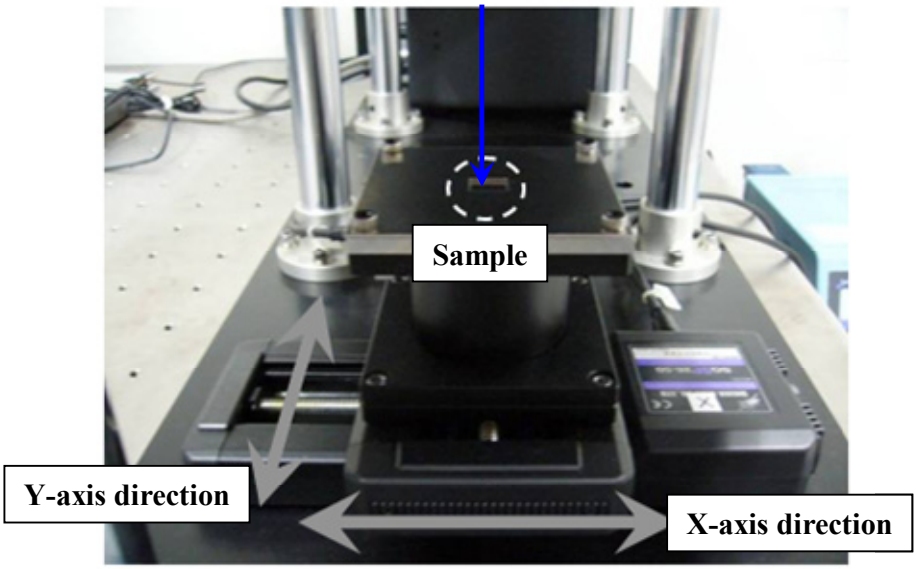


Figure 5.1 Photograph of 355nm Nd^{3+} YAG laser system used in this study

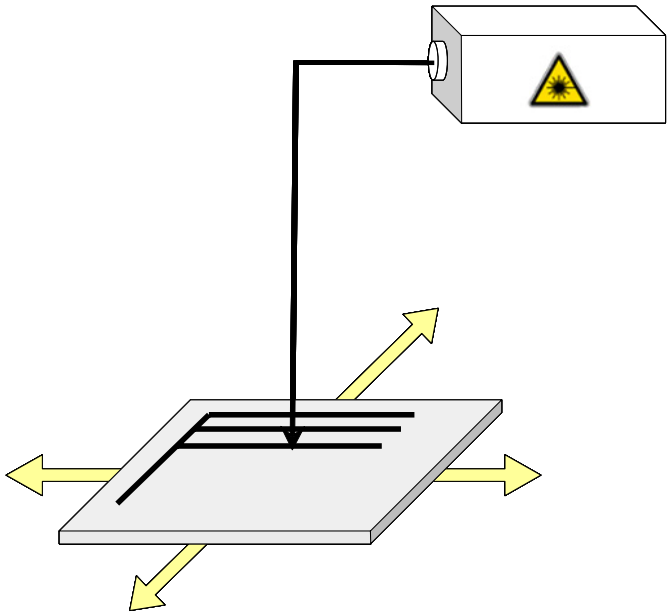


Figure 5.2 The sketch of 355nm Nd YAG laser system

5.2.2 The structure and fabrication of total resistance samples and bulk type LFC cells

The solar cell performance of LFC cell strongly depends on laser parameters [3-4]. Firstly, we fabricated and analyzed total resistance measurement samples and Bulk type LFC cell for LFC process parameter optimization. Both samples were used as the substrate: (100) p-type Fz c-Si wafer 300 μm thickness, 1.0 x 1.0 cm^2, 2 Ωcm. After optimization of LFC process, the LFC-SPS cell was formed by optimized LFC process parameter.

In the Bulk type LFC cell sample (in Fig. 5.3): after fabrication of pn junction, 100 nm SiN_X layer was deposited on rear side by PECVD, 1 μm aluminum layer was deposited on the rear SiN_X layer. Figure 5.4 shows structure of Bulk type LFC cell. For the evaluation of the rear contact resistance without other influence (junction, front contacts, etc.), the total resistance samples (in Fig. 5.5) were also produced by LFC process. All samples used identical resistivity wafers and front contact fabrication process.

In the total resistance sample: 1 μm-thick aluminum layer was evaporated on both sides after passivation of rear surface with 100 nm SiN_X layer. Finally the total resistance of each samples was measured by applying bias varied from -0.6 to 0.6 V (in Fig. 5.5).

Schneiderlochner et al. proposed LFC process formed point local contact. However, our contact shape is not point but stripe for simply controlling in Fig. 5.6. In this study, spacing of stripes were designed to 650 μm. Laser irradiation parameters for both samples were with varied pulse energy from 0.0077 to 0.024 mJ/pulse at below 15 kHz. The computer controlling of X-Y stage. The laser irradiation area was 10 % of full rear surface. Figure 5.7 shows Normarski image of stripe contact by LFC process. Most of irradiated areas were melted.

5.2.3 The results of contact resistance and bulk type LFC cells

Figure 5.8 show the total resistance of LFC with SiN_X passivation as a function of pulse energy. Total resistances of each sample have difference value. Compare with 2 Ω cm Fz c-Si material, 0.024 mJ/pulse sample indicated same values. We predicted this laser firing locally alloys aluminum in to the silicon, reducing the total resistance [5]. In contrast, 0.015 mJ/pulse and 0.02 mJ/pulse samples gave higher resistance. This reason is insufficient fabrication of rear contact. Current-voltage characteristics of the Bulk type LFC cell were measured under AM.1.5, 100mW/cm^2 illumination. The solar cell performance of Bulk type LFC cell as a function of laser pulse energy is shown with Bulk normal cell using same process for a reference in Fig. 5.9. The open circuit voltage (V_{OC}) showed slightly dependence on the laser pulse energy. However, the fill factor (F.F.) and the short circuit current density (J_{SC}) showed greatly dependence on the laser pulse energy. Both F.F. and J_{SC} showed a peak at 0.024 mJ/pulse. These results are indeed consistent with the result of Fig. 5.8. The low total resistance sample condition shows the high values of F.F. and J_{SC}.

Finally, Bulk type LFC cell sample with 0.024 mJ/pulse were achieved highest conversion efficiency by influences of both F.F. and J_{SC}. However F.F. could not reach over 0.7 and conversion efficiency of Bulk type LFC cell shows lower in comparison with Bulk normal cell.

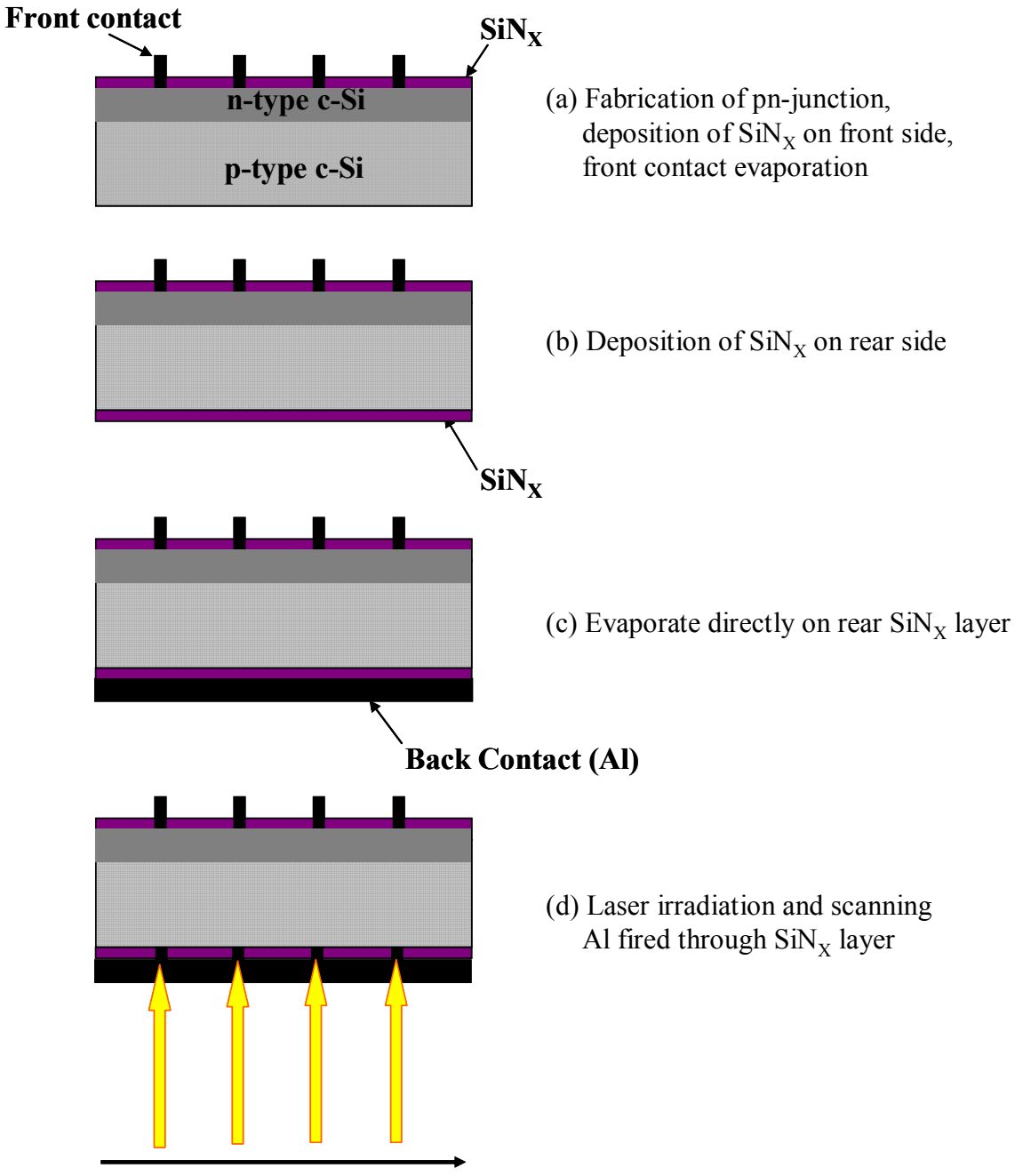


Figure 5.3 Process scheme of LFC

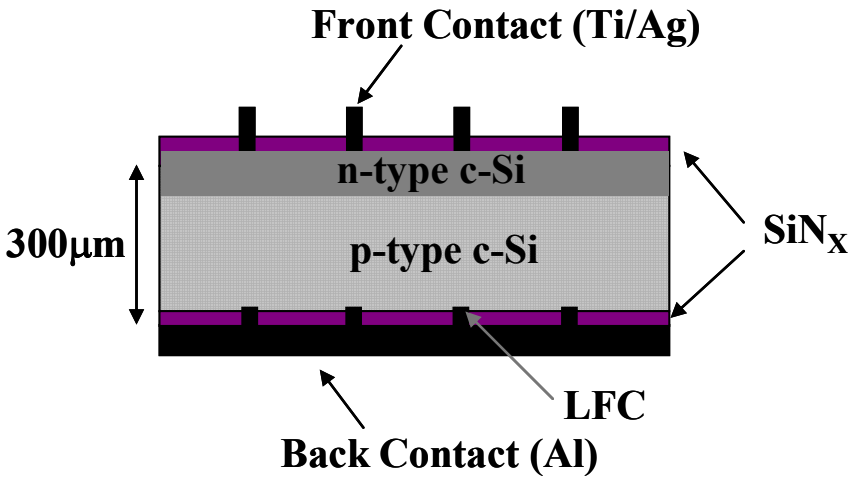


Figure 5.4 The structure of Bulk type LFC cell

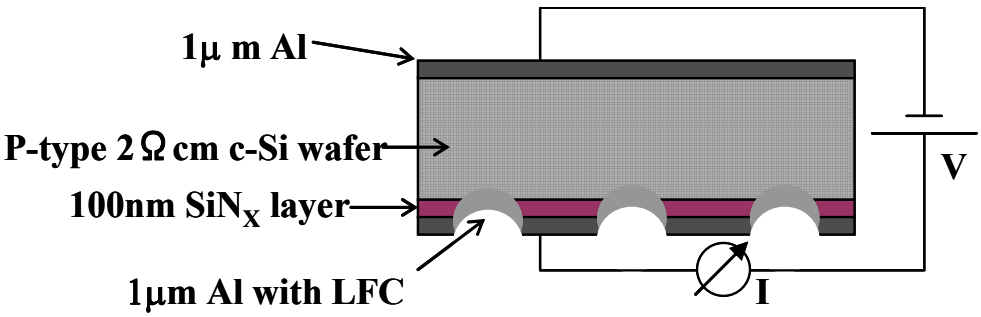


Figure 5.5 The structure of contact resistance samples

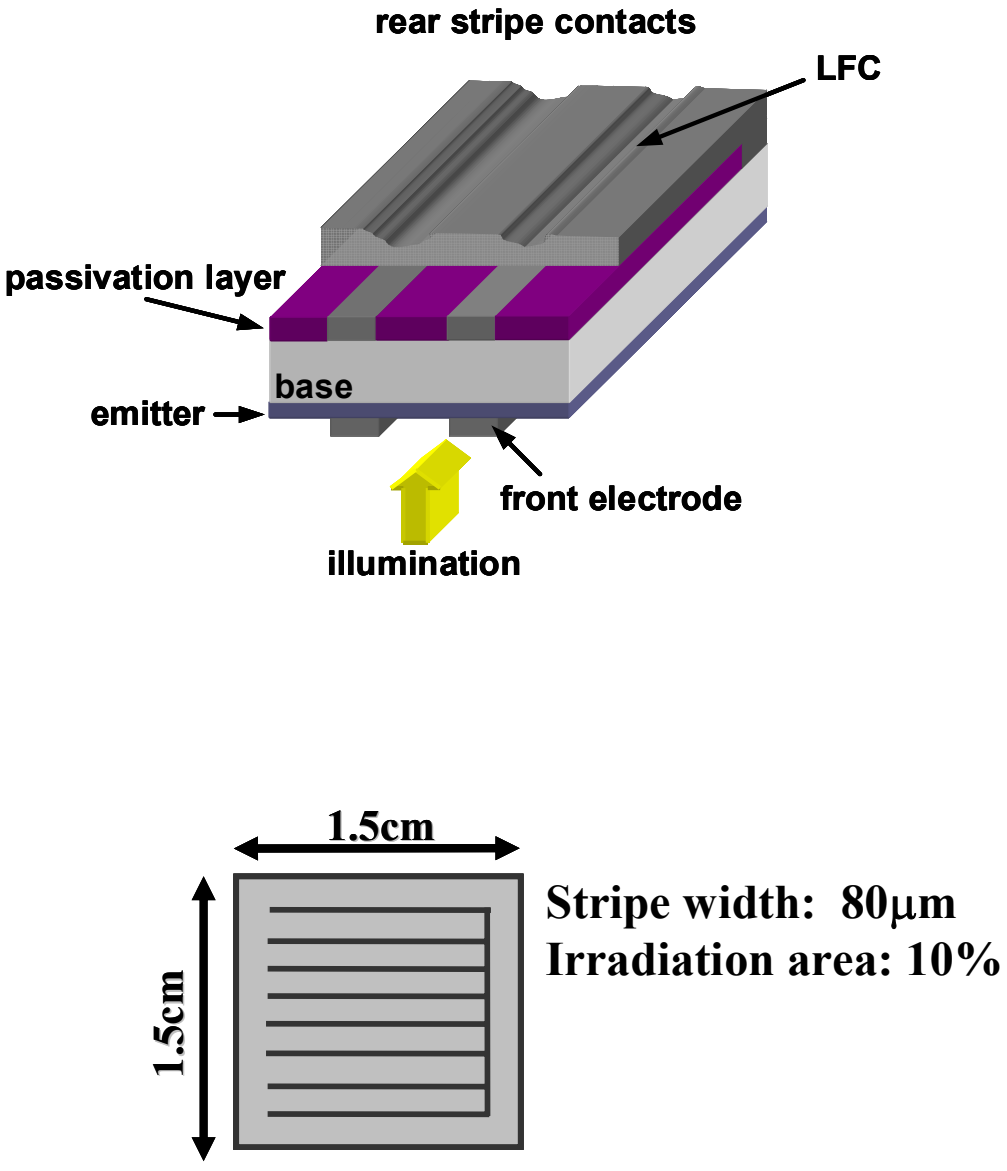


Figure 5.6 The sketch of LFC structure and stripe backside contact

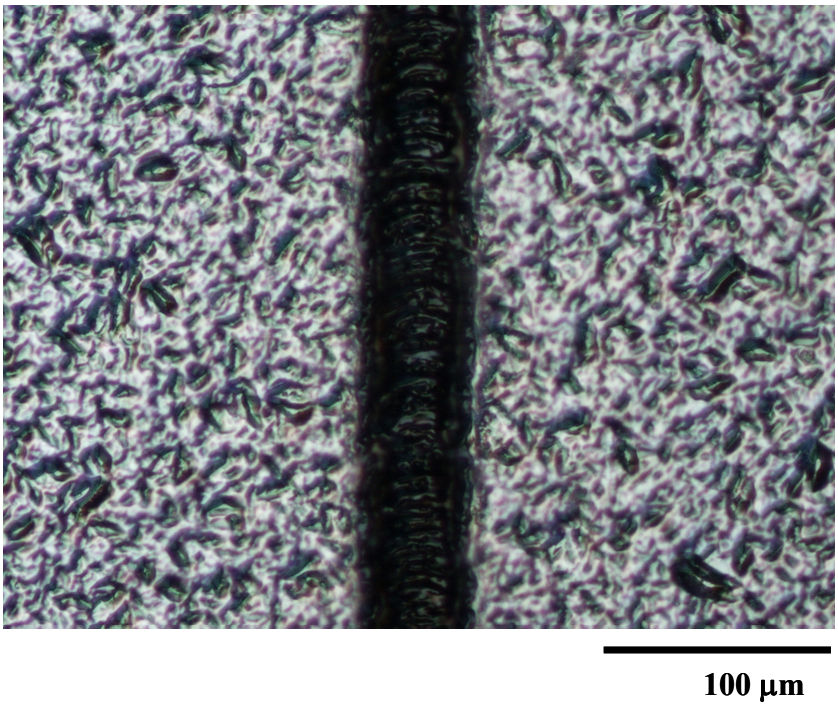


Figure 5.7 Normarski image of stripe contact on contact resistance sample

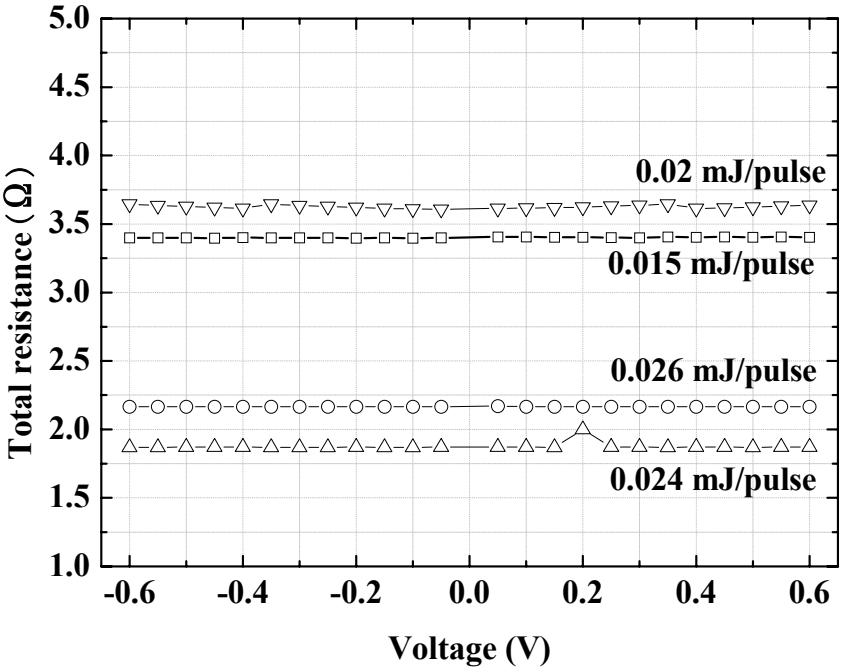


Figure 5.8 The total resistance of LFC with SiN passivation as a function of pulse energy

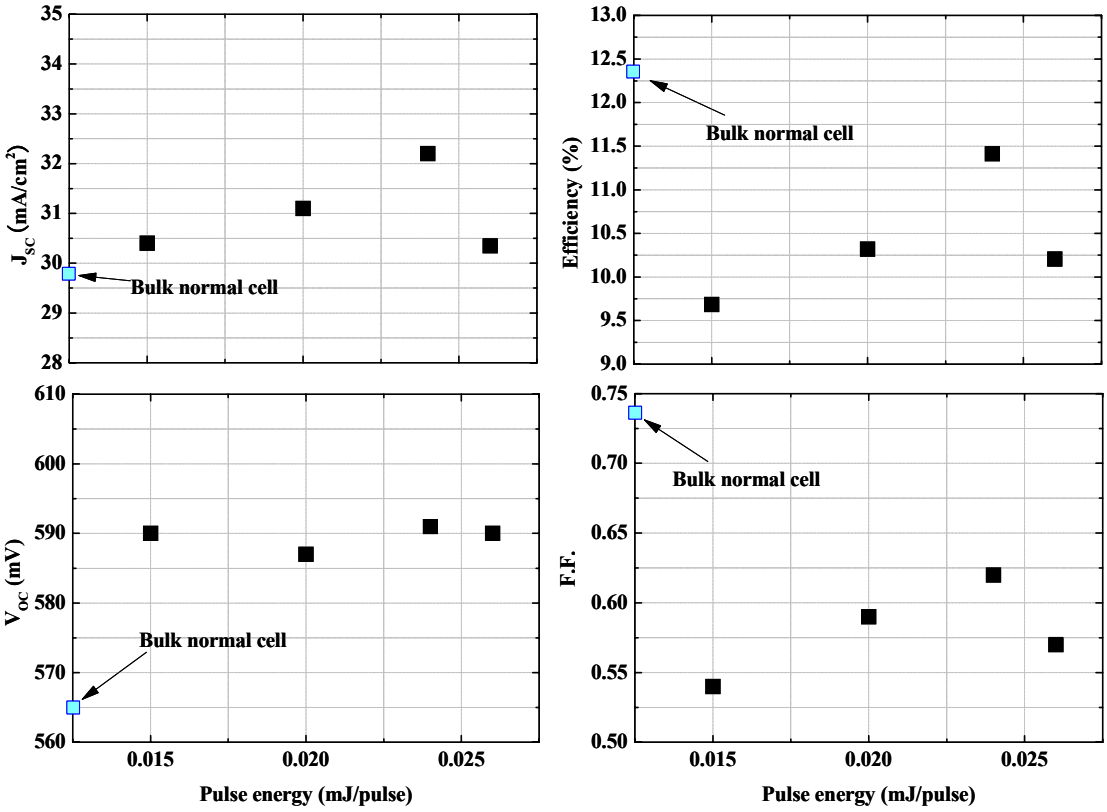


Figure 5.9 Electric properties of Bulk type LFC cell with SiN_X passivation as a function of pulse energy

5.3 Fabrication of LFC-SPS cells

5.3.1 The device structure of LFC-SPS cells

Two types of c-Si foil solar cell were fabricated for comparison passivation effect. First type is conventional both-side contact cell (so call it SPS cells) and second type is both contact SPS cell with LFC (so call it LFC-SPS cells). These structures are schematically illustrated in Fig. 5.10. In the SPS cell structure, front and rear side contacts are finger electrodes and full surface contact, respectively. This cell structure is lager rear surface recombination than LFC-SPS cells and common type in present production line.

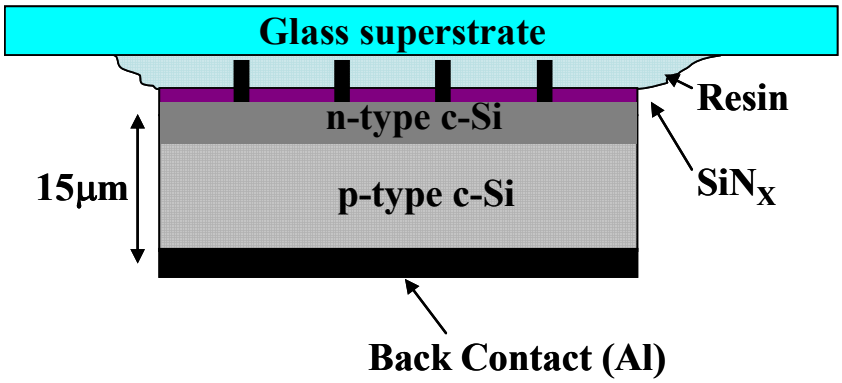
SPS and LFC-SPS cell sizes are 15 mm × 15 mm and front side contact is finger electrode. LFC-SPS cell structure has SiN_X passivation layer on rear surface and the rear side contact is local contact. SPS and LFC-SPS cell structures have SiN_X layer on front side for passivation and antireflective coating [6].

5.3.2 The fabrication process of LFC-SPS cells

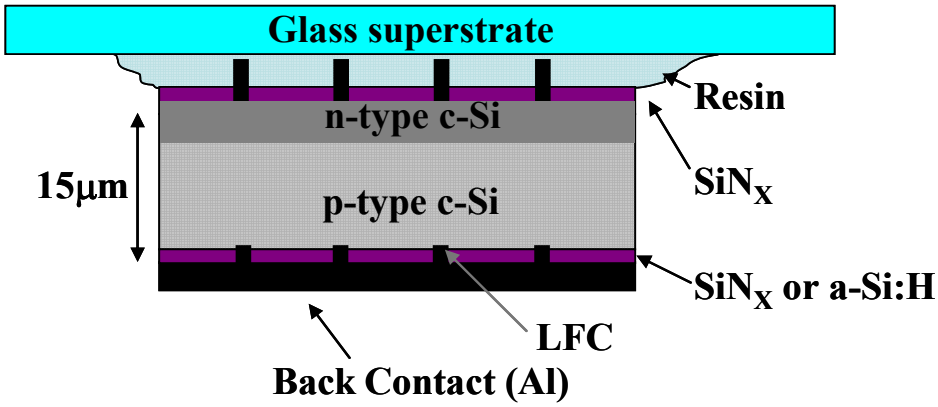
The processing sequence for two type structures of c-Si foil solar cells was established using standard pn-junction fabrication process. We adjusted several process parameters for the successful fabrication of c-Si foil solar cell through many experiments of solar cell fabrication. The solar cell fabrication sequence consists of following processing steps:

1. 2 inch p-type Cz c-Si (100) wafers were used as substrates. The resistivity of the wafer was 0.01-0.02 Ω cm. 1. Anodization: formation of three different porous silicon layer using Step 1: for 4 min, Step 2: for 4 min, Step3: for 4 sec, (process sequence: refer to section 3.2.3)

2. Hydrogen annealing, optimum condition: 1100 ˚C for 35min
3. 15μm c-Si epitaxial growth on sintered porous silicon by APCVD,
   growth condition: 1050 ˚C for 20 min with boron doping density of 5.8×10^{15} cm^{-3} and the growth rate of 0.75 μm/min.
4. The wafers were dipped in diluted HF (1 %) to remove an oxide layer, the wafers were rinsed in de-ionized water and drying of the wafers with nitrogen.
5. RCA cleaning (Table V-I.), Formation of pn-junction; diffusion of pn-junction from $POCl_3$ at 900 ˚C.
6. Phosphorous glass removal in diluted HF (1%).
7. Evaporation of Ti/Ag front contact and PMA (Post Metallization Annealing); 400 ˚C for 15 min in N_2
8. Front side surface passivation with SiN_X layer (reflective index = 2.03 at 633nm, 73 nm thick) by PECVD
9. Transfer to glass superstrate using UV cure adhesive
10. 3 - 4 μm sintered porous silicon layer on rear side removal by RIE (Reactive Ion Etching);
11. Rear side processing, SPS cell; Evaporation of Al full surface contact,
    LFC-SPS cell; Rear side surface passivation with SiN_X layer by PECVD,
    followed by evaporate 500 nm-thick Al full surface and then Laser Fired Contact and evaporation of 500 nm-thick Al full surface



(a) SPS cell



(b) LFC-SPS cell

Figure 5.10 Three types structure of c-Si foil solar cell: (a) SPS cell and (b) LFC-SPS cell

Table V-I. RCA cleaning sequence used for Si wafers.

No.	Process	Chemicals	Conditions
1	SPM	H_2SO_4 (97%) → 1 : 1 H_2SO_4 (97%) : H_2O_2 (30%)	30 min at 80 °C → 30 min at 80 °C
2	Rinse	deionised H_2O (~18 MΩ)	1 min at 20 °C
3	HF	HF (5%)	1 min at 20 °C
4	Rinse	deionised H_2O (~18 MΩ)	1 min at 20 °C
5	RCA-1 (SC-1)	1 : 5 : 1 NH_3 (27%) : H_2O : H_2O_2 (30%)	5 min at 80 °C
6	Rinse	deionised H_2O (~18 MΩ)	1 min at 20 °C
7	HF	HF (5%)	1 min at 20 °C
8	RCA-2 (SC-2)	1 : 5 : 1 HCl (27%) : H_2O : H_2O_2 (30%)	5 min at 80 °C
9	Rinse	deionised H_2O (~18 MΩ)	1 min at 20 °C
10	HF	HF (5%)	1 min at 20 °C
11	Rinse & dry	deionised H_2O (~18 MΩ)	1 min at 20 °C

5.4 Characterization of LFC-SPS cells

5.4.1 Electrical properties of LFC-SPS cells

Figure 5.11 shows photograph of c-Si foil solar cell separation from mother silicon substrate. We corroborated with Glue lab Co. for development of UV cure adhesive. Figure 5.12 shows photograph of free-standing 15 μm c-Si foil solar cell. This c-Si foil solar cell is very flexible. So it will be able to apply to plastic superstrate. We applied LFC process with optimized laser parameter which is 0.024 mJ/cm pulse energy to 15 μm c-Si foil. However, this laser condition was too strong for 15 μm c-Si foil, laser beam fired through not only 1 μm Aluminum and 100 nm SiN_X layers but also 15 μm c-Si foil. This was caused by irradiated energy changed into thermal energy on the surface of Aluminum. While, Bulk type LFC cell has enough thickness and thermal energy while was changed from irradiated energy couldn't pass through. Therefore, we reduced laser pulse energy (from 0.024 mJ/pulse to 0.015 mJ/pulse) and apply to 15 μm c-Si foil.

I-V curves under illuminated were shown in Fig. 5.13. The electric properties of SPS cell and LFC-SPS cell were shown in Table V-II. In spite of non-light trapping structure, the high J_{SC} can be obtained from both cells. This is possibly due to high quality of c-Si foil. The V_{OC} of 533mV and 553mV have been achieved for the SPS cell and LFC-SPS cell, respectively. The V_{OC} of LFC-SPS cell is higher than those of SPS cell. The carrier recombination on rear surface was decreased by rear surface passivation effect. Figure 5.14 shows the Electroluminescence (EL) images of LFC-SPS cell and Bulk type LFC cell with metal sintering at 400 ˚C. Compared with Bulk type LFC cell, LFC-SPS cell designed many inhomogeneity in EL image. In the evaluation of EL image, when minority carriers injected uniformly, EL intensity is strong as minority carriers are much present. LFC-SPS cell showed inhomogeneous EL image which was caused by poor rear contact.

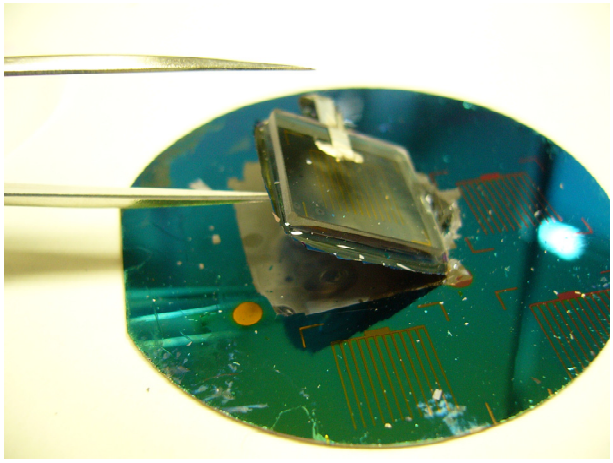


Figure 5.11 Photograph of c-Si foil solar cell separation from mother silicon substrate

Figure 5.12 Photograph of free-standing 15μm c-Si foil solar cell

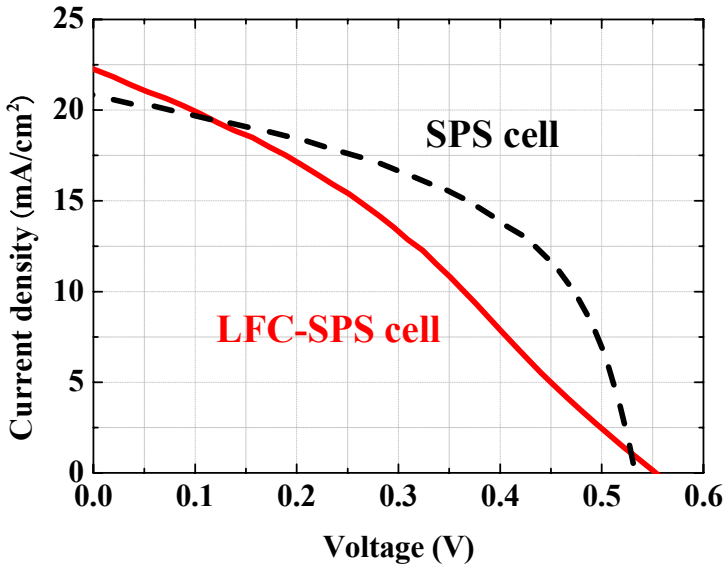


Figure 5.13 I-V curve of SPS and LFC-SPS cell under the illumination (AM 1.5, 100 mW/cm^2)

Table V-II. Electric properties of SPS and LFC-SPS cell

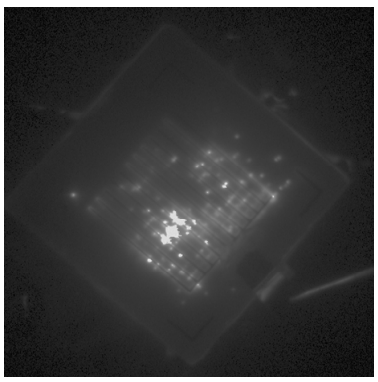
sample	J_{sc} (mA/cm^2)	V_{oc} (V)	F.F.	Eff (%)
SPS	20.80	0.533	0.50	5.54
LFC SPS	22.20	0.553	0.33	3.90
300μm Fz	29.83	0.565	0.73	12.30

5.4.2 Internal Quantum Efficiency analysis of LFC-SPS cell

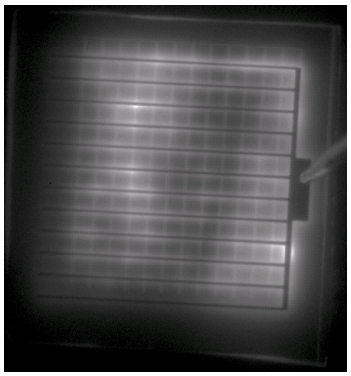
In the Internal Quantum Efficiency (IQE) results (in Fig.5.15), response of LFC-SPS cell increased by over 15% compared with SPS cell in the long wavelength region. This results suggested the increase of an effective minority carrier diffusion length (L_{eff}). When the optical absorption in the emitter of solar cell is neglected, the inverse internal quantum efficiency can be expressed [7],

$$IQE^{-1} = 1 + \frac{1}{\alpha(\lambda)} \cdot \frac{1}{L_{eff}} \tag{5-1}$$

where λ is the wavelength and α is the absorption coefficient. In order to exclude the effect of carrier recombination at front and back surface, normally, L_{eff} was estimated from the spectral response in the wavelength region from 600 to 800 nm. After calculation using eq.(5.1), L_{eff} of SPS cell and LFC-SPS cell indicated 22 μm and 38 μm, respectively. LFC-SPS cell has longer L_{eff} compared with SPS cell from this result. However, Wolf et al. published 128μm as the bulk diffusion length of new concept PSI cell [8]. Our result is very low comparison with Wolf's result. And so, we demonstrated our c-Si foil has over 110 μm as effective diffusion length in chapter 3. It means bulk lifetime of c-Si foil decreased through solar cell fabrication process.



(a) LFC-SPS cell
F.F.= 0.33



(b) Bulk type LFC cell
F.F.= 0.73

Figure 5.14 Electroluminescence image of (a) LFC- SPS cell and (b) annealed Bulk type LFC cell

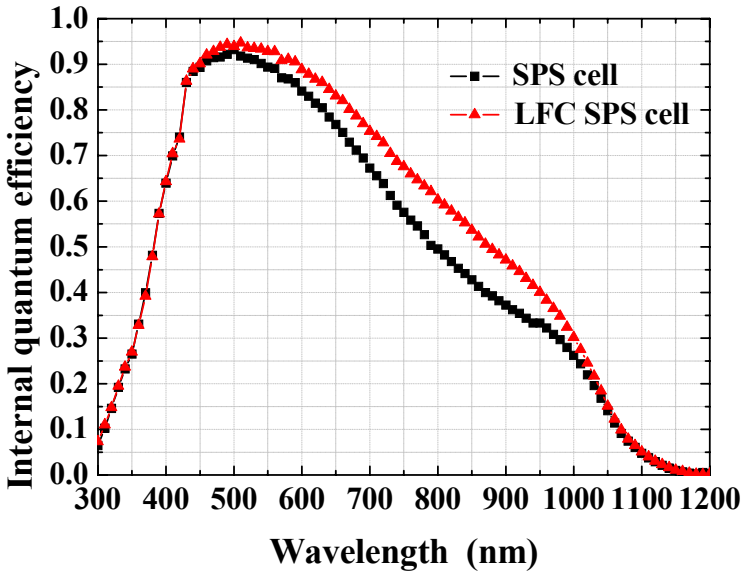


Figure 5.15 Internal quantum efficiency of SPS and LFC-SPS cell

5.5 Summary

We proposed LFC-SPS cell to c-Si foil solar cell to solve another issue as the processing rear side contact at below 200 ℃. And on the same time, the fabrication process of c-Si foil solar cell using SPS process was developed and optimized. We applied optimized LFC process condition for Bulk type LFC cell with 0.024 mJ/pulse pulse energy to15 μm c-Si foil. However, this laser condition was too strong for 15 μm c-Si foil, laser beam fired through not only 1 μm Aluminum and 100 nm SiN_X layers but also 15 μm c-Si foil. And so, we changed to 0.015 mJ/pulse laser pulse energy and irradiated rear side of 15 μm c-Si foil solar cell. We got 3.90 % (J_{SC}: 22.2 mA/cm^2, V_{OC}: 0.553 V, F.F.: 0.33) on LFC-SPS cell, and also SPS cell achieved 5.54 % (J_{SC}: 20.8 mA/cm^2, V_{OC}: 0.553V, F.F.: 0.50). We assumed LFC-SPS cell get over 10 % from calculated efficiency using minority carrier lifetime. In addition to badly rear contact, we found that bulk lifetime of c-Si foil decreased through solar cell fabrication process. We have to investigate optimization of solar cell fabrication process including laser parameter in LFC process. After improved rear side contact, it is seemed that cell efficiency increase dramatically, LFC-SPS cell has high potential for high efficiency.

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Chapter 6

Conclusion

6.1 Conclusion

The target of this thesis is to develop single crystalline silicon foil solar cells with active layer thickness as thin as 15 μm grown epitaxially on porous silicon separation layer after hydrogen annealing using SPS process. Especially, we noticed two things which are high quality epitaxial c-Si layer and excellent rear surface passivation at low temperature by the evaluation of minority carrier lifetime for the high efficiency c-Si thin film solar cells.

In Chapter 2, we found out the required electrical properties, which are especially bulk carrier lifetime and surface recombination velocity in c-Si foil, and the structure of c-Si foil solar cell using device simulation. And we discussed about the practical theories and measurement technique for minority carrier lifetime and surface recombination.

We obtained the required electrical properties which are bulk carrier lifetime: over 4.8 μs and rear surface recombination velocity: below 100 cm/s by device simulation. And we also obtained 2.9 μs as the required effective carrier lifetime by calculation. These bulk carrier lifetime and surface recombination velocity became the target for the development of LFC-SPS cell.

In Chapter 3, Layer Transfer using SPS process was demonstrated and optimized. The quality of epitaxial silicon layer dependence on anodization and hydrogen anneal conditions was discussed through the evaluation of carrier lifetime.

Layer Transfer using SPS process was demonstrated and optimized in this chapter. We got homogeneous three different porous-Si layers by improvement of anodization apparatus. On the quality of epitaxial growth silicon layer dependence on anodization and hydrogen annealing conditions, accompanying the anodization current of forming third porous-Si layer increase was a decrease in the crystal quality and minority carrier lifetime. And accompanying the annealing temperature increase was an increase in crystal quality and minority carrier lifetime. We achieved minority carrier lifetime: 4.6 μs, which is nearly the same as required minority carrier lifetime in the Chapter 2. In Chapter 5, 15 μm c-Si foil solar cell is produced by this best condition of forming c-Si foils (first step: 5 mA/cm^2, second step: 20 mA/cm^2, third step 250 mA/cm^2 hydrogen annealing: 1100 ˚C for 35 min).

In Chapter 4, NH_3 plasma-treatment for interface modification was performed at low temperature. For applied SiN layer passivation to 15 μm c-Si foils, NH_3 plasma-treatment condition was investigated. The p-type c-Si material was exposed to the NH_3 plasma before depositing the SiN_X layer in a PECVD system. The effective lifetime of the samples with NH_3 plasma-treatment were superior to the samples without NH_3 plasma-treatment regardless of the following deposition temperature. It was found that the excellent surface passivation effects would be formed even at a very low temperature, 100 ℃, using the NH_3 plasma-treatment. Moreover, the SIMS measurement results indicated that the mechanism of NH_3 plasma-treatment affected hydrogenation and carbon cleaning. The XPS spectra results confirmed that the nitrogen atom existed on passivation layer/c-Si interface by NH_3 plasma-treatment. It is possible that nitrogen leads to increasing the fixed charge and suppresses interface recombination. By NH_3 plasma-treatment, passivation layer/c-Si interface was modified and passivation effect increased even when the passivation layer was deposited at 200 ˚C. Finally, we obtained effective recombination velocity of SiN_X pssivation as 20 cm/s.

In Chapter 5, 15 μm c-Si foil solar cell fabrication process was produced. We applied

optimized LFC process condition for bulk type LFC cell with 0.024 mJ/pulse pulse energy to 15 μm c-Si foil. However, this laser condition was too strong for 15 μm c-Si foil, laser beam fired through not only 1 μm Aluminum and 100 nm SiN_X layers but also 15 μm c-Si foil. And so, we changed to 0.015 mJ/pulse laser pulse energy and irradiated rear side of 15 μm c-Si foil solar cell. We got 3.9 % (J_{SC}: 22.2 mA/cm^2, V_{OC}: 0.553 V, F.F.: 0.33) on LFC-SPS cell, and also SPS cell achieved 5.54 % (J_{SC}: 20.8 mA/cm^2, V_{OC}: 0.553V, F.F.: 0.50) The LFC-SPS cell was expected to achieve 10 % efficiency after the improvement of rear contact In addition to poorly rear contact, we found that bulk lifetime of c-Si foil decreased through solar cell fabrication process. We have to optimize the solar cell fabrication process including laser parameter in LFC process condition. After improved rear side contact, it is seemed that cell efficiency increase dramatically, LFC-SPS cell has high potential for high efficiency.

6.2 Future work

In order to realize higher efficiency for the actual solar cells and wide use of the c-Si foil solar cells, there are many issues to study as follows;

1. Development of easy cell fabrication process. Also, increasing the number of times of Si wafer reuse is indispensable. In this thesis, the carrier lifetime decrease after cell fabrication compared with the carrier lifetime after separation from Mother c-Si substrate. The optimization of cell fabrication process is needed.

2. More and more optimization of LFC process using new laser system. Including analysis of the laser damage, LFC process must be reviewed. The improvement of the laser system is also needed
3. Control of a light trapping structure using dry etching. In this thesis, we didn't

discuss and indicate about light trapping structure. The results that J_{SC} increase over 30% by the effective light trapping structure was obtained using device simulation. The increasing J_{SC} is leads to increase efficiency. The development of effective light trapping technique for c-Si foil solar cells is needed (Refer to Appendix A.).

Appendix A.

Sub-micron surface texturing of monocryslline silicon thin film solar cells using Reactive Ion Etching method

*This paper was published in 19th EU-PVSEC

1 Introduction

Crystalline silicon thin film solar cells on low cost substrate are one of the most promising and challenging approches to reduce costs of solar cells. Specifically, monocrystalline silicon (c-Si) thin film solar cells gather much attention in the view of reducing silicon with high conversion efficiency. The efficiency of over 18% is expected according to the simulated results for 3μm-thick c-Si thin film solar cells [1]. However, experimental results of only about 12% have been obtained for the 12 μm-thick c-Si thin film solar cells [2]. For improving the efficiency, the high quality epitaxial c-Si layer, high-light trapping technique, and lowering the surface and rear recombination velocity are strongly required. In the light trapping technique, alkaline solution is commonly used to etch c-Si (100) to improve the light trapping. However, the fabrication process is difficult to control the pyramid size for 10 μm-thick c-Si thin film solar cells.

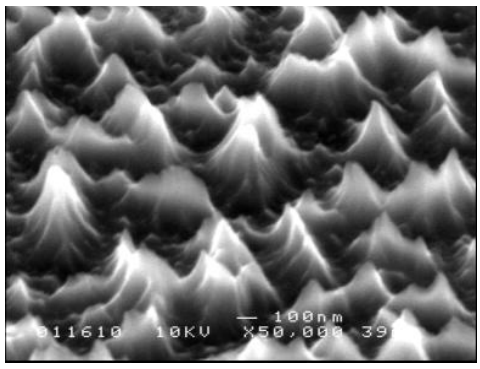
Several research groups have been studied the surface texturing of multicrystalline silicon solar cells using RIE [3, 4]. This process provides the maskless submicron size pyramid on multicrystalline silicon surface. In this study, we propose a new surface texturing tequnique of c-Si thin film solar cells using RIE. Previouly we reported the effect of texturing

on solar cell performances. Processed surface texture had needle pyramids, and the size of pyramid could be controlled by O_2 gas flow ratio. Sub-micron surface texturing was fabricated on c-Si thin film solar cells, we discussed relatioship between sub-micron suface texturing focussing on the shaollow junction fabricated on sub-micron texturing.

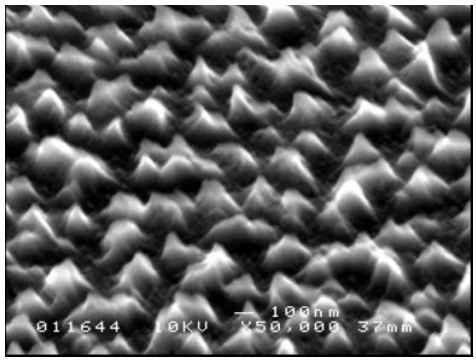
2 Texturing on silicon surface by RIE

2.1 Experimental

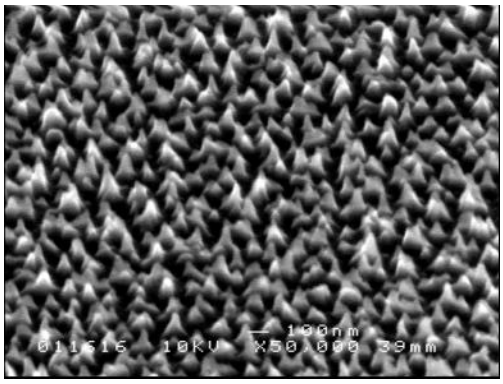
P-type (1.0×10^{17} cm^{-3}) c-Si film with a thickness of 10 μm were grown epitaxially on (100) p^+ substrate (2.0×10^{20} cm^{-3}) by atmospheric pressure chemical vapor deposition (APCVD). Dichlorosilane (SiH_2Cl_2), BCl_3 and H_2 were used as source, dopant, and carrier gases, respectively.



(a) $O_2/(SF_6+O_2)$ = 20%



(b) $O_2/(SF_6+O_2)$ = 40%



(c) $O_2/(SF_6+O_2)$ = 70%

Fig.1 SEM images of surface structures prepared by RIE with the different flow ratios of O_2.

The etching was performed with the mixtured gas of SF_6 and O_2 at 0.8 Pa with RF-power of 200 W at room temperature for 8 minutes. The SF_6 gas flow rate was fixed at 20 sccm, and the ratio of actual SF_6 to O_2 flow rate (O_2 / SF_6 + O_2) was varied from 0 % to 70%. The damage surface layer (radiation, contaminations) was observed by plasma process. Therefore after RIE texturing, The samples were dipped in a mixed solution of H_2SO_4 (100%), and H_2O_2 (30%) at 80^{o}C for 30min. Then the samples were rinsed in de-ionized water. They were dipped in diluted HF (0.5%) to remove the oxide layer (damage layer etching).

2.2 Result and discussion

Figure 1 shows a scanning electron microscope (SEM) image of surface structure prepared by RIE method with different O_2 flow ratio. The shape of pyramid structure depended on (O_2 / SF_6 + O_2) flow ratio. A small number of needle pyramid was obtained under the condition of no O_2 mixed. As O_2 flow ratio increases, more numbers of needle pyramid and smaller pyramid size were obtained. The average size of 150 nm width (w) and 350 nm height (h) needle pyramid structures were obtained from O_2 ratio of 20%. The size of pyramid is 110 nm (w) by 200 nm (h) for O_2 ratio of 40% . And the size of pyramid is 80 nm (w) by

100 nm (h) for O_2 ratio of 70%.

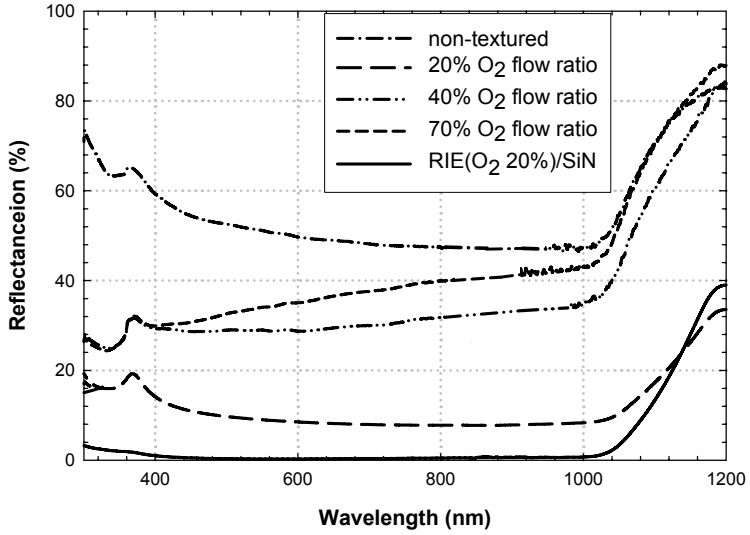


Fig.2 Reflectance of silicon with different surface texturing on O_2 flow ratio.

The effect of oxygen flow ratio in each etching condition on the reflectance was compared, as shown in Fig 2. The larger needle pyramid had the lower reflectance. However, the amount of O_2 gas mixture is had to be carefully controlled since the less O_2 ratio in etching gas can also produce too large needle pyramid size and this can lead to higher reflectance. The lowest reflectance etching condition was 20% O_2 mixed gas ratio and the reflectance showed less than 15% in a wavelength region of 400-800 nm. After RIE, the reflectance of SiN layer on needle pyramids prepared by PECVD is shown in Fig.2. The reflectance still decurased, its close to 0% in a wavelength region of 500-1000 nm.

3 Fabrication of c-Si thin film solar cell using RIE texturization

3.1 Conventional process

The suructure of RIE textured c-Si thin film solar cell is shown in Fig.3. We

fabricated this cell by conventional process. The surface textured of c-Si thin films solar cells was fabricated using RIE by 20 % O_2 mixed gas ratio. After RIE texturing, we fabricated emitter. The fabrication process consists of mainly six steps:

1. Conventional RCA clean.
2. Growth of p-type ($1.0\times10^{17}cm^{-3}$) c-Si films on (100) p^+ substrate ($2.0\times10^{20}cm^{-3}$) with a thickness of 10 μm by APCVD . The cell area is $1cm^2$.
3. Formation of Sub-micron surface txturing by RIE
4. Removal of damaged surface layer by H_2SO_4 / H_2O_2 liquid.
5. Phosphorus diffusion, The solid diffusion method indicated a coating of phosphorus doped spin-on glass layer on surface by the spinner process. Then, a thermal diffusion process was carried out for emitter layer.
6. Fabrication of front contact (Ti/Ag) and rear contact (Al) by vacuum evaporation.

It is very important to optimize a suitable doping process for emitter formed on a needle pyramid structure. Two types of emitter structure were fabricated by solid phase diffusion method, as shown in Fig.4. One was the deep emitter (Fig.4a); The emitter layer with a thickness of 400 nm was fabricated entirely on the needle pyramids. Another one was the shallow emitter (Fig4b.); Emitter layer with a thickness of less than 180nm was fabricated on surface of needle pyramid.

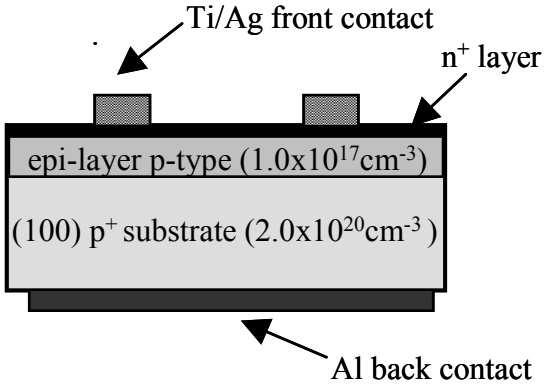
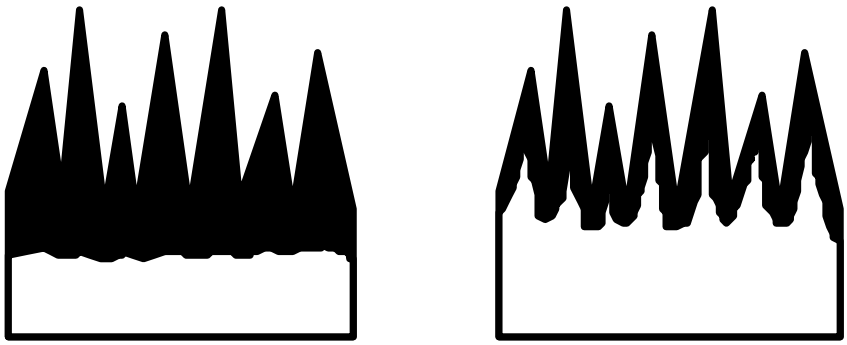


Fig.3 The suructure of Sub-micron texturinf c-Si thin film solar cell.



(a) Deep emitter (b) Shallow emitter

Fig.4. Model of emitter formation on needle pyramid by deep doped (a) shallow doped (b)

3.2 Result of cell performance

Table I shows the comparison of electrical properties of textured and non-textured c-Si thin film solar cells with different emitter by solid phase diffusion method. The mirror/shallow show mirror surface, shallow emitter layer in table and figure. J_{sc} of textured cells with both depth of emitter layer increased by over 20 %. However, other electrical data of the textured cells are low as compared with the non-textured cells for both depth of emitter layer. Finally efficiency of textured cells with both depth of emitter layer decreased by over 10 %. The electrical performance of the shallow emitter cells is also low as compared with the deep emitter cells.

Figure 4 shows the Internal Quantum Efficiency (IQE) measurement of shallow and deep emitter solar cells. When photons are absorbed, photo-generated carriers in the p^+ substrate cannot be contributed to the solar cell output. Deep emitter textured and non-textured solar cells were lower than those of shallow emitter solar cells. The IQE in short wavelength (300-500 nm) of shallow emitter cells indicated higher value than those of deep emitter cells. Because the emitter layer thickness was different from each other. And the IQE in short wavelength of shallow and deep emitter textured solar cells was lower than that

of non-textured solar cells. We expected plasma damage and contamination lead to create the defects. Therefore, after RIE texturing, the damage layer of textured cells were not removed completely in damage layer etching process (step 4). We consider that low electrical properties of textured c-Si thin film solar cells were due to poor pn junction.

Table I ; Result of mirror and RIE textured c-Si thin film solar cells with different depth of emitter layer.

	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF	Eff (%)
Mirror/solid/deep	16.11	590	0.75	7.13
RIE/solid/deep	19.87	560	0.58	6.45
Mirror/solid/shallow	17.61	580	0.68	6.90
RIE/solid/shallow	21.34	540	0.52	5.99

No AR coat, 25°C 100 mW/cm^2, AM1.5G

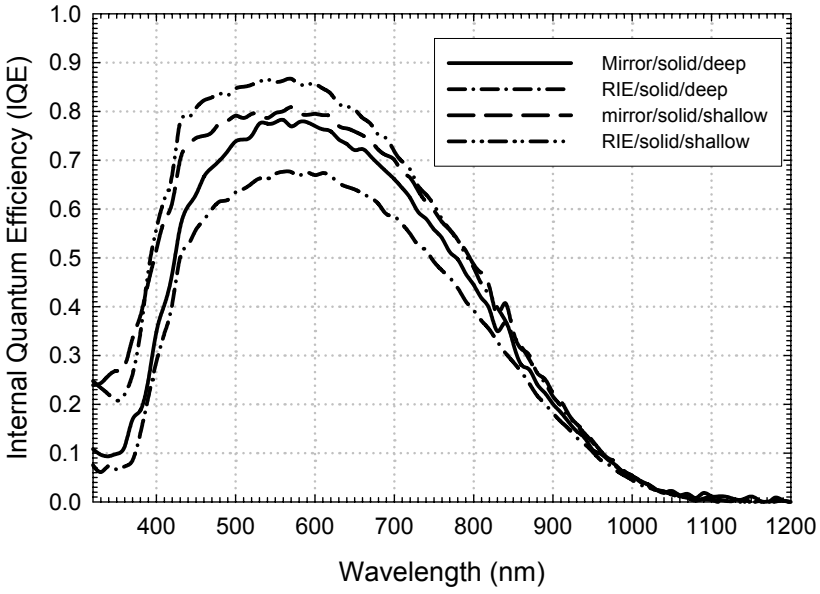


Fig.4 Internal quantum efficiency (IQE) of solar cells

Figure 5 shows dark current-voltage characteristics of these cells. We measured

forward J-V characteristics to understand the conditon of pn junction. The performance of RIE textured cells with high aspect ratio (hight / width of needle pyramid) surface was not prefarable. Large saturation current was observed in this structure.

Table II shows ideality diode factor (n) and reverse saturation current density (J_0) of these cells. These parameters in solar cells of deep emitter showed lower than those in shallow emitter cells. Moreover J_0 of deep emitter solar cells indicated lower value than that in shallow emitter solar cells. J_0 and n in RIE textured solar cells were higher than those in non-textured solar cells. We consider that the time of diffusion is too short to fabricate uniformly distributed shallow pn junction by solid phase diffusion method. Therefore, ideal diode structures could not be fabricated. Spiner process is difficult to apply to sub-micron pyramid on solid phase diffusion method.

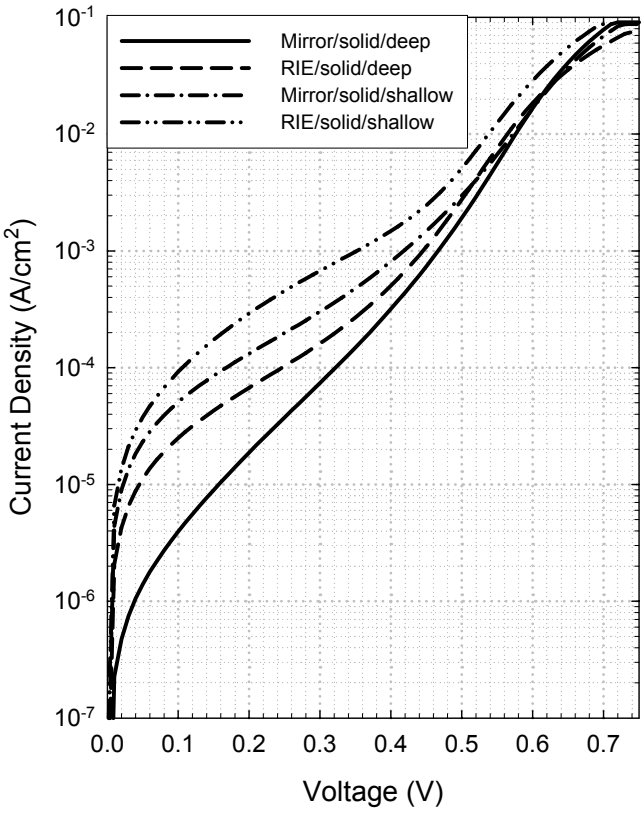


Fig.5 Forward J-V characteristics of solar cells

Table II : J_0 and n of solar cells prepared by solid phase diffusion method.

	J_0 (A/cm²)	n
Mirror/solid/deep	4.08×10^{-8}	1.8
RIE/solid/deep	1.85×10^{-8}	1.89
Mirror/solid/shallow	2.29×10^{-7}	2.12
RIE/solid/shallow	8.73×10^{-7}	2.23

3.3 Fabrication of shallow p/n junction by gas phase diffusion method

Next gas phase diffusion method was used to fabricate conformal shallow p/n junction on needle pyramids surface. The gas diffusion method consists of diffusion process of $POCl_3$ liquid dopant source to form the emitter. The comparison of electrical properties of textured c-Si thin film solar cells with non-textured is shown in Table III. J_{sc} of textured cells with shallow emitter layer increased considerably by over 40%. And other electrical properties of the textured cells are higher as compared with the non-textured cells. Finally efficiency of textured cells with shallow emitter layer increased by over 60%.

The highest efficiency was btained in the solar cell with shallow emitter for RIE textured. The efficiency as high as 10.9% was achieved.

Table III: Result of mirror and RIE textured c-Si thin film solar cells with shallow emitter layer by gas phase diffusion method

	J_{sc} (mA/cm²)	V_{oc} (mV)	FF	Eff (%)
Mirror/gas/shallow	16.17	580	0.76	7.13
RIE/gas/shallow	23.65	607	0.76	10.90

No AR coat, 25°C 100 mW/cm², AM1.5G

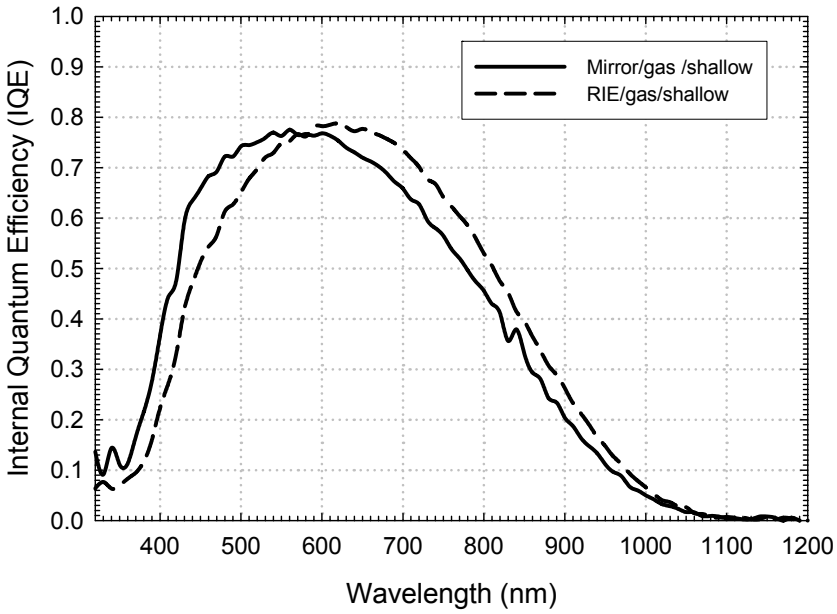


Fig.6. Internal quantum efficiency (IQE) of solar cells

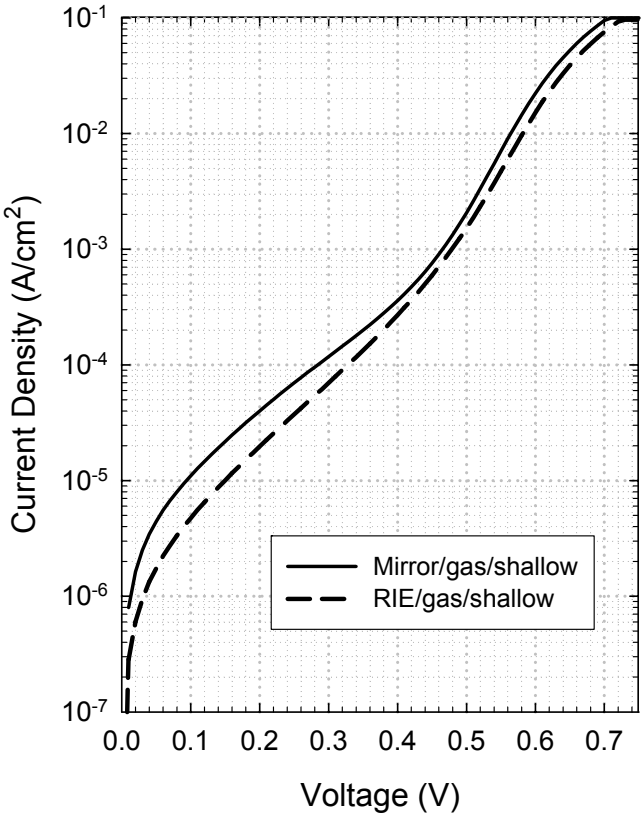


Fig.7 Forward J-V curve of solar cells prepared by gas phase diffusion method.

Table IV : J_0 and n of solar cells prepared by gas phase diffusion method.

	J_0 (A/cm^2)	n
Mirror/gas/shallow	9.28×10^{-9}	1.57
RIE/gas/shallow	9.67×10^{-9}	1.63

Figure 6 shows the IQE measurement of shallow emitter cells. RIE textured solar cell was higher than non-textured solar cells in the wavelength region of 600nm to 1000nm. This would be due to expanding light path length. The IQE in short wavelength region (300-550 nm) of RIE textured solar cell indicated lower than that of non-textured solar cell.

Figure 7 shows dark J-V characteristics of these cells by gas phase diffusion method. Lower saturation current than that of solid phase diffusion method was obtained.

Table IV shows J_0 and n in solar cells prepared by gas phase diffusion method. The n in solar cells prepared by gas phase indicated lower value than that in solar cells prepared by solid phase diffusion method. The J_0 and n in RIE textured solar cells showed lower value than that of non-textured solar cells. Sub-micron pyramid as fabricated in this study is very effective on gas phase diffusion method.

4 Conclusions

The reflectance of silicon surface was reduced less than 15% (400-1000nm) by needle pyramid in submicron scale fabricated using RIE. The reflectance of silicon surface is controlled by SF_6, O_2 flow ratio. We understood Phosphorus diffusion process was performed to form a shallow emitter by gas phase diffusion methods. This study proved that shallow

emitter layer is applicable to sub-micron pyramid by gas phase diffusion method. Analysis of the relationship between needle pyramid and shallow emitter layer by 2-diode model will be performed in detail[6]. Finally, we deposited SiN layer on front surface of RIE/gas/shallow cell by PECVD for passivation and antireflection coating. The efficiency as high as 11.26% was achieved. However, further optimization of conditions for diffusion and passivation by SiN deposition will be necessary for sub-micron needle pyramids. When the refractive index and thickness of SiN layer is optimized for RIE textured c-Si thin film solar cells with a thickness of 10 μm. Efficiency will go over 13%.

Reffernces Appendix A.

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[2] H. Tayanaka, K. Yamauchi and T. Matsushita, Proc. 2nd WCPEC. (1998), p1272.

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Appendix B.

-"Luminoscopy"- Novel tool for the diagnosis of crystalline silicon solar cells and modules utilizing Electroluminescence

*This paper was published in 4th WCPEC

1 Introduction

In these days, the production scale of crystalline silicon solar cells shows remarkable increase. These production lines are required to fabricate thin solar cells with thickness equal or less than 200 μm. In the mass production process for thin film cells, serious problems such as wafer cracking, breakage, and/or electrode break down occur. Quick and precise evaluation is indispensable to ensure the reliability.

In this report, we will propose a novel technique of "Luminoscopy" in which the deficiencies in the cells and modules can be clearly detected by photographic surveying of EL without any probing tools. The new detection method of the spatial distribution of minority carrier diffusion length ($\mathbf{L_e}$) was proposed utilizing the photographic measurement of EL emitted from multicrystalline silicon (mc-Si) solar cells [1].

Cell and module under forward current injection emit infrared light at a peak of 1150 nm. EL intensity is proportional to the total excess minority carrier density. Deficiencies such as cracks and defects reduce the minority carrier density, and so they can be clearly detected as dark parts (spots, lines and areas) due to decreased EL intensity. The EL is not reabsorbed by silicon substrate, so, we can get the deficiency mapping integrated along the depth just like

"fluoroscopy". Some parts of figures are covered by black strips, which do not affect the main points of arguments in this manuscript.

2 Experiments

We evaluated solar cells and modules by using this new detection method "Luminoscopy". The schematic measurement setup is shown in Fig.1. The sample cell and module biased at an appropriate forward voltage emitted infrared light which was collected by the cooled CCD camera using a selected objective lens. Areas of cell or module used in this experiment were 105 x105 mm, 125 x 125 mm cell areas and 800 x 1000 mm. The cooled (at around -50 ^{o}C) CCD could detect light by 512 x 512 pixels in the sensitive wavelength region of 300-1200 nm at room temperature in the darkroom. The resolution depends on optical lens. Forward bias voltage was applied to the current of 0 - 80 mA/cm^2. The current range corresponded to that in the cell operation under 1 - 2 Suns.

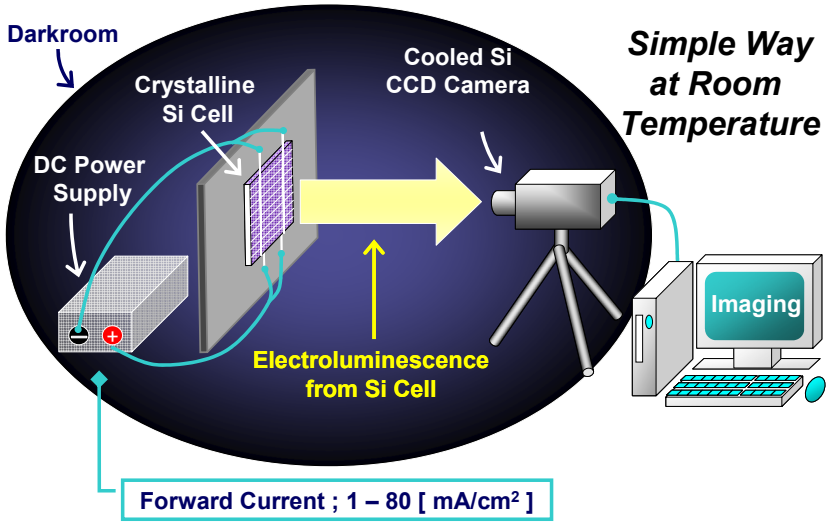
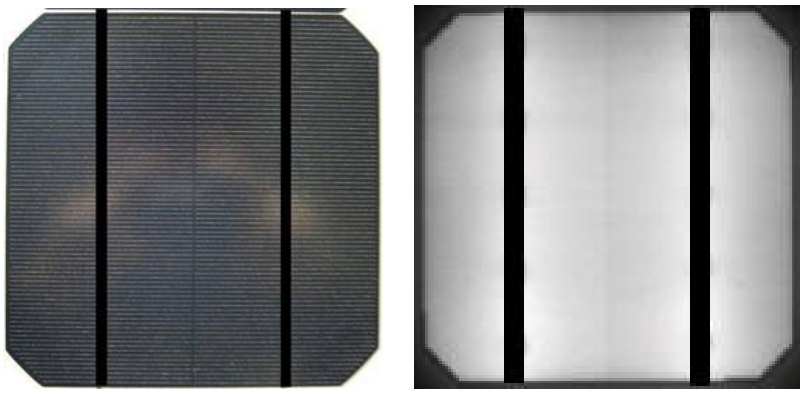


Figure 1: Schematic drawing of "Luminoscopy" setup

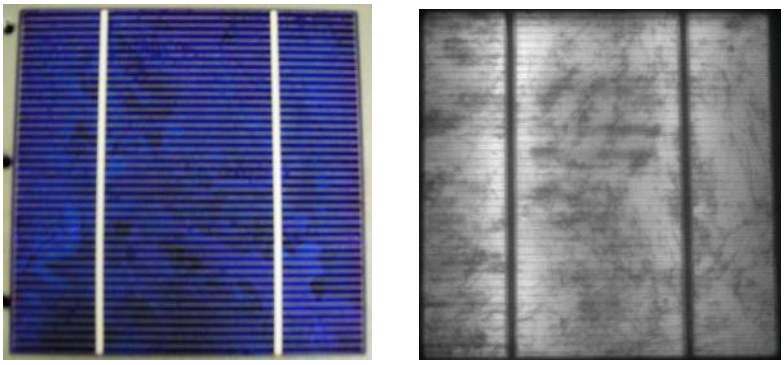


(a) (b)

Figure 2: Optical and EL images of monocrystalline silicon reference cell without cracks.

Figures 2(a) and 2(b) shows optical image and EL image of monocrystalline silicon (c-Si) reference solar cell, respectively. As reference, sample without crack was prepared. Figure 2(b) shows EL image under forward current density of approximately 35mA/cm^2 with measurement time of five hundred milliseconds.

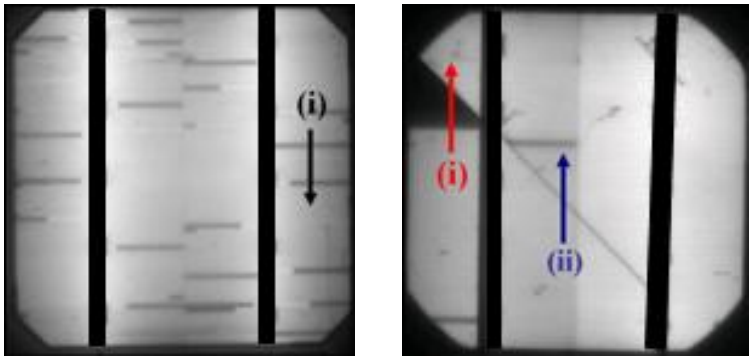
Figures 3(a) and 3(b) show optical image and EL image of poly-Si reference solar cell, respectively. Figure 3(b) shows EL image under forward current density of approximately 40mA/cm^2 with measurement time of one second. Many crosswise fine black lines indicated finger electrodes. The lengthwise bold two black lines indicated bus bar.



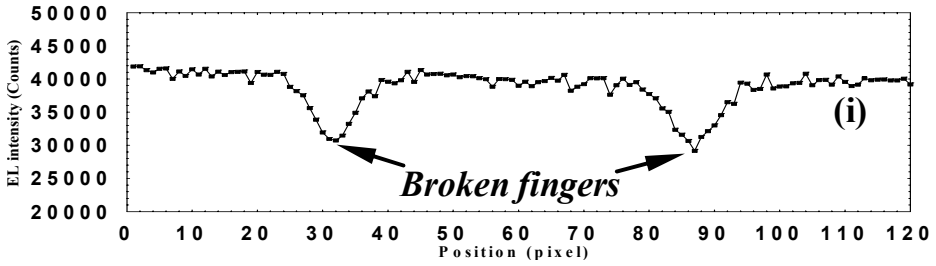
(a) (b)

Figure 3: Optical and EL images of poly-Si reference cell without cracks.

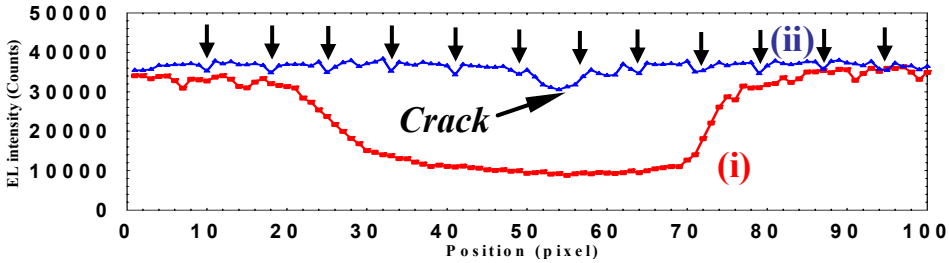
The EL intensity is expressed in the gray scale. In the case of c-Si solar cells, there is no dark spot corresponding to crystal defect. On the contrary, in the case of poly-Si solar cell, black and grey areas corresponded to grain boundary, crystalline defect and the uniformity of surface passivation in cell fabrication process are observed [2].



(a) (b)



(c) :Line scan (i) of EL image (a)



(d): Line scan (i) and (ii) of EL image (b)

Figure 4: EL images of cracks in c-Si solar cells.

3 Detection of solar cell EL image

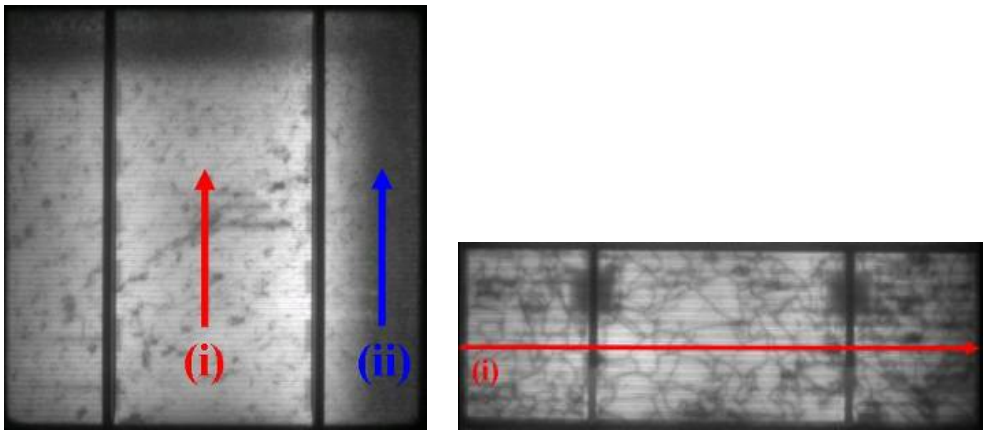
3.1 c-Si solar cell

Figures 4(a) and 4(b) show an EL image of c-Si solar cell under forward current

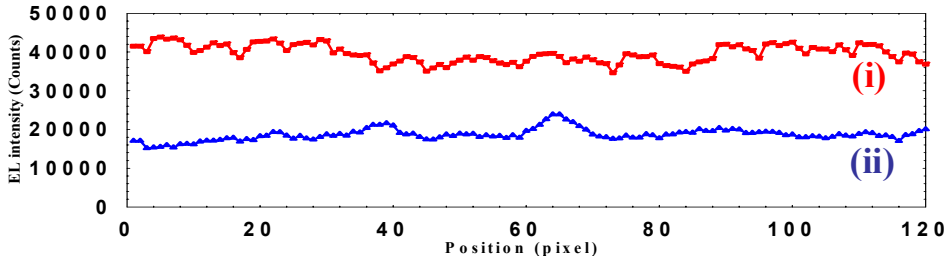
density of approximately 35mA/cm^2 with measurement time of five hundred milliseconds. These crosswise discriminative patterns corresponded to the broken fingers in the Fig.4 (a). The electrons weren't injected into the surface due to broken finger-electrodes. Figure 4(c) shows a line scan (i) in Fig.4 (a). The broken finger did not affect only the area beneath finger but also the area around it. EL intensity shows a sharp drop in the range of approximately 42000 and 31000 (counts). The diagonal line and the quarter sector-shape show cracks in Figure 4(b). This crack in Fig.4 (b) was not completely cracked. Figure 4 (d) show a line scan (i) and (ii) in Fig.4 (b). The line scans (i) and (ii) through the crack like quarter sector and the diagonal line crack, respectively. In the line scan (i), compared with EL intensity of no crack area, EL intensity of crack area is reduced from approximately 35000 to 10000 (counts). In the line scan (ii), compared with EL intensity of no crack area, EL intensity of crack decreased from approximately 36000 to 31000 (counts). Arrows in Fig.4 (d) indicate the decrease in EL intensity by finger electrodes. Compared with the diagonal line crack, the crack like quarter sector has a profound effect on EL intensity. It was found that not only silicon layer but also finger electrode were broken in the crack like quarter sector.

Figures 5(a) and 5(b) show an EL image of poly-Si solar cell under forward current density of approximately 50mA/cm^2 with measurement time of two seconds. In Fig. 5(a), the decrease of EL intensity around the upper area and right edge area suggested large defect area for wafer from edge of the poly-Si block. Figure 5(c) shows a line scan (i) and (ii) in Fig.5 (a). The line scans (i) and (ii) through the normal area and the many defect area, respectively. The line scan (i) indicates 36000-42000 (counts) on an average and (ii) indicates 15000-20000 (counts) on an average. The EL intensity under the forward bias condition showed the one-on-one relationship with $\mathbf{L_e}$ [1]. This low EL intensity area indicates low minority carrier diffusion length area. Figure 5(b) shows unique grain boundary EL image of poly-Si solar cell. Most grain boundaries indicate low EL intensity clearly. Figure 5(d) show a line scan (i) in Fig.5 (b). In the line scan (i), compared with EL intensity of intra-grain, EL

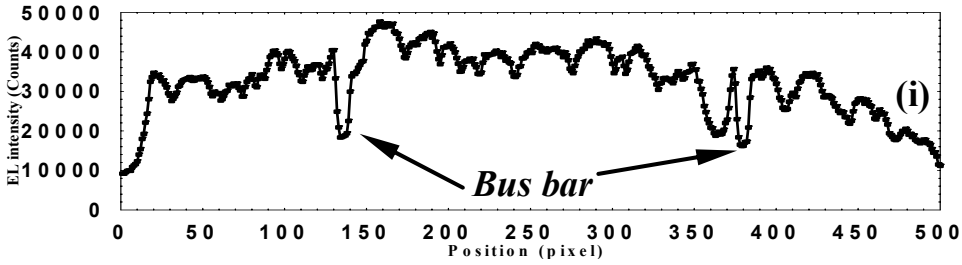
intensity of grain boundary is reduced by approximately 25% of EL intensity. For the cells used in this measurement, the effects in EL intensity by crystalline defects such as grain boundaries or dislocation were below 20%.



(a) (b)



(c): Line scan (i) and (ii) of EL image (a)



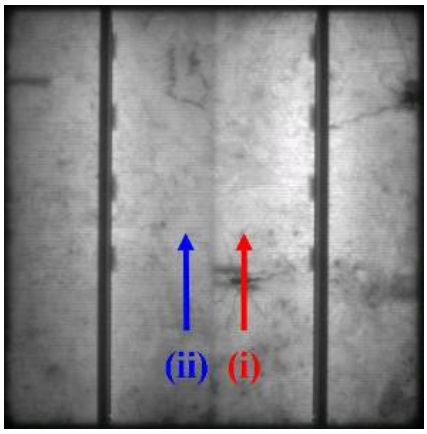
(d): Line scan (i) of EL image (b)

Figure 5: EL images of defect in mc-Si solar cell.

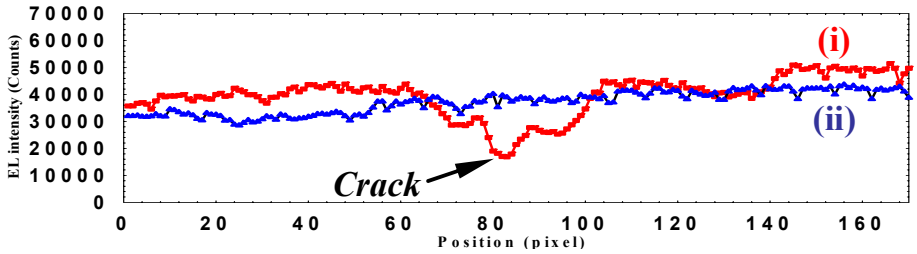
3.2 multicrystalline solar cell

Figure 6(a) and 6(b) shows an EL image of mc-Si solar cell with cracks under forward current density of about 40mA/cm^2 with measurement time one second. Figure 6(b) shows a line scan (i) and (ii) in Fig.6 (a). The line (i) and (ii) scanned the areas with and without cracks, respectively. The line scan (i) indicates the decrease from 42000 to17000 (counts) and (ii) indicates 32000-38000 (counts) on an average. The crack on upper right of cell indicates the result of same EL intensity.

Figure 7 shows an EL image of mc-Si solar cell with crack area. Magnified image shows optical and EL image for the same crack area. The crack could not be observed by an optical microscope in this area. However the crack could be observed by "Luminoscopy".



(a)



(b): Line scan (i) and (ii) of EL image (a)

Figure 6: EL images of mc-Si solar cell with cracks.

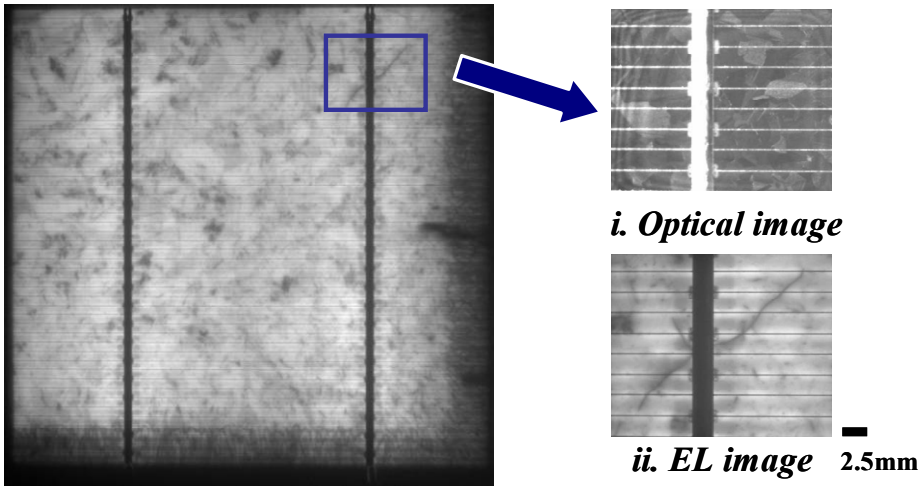
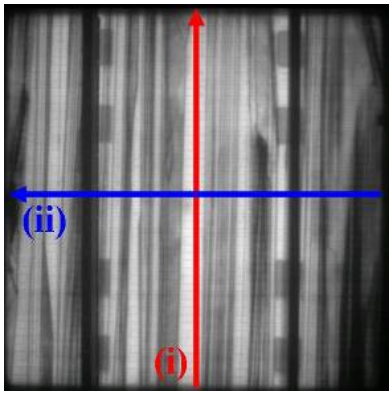
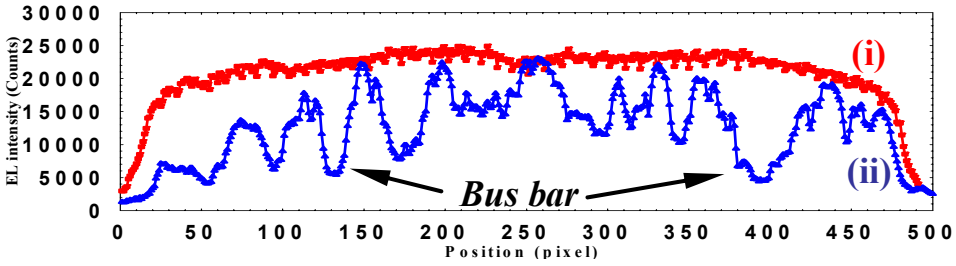


Figure 7: EL images and optical image of cracks in mc-Si solar cell.



(a)



(b): Line scan (i) and (ii) of EL image (a)

Figure 8: EL images of ribbon substrate solar cell

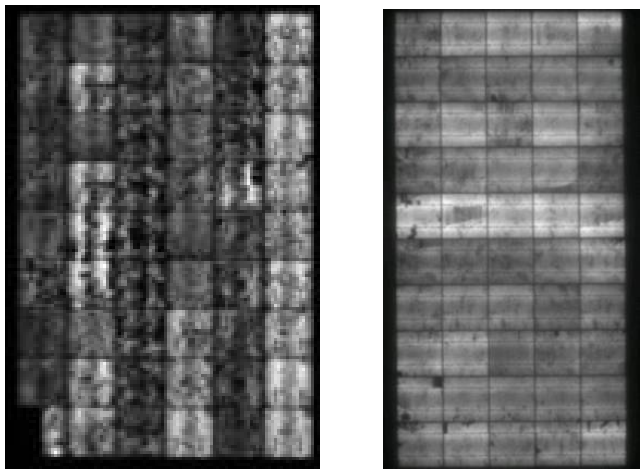
3.3 Ribbon substrate solar cell

Various kinds of crystalline silicon solar cell could be observed by “Luminoscopy”. Figure 8(a) shows an EL image of ribbon substrate solar cell under forward current density of

approximately 55mA/cm^2 with measurement time of five seconds. This EL image indicates the unique grains by one-directional growth. Figure 8(b) shows a line scan (i) and (ii) in Fig.8 (a). The line (i) and (ii) scanned through the inside of one grain and across the grain boundaries, respectively. The line scan (i) indicates around 26000 (counts) on an average. However, the line scan (ii) indicates considerable decreases of over 40%. The effect of grain boundary on EL intensity was too big. In the ribbon substrate solar cell, the crack of vertical to grain boundary could be observed easily by "Luminoscopy".

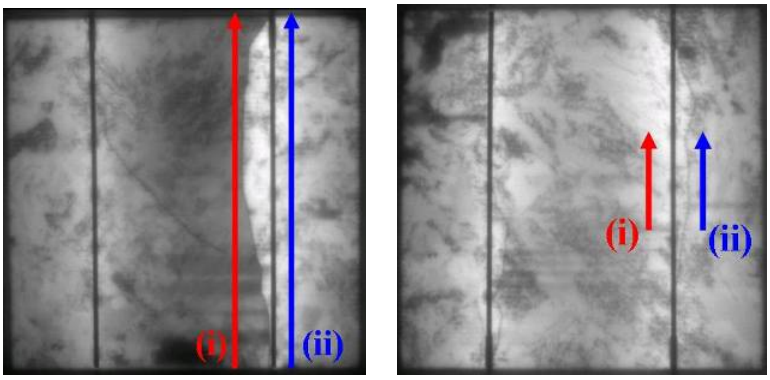
4 Detection of module EL image

This "Luminoscopy" can be applied not only to the cells but also fabricated modules and panels. Figure 9(a) and 9(b) show an EL image of mc-Si solar cell module under forward current density of approximately 35-45 mA/cm^2 with measurement time of one second, respectively. In the mc-Si solar cell module, we could detect position of crack cell and difference in performance of each cell.

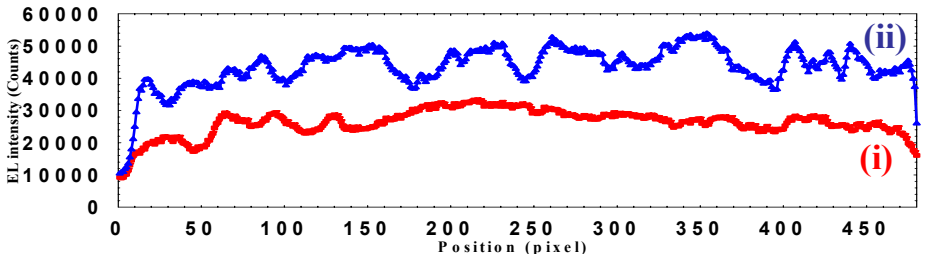


(a) (b)

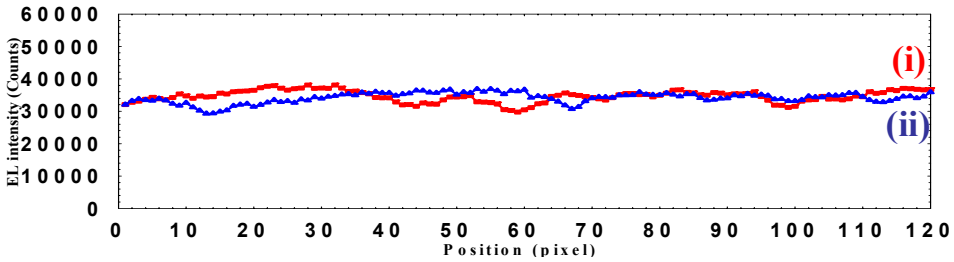
Figure 9: EL images of mc-Si solar cell module.



(a) **(b)**



(c): Line scan (i) and (ii) of EL image (a)



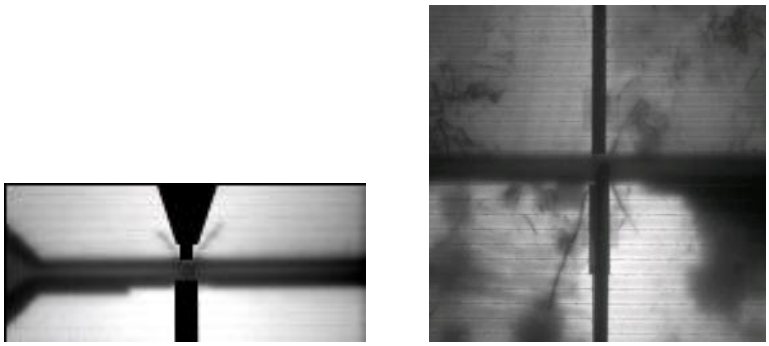
(d): Line scan (i) and (ii) of EL image (b)

Figure 10: EL images of cracks in mc-Si solar cell.

In the module, the typical cracks caused by lamination process and other fabrication process could be observed. Figure 10 (a) and 10 (b) show EL image of mc-Si solar cell in the mc-Si solar cell module under forward current density of approximately 35-45mA/cm^2 with measurement time of one second. Both cells have the long cracks along the bus bar. However, the effects of crack indicate different result. In Figs.10 (a) and 10(b), both cells have the long cracks along right side bus bar. In Fig.10 (a), the left side of crack indicates a reduced EL intensity. Figure 10(c) shows a line scan (i) and (ii) in Fig.10 (a). The line scans (i) and (ii) through the left side of crack and right side of bas-bar respectively. Compared to the line scan

(ii), the line scan (i) indicates higher EL intensity on an average. The electrons weren't injected into the surface from finger-electrodes by crack. This crack was occurred not only in silicon layer but also finger electrode. In Fig.10 (b), the left side and right side of crack showed similar EL intensity. Figure 10(d) shows a line scan (i) and (ii) in Fig.10 (b). The line (i) and (ii) scanned through the left side of crack and right side of bus bar, respectively. Compared with the line scan (ii), the line scan (i) showed similar EL intensity.

In addition, most of the cells (c-Si and mc-Si) in the module have the crack on both sides of a bus bar of cell edge in fig.11 (a): c-Si module, (b): mc-Si module.



(a) (b)

Figure 11: EL images of cracks in mc-Si solar cell.

5 Conclusions

We proposed a novel technique of "Luminoscopy" in which the deficiencies in the cells and modules can be clearly detected by photographic surveying of electroluminescence (EL) without any probing tools. It could be shown that cracks or defects in cell or modules were detected within very short time less than 1s at room temperature. After the reliability test such as heat cycle or pressure warping, cracks were detected clearly even though any indications could not be obtained by an optical microscope. This result demonstrated that "Luminoscopy" have the potential of in-line inspection for production.

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[2] Y. Takahashi, H. Kondo, T. Yamazaki, Y. Uraoka, and T. Fuyuki, 20th EUPVSEC, (2005), p. 1375-1378

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Submitted to Japanese Journal of Applied Physics.

[3] "Rear side passivated monocrystalline silicon thin film solar cells with laser fired contact process"

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J. Appl. Phys. **101**, 023711 (2007)

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Biography

Yu Takahashi was born in Hokkaido, Japan in December 7, 1978. He saw solar car “Phoebus III” in Kitami, in September, 1991. He graduated from Kitahiroshima high school, in March, 1997 and entered Chitose institute of science and technology in Hokkaido, in April, 1998. He took part in “World Solar Challenge 1999” as a member of Team Junk Yard (TJY) in Australia. They managed to complete the race of moving down Australian continent with 480 W solar car “Gamera”. After arrived goal, he believed Sun power is greatness.

He graduated from Chitose institute of science and technology in March, 2002. He entered the Microelectronic Device Science Laboratory, Graduate School of Material Science, Nara Institute of Science and Technology in Ikoma, Nara, in April, 2002. He went abroad to study and stayed at The Institut fùr Solarenergieforschung Hameln (ISFH), Germany in April, 2006. He returned to Japan in March, 2007. He will graduate and work at Sharp Corp in April, 2008.

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