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Primary Visual Cortex Inspired Feature Extraction Hardware Model and Applications

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Abstract

Convolutional neural networks (CNNs) have dominated various applications, from advanced manufacturing to autonomous cars. The layers of CNNs are placed in a hierarchy to solve complications on image processing or speech recognition applications. However, the main challenges in using CNNs are latency and memory access due to tens to hundreds of megabyte parameters and operations, which require data movement between on-chip and off-chip to support the computation. Besides, with edge applications such as smart sensors, wearable, and autonomous devices, security and latency are essential considerations. There is a gap between the designers who try comprehensive CNNs with better efficiency and the hardware architects who simplify them. Many researchers have attempted to speed up the CNN performance by using graphical processing units (GPU); yet, the power consumption on GPU remains a critical issue. Moreover, the computation is subject to rigorous area and power constraints in the inference stage due to limited resources. For energy cost-efficiency, developing low-power hardware for CNNs is a research trend. In the third generation, the Spiking Neural Networks (SNNs) with biological plausibility and similarity to the functionality of the human brain are emerging. A more comprehensive study is expected to understand the inherent behavior of SNNs, especially under adversarial attacks. My research focuses on the following problems to address these challenges:

1. A primary visual cortex inspired feature extraction hardware model is created. To combine the edge and SLIT functions, the model can reduce the

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training time in deep neural networks. Training time is diminished by 40%, 40%, and 32%, respectively, with MNIST, CIFAR, and SVHN databases on Lenet-5 and CNN models. It also decreases by about 10% on larger paradigms such as VGG-16 and VGG-19 with the CIFAR database. Notably, the SLIT architecture efficiently merges with most popular CNNs at a slightly sacrificing accuracy of a factor of 0.27% on MNIST, ranging from 0.5% to 1.5% on CIFAR, approximately 2.2% on ImageNet, and remaining the same on SVHN databases.

2. An optimization hardware model for the inference phase is showed extremely efficiently when applying the SLIT function. Latency, power, and hardware resources of the inference step are evaluated on the chip ZC7Z020-1CLG484C FPGA with Lenet-5 and VGG schemes. On the Lenet-5 architecture, the results are reduced by 39% of latency and 70% of hardware resources with a 0.456 W power consumption compared to previous works. It is also decreased approximately 10% on hardware resources and latency with the VGG models. An advance in latency is also proved in this research, with an enhancement in the range of 2.6% to 16% when being compared with the traditional approach.

3. An efficient success in adversarial attack applications when applying SLIT function into deep spiking neural networks. In against adversarial attack for deep spiking neural networks through white-box settings with different noise budgets and variable spiking parameters, the proposal also improves the accuracy of the results when increasing noise budget. With white-box adversarial attack applications on SNNs, the accuracy of the proposal is approximately 70% higher robustness than the previous works.

Keywords:

primary visual cortex, image classification, convolutional neural network, FPGA, feature extraction, spiking neural network, vitis AI, adversarial attack

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1 Introduction

1.1 Overview

The human visual resolution is about 20K×20K neurons, and the primary visual cortex (V1) comprises 140 million neurons [1]. V1 has special functions such as detect object angles in a steady increase every 10°, left and right parallax, movement direction, and approach. The 1K×1K central area is more sensitive than the periphery, and 25 neurons corresponding to a 5x5 pixel block in the image are arranged in 18 separate directions for each left and right hemisphere [2]. Following the general theory, this research assumes that there are the same amount of neurons in 36 motion directions, and it is estimated that about half ($(18 \times 2 + 36) \times 1\text{K} \times 1\text{K} = 72$ million) of the neurons will be placed in the middle. The average ratio of the number of neurons to the number of pixels is 2.8:1 (36 neurons/25 pixels). There are $25 \times (36 + 36) = 1800$ neurons in the center, and (140 million - 72 million)/(20K x 20K - 1K ×1K)× $25 = 4260$ neurons in the periphery. Therefore, it is reasonable to think that the detailed structure above is based on the blueprint, not acquired by learning.

Many prototypes based on biological [3], statistics [4], or physical principles [5] are presented as the primary visual cortex model. Due to the complexity of fashioning the visual cortex, only specific functions of the visual system are usually considered. A feature extraction model is hypothesized to be made through a sequence of feed-forward and feed-backward loops. This process is often represented as an imitation of the receptor fields of neurons in the layer. A regularly feed-forward processing hierarchy of visual information is convolutional neural networks [6]. The first layers extract features from inputs, and the last layers perform classification.

The main challenges in using CNNs are latency and memory access [7, 8] due to tens to hundreds of megabyte parameters and operations, which require data movement between on-chip and off-chip to support the computation. Security and latency are important considerations in edge applications such as smart sensors, wearable, and autonomous devices [9, 10]. We have recently surveyed the performance of state-of-the-art CNNs in terms of accuracy, size, and potentiality

of various hardware platforms. The results reveal a gap between the designers who strike for comprehensive CNNs with better efficiency and the hardware architects who try to simplify them [11, 12]. Many researchers have attempted to speed up the CNN performance using graphical processing units (GPU) [13, 14]. Moreover, the computation is subject to rigorous area and power constraints in the inference stage due to limited resources. Therefore, many data scientists are focusing on increasing inference performance by designing various accelerators.

Field Programmable Gate Arrays (FPGAs) have become the best candidate for trade-off cost, flexibility, and performance in deep learning processor designs [15]. FPGAs are suitable for computationally intensive algorithms that result in a faster speed and efficient energy. A few highlights of these approaches include binary weight quantization, parameter reduction, memory bandwidth optimization, and data-flow optimization [16, 17, 18, 19]. It is essential to create a highly flexible architecture that can mold itself into the given CNNs and achieve a higher resource utilization reduction. Moreover, due to the largest input size, the first few layers that typically contribute to the most significant latency on CNN leave plenty of room for improvement.

Because of their biological plausibility and comparison to the human brain functionality, Spiking Neural Networks (SNNs) have appealed to many researchers [20, 21, 22, 23, 24]. SNNs consume lower energy when executed on neuromorphic hardware than other network topologies. The asynchronous interaction between neurons and the event-based propagation of the information through layers can achieve high energy efficiency. These features strengthen attention on neuromorphic structures, for example, IBM TrueNorth [25] and Intel Loihi [26]. Besides investment in enhancing accuracy, a recent security perspective also considers SNNs compared to conventional deep neural networks (DNNs).

1.2 Research Contribution

This dissertation aims to create the feature extraction hardware model inspired primary visual cortex principle and apply it in the current deep neural network model to improve performance. This thesis not only provides the algorithms but also describes evaluation both on software and hardware architecture. In summary, the main contributions of this dissertation are:

- The first proposal presents the primary cortex hardware structure, which includes five functions: edge detection, SLIT detection, parallax detection, moving XY detection, and approach detection. These algorithms are efficient for hardware resources when comparing with current algorithms in state-of-the-art.

- The first layer, which contributes most of the training time and latency on current CNNs, is replaced with the SLIT function. The new scheme for the deep neural network has an efficient performance. With MNIST, CIFAR, and SVHN databases on Lenet-5 and CNN models, training time is diminished by 40%, 40%, and 32%, respectively. It also decreases by approximately 10% on larger paradigms such as VGG-16 and VGG-19 with the CIFAR database. Notably, the SLIT architecture efficiently merges with most popular CNNs at a slightly sacrificing accuracy of a factor of 0.27% on MNIST, ranging from 0.5% to 1.5% on CIFAR, approximately 2.2% on ImageNet, and remaining the same on SVHN databases.

- The hardware circuit optimization for the inference step on the Lenet-5 scheme is proposed. The architecture reduces 39% of latency and 70% of hardware resources with a 0.456 W power consumption compared to previous works. The proposal has the same accuracy with higher throughput on most deep neural networks when implementing on the DPU platform.

- An efficient success in adversarial attack applications when applying SLIT layer on spiking neural networks that investigate the effect of structural parameters such as membrane threshold and time window. The input extracted from our model increases the security of SNN under adversarial attack problems. In against adversarial attack for deep spiking neural networks through inherent structural parameter method, the proposal also improves the accuracy of the results when increasing budget noise.

1.3 Dissertation Layout

The thesis is divided into six chapters which are organized as follows:

- Chapter 1 introduces the overview, contributions, and layout of this research.
- Chapter 2 gives an overview of the deep neural network. Then, the preliminary of convolution neural networks is summarized. Finally, the related works are presented.
- Chapter 3 presents the details of each function in our primary visual cortex hardware. In this context, the simple algorithm to integrate hardware design is described. All of the algorithms include just simple circuits such as AND, OR, COMPARISON, SHIFT. The optimized circuits, when implementing on the hardware platform, are showed in this chapter. The first three layers are currently optimized for the network like the Lenet-5 scheme, and the first two layers are reconfigured on the systems like VGG-16
- Chapter 4 shows the details of the results on the software platform. In this chapter, the experiments are conducted on Tensorflow and Keras to the compare accuracy and the training time.
- Chapter 5 analyses the extracted hardware resources and latency with the Vivado_HLS. This chapter also manifests the IP core of Lenet-5, which is embedded into the SoC. The DPU architecture based on the Vitis AI platform that conducts the inference on the ZCU_102 board to compare with state-of-the-art is also presented.
- Chapter 6 give a proposal on adversarial attack application for spiking neural network. How to improve the accuracy of SNN under the adversarial attack phenomena is clearly presented in this chapter
- The last chapter of this thesis concludes and emphasizes the main contributions to my work. Then, some ideas for future works are addressed.

2 Background and Related Work

This chapter introduces the basic concepts relating to the arguments discussed in the thesis. First, the meaning of Artificial Intelligence (AI) and related topics are presented to understand the evolution of neural networks (NNs). Next, I summarize the content of CNNs. Finally, the related works that optimize the architecture of deep neural networks on software and hardware are reviewed.

2.1 Machine Learning

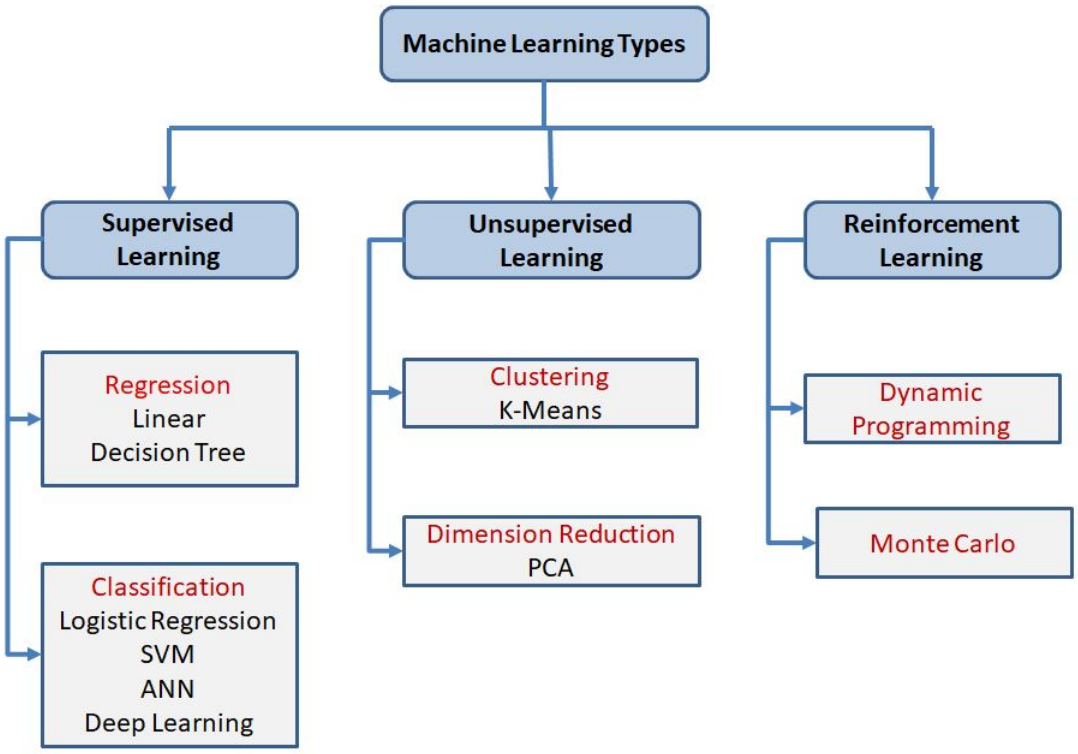


Figure 1. Machine learning category

Artificial intelligence (AI) is the psychology of imagining intelligent machines to accomplish specific goals and tasks as humans do is artificial intelligence (AI). It is a vast topic, going from video games to autonomous driving and including every

application in which a machine can learn or predict something. AI indicates the ability of a machine to learn information (training) and solve problems without being explicitly programmed every time. We temporal categorize the AI into these subgroups, as shown in Fig. 1.

2.1.1 Supervised learning

Supervised learning is a method for predicting a label of a previously unseen instance from the previous information about input and the target output [27, 28, 29, 30]. It can be seen as a machine learning task of inferring a function from training data to correctly map a class for invisible cases. Each training sample (consisting of an input vector X and its corresponding target output vector Y) may feed into the network several times so that the actual output can approach the target output. An error value is calculated from each given sample as a function of the difference between the target outputs vector, Y, and the actual output vector, Z (for example, min square error or entropy error). In neural networks, this error is utilized to update connection weights in the network. That network can generate a result closer to or exactly the desired output next time if a similar input pattern appears. The two most common approaches to minimize this error in deep neural networks are the gradient descent rule and the learning windows rule [31, 32]. First, to reduce error, a gradient descent-based learning algorithm finds a local minimum of linear systems. The second type changes the synaptic weights as a function of the relative timing of pre-and post-synaptic action potentials.

2.1.2 Unsupervised learning

Unsupervised learning is a technique for searching data to find some natural structures in the input under an unknown probability distribution. The convergence examination of unsupervised learning is much more difficult than other learning as the input datasets are unlabelled. For traditional artificial neural networks, an n-dimensional input is processed by the same number of computing units or by minimizing a cost function for feature extraction, dimension reduction, clustering, etc. Self-organizing map (SOM), adaptive resonance theory (ART), independent component analysis (ICA), Hebbian learning, principal component analysis

(PCA) [33, 34], and BCM rule are generally employed unsupervised learning algorithms. In spiking neural networks, Hebbian learning, BCM rule, and STDP rules are famously used as unsupervised learning methods in real-world applications. STDP learning is an asymmetric form of Hebbian learning in tightening temporal correlations between weakening and strengthening connections. Since unsupervised learning takes into account competition and sidelong interference, the weights of the winner neurons are increased. In contrast, other neurons sustain a small weight reduction. Furthermore, the STDP learning rule regards the lateral inhibition between pairs of spikes: a pre-post pairing causes potentiation, and a post-pre pairing causes depression. The most recent presynaptic and postsynaptic spike pair is adapted to detect the correlations of the next attempting fire.

2.1.3 Reinforcement Learning

Reinforcement learning is a control optimization technique that is used to recognize the best action in every state visited by the system [35, 36, 37, 38]. In reinforcement learning, a general error signal back ("reward") is determined in every state that describes how well the system performs. The typical framing of reinforcement learning is the following scenario. An agent takes action in an environment. Based on the action, the agent changes state, and the learning algorithm also receives a reward signal a short time later. The current state and reward are both then fed back into the agent. The algorithm modifies its strategy to achieve the highest reward.

2.2 Artificial Neural Networks

Humans aim to create machines that work like the brain, so it is reasonable to talk about brain-inspired computation. The artificial structures that model the real biological neural networks are called artificial neural networks (ANNs) [39] or just neural networks (NNs). They are computational models composed of many layers of artificial neurons, which is the main computational unit of the brain. The structure of ANN is shown in Fig. 2. The neurons are connected in a NN, so the output of one neuron, called the axon, represents one of the inputs of another

one, called dendrites. The outcome of a neuron corresponds to the weighted sum of the inputs. A synapse is a connection between an axon and a dendrite. This link between the output and input of two neurons is called presynaptic and postsynaptic neurons, respectively. Scales the axon output signal by a quantity called weight. A neural network learns information by updating the values of the weights in response to input stimuli. This process is called learning or training. Once the NN is trained using the training data, the values of the weights are determined. Performances of the NN are evaluated on the test data. Hence considering a complete dataset, we can recognize the training data used for the training process and the test data used for the inference process.

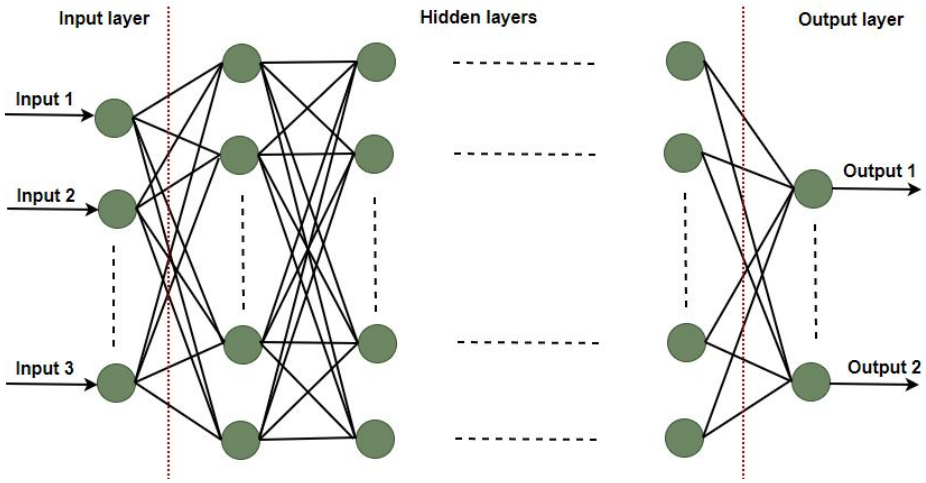


Figure 2. General ANN architecture

2.3 Preliminary Convolutional Neural Networks

Through development over 20 years, the network initially inspired by neuroscience has attracted spacious attention in image processing and computer science [40, 41, 42]. Today, some object recognition systems based on CNN can recognize objects with super-human accuracy. As we can observe in Fig. 3, a convolution neural network (CNN) is a subset of NN with more than three layers. In general, the first layer is called the input layer, while the last one output layer. The layers between these two ones are called hidden layers. The network is deeper, increasing the number of hidden layers. CNN perceives an object using the feature

extraction step and the classification phase. The feature extraction step included the convolutional and sub-sampling layers to find variances of an input image such as lines and edges. Combining the fully connected (FC) layers, the classification phase decides the most likely class object based on the extracted features. CNN can achieve a highly accurate classification performance using the convolutional (CONV), sub-sampling, and FC layers.

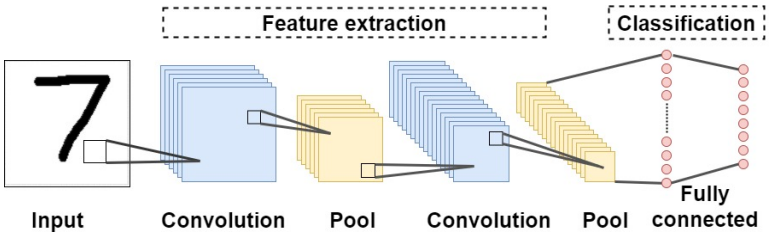


Figure 3. General CNN architecture

The CONV layer receives features as input and executes convolution operation with a filter kernel window to generate one pixel in one output feature map. The output channels are filtered through an activation function such as Relu, Sigmoid, and Tanh. Total output feature maps form a set of the input channels for the next CONV layer. Summary of the process which calculates one output channel is formulated in Eq. 1.

$$O_j^k = f(\Sigma_{i \in M} I_i^{k-1} * W_{ij}^k + b_j^k) \tag{1}$$

where O_j^k is the current output of the j^{th} channel at k^{th} layer, I_i^{k-1} is the previous feature map of the i^{th} channel in M channels, W is the ij^{th} kernel filter, b_j^k is corresponding the bias of the j^{th} channel, and f is the activation function, the symbol "$*$" is the element-wise multiplication operation.

The sub-sampling layer or the pooling layer is generally sandwiched between the two CONV layers. The pooling layer reduces the size of feature maps from the previous layer. Besides, this layer is employed to avoid the over-fitting problem and redundancy in the channels. There are two main pooling methods: mean-pooling and max-pooling. The output of the max-pooling (MP) layer is determined as shown in Eq. 2.

$$u_{i,j}^m = \max_{0<=i,j \in P} u_{(i,P+i),(j,P+j)}^n \tag{2}$$

where u^m is the max output value in the kernel size P of the m^{th} channel, the u^n is input value in the kernel size P.

The FC layers that control object classification into various categories in CNNs are conjoined after multiple convolutional and sub-sampling layers. The term "fully connected" means that all neurons in the previous layer are connected to all neurons in the next layer. For example, the last layer of the Lenet-5 has ten possible outputs, and each output corresponds to a number from "0" to "9". A neuron output V_k^{out} in the FC layer is obtained by using Eq. 3. It is a typical matrix multiplication and addition with a bias.

$$V_k^{out} = \Sigma_{i=0}^{N} W_{ki} \times V_i^{in} + bias_k \tag{3}$$

where W_{ki} is weights corresponding with N input neurons at k^{th} position, V_i^{in} is the total neurons of the previous layer, and $bias_k$ is the bias of k^{th} output neuron.

2.4 Related Work

2.4.1 Researches on primary visual cortex

The purpose of the visual system is to predict neural responses to arbitrary stimuli, including those seen in nature. To achieve this goad, researchers create models based on one or more linear receptive fields. Basic models of neurons at the earliest stages of visual processing (retina, LGN, and V1 simple cells) typically include a single linear filter. On the other hand, models of neurons at later processing stages (V1 complex cells and beyond) require multiple filters [43].

The primary visual cortex model following the feedforward pathways begins with the description by Hubel and Wiesel (1962) [44]. Two functional classes of cortical cells: simple cells and complex cells, are famously described in the research of Hubel and Wiesel. The simple cells respond to oriented stimuli (e.g., bars, edges, gratings). The complex cells tuned to oriented stimuli tend to have larger receptive fields and exhibit the location of the motive within their receptive fields. A V1-like circuit that connects a complex cell to an array of simple cells is shown in Fig. 4. A simple cell in Fig. 4(a) (lower green cell) was gained by pooling over upper green cells aligned along a preferred axis of orientation. At the next stage, a complex cell in Fig. 4(b) can be obtained by selectively pooling over simple afferent cells with the same preferred orientation.

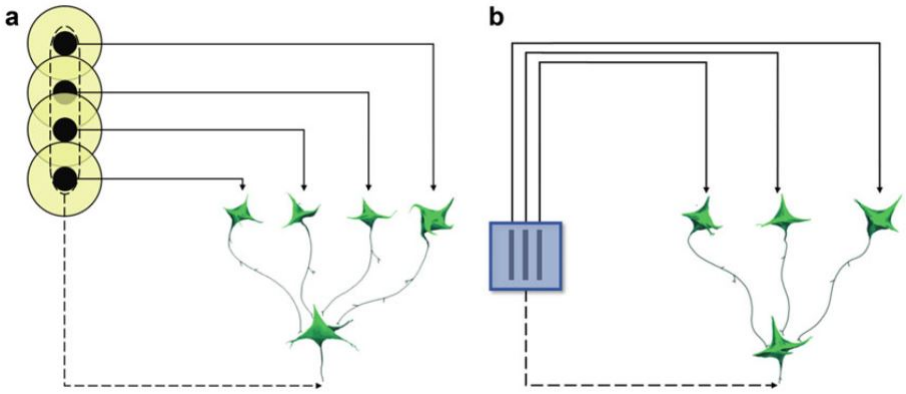


Figure 4. V1_like or Hubel and Wiesel model. Source: Fig.1 of the reference [44]

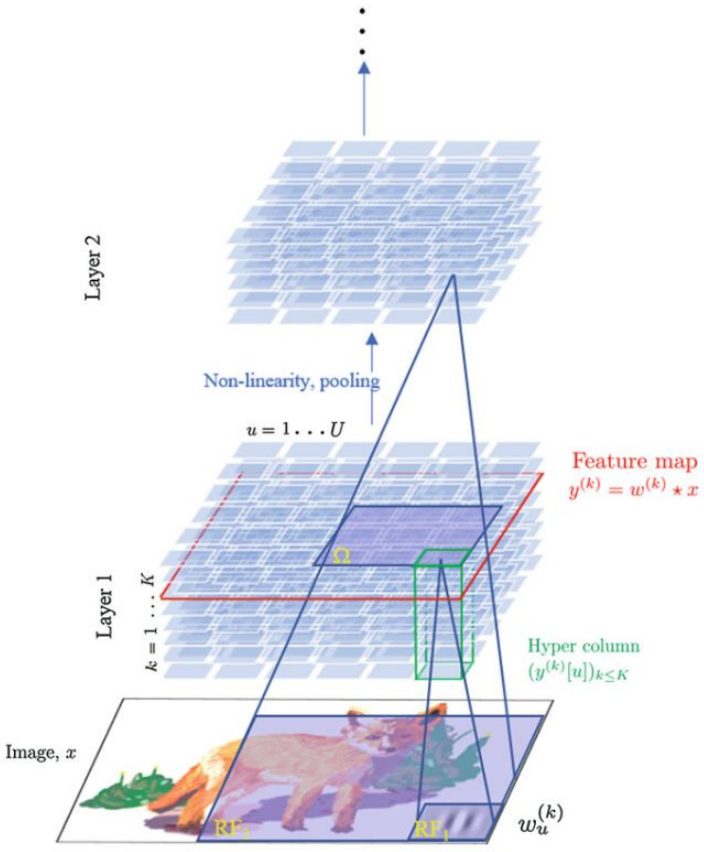


Figure 5. Models of the visual system based feed-forward wiring diagram. Source: Fig. 4 of reference [44]

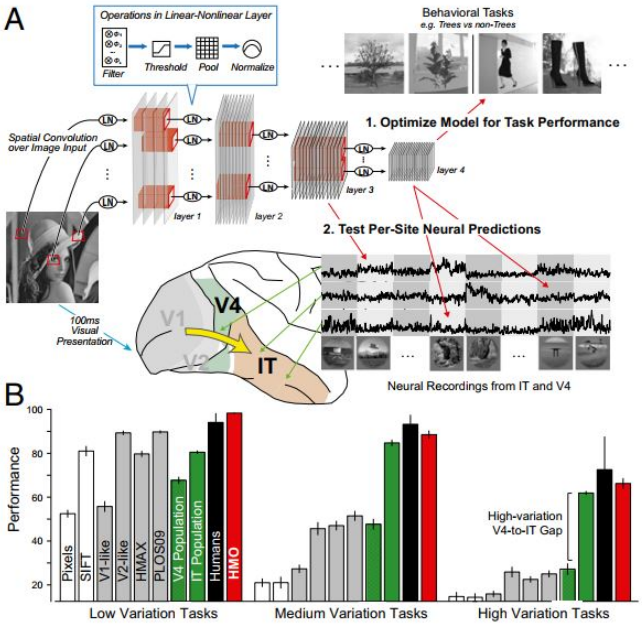


Figure 6. Neural-like model via performance on image classification task. Source Fig. 2 of reference [45]

Up-to-date feedforward models that determine the part of the operation in the visual cortex by introducing further, "deeper" processing stages, each with numerous learned filters. These models extend the Hubel and Wiesel's circuit from V1 to higher areas of the ventral stream. A general wiring diagram of a feedforward model of the visual system is shown in Fig. 5. Using the same classifier training protocol as with the neural data and control models, the hierarchical modular optimization (HMO) got better results on low variation tasks. However, for more variation tasks, HMO is not equal to the human object recognition ability like in Fig. 6. So, there is a need for more study to visualize exactly what happened in V1 and V4 regions [45].

2.4.2 A review feature extraction methods for image classification

Feature extraction creates new features by merging original bands. The new features store most of the important information. The feature extraction methods can be subdivided into four classes: knowledge-based such as non-parametric weighted feature extraction (2004), maximum noise fragment (1998), local binary

pattern (1990), statistical, for example, principal component analysis (2002), independent component analysis (2011), wavelet-based such as discrete wavelet transform (2002), and deep learning-based: convolutional neural network (2012), deep belief network (2016). Knowledge-based methods improve specific characteristics of the relevant bands to separate the objects or surface features of interest. The statistical feature extraction transforms the high-dimensional data into some lower-dimensional feature space reducing redundancy and enhancing class separability. The progress of these methods depends on their capacity to feature transformation without sacrificing the loss of information. The wavelet-based feature extraction relies on wavelet transform decomposing the signal into constituent wavelets of different scales and positions.

Table 4. Classwise and global classification accuracies obtained using major conventional spectral feature extraction techniques for Pavia University. The number of features is given within brackets.

Class	Raw	PCA (6)	MNF (5)	DWT (7)	ICA (15)	NWFE (40)	CNFE (11)	DBFE (27)
Class 1	0.8050	0.8394	0.8255	0.8134	0.8357	0.7593	0.7579	0.9155
Class 2	0.7185	0.6692	0.6673	0.6619	0.6525	0.5606	0.7691	0.8683
Class 3	0.7612	0.7254	0.7226	0.7374	0.6762	0.6986	0.7774	0.8144
Class 4	0.9627	0.9429	0.9287	0.9469	0.9504	0.8301	0.8619	0.9461
Class 5	0.9861	0.9776	0.9981	0.9907	0.9981	0.9870	0.9946	1.0000
Class 6	0.8263	0.8235	0.7887	0.7555	0.7927	0.5093	0.6721	0.9232
Class 7	0.8849	0.8751	0.8663	0.8784	0.8470	0.8394	0.9046	0.8950
Class 8	0.8428	0.8176	0.7746	0.8069	0.8156	0.7433	0.8937	0.8710
Class 9	1.0000	0.9917	0.9986	1.0000	0.9945	0.9807	0.9798	1.0000
Global κ	0.8041	0.7838	0.7717	0.7691	0.7702	0.6710	0.7269	0.8968
OA (%)	85.16	83.49	82.65	82.46	82.81	74.92	79.21	92.34

Table 5. Classwise and global classification accuracies obtained using major deep learning spectral feature extraction techniques for Pavia University. The number of features is given within brackets.

Class	SAE (60)	SSAE (60)	DBN (30)	CNN (9)
Class 1	0.9146	0.9188	0.9276	0.9346
Class 2	0.9524	0.9465	0.9432	0.9518
Class 3	0.8812	0.8937	0.9128	0.9124
Class 4	0.9627	0.9598	0.9584	0.9457
Class 5	0.9894	0.9914	0.9926	0.9842
Class 6	0.9063	0.9126	0.9077	0.9014
Class 7	0.9149	0.9189	0.9209	0.9165
Class 8	0.8928	0.8876	0.9143	0.9248
Class 9	0.9924	0.9925	0.9915	0.9965
Global κ	0.9236	0.9284	0.9316	0.9368
OA (%)	93.16	93.48	94.31	94.62

Figure 7. Classwise and global classification accuracies using various feature extraction techniques for Pavia University database. Source Table 4 and Table 5 of reference [46]

Comparison performance on image classification application based on Pavia university dataset show on Fig. 7. The results show that feature extraction can reduce dimensions without significantly compromising classification accuracy. Supervised techniques provide better accuracy than their unsupervised counterparts. In the vacancy of training data, unsupervised feature extraction can provide acceptable solutions. It is also observed from the results that spatial features produce complementary information that can help to improve classification accuracy. Recently emerged deep learning techniques have shown promising performance. Deep learning methods hierarchically learn features with the help of complex, layered architecture [46].

2.4.3 Approaches to accelerate CNN inference on FPGAs

In response to the hurdles of CNNs, many researchers have tried to optimize memory access or convolution operations. Recent works showed that sparsity optimization involving pruning and exploiting activation sparsity could reduce 89% of memory access and 67% of computation operations [47]. Activation sparsity, which can cut memory accesses and multiply-accumulate (MAC) operations by a half [48] based on rectified linear unit non-linearity to produce many zero outputs. The pruning and compression were also investigated with the Bayesian network. These reductions have nevertheless required hardware that was customized with the data movement and control. The reducing parameter approaches [49, 50] with a factor of 50× were studied due to the expense of many MAC operations. The low-rank approximation (LRA) that obtained a sparse convolution 2 - 4.5× faster than the corresponding value at the absence of sparsity with a 1% accuracy loss was reported by Denton et al. [51] . Due to a large number of hyper-parameters, the LRA has remained to be a big problem in training.

Another approach is bit-width optimization, which aims to decrease parameter bit-width from a floating point to a fixed point. This investigation reduced the precision to get higher efficiency in exchange for memory access and computation operations. Ternary weight network and BinaryConnect [52, 53] diminished the bit-width of weights to 2-bits or 1-bit. Some studies quantized the activation function of the neural network, which achieved a significant reduction in memory or computation cost [8, 54]. These proposals, nevertheless, were a trade-off for

a considerable accuracy loss. Researchers have also discovered the computation of CNNs in other domains to reduce complexity. Fast Fourier transform (FFT) applied a single filter in the CONV layer is an example of this attempt. As a result, the gain of compact network architecture is the loss of accuracy.

When accelerating a CNN to an FPGA device, the challenge is to find an efficient mapping model [55]. Current FPGA-based accelerators for CNNs rely on three main optimizations to efficiently infer CNNs. Algorithmic Optimizations for FPGA-Based CNN Acceleration accelerate the execution of convolutional and fully connected layers [56, 57, 58, 59, 60, 61, 62]. Computational transforms are employed on the feature maps and kernels to accelerate the execution of conv and FC layers. This method focuses on vectorizing the implementations and reducing the number of arithmetic operations occurring during inference. Various software libraries, such as OpenBlas CPUs and cuBLAS for GPUs, are a platform to deploy these computational transforms. Besides this, multiple implementations make use of such transforms to map CNNs on FPGAs.

The FPGA datapath optimizations for FPGA accelerators aim to solve the resource limitation of FPGA devices. [57, 63, 64, 65, 66, 67, 17, 68, 69, 70, 71]. Early FPGA-based accelerators for CNNs implemented systolic arrays to accelerate the 2D filtering in convolutions layers [72, 73, 74, 75, 76]. Finding the optimal PE configuration can be seen as a loop optimization problem [77, 78, 79, 18]. It is impossible to fully exploit all the parallelism patterns, especially with the sheer volume of operations involved in deep topologies. Applying dataflow process networks (DPNs), static data-flow (SDF) to accelerate CNN implementations on FPGAs is investigated in [80, 81, 82].

Approximate computing of CNN models the computational transforms, pruning, and quantization technologies are other approaches for accelerating FPGA CNNs [16, 83, 84, 85, 86, 16, 87, 88, 89, 54, 52, 90, 91, 92, 93, 94, 95, 96]. Several studies in [97, 98, 99] demonstrate that inference of CNNs can be achieved with reduced precision of operands. Also, works in [100, 101, 102] demonstrate fixed-point arithmetic applicability to train CNNs. As highlighted in [103], CNNs as over-parametrized networks and many weights can be removed or pruned without critically affecting the classification accuracy. In its simplest form, pruning is performed according to the magnitude, such as the lowest values of the weights

are truncated to zero [104]. The summary of optimization for FPGA accelerators is showed in Fig. 8.

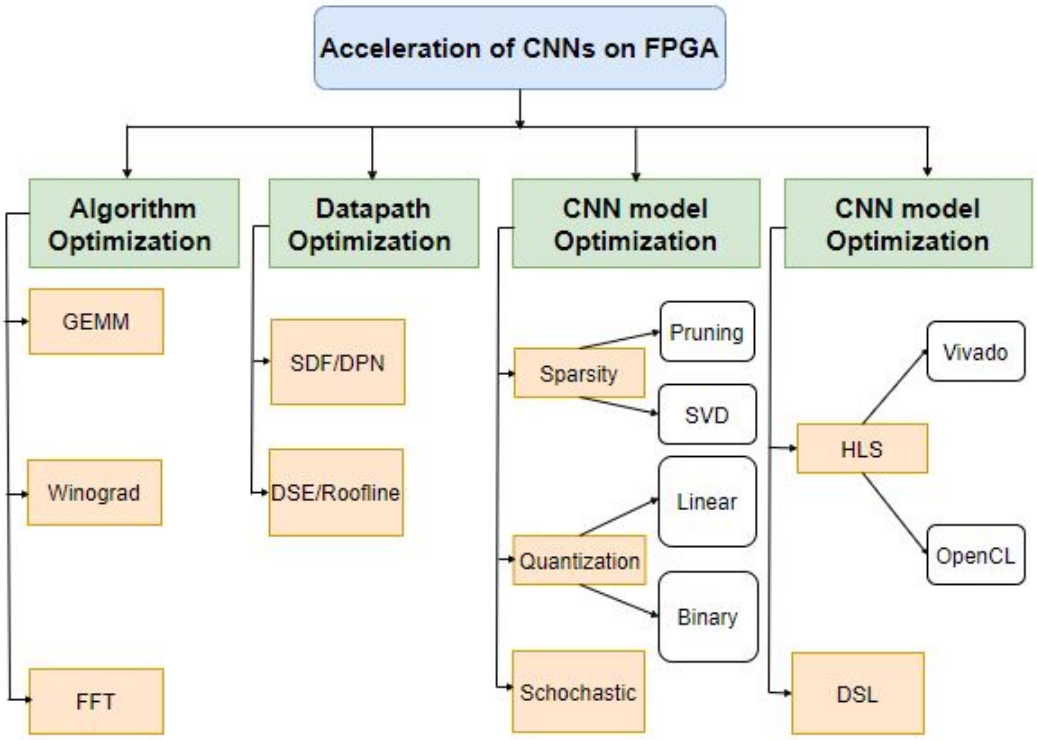


Figure 8. Approaches to accelerate CNN inference on FPGAs

For hardware generation, the using tools supporting circuit implementation on FPGA are investigated. These tools support estimating the new idea algorithm on hardware without deep expertise on FPGA/ASIC. The high-level synthesis (HLS) tools [105, 106, 107, 108] that emerge and use frequently on research is Vivado of Xilinx and OpenCl of Intel [109, 110]. Domain-specific languages (DSLs) [111, 112] are another approach.

3 Feature Extraction Primary Visual Cortex Hardware Model

The proposed prototype is a partial implementation of the standard model, which focuses on information-processing mechanisms in V1 [1, 113]. Generally, realizing the large-scale computations needed for the simulation is the biggest challenge in making a biologically accurate model. The complex calculations are simplified with uncomplicated hardware circuits. The results indicate that the proposal is able to keep the information necessary for the feature description

3.1 The Functions of the Primary Visual Cortex Hardware Model

3.1.1 Edge Detection

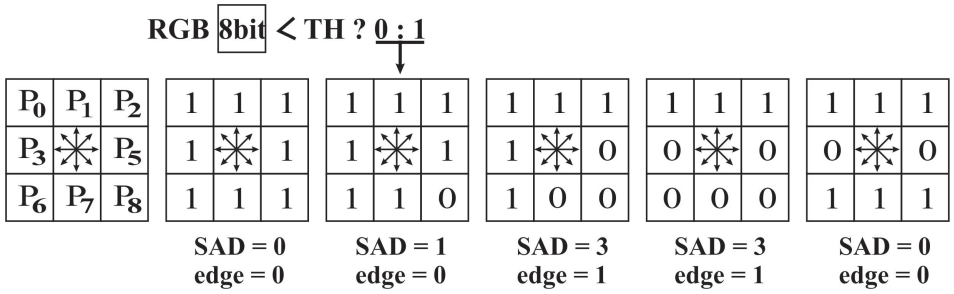


Figure 9. Edge detection

Edge detection plays a vital role in feature extraction. My proposal was formulated in Fig. 9 to achieve high efficient energy architecture. I recommended an edge detection algorithm that is performed by comparing the sum of absolute differences (SAD) of values applying Eq. 4 in four distinct directions with a threshold (TH) in a 3x3 area like in Eq. 5.

$$SAD = \begin{cases} 0 & if \quad P_i = P_{8-i} \\ 1 & if \quad P_i \neq P_{8-i} \end{cases} \tag{4}$$

where P_i is the value of a pixel in 3x3 window with i = (0, 1...8).

$$edge = \begin{cases} 0 & if \quad \Sigma_{i=0}^{3} SAD(P_i, P_{8-i}) < TH \\ 1 & otherwise \end{cases} \tag{5}$$

$$P_i = \begin{cases} 0 & if \quad RGB_{8bit} < TH1 \\ 1 & otherwise \end{cases} \tag{6}$$

For simplification toward hardware, the RGB 8-bit was diminished to 1-bit by considering with the other threshold (TH1) in Eq. 6. There was no edge if the sum of SAD was less than TH1; otherwise, the output was an edge. The four directions we suggested were 0°, 45°, 90°, and 135°. The hardware includes AND gate, OR gate, Comparison, and Shift circuits, which help enhance the effectiveness of the edge problem over other studies. This design can realize a parallel circuit with high speed and low resources on a field-programmable gate array (FPGA).

3.1.2 SLIT Detection

According to the principle of V1, most of the significant information is discovered in the central radius than at the periphery when observing an object. To replace the first layers, which was inspired by the primary visual cortex in the CNN model, a shift circuit in a range of 0° to 157.5° with a gradual increase every 22.5° for 4x4 window shown in Fig. 10 is proposed. The SLIT detection is executed at the base of the edge detection results.

$$ch_t = AND(\Sigma_{i=0}^{3} \Sigma_{j=0}^{3} \theta_{i,j}) \tag{7}$$

$$\theta = \frac{\triangle y}{\triangle x} \tag{8}$$

where θ is a gradually increase every 22.5°, $\theta_{i,j}$ is the E patterns shown in Fig. 9 at examining slope θ in 4x4 window. ch_t is the result of channel or S letters with t = (0, 1,...7)

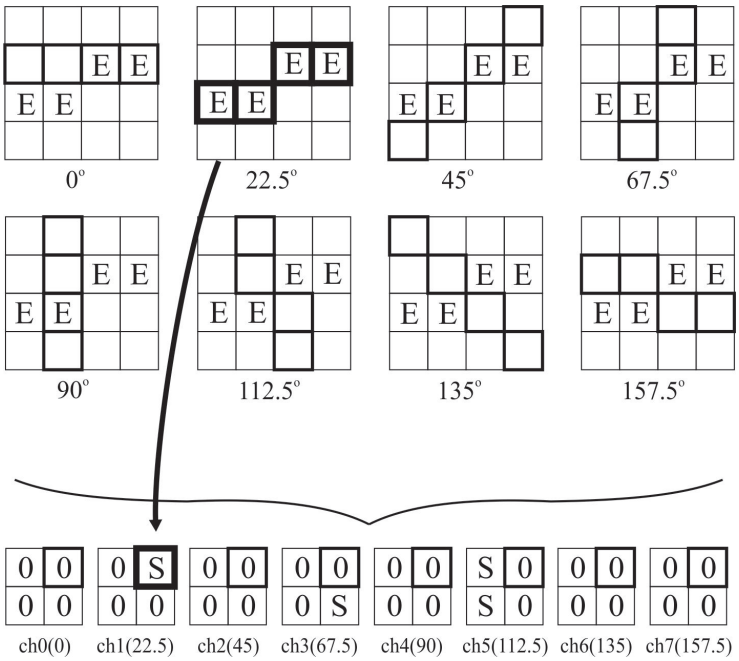


Figure 10. SLIT detection

The result of SLIT detection or ch0 to ch7 in Eq. 7 was an AND gate of 4 input values at the examining slope in Eq. 8. Each element was 1 bit. The number of elements in each channel was equivalent to that in the input image.

3.1.3 Left-Right Parallax Detection

Left-right parallax detection is the equivalent function as a stereo matching. Generally, stereo matching requires about 16x16 SAD operations in Eq. 9, which is not suitable for hardware [114].

$$SAD_{16} = \Sigma_{i=0}^{3}\Sigma_{j=0}^{3}|C_{i,j} - r_{i,j}| \tag{9}$$

where $r_{i,j}$ are the values of reference 4x4 window and $C_{i,j}$ are the values of the candidate 4x4 block.

In Fig. 11, we used the information of the SLIT function above to build the new idea for the parallax algorithm. In the range of 1/16 the width of the vision, a 3x3 window was used to analyze the level overlap of the SLIT information in the left image and right image. The ratio of overlap was the sum of the values of 1 of

AND operation from ch0 to ch7. At the same time, the SAD of the original left and right 3x3 images was obtained. Finally, the right and left parallax detections were for maximizing the SLIT coincidence and minimizing the SAD.

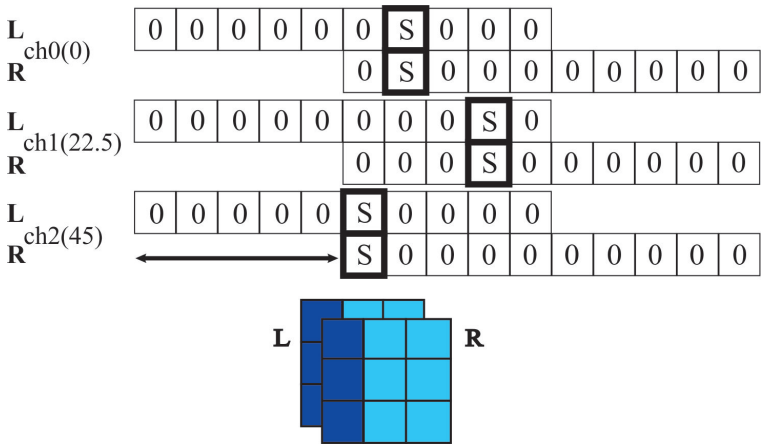


Figure 11. Left/right parallax detection

3.1.4 XY Movement Direction Detection

The Gunnar Farnebäck's optical flow algorithm was applied to determine moving object detection [115]. The horizontal and vertical components were obtained by utilizing Eq. 10 and Eq. 11.

$$H(x,y) = h_1(x,y) + h_2(x,y) \tag{10}$$

$$V(x,y) = v_1(x,y) + v_2(x,y) \tag{11}$$

$$M(x,y) = \sqrt{H^2(x,y) + V^2(x,y)} \tag{12}$$

$$N(x,y) = \frac{M(x,y) - M^{min}}{M^{max} - M^{min}} \times I_{max} \tag{13}$$

$$B(x,y) = \begin{cases} 1 & if \quad N(x,y) \geq \lambda \\ 0 & otherwise \end{cases} \tag{14}$$

where H and V are the horizontal and vertical images. (x,y) is the pixel coordinate, h and v are the horizontal and vertical optical flow components.

The magnitude M(x,y) of the horizontal and vertical optical flows, was calculated, using Eq. 12. The normalizing value N(x,y) of a pixel position (x,y) was processed by using Eq. 13. The output B(x,y) was the comparison to one threshold from Eq. 14.

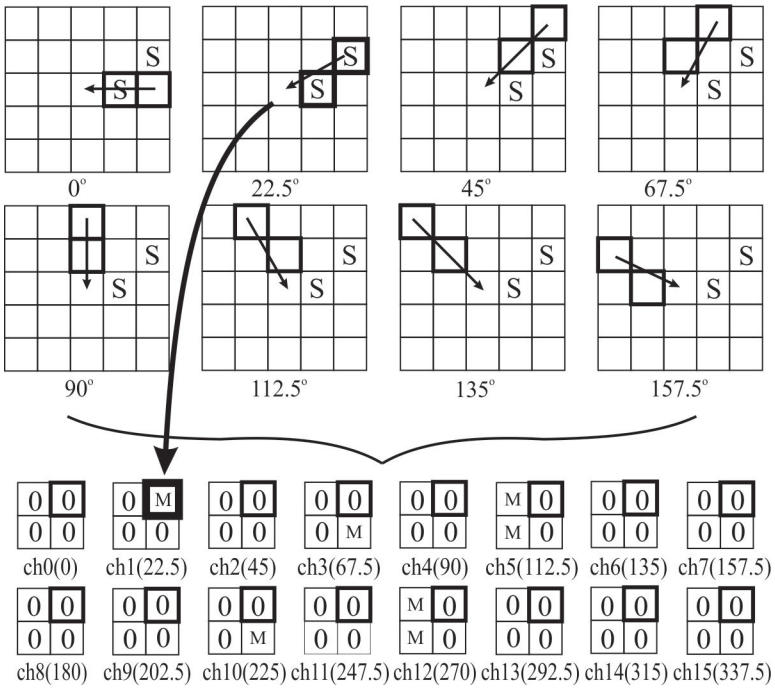


Figure 12. XY movement direction detection

According to the analyzed scheme, multiply, and square root operations are not proper for optimal parallel hardware performance. Antithetical to the above interpretation, in the design, the results of the SLIT function have been applied to determine motion. Unlike the feature detection based on spatial differentiation, the moving direction detection requires time differentiation. M characters or the results of the XY motion detection presented in Fig. 12 is a combination of SLIT detection and the concurrent comparison in which the left and right directions occur at the same moment. AND, Shift, OR, and Comparison functions are simpler than the above operations. The idea can be straightforward to build a high-speed circuit in FPGA. There were 16 output channels, and these channels

could discover the change in the vertical and horizontal directions when the left and right SLITs moved similarly.

3.1.5 Approach Detection

When the left and right SLITs are moved in the same way, the XY moving direction is detected. In contrast, the difference in movement between the left and right SLITs means the approach or separation detection. Six separate output channels in Fig. 13 are the combination of the left and right SLIT information in Fig. 10. It incorporates approach/separation for the right, center, and left eye.

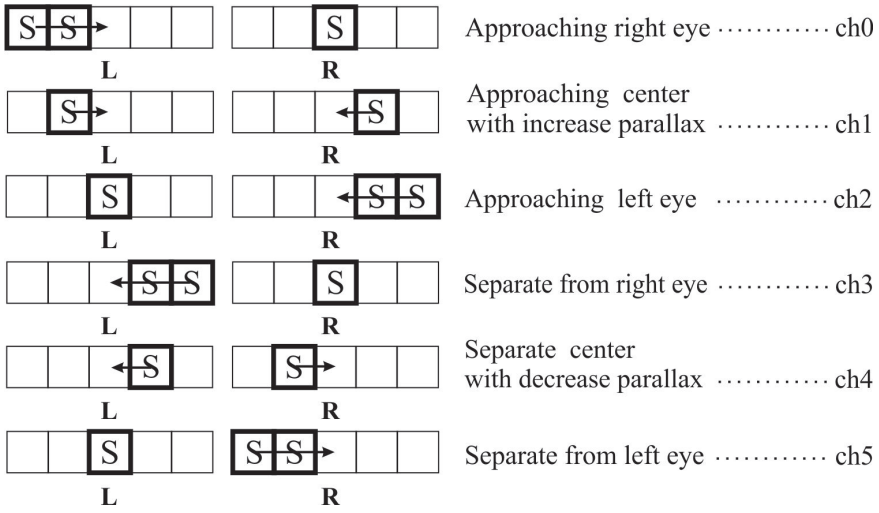


Figure 13. Approach detection

3.2 Reconfigurable Deep Neural Network Using the SLIT Function

3.2.1 SLIT Layer Architecture

In many CNNs such as VGG [116], AlexNet [117], ResNet [118]..., the CONV layer is always the first layer. This layer typically performs a whole number of sliding convolution operations due to the largest input size. The first layer requires much computation time when being compared with other layers. In the CONV layer, with a number of input channels (ICs) and the K×K filters,

there compute six consecutive loops for producing output channels (OCs) in the traditional approach.

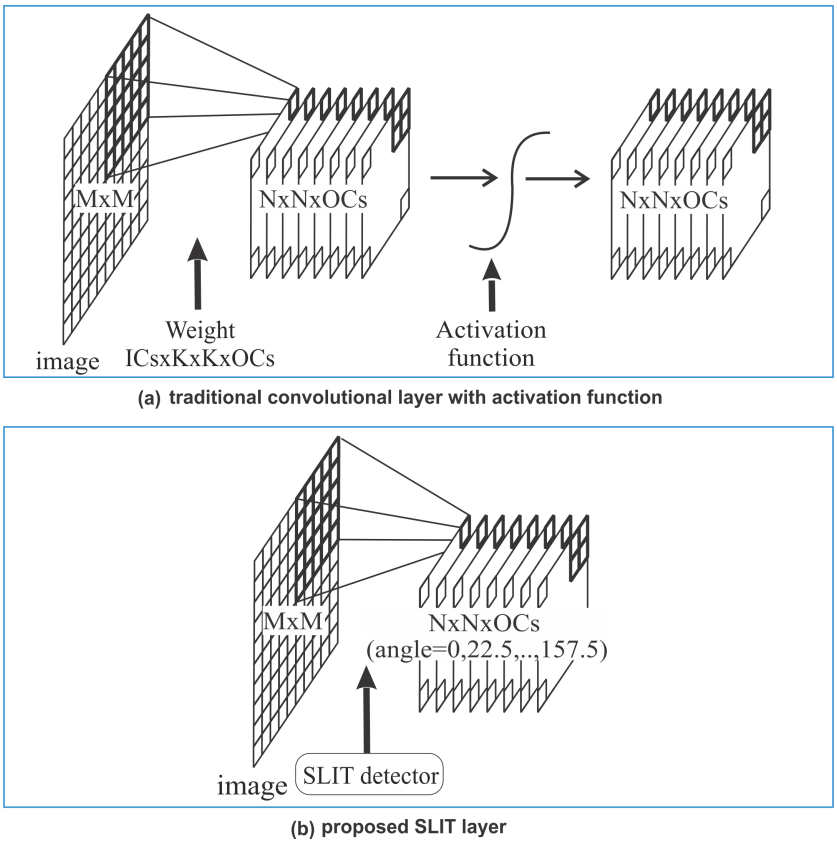


Figure 14. Proposed SLIT layer

In contrast, the proposed SLIT layer presented contains only four continuous loops. Fig. 14(a) explains how to calculate the first CONV layer with the traditional approach. The first CONV layer with a M×M input image is convoluted with ICs×K×K×OCs kernel filters to yield N×N×OCs output channels. Subsequently, the Relu activation function is employed to normalize the output values into a range between 0 and 1. In Fig. 14(b), to obtain N×N×OCs output feature maps like the first CONV layer, we leverage the SLIT layer, as explained beforehand in the motivation section. Due to the binary output, the activation function is discarded after the SLIT layer.

In comparison with the first CONV layer on the original CNNs, the MAC

operation and activation function are eliminated in the proposal. Each input is reused across all filters of different output channels within the same layer in the CONV layer. Therefore, storing memory and power consumption have become enormous. On the other hand, since there are no parameters required for the SLIT layer during the training phase and inference step, memory access and latency are significantly reduced in the proposal. The normalization step for inputs, which are divided by 255, is also ignored in our idea. The Shift, AND, and comparator operations are used to extract feature maps. Consequently, this approach decreases many resources, latency, and energy. Total parameters ($params$) are presented in Eq. 15, and MAC operations ($MACs$) are shown in Eq. 16 are ricocheted in the way that reconstructs with the SLIT layer.

$$params = C\_in \times K \times K \times C\_out \tag{15}$$

where C_in is the number of input channel, K is the size of kernel filter and C_out is the number of output channel.

$$MACs = C\_in \times K \times K \times N\_in \times N\_in \times C\_out \tag{16}$$

where C_in is the number of the input channel, K is the size of kernel filter, N_in is the dimension of output channel, and C_out is the number of output channel.

3.2.2 Next Layer Reconfiguration

Due to the binary output of the SLIT layer, we propose a new scheme to reconfigure the second CONV, max-pooling (MP), and fully connected (FC) layers. We name SCONV, SMP, and SFC layers for the proposed second CONV, MP, and FC layers. MAC operations also occupy most computation time in the second CONV layer, directly following the first CONV layer on CNN. Many works have been investigated to optimize MAC operations, such as using XOR functions [87, 89, 93] . In contrast, we suggest the architecture that employs multiplexer (MUX) operation to determine output feature maps for the second CONV layer. Fig. 15(a) illustrates the process with a 3×3 kernel filter. To receive the second CONV output channel, there require nine multiplication operations. On the other hand, the proposal only uses 9 MUX operations to generate a feature map for the second CONV layer showed in Fig. 15(b).

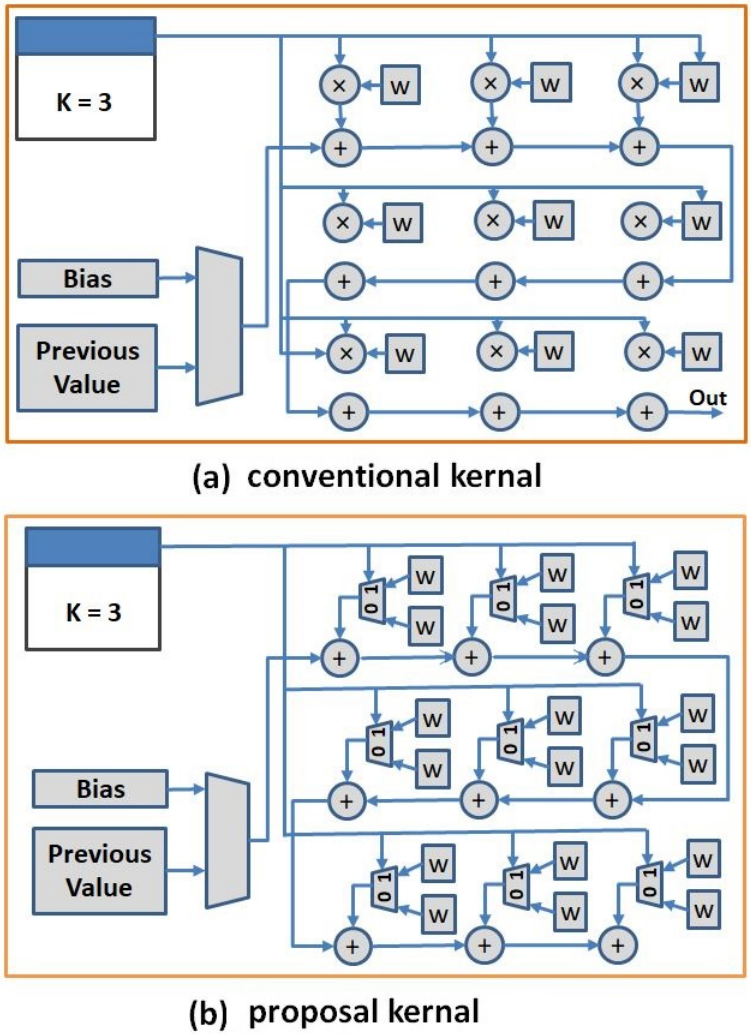


Figure 15. Proposed kernel for the second layer

The proposal excretes all or a part of multiplication operations in the second CONV layer. First, the complete replacement will affect the situation if the SLIT layer only generates eight binary output feature maps in which the input image has one channel like the MINST database. Second, a part of the replacement will take place when the input image has three channels, such as CIFAR, SVHN, or ImageNet database. The SLIT layer yields 11 channels by concatenating eight binary output feature maps of SLIT function with three original channels normalized in range 0 and 1. In this case, output channels of the second CONV layer

are determined by concatenating eight binary output channels of the SLIT layer with three feature maps of the normalized input image.

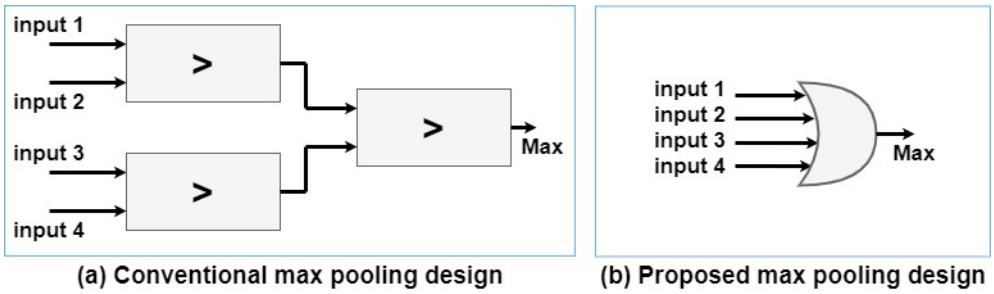


Figure 16. Proposed max pooling kernel

The max-pooling (MP) layer mentioned in Fig. 16 is optimized by utilizing an OR gate to determine the maximum value. Fig. 16(a) reveals that at least three comparator operations are required to detect the maximum value in the 2×2 window at a stride of 2 with the conventional approach. In contrast, the proposed circuit showed in Fig. 16(b) only uses the OR gate to estimate the maximum value for the MP layer. Assuming that there have eight 14×14 output channels from the previous layer, a total of 14×14×3×8 = 4704 comparator operations are expected by applying Eq. 17. On the other hand, the proposal demands 14×14×8 = 1568 OR gates with four inputs.

$$Comp = N \times N \times (K \times K - 1) \times Cout \tag{17}$$

where $Comp$ is total comparator operations required to determine the maximum value, N is the size of the previous channel, K is the kernel size, and $Cout$ is the number of output channels.

The FC proposed layer is affected by a model that consolidates the previous CONV layer and an MP layer. The basic information processing unit of one neural in the artificial network is demonstrated in Fig. 17(a). The inputs are multiplied with corresponding weights, and then outcomes are added with a bias. Fig. 17(b) shows the matrix multiplication replaced by the MUX operations, where the weight values are one. Eq. 18 defines the entire multiplication operations, which occupy most time consumption in the FC, are reduced by the multiplexer operations. Assume that there have 1024 input neurons and 1024

output neurons; by using Eq. 18, the entire 1024×1024 = 1M multiplication operations are pruned.

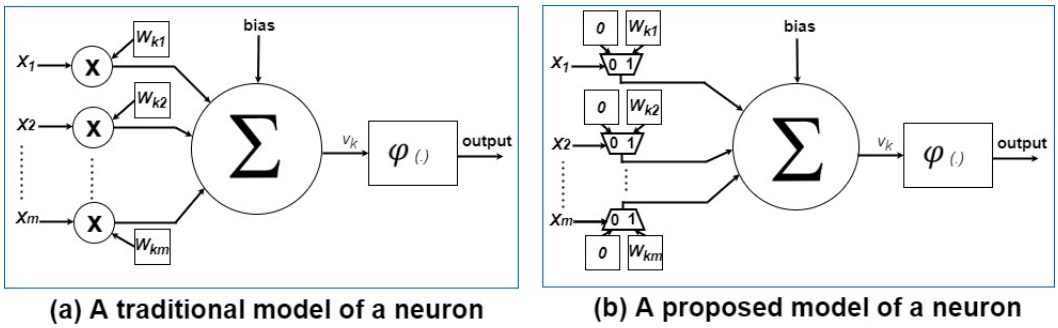


Figure 17. Proposed model of a neuron

$$Muls = Num\_in \times Num\_out \tag{18}$$

where $Muls$ is total multiplication operation to calculate one output. Num_in is the entire input neurons and Num_out is the whole output neurons.

3.2.3 Complete Proposed System

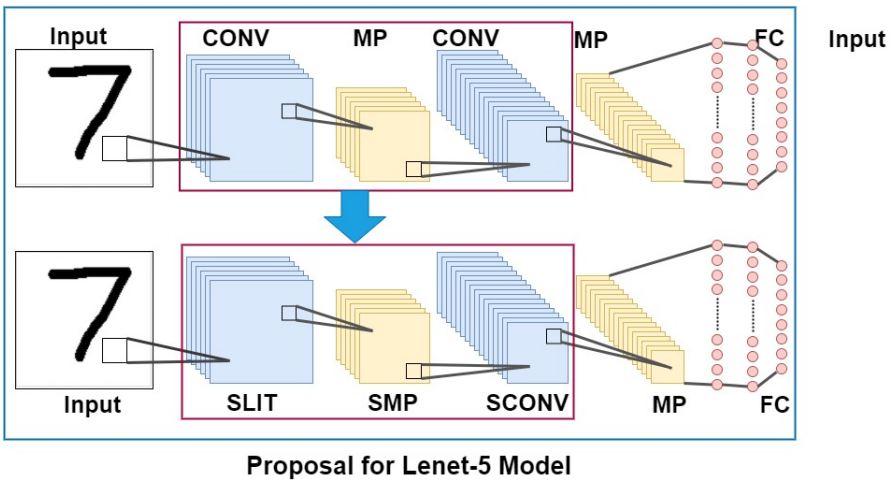


Figure 18. Proposed for Lenet-5 model

This section demonstrates how to reconstruct the first two layer or the first three layers of the proposal in practical applications. The Lenet-5 that combines one CONV + MP + another CONV layer in the model is chosen to manifest how to reconfigure with SLIT + SMP + SCONV layers. In Fig. 18, the CONV + MP + CONV layers are replaced with SLIT + SMP + SCONV layers. The remaining layers stay the same as the original model. The first two CONV layers occur in some famous models such as VGG-16, VGG-19 is reconfigured in Fig. 19. These models include two CONV layers before the MP layer. In this fashion, the first two CONV layers are changed by SLIT and SCONV layers.

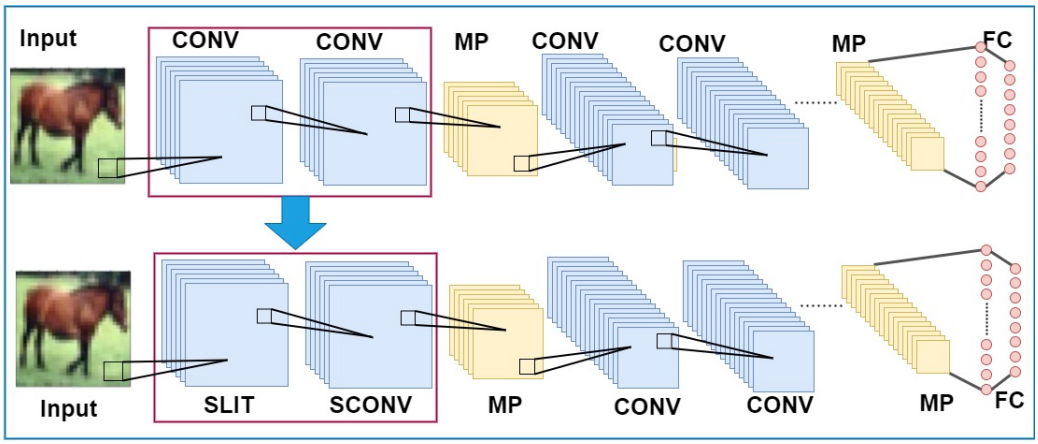


Figure 19. Proposed VGG model

4 Performance of the SLIT Function on Software Platform

4.1 Detail Performance of the SLIT Function with Simple Architecture on MNIST dataset

The network includes a 28x28 pixel input, one 5x5x8 kernel for the convolutional layer with the Relu activation function, one 8x12x12 pooling layer, and one fully connected layer. Fig. 20(a) illustrates a standard CNN network. The proposed scheme is manifested in Fig. 20(b). The SLIT function is divided in the range from 0° to 157.5° yielded 8x24x24 channels that are equivalent to the output of the convolutional layer. Due to the binary outputs of the SLIT function, the Relu activation function is eliminated in the suggested model. The purpose of the pooling layer in the CNN network reduces the feature size to minimize the multiplier-accumulator operations (MACs) in the next convolutional layer. In the proposed architecture, to get the inputs of the next layer, the pooling layer and optimize MACs are excluded by adding weight values that correspond with the previous inputs that are 1.

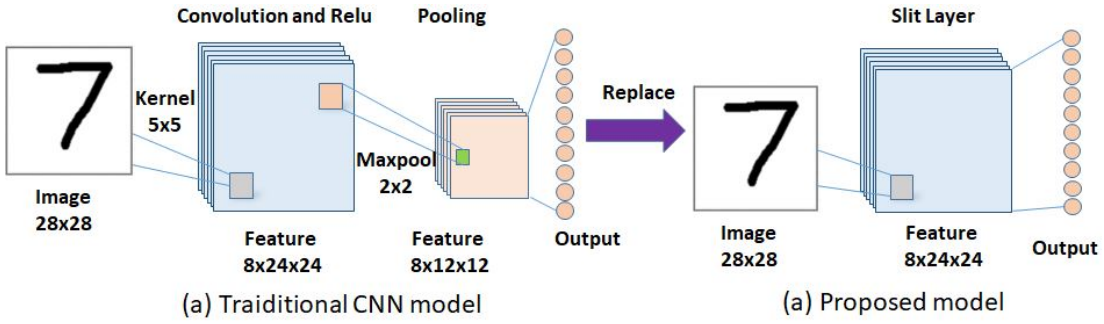


Figure 20. Apply SLIT function on small CNN architecture using MNIST database

This design is verified with the MNIST database [119] with 60,000 images for learning and 10,000 images for evaluation. The batch size consists of 100 images, and the number of epochs is 20. C programming language and the matrix calculation library Atlas are utilized to evaluate this method. Intel(R) Xeon(R)

Gold 6144 CPU @ 3.50GHz is used to measure the execution time. As represented in Table 1, this model evaluated by software using C programming language shows that the SLIT function only takes 15.3 seconds to extract features of the input images.

Table 1. Execution time and point convergence measurement using C programming language

Metrics	**Traditional CNN**	**Proposal**
The first layer	190 sec (Conv)	15.3 sec (SLIT)
Forward	231.8 sec	121 sec
Conv.backward	446.9 sec	0 sec
Backward	511.5 sec	102 sec
Training time	743.5 sec	239 sec
Inference time	38.7 sec	22.8 sec
Point convergence	13^{th}	5^{th}

Conv: Convolutional layer, **SLIT**: SLIT function
sec: Seconds, **th**: n^{th} within 20 epochs.

In comparison, it requires 190 seconds for the convolutional layer. Notably, execution time is approximately 446.9 seconds for the convolutional layer in back-propagation, which needs no time in the proposal. The total forward time is smaller by a factor of 1.91 when being compared to the conventional CNN. Furthermore, it also reduces the feed-backward time from 511.5 seconds to 102 seconds. The learning time is decreased by 3.1 times from our model equaled to CNN. In brief, total time consumption on CNN is extensive because it takes much time for feed-backward. The identification consumes 22.8 seconds, which is smaller than 38.7 seconds of the CNN model. The proposed scheme convergence is achieved after only five epochs, while the CNN model requires 13 epochs during 20 iterations. Analyzing the execution time analysis of the two models shows that the SLIT function efficiently replaces the convolutional operand. The suggested architecture has significantly reduced the time demand for the training phase and inference step in the deep neural network.

The fundamental idea in the proposed method is the SLIT function with input

as the result of the edge function. We propose three different designs for the SLIT function. The result of the 4x4 window gains the highest performance of all three models. The V1 region of the brain extracts the feature properties of objects from the eye, and it corresponds with the first layers of CNN, mimicking V1 [2, 113]. The 4x4 window in Fig. 10 rotates in a resolution from 0° to 157.5°, which perfectly coincides with the eye vision. It is considered that they are eight different combinations in this range.

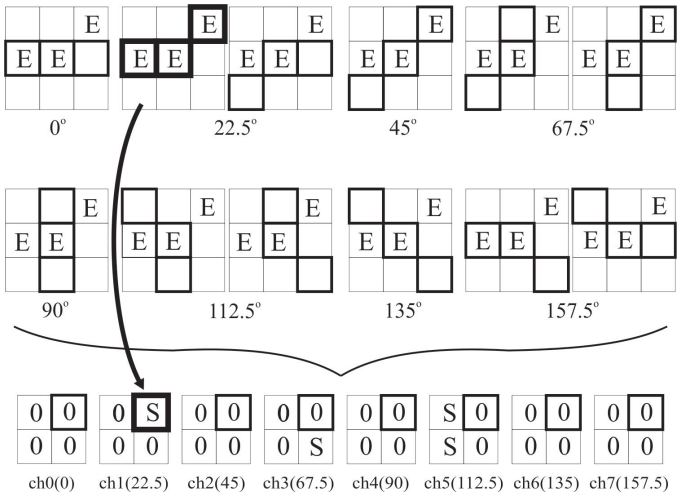


Figure 21. SLIT function using 3×3 window

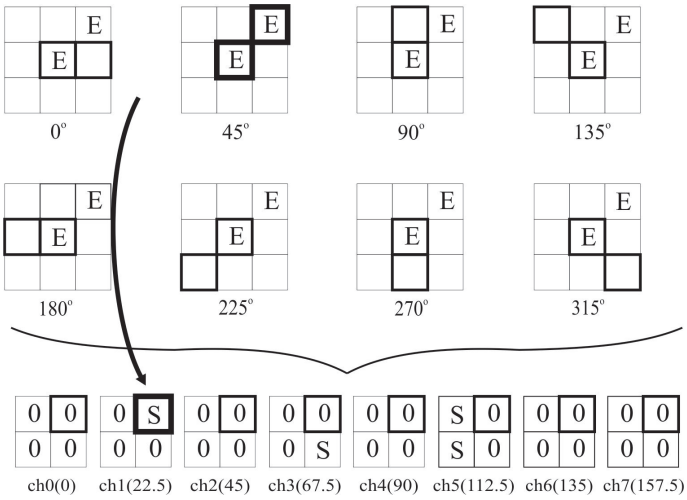


Figure 22. SLIT function using 2×2 window

For the 3x3 window in Fig. 21, the resolution is still within the eye vision, but there are many overlapping slopes at 22.5°, 67.5°, 112.5°, and 157.5°. Therefore, its result is nearly the same as the 4x4 kernel. The 2x2 window in Fig. 22 scans with an angle from 0° to 315° with a gradual increase every 45°, but with only four cases of necessary information contribute to the network, and the remaining cases pass the eye's perspective. It is assumed that we choose the 5x5 window and reduce the step in the range of 0° to 157.5° to extract more features, the overfitting problem and hardware resources are a trade-off. For balancing resources and precision, the 4x4 window is the best candidate.

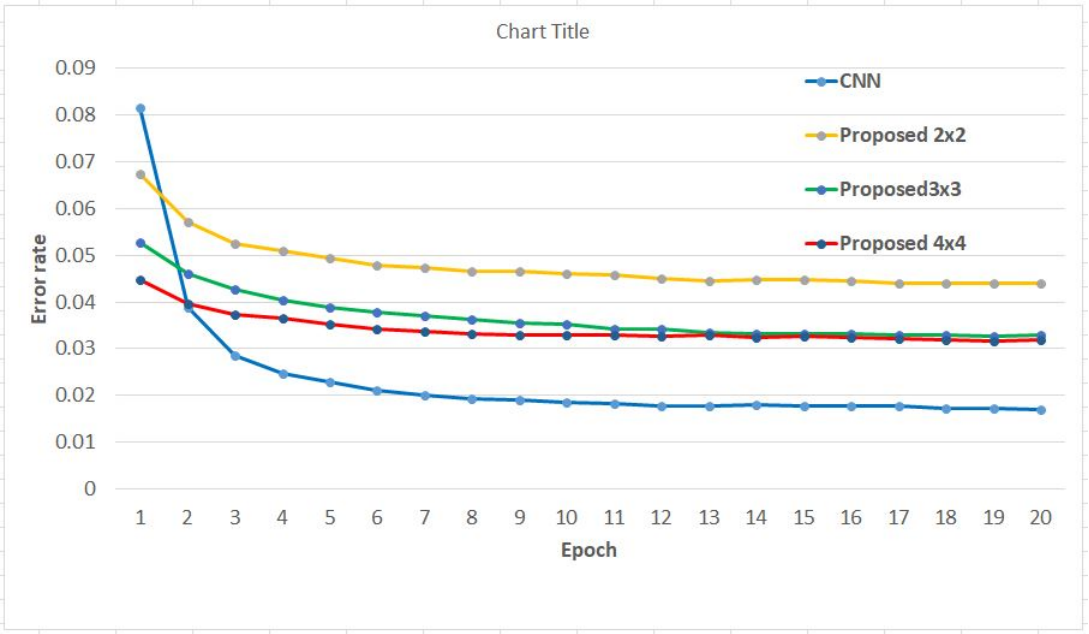


Figure 23. Comparison error rate between SLIT and CNN on MNIST database

Fig. 23 summarizes the comparison of three suggested concepts for SLIT function with conventional CNN. Comparison of three proposals, the window 4×4 gets better results than others. In short, the accuracy of our model with the proposed 4×4 window is slightly decreased from 97.89% to 97.34% when comparing with that of the CNN model.

4.2 Performance of Reconfigurable Deep Neural Network

4.2.1 Software Configuration

In this section, the utilization of the SLIT layer in various models is investigated. I conduct extensive experiments on the standard Lenet-5, VGG-16, and VGG-19 prototypes with the MNIST [119], SVHN [120], CIFAR-10, CIFAR-100 [121], and ImageNet [122] datasets. Tensorflow, Keras [123], and Pytorch [124] platforms are used to build the models. Training time and accuracy of the MNIST, CIFAR, and SVHN databases are analyzed by using the Intel(R) Core(TM) i7-3970X CPU @ 3.50GHz. The GeForce GTX 1080 is used for training the ImageNet dataset. To determine hyper-parameter values in the proposed model, first, training the examining database on the traditional model to estimate the hyper-parameters at an acceptable accuracy like benchmarks. Then, during the training phase of the proposed model, I increase or decrease appropriately the value of the reference hyper-parameters extracted from the conventional model. Finally, the hyper-parameters of the proposal are determined when the over-fitting and under-fitting phenomena disappear, and the model converges with the highest accuracy. In comparison with the traditional model at the same database, the hyper-parameters are nearly identical between the two models. Therefore, I have used the same values when training conventional and proposed models. I evaluate latency, hardware resources, and power consumption of the inference phase on the chip ZC7Z020-1CLG484C FPGA.

Handwritten digits (MNIST): The MNIST database [119] consists of 28×28 gray images of the handwritten digits "0" through "9". A total of 60000 images are provided for training, and 10000 images leave for testing. In the reported experiment, training images are sliced further into a training set (50000 images) and a validation set (10000 images), equal to the distribution of digit classes. Fig. 24(a) shows samples of the MNIST dataset. The Lenet-5 paradigm is considered for performance analyses. From the original Lenet-5 model which combines CONV(6) + MP(2) + CONV(16) + MP(2) + FC(120) + FC(84) + FC(10), the design that mixes of SLIT(8) + SMP(2) + SCONV(16) + MP(2) + FC(120) + FC(84) + FC(10) is proposed. The simulation is carried out using a batch size of 100 images, 20 epochs, and the stochastic gradient descent (SGD)

optimization function with a learning rate of 0.1.

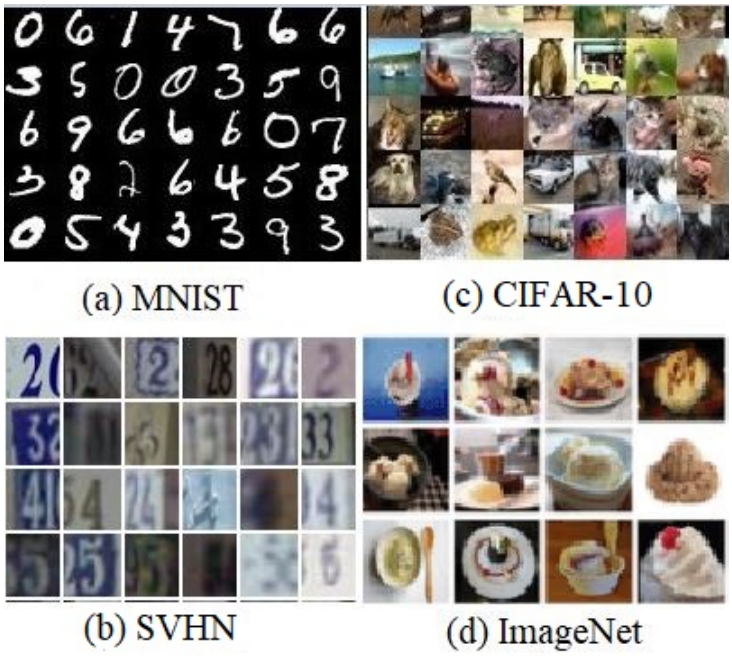


Figure 24. Examples of MNIST, CIFAR, SVHN and ImageNet databases

SVHN dataset: the SVHN dataset [120] has three channels in an image is also examined in this proposal. SVHN is collected from house numbers in Google Street View images. It includes 73257 images for training and 26032 images for testing. Examples of the SVHN dataset are displayed in Fig. 24(b). I investigate the SVHN dataset with the model that combines 2CONV(32) + MP(2) + 2CONV(64) + MP(2) + FC(512) + FC(10). In this manner, two CONV(32) layers are replaced with SLIT(11) and SCONV(32) layers. The model is trained with a batch size of 128 images, 20 epochs, and the SGD optimization function with a learning rate of 0.01.

CIFAR database: The proposal is interpreted in detail on the CIFAR-10 and CIFAR-100 datasets [121]. These datasets are composed of 60000 samples from ten categories for CIFAR-10 and 100 categories for CIFAR-100. Fig. 24(c) shows examples of the CIFAR-10 dataset. This experiment utilizes 45000 images for training, 5000 images for validation, and the last 10000 images for testing, and augment the database by exerting flip and shift operators. The Lenet-5, VGG-16,

and VGG-19 models are employed for measuring performance. These models are assessed with a batch size of 128 samples, 200 epochs, and the SGD optimization function with learning rate change from 0.1 in a range of 0 to 100 epochs, 0.01 in a range of 100 to 150 epochs, and 0.001 for larger than 150 epochs. Since the CIFAR dataset has three input channels, I have concatenated eight output feature maps of the SLIT function with three input channels normalized in a range of 0 and 1 to create the SLIT layer. For the Lenet-5 design, we validate with SLIT(11) + SMP(2) + SCONV(16) + MP(2) + FC(120) + FC(84) + FC(10) as the equivalence of the conventional Lenet-5 scheme which stacks up of CONV(6) + MP(2) + CONV(16) + MP(2) + FC(120) + FC(84) + FC(10). In the VGG-16 and VGG-19 forms, two first CONV layers with 64 output channels are switched by SLIT(11) + SCONV(64) layers.

ImageNet database: The ILSVRC2012 ImageNet dataset [122] has also been chosen as a target to assess our topology in a complicated case. ImageNet includes approximately 1.2M training images with 1K classes and 50K validation images. This dataset covers natural images with reasonably high resolution compared to the CIFAR, MNIST, and SVHN datasets, which have relatively small images. The examples of the ImageNet database are shown in Fig. 24(d). The image classification performance has been conducted to report Top-1 and Top-5 accuracy. The VGG-16 architecture is adopted as the base proposal. Two first CONV layers of the VGG-16 model is reconstructed with SLIT(11) and SCONV layers. The design is simulated with a batch size of 16 samples, 100 epochs, and the SGD optimization function at a learning rate of 0.001.

4.2.2 Software Results

Figure. 25 shows the accuracy of the MNIST, CIFAR-10, CIFAR-100, SVHN, and ImageNet datasets. A small decrease in accuracy of 0.27% from 99.07% to 98.8% with the MNIST database has been observed when being compared between the Lenet-5 proposal and the conventional Lenet-5 paradigm. Moreover, it slightly decreases from 0.5% to 1.5% with CIFAR-10 and CIFAR-100 datasets and around 2.2% on the ImageNet. It also remarks efficiently on the small CNN model that is experimented on the SVHN dataset. With complicated models such as VGG-16 and VGG-19, the loss of accuracy ranges from 0.5% to 2.2%.

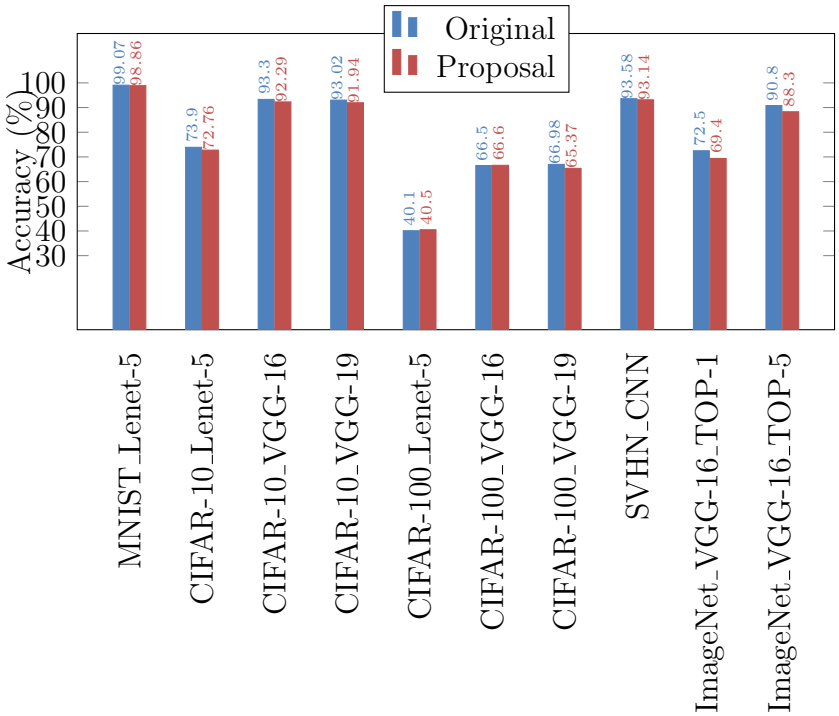


Figure 25. Comparing accuracy between the original model and the proposed model

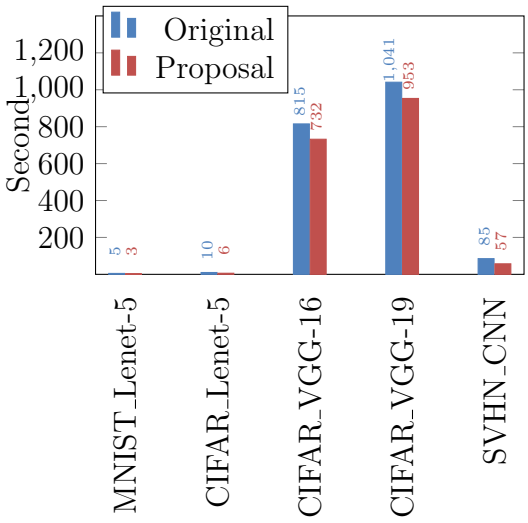


Figure 26. Comparing training time of one epoch between the original model and the proposed model

A training time reduction shown in Fig. 26 compensates for the loss of accuracy when the proposal is applied. A decrease training time in a range of 10% to 40% has been verified from small scheme to complex topology models. Total training time is diminished by 40%, 40%, and 32%, corresponding with MNIST, CIFAR, and SVHN databases on Lenet-5 and CNN models. It also decreases by approximately 10% on larger paradigms such as VGG-16 and VGG-19 with the CIFAR database. Because the model verified with the VGG-16 on ImageNet takes a long time for training one epoch, this case is not revealed in Fig. 26.

Table 2. Comparison parameters on Lenet-5 and VGG-16 model

Layer	**Kernal**	**Original**	**Optimized [50]**	**Proposal**
Lenet-5 model				
CONV1	1×5×5×6	150	336	0
CONV2	6×5×5×16	2400	2752	2400
VGG-16 model				
CONV1	3×3×3×64	1728	41K	0
CONV2	64×3×3×64	2400	49K	2400

Table 3. Comparison operations on Lenet-5 and VGG-16 model

Layer	**Dimension**	**Original**	**Optimized [50]**	**Proposal**
Lenet-5 model				
CONV1	1×28×28	117.6K (a)	225K (a)	0
MP	6×24×24	27.6K (b)	27.6K (b)	9216 (c)
CONV2	6×12×12	345.6K (a)	419.5K (a)	345.6K (d)
VGG-16 model				
CONV1	3×32×32	1.77M (a)	37.6G (a)	0
CONV2	64×32×32	37.7M (a)	50.3G (a)	37.7M (d)

a: MAC, b: Comparator, c: OR, d: Multiplexer

Ordinarily, the first and second CONV layers contribute 92.4% of MAC operations, while the FC layers offer 7.6% of MAC operations on the Lenet-5 model.

Parameter and operation reduction highlight the contribution of the proposed model for the training phase on CNNs. Results indicate a considerable efficiency obtained on the proposed Lenet-5 model. Table 2 and Table 3 show that a total of $1\times5\times5\times6 = 150$ parameters and 463K MAC operations are pruned in the proposal when evaluated with the MNIST database. Remarkably, with the CIFAR dataset that has three channels, $3\times5\times5\times8 = 450$ parameters and a total of $3\times5\times5\times32\times32\times6 + 6\times5\times5\times16\times16\times16 = 1.07$G MAC operations are excluded. The proposal decreases approximately by 90% MAC operations and leads to training time reduction during the training phase on the Lenet-5 model. An entirety of 1728 parameters and 1.77M MAC operations are also eliminated in the first layer on the VGG-16 model. In short, to compare with the original approach and reference, my model illustrates better MAC operation optimization on the Lenet-5 and VGG-16 models.

5 Performance of the SLIT Function on Hardware Platform

5.1 Hardware Setup

Among the various available tools for implementing hardware designs of CNNs on different FPGAs, Xilinx Vivado ® High-Level-Synthesis (Vivado_HLS) is commonly used in literature for the sake of productivity at the cost of hardware efficiency and performance [50, 105, 106, 107, 108]. Hence, I leverage the Vivado_HLS and Vivado_IDE (v2018.3) tools to realize hardware circuits. The FPGA synthesis is executed with chip ZC7Z020-1CLG484C for the property with benchmarks in comparison. I use Vivado_HLS to compare hardware resources and latency of the IP core between the original approach and the proposal with a 32-bits floating-point and 16-bits fixed point at a frequency of 100 Mhz. My IP core is conducted into an embedded system to verify area and power on real FPGA at 115MHZ of the frequency with 24-bits fixed point.

First, the SLIT layer is evaluated in two cases with eight binary output feature maps and eleven output channels that concatenate eight binary channels with three input channels. Second, I stack another CONV layer after the first CONV layer to assess how to compose the SCONV in the proposed topology. There have two CONV layers in the primary, but the proposal is concatenated SLIT and SCONV layers. Third, the MP proposal on CNNs is analyzed by appending one MP after the first CONV layer. I explain two cases: the first case is the structure having CONV, MP layers and the second is CONV, MP, CONV layers in the model. I handle the SLIT, SMP layers, and the SLIT, SMP, SCONV layers to compare with the data obtained from the conventional scheme. Next, the FC proposal is studied by linking the SLIT, SMP, and SFC layers. Finally, I investigate the architecture of the Lenet-5 and VGG-16 models as the analyzed standard of the proposed networks on hardware to compare with state-of-the-art. How to replace the first three layers is showed in the Lenet-5, and VGG-16 represents how to reconstruct the first two layers on the deep neural networks.

5.2 Comparison Hardware Resources and Latency with Vivado_HLS

Table 4. Comparing hardware resources and latency for the first layer

Metrics	CONV(8)	SLIT(8)	CONV(11)	SLIT(11)
Floating-point	**32-bits**	**32-bits**	**32-bits**	**32-bits**
LUT	724	241	815	549
FF	960	233	1073	657
DSP48E	8	0	8	3
BRAM	2	1	8	1
Latency (ms)	13.47	0.427	40.17	1.04

Table 4 exposes the reduction of hardware resources and performance for the first layer. The SLIT layer employs fewer LUTs, FFs, BRAM and DSP48E blocks than the CONV layer. Especially, the DSP48E blocks are humbled eight times in the case of SLIT(8). Latency achieves a $13.47/0.427 = 31.5\times$ reduction compared with the CONV(8) layer and a factor of $38\times$ decrease with the CONV(11) layer.

Table 5. Comparing hardware resources and latency for the second layer

Metrics	CONV(8)+ CONV(16)	SLIT(8)+ SCONV(16)	CONV(11)+ +CONV(16)	SLIT(11)+ SCONV(16)
Floating-point	**32-bits**	**32-bits**	**32-bits**	**32-bits**
LUT	1303	736	1425	1223
FF	1649	769	1811	1399
DSP48E	13	2	13	8
BRAM	18	2	40	10
Latency (ms)	160.7	96.5	266.3	210.9

Table 5 reveals the hardware resources and latency for the second layer. By replacing all MAC operations with the MUX function in case SLIT(8) +

SCONV(16), hardware utilization is notably reduced. For example, 2 DSP48E blocks are proportional to 13 DSP48E blocks in the standard design. BRAM blocks are lessened $18/2 = 9\times$ between two models. Latency is also decreased remarkably in our proposal when being compared with the traditional topology.

Table 6. Comparing hardware resources and latency for the max pooling layer

Metrics	**CONV(8) +MP(2)**	**SLIT(8) +SMP(2)**	**CONV(11) +MP(2) +CONV(16)**	**SLIT(11) +SMP(2) +SCONV(16)**
Floating-point	**32-bits**	**32-bits**	**32-bits**	**32-bits**
LUT	1028	341	1686	1497
FF	1255	334	2071	1673
DSP48E	8	0	13	8
BRAM	18	2	48	13
Latency (ms)	13.6	0.46	96.9	53.6

Table 6 reveals the max-pooling layer performance. By replacing three comparator operations with an OR gate, latency or speed is reduced from 13.6 ms to 0.46 ms. Hardware resources that estimate the IP core area extremely decrease on DSP48E and BRAM blocks. A factor of approximately 92% hardware resource reduction is observed when our SMP layer is compared to the second traditional MP layer. In a more complicated case like SLIT(11) + SMP(2) + SCONV(16), the proposed reconfiguration not only reduces significant hardware resources but also demand 53.6 ms, a reduction from 96.9 ms as in the case of CONV(11) + MP(2) + CONV(16).

The FC proposal is analyzed by combining SLIT, SMP, and SFC layers. By replacing the multiplication matrix with MUX functions, Table 7 proves that my suggestion also works better than the traditional process in terms of hardware resource utilization and execution time requirements. In short, four loops in the SLIT layer, OR gate in the SMP layer, and MUX operation in the SCONV layer result in enormous hardware resources and latency reduction.

Table 7. Comparing hardware resources and latency for the fully connected layer

Metrics	**CONV(8) +MP(2)) +FC(512)**	**SLIT(8) +SMP(2) +FC(512)**	**CONV(11) +MP(2) +FC(1024)**	**SLIT(11) +SMP(2) +FC(1024)**
Floating-point	**32-bits**	**32-bits**	**32-bits**	**32-bits**
LUT	1531	741	1549	1359
FF	1924	829	2006	1578
DSP48E	13	2	13	8
BRAM	22	3	48	13
Latency (ms)	105.5	60.5	454.3	379.9

Table 8. Comparing hardware resources and latency on Lenet-5 and VGG-16 models

Metrics	**Proposal Lenet-5**		**Proposal VGG-16**	
	Traditional	**Proposal**	**Traditional**	**Proposal**
Floating-point	**32-bits**	**32-bits**	**32-bits**	**32-bits**
LUT	4568	3854	43442	43140
FF	4371	3405	11276	10852
DSP48E	24	16	62	57
BRAM	17	8	480	354
Latency (ms)	34.3	20.78	49820	44503

Compared with the traditional CNNs on Lenet-5 and VGG models, our scheme replaces the first three layers on the conventional Lenet-5 model and the first two layers on VGG. By synthesizing with the Vivado_HLS tool, Table 8 shows the proposal has consumed less than 52.9% BRAM and 33.3% DSP48E blocks compared with the traditional Lenet-5 model. Moreover, my scheme achieves about 1- 20.78/34.3 = 0.394 or 39% latency reduction without using the optimized methods such as #parama HLS_PIPElINE or #parama HLS_UNROLL. I have also investigated hardware resources and latency for the VGG-16 scheme. The hardware resources also degrade 26% in BRAM blocks and 8% in DSP28E blocks

for the complete proposed VGG-16 design. The latency reduces about 10% as comparing the conventional approach.

5.3 Comparison Hardware Resources and Power Consumption on IP Core with Orther Researhes

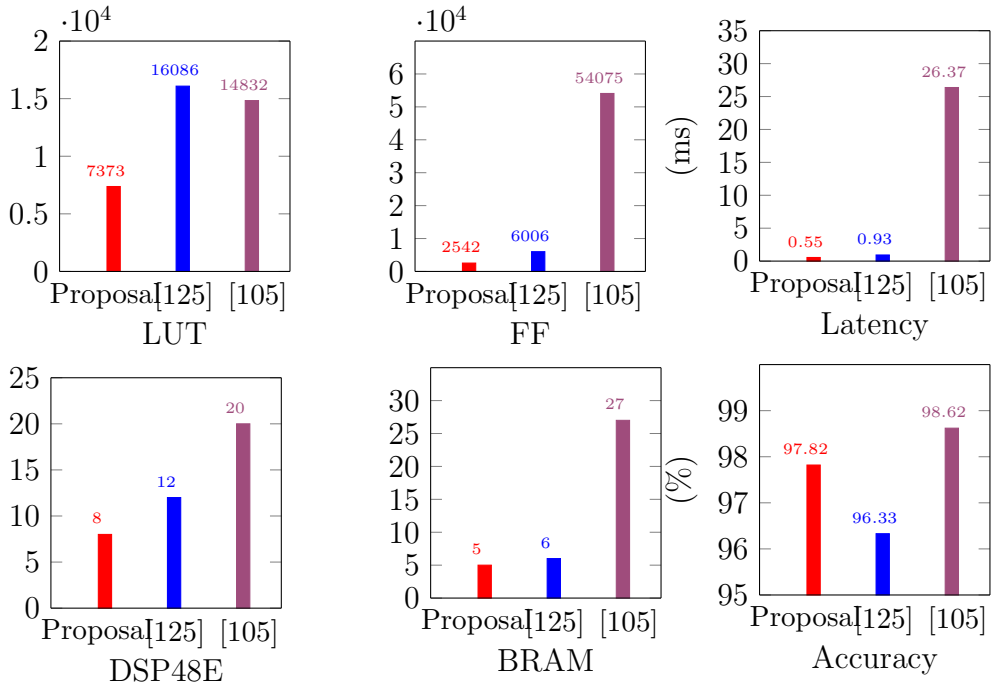


Figure 27. Comparison hardware resources and latency of our IP core proposal with other works on Lenet-5 model at 100 MHz using Vivado_HLS tool

For the IP core comparison between the proposal and existing state-of-the-art using the MNIST database, the network combining CONV(8) + MP(2) + CONV(8) + MP(2) + FC(10) is proved. The proposed model consists of SLIT(8) + SMP(2) + SCONV(8) + MP(2) + FC(10). In addition to constructing the first three layers, I also use #parama HLS_PIPELINE and #parama HLS_UNROLL technologies to improve the hardware design performance. I utilize a 16-bits fixed point while still maintaining accuracy. Fig. 23 reveals that the proposal demands a smaller number of hardware resources than previous works at higher accuracy. Especially, the latency achieves a 40.8% reduction over the work, and a factor

of 26.3/0.55 = 47× decrease compared with the result reported in the previous study. Besides, the hardware resource is lower with 1 BRAM block, 4 DSP48E blocks, 6006/2542 = 2.3× FFs, and 16086/7373 = 2.18× LUTs as compared with the highest current performance. Moreover, the proposal maintains 97.82% accuracy higher than 96.33% in reference.

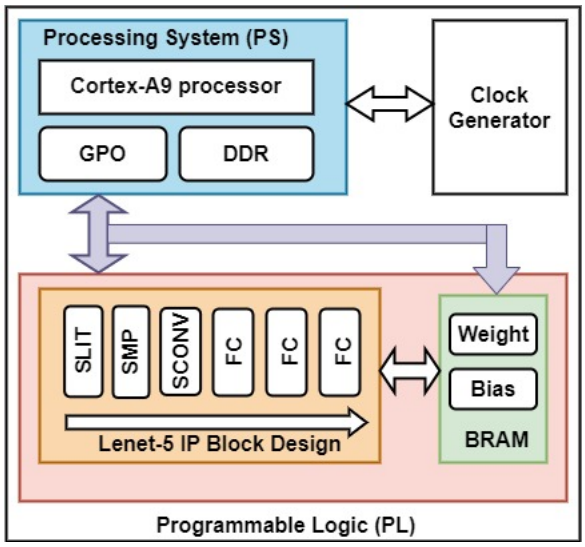


Figure 28. System on chip implementation of the Lenet-5 model on zynq7020 FPGA

As shown in Fig. 28, the CNN accelerator design includes ARM, AXI, BRAM, and my IP core. The IP core is called in an ARM CPU-based embedded system to analyze the effectiveness of the proposed optimization technique. Table 9 exposes the comparison between my model and the previous works in hardware resources used to estimate area and power consumption. Due to the binary calculation on SLIT, SMP, and SCONV layers, the DSP48E blocks are extremely reduced in the proposal. To fairly assess, I convert 16 DSP48E blocks into 1003 LUTs, and 537 FFs in the way reference [108] measurement and estimate equivalently one BRAM into 256 LUTs as references [126, 127]. As a result, my topology utilizes the same LUTs with a 72.5% reduction in FFs compared with the other works. Moreover, the proposal also employs a 0.456 W power consumption lower than works [106, 107, 108].

Table 9. Comparing resource utilization and power consumption on chip zynq7020 FPGA for Lenet-5 model

Parameter	**[106]** 24-bits fixed point	**[107]** 32-bits floating-point	**[108]** 8-bits fixed point	**Proposal** 24-bits fixed point
Frequency	166 MHZ	100 MHZ	100 MHZ	115 MHZ
LUT	38836	14659	39898	6853
FF	23408	14172	25161	6378
DSP48E	95	125	0	16
BRAM	92	119.5	24	127
Power (W)	3.32	1.8	1.758	0.456

5.4 DPU architecture for SLIT+CNN on Vitis AI platform

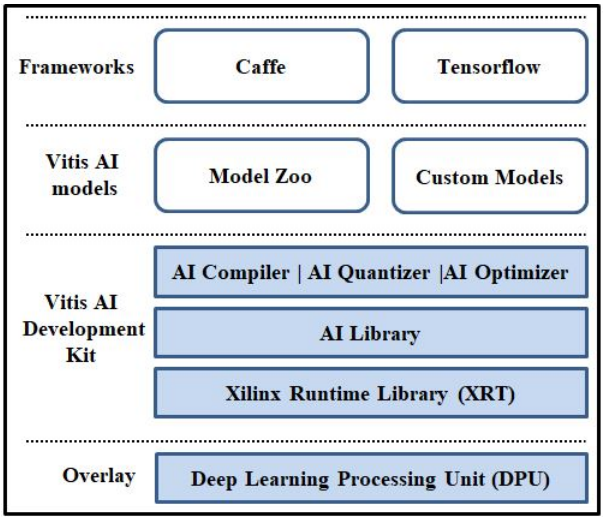


Figure 29. Flow vitis AI platform[128]

Vitis AI supporting AI inference acceleration is an integral part of Vitis from the Xilinx platform [128]. The Vitis AI produces high-throughput CNN inference

engines for FPGAs and ASICs. It offers a complete series of tools and APIs for pruning, quantizing, optimizing, and compiling pre-trained models to reach the highest AI inference performance on Xilinx platforms. This program is a foundation for the gap between deep learning frames such as Tensorflow, Keras, Caffe, and hardware circuits. Vitis AI permits software developers to exploit FPGA or ASIC acceleration benefits without demanding HDL progress and low-level circuit expertise. The overall flow chat of Vitis AI is summarized in Fig. 29.

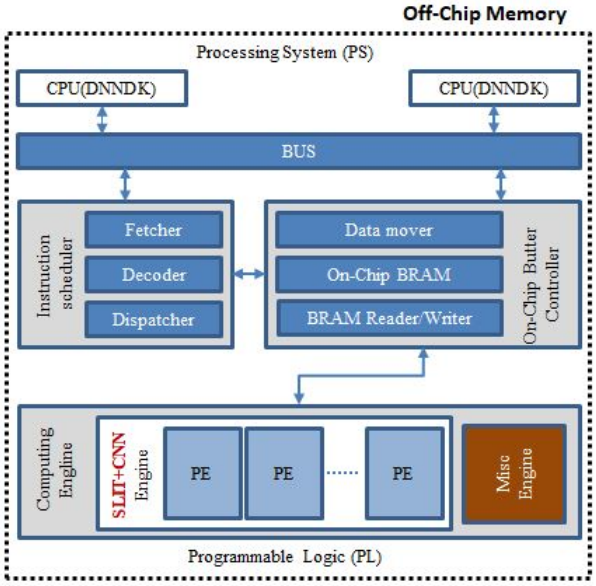


Figure 30. The proposal SLIT + CNN on the DPU architecture

In this research, the SLIT layer is mixed with conventional CNNs on the DPU structure to reduce the latency of the inference step on the Xilinx ZCU_102 FPGA board. The Xilinx® Deep Learning Processing Unit (DPU) [129] is an optimized programmable tool for deep neural networks. It comprises an instruction fetch unit, a high-performance scheduler module, a global memory pool module, and a hybrid computing array. A specific instruction set conceding for the satisfactory implementation of CNNs is integrated into the DPU. Fig. 30 shows the proposal of the SLIT layer on DPU architecture in the deep neural network topology. The first layer of CNNs replaced by the SLIT layer. After training the hybrid network, the parameters are quantized and optimized to measure the accuracy and latency of

the inference stage on the ZC7Z020-1CLG484C FPGA. The MNIST and CIFAR-10 datasets are employed to validate the execution. Due to hardware resource limitations, I only assess the schemes, for example, Lenet-5, VGG-11, and VGG-13.

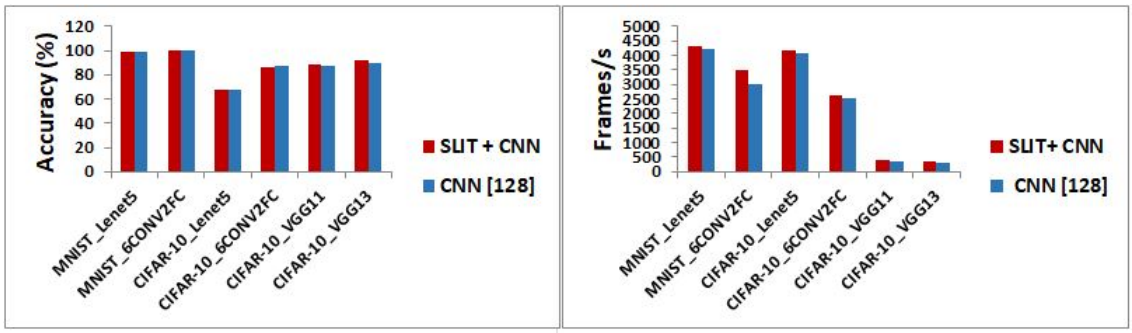
Table 10. Comparison resource utilization on DPU platform

Parameter Size (MB)		
	SLIT + CNN	**CNN [129]**
MNIST_Lenet5	**0.04**	0.04
MNIST_6Conv2fc	**0.86**	0.86
CIFAR10_Lenet5	**0.06**	0.06
CIFAR10_6Conv2fc	**1.09**	1.09
CIFAR10_VGG11	**9.74**	9.8
CIFAR10_VGG13	**9.94**	9.97
MAC (MOPs)		
	SLIT + CNN	**CNN [129]**
MNIST_Lenet5	**0.56**	0.72
MNIST_6Conv2fc	**41.89**	43.61
CIFAR10_Lenet5	**1**	2.29
CIFAR10_6Conv2fc	**43.89**	58.14
CIFAR10_VGG11	**1330.56**	1451.45
CIFAR10_VGG13	**1744.3**	1810.36
I/O Memory space		
	SLIT + CNN	**CNN [129]**
MNIST_Lenet5	**0.008 (KB)**	2.02 (KB)
MNIST_6Conv2fc	**0.03 (MB)**	0.05 (MB)
CIFAR10_Lenet5	**0.01(KB)**	5.23(KB)
CIFAR10_6Conv2fc	**0.04 (MB)**	0.07 (MB)
CIFAR10_VGG11	**0.19 (MB)**	0.2 (MB)
CIFAR10_VGG13	**0.3 (MB)**	0.31 (MB)

The board FPGA Zybo Zynq-7000 (XC7Z010) containing 240KB block RAM, 28K logic cells, and 80 DSP slices is handled to measure the performance. The

target FPGA board includes the DPU B4096 built at a frequency of 325 MHz. The parameter size is utilized to save weight and bias in MB, KB, or bytes for the DPU kernel. The computation workload in the unit of MOPs for the DPU kernel is called workload MACs (MACs). The required DPU memory space in MB, KB, or bytes for the intermediate feature map is named I/O memory space.

Table 10 compares the resource utilization outcomes from the FPGA accelerator on the DPU platform. Due to optimizing the first layer in traditional CNN architecture, the parameter size, workload MACs, and I/0 memory space are reduced from 1% to 10% on the new topology. The accuracy depicted in Fig. 31(a) has remained the same as the conventional CNN when comparing the previous work [128]. Furthermore, an enhancement throughput from 2.6% to 16% is demonstrated in Fig. 31(b) when comparing with the outcomes reported in the reference [128].



(a) Comparison accuracy between SLIT + CNN and CNN

(b) Comparison throughput between SLIT + CNN and CNN

Figure 31. Comparison accuracy and throughput between SLIT + CNN and CNN on DPU platform

6 Apply SLIT Function into Spiking Neural Networks on Adversarial Attack Application

6.1 Overview Spiking Neural Network and Adversarial Attack

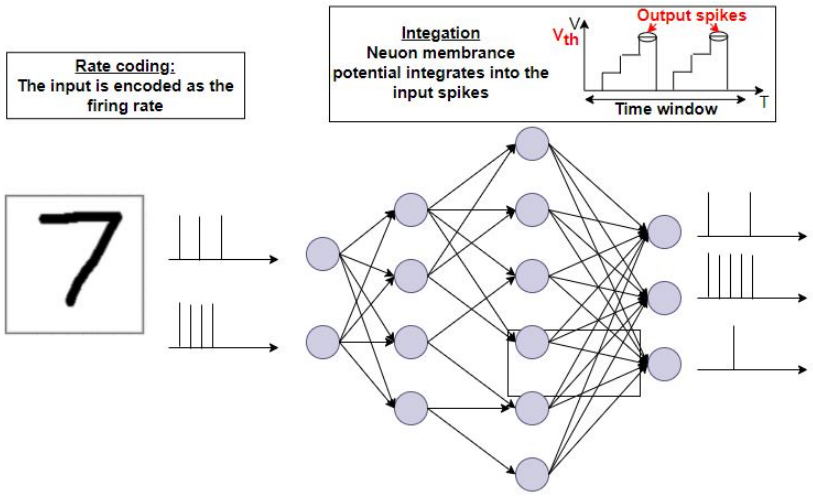


Figure 32. Overview of Spiking Neural Network

An illustration of the SNN diagram is portrayed in Fig. 32. The input data has to be suitably coded using encoding techniques such as rate coding, temporal coding. Coding schemes can be based on the number of spikes, the delay between consecutive spikes, or the latency between starting the stimulus to the first spike. Rate encoding is chosen as the most common mechanism. In rate coding, the activation intensity corresponds to the mean firing rate over a determined time window. A time window represents the measurement period in which the SNN takes the same input. An incoming spike is multiplied by its associated synaptic weight and integrated into the membrane potential V, following Eq. 19, when it arrives at the input of the neuron.

$$V = \sum_{i=1}^{N} w_i \cdot s_i \tag{19}$$

The leaky integrate and fire (LIF) model [130, 131] is the most universally utilized SNN model. The presence of each LIF neuron can be concisely expressed as Eq. 20

$$\begin{cases} \alpha \frac{dv(t)}{dt} = -v(t) + \sum_j w_j o_j t \\ \begin{cases} o(t) = 1 \quad \& \quad v(t) = v_0, \quad if \quad v(t) \geq v_{th} \\ o(t) = 0, \quad if \quad v(t) < v_{th} \end{cases} \end{cases} \tag{20}$$

where t means the time step, α is a time constant, and v and o express the membrane potential and produce output spike, respectively. o_j is the output spike of the j^{th} pre-neuron. w_j is the synaptic weight between the j^{th} pre-neuron and the current neuron. v^{th} is the considered firing threshold, and v_0 is the reset potential applied after firing a spike. Note that a spike should be fashioned as the Dirac delta function in the continuous-time domain; otherwise, it cannot increase the potential.

The adversarial attacks have been inspected on SNNs. The sensitivity of SNN w.r.t. different encoding types when subjected to white-box adversarial attacks was researched by Bagheri et al. [132]. Applying black-box adversarial attacks to DNNs and SNNs, the comparison showed that the SNNs studied by Marchisio et al. [133] were more robust. Sharmin et al. [134] also suggested a methodology to make the adversarial attack on (non-spiking) DNNs by applying the DNN-to-SNN conversion. The adversarial accuracy of SNNs trained by mixing inference latency and leak factors in leaky integrate-and-fire (LIF) spiking neurons was too analyzed. But, this study did not examine the influence of the membrane voltage threshold along with the time window. Recently, Massa et al. [135] tuned the threshold voltage and the time window to minimize the accuracy loss in the DNN-to-SNN conversion. However, this work did not consider the robustness of adversarial attacks. DIET-SNN [136] was introduced to tailor the membrane threshold and membrane leak to optimize the accuracy and the latency. Liang et al. [137] proposed a gradient-based adversarial attack methodology for SNNs and pointed the impact of the adversarial attack success rate on the loss function and threshold voltage types. The effect of structural parameters, i.e., membrane threshold and time window, was analyzed in work [138].

6.2 Apply SLIT Layer into Adversarial Attacks with Spike Compatible Gradient

Algorithm 1 Algorithm adversarial attack based on inherent structural parameters

Data: Combining SLIT layer and orginal data
Membrane voltage thresholds: $V\_th = V_i/i \in [1, n]$
Spiking time window: $T = T_j/j \in [1, m]$
Noise budget: $\epsilon = \epsilon_k/k \in [1, p]$
SLIT+SNN Architecture: $S_{ij} = SLIT + SNN(V_i, T_j)$
Label test set: $L = (X_t, L_t)$
Accuracy threshold: A_{th}

for $i \leftarrow 1$ to n **do**
  for $j \leftarrow 1$ to m **do**
    Train $S_{ij} = SLIT + SNN(V_i, T_j)$
    if Accuracy $(S_{i,j}) \geq A_{th}$ **then**
      // S_{ij} learns
      for $k \leftarrow 1$ to p **do**
        Adv = 0
        for $X_t \leftarrow 1$ to L do **do**
          // Adversarial attack
          $X_t^* = PGD(S_{ij}, \epsilon_k, X_t)$
          if $S_{ij}(X_t^*) \neq L_t$ **then**
            Adv++
          else
            NOP
          end if
        end for
        $\epsilon_k = 1 - Adv/L$
      end for
    else
      NOP
    end if
  end for
end for

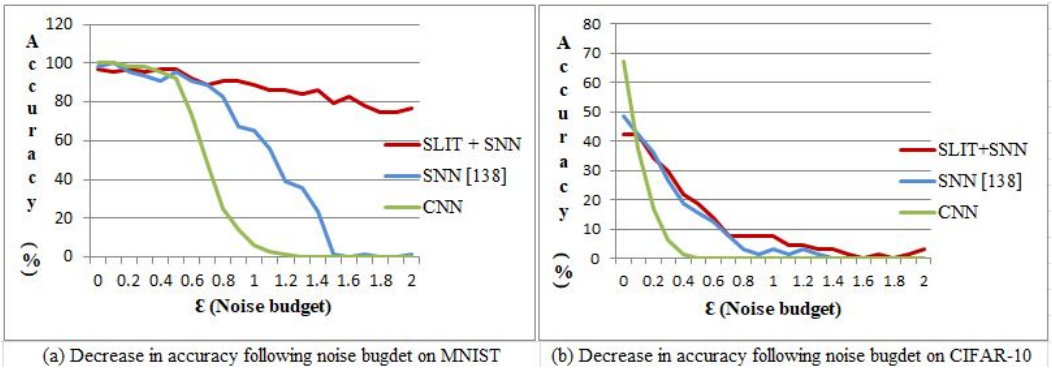
The suggested idea in the reference [138] is used to verify the performance of the SLIT layer on the adversarial attack application. The robustness exploration details in Algorithm 1. The input data is a concatenation of the SLIT layer with original data. The n threshold voltages and m time windows are browsed in Line 1 and 2. When the training stage is launched in Line 3, I treat the SLIT + SNN training analysis for the given combination of spiking threshold voltage V_th and time window boundary T. Being shown in Line 4, the learnability is quantitatively tested by fixing a minimum baseline accuracy level below to consider the SLIT+SNN learning vulnerable diagram. The security study begins from Line 6; it generates adversarial examples with different noise budgets (ϵ) to fool the SNN.

The noise budget models the aggressiveness allowed within the attack generation; the higher the noise budget, the more aggressive the attack is considered. The counter of successful attack generation states is initialized at Line 7. Then, at Line 8, the dataset L is browsed to generate the adversarial attacks. The PGD method at Line 10 is employed to assess the performance. Afterward, the algorithm verifies if the generated example can fool the SNN from Lines (11 - 17). Accordingly, increment the adversarial success counter if the attack forces the output to a wrong label. The robustness is then evaluated for every ϵ value as the attack rate where the adversary failed to generate an adversarial example that fools the victim SNN at Line 17. Therefore, by following the accuracy slope, we can compare the robustness of each topology to adversarial attacks.

The proposed investigations are conducted using the Norse library based on the PyTorch platform with primitives bio-inspired neural components. This library supports training and running SNNs in the spiking domain. The adversarial attacks are performed by employing the Foolbox v3.1.1 [139]. The SNN architecture is adapted from the Lenet-5 architecture to the spiking domain and trained on the MNIST and CIFAR-10 databases. The LIF neuron is used and run the experiments on the Nvidia GeForce GTX 1080. Preprocessing input data before implementing the adversarial attack application is proposed in this research. The input MNIST dataset is modified by concatenating eight channels of the SLIT layer with one original feature. For a complicated case dataset like CIFAR, eight channels of the SLIT layer are combined with three initial channels to produce

the input data. The detailed hyper-parameters are initialed as the work [138].

6.3 Improve Accuracy with SLIT+SNN for Adversarial Attack Application



(a) Decrease in accuracy following noise bugdet on MNIST (b) Decrease in accuracy following noise bugdet on CIFAR-10

Figure 33. Comparison decrease in accuracy on MNIST and CIFAR-10 between SLIT+SNN, SNN and CNN at V_th=0.25, T=80

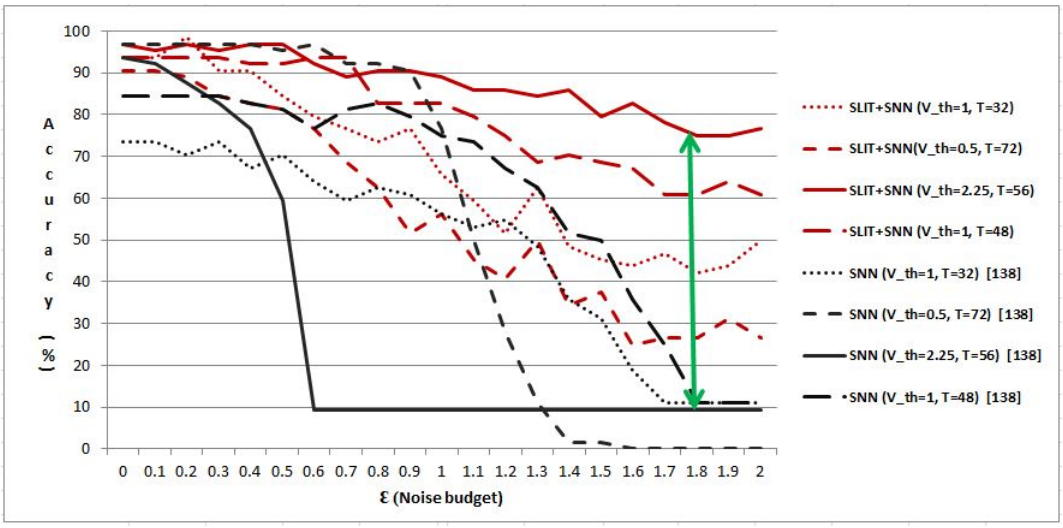


Figure 34. Comparison decrease in accuracy between SLIT+SNN and SNN tested on MNIST with different V_th and T parameters

Figure. 33 have illustrated the accuracy variation w.r.t the noise budget ϵ with the white-box PGD attack on MNIST and CIFAR-10 datasets. In Fig. 33(a), the result reports on the MNIST database that the combination SLIT+SNN keeps the same accuracy as SNN and higher than CNN at a low noise margin ϵ from 0 to 1.0. In the region of $\epsilon > 1$, the slope of SLIT+SNN has just slightly decreased; however, the slope of SNN decreases so fast, and the accuracy of CNN is nearly zero. With complicated datasets like CIFAR-10, Fig. 33(b) also reveal that SLIT+SNN looks better than SNN and CNN at every point of $\epsilon > 1$. Fig. 34 is a comparison of SLIT+SNN and SNN. This figure exhibits the impact of the concatenation of SLIT+SNN in the inherent structural parameters on SNN security. For example, combinations of (V_th, T) = (1.0, 32), (2.25, 56), (1.0, 48) have higher accuracy of 10%, 70%, 20% respectively than what is compared with SNN. With the case (V_th, T) = (0.5, 72), there is a decreased accuracy of around 20% in the SLIT+SNN at the region of ϵ from 0 to 1.2, but an increased accuracy on the proposal is nearly 28% at $\epsilon > 1.2$ when compared with SNN.

7 Conclusion

In this research, the SLIT layer that imitated the primary visual cortex principle and replaced the first layer of conventional CNN has proved efficiency. The backpropagation step of the proposed scheme requires no execution time, while it takes approximately 446.9 seconds in the traditional CNN model on the small network that includes one CONV and one FC layer. Training time is decreased by 40%, 40%, and 32%, respectively, with MNIST, CIFAR, and SVHN databases on Lenet-5 and CNN topologies. It also reduces by about 10% on larger paradigms such as VGG-16 and VGG-19 with the CIFAR database. Accuracy of the proposal has just slightly degraded, for example, a factor of 0.27% on Lenet-5 with MNIST dataset, approximately 1.5% on VGG-16 and VGG-19 with CIFAR dataset, 2.2% on VGG-16 with ImageNet database, and remained the same with the SVHN database. The innovative reconfigurations for the Lenet-5 scheme have achieved a 70% discount in hardware resources and an improvement of 39% latency at a power consumption of 0.456 W for the inference phase on FPGA. The entire convolution operations in the first two convolutional layers of the traditional CNN models are removed efficiently. This architecture is relevant for real-time applications, especially due to a significant reduction in latency. A latency enhancement in the range of 2.6% to 16% has been confirmed on the DPU platform. The SLIT layer is also discovered actively in adversarial attack applications on the third generation network that is plausible for human brain functionality. The accuracy boosts nearly 70% on scheme SLIT+SNN.

Future Work The proposed method is elastic to concatenate with various conventional models at high efficient energy and minimum hardware resources on FPGA. Hence, it gives a new inspiration toward combining our proposal with BinaryConnect or SqueezeNet method to obtain higher hardware design optimization. In the future, I plan to study a more extensive and scalable CNN accelerator that will integrate our scheme with other optimization approaches. I further aim to develop the SLIT layer on a neuromorphic hardware platform. I expect this proposal will resolve the obstacle when utilizing the traditional datasets in a new network topology. I also plan to explore the performance of different functions from the proposed model.

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List of Publication

1. TRAN, Thi Diem; KIMURA, Mutsumi; NAKASHIMA, Yasuhiko. Primary Visual Cortex Inspired Feature Extraction Hardware Model. In: 2020 4th International Conference on Recent Advances in Signal Processing, Telecommunications & Computing (SigTelCom). IEEE, p. 20-24, 2020. [Correspond to Chapter 3 and 4]

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3. TRAN, Thi Diem; NAKASHIMA, Yasuhiko. Exploring Versatility of Primary Visual Cortex Inspired Feature Extraction Hardware Model through Various Network Architectures. In: 2021 4th International Conference on Computing, Electronics & Communications Engineering (iCCECE2021). IEEE, p. 53-58, 2021. [Correspond to Chapter 5 and 6]