Doctoral Dissertation

VLSI Architectures for Selective FEC-based Transceivers in Optical Wireless and Radio Frequency Communication Systems

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Nguyen Duc Phuc

Abstract

Fifth-generation and beyond communication networks include heterogeneous wireless communication systems, in which the convergence of hybrid radio frequency (RF) and optical wireless networks is one of the key targets. In this thesis, we focus on channel-reliability enhancement of Forward Error Correction (FEC) based transceivers which are now applied widely in optical and RF wireless systems; specifically, Visible Light Communication (VLC) systems and Wireless Sensor Networks (WSNs) are taken into account.

Firstly, expected features of FEC solutions in WSNs transceivers are high coding-gain, low-complexity, and transmission-power efficiency. Therefore, we introduce an FEC approach based on splitting and concatenating of a low-constraint convolutional code and a truncated-iterative layered-decoding LDPC (TILD-LDPC) block code. Our solution offers four operational modes with different levels of error-correction performance and transmission power. Besides achieving competitive bit-error-rate performance, the proposed scheme could be applied in many operational scenarios of WSN nodes.

Secondly, VLC systems are now applied widely in indoor positioning systems (IPS) in which VLC-LED beacons are assigned with fixed position identifications. In IPS, the massive installation costs of dedicated embedded boards or programmable oscillators for VLC-LED beacons could be reduced if the VLC beacon network is managed by a central processing node. Unfortunately, due

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to limited memories and minimal processing capabilities, embedded processors should not be employed for the central node. On the other hand, VLC-specialized hardware could be implemented to accelerate the processing delay of the central node. However, hardware implementations of VLC transmitters and receivers have not been investigated before this, and typical VLC transmitter/receiver routines, such as encoding/decoding of run-length limited (RLL) codes and FEC codes, have been processed purely on embedded processors' firmware. However, recent work on soft-decoding of RLL and FEC have shown that they are bulky and time-consuming computations. This makes a hardware implementation in the VLC transmitter/receiver heavy and unrealistic. In this thesis, we introduce a couple of compact Polar-code-based VLC transmitters and receivers. Compared with related works, our VLC transmitter is a non-RLL one, which means flicker mitigation can be guaranteed even without RLL codes. In particular, we utilized the centralized bit-probability distribution of a pre-scrambler and a Polar encoder to create a non-RLL flicker mitigation solution. Moreover, at the receiver, a 3-bit soft-decision filter was implemented to analyze signals received from the real VLC channel to extract log-likelihood ratio (LLR) values and feed them to the Polar decoder. Therefore, soft-decoding of the Polar decoder could be implemented to improve the bit-error-rate (BER) performance of the VLC system.

Finally, we introduce novel very-large-scale integration (VLSI) architectures for the proposed VLC transmitter and receiver, along with a synthesis of our design using FPGA/ASIC synthesis tools. Due to the non-RLL nature, our system has a preeminent code-rate and reduced complexity compared with other RLL-based receiver work. In this thesis, we also present evaluation results of the power consumption, area, and energy-per-bits of the proposed method.

Keywords:

VLSI architecture, Forward Error Correction (FEC), Visible Light Communication (VLC), Wireless Sensor Network (WSN), Transceiver

List of publications

Peer review journal papers (J)

1. Dinh-Dung Le, Duc-Phuc Nguyen, Thi-Hong Tran, Yasuhiko Nakashima; "Log-Likelihood Ratio Calculation using 3-bit Soft-Decision for Error Correction in Visible Light Communication Systems"; IEICE Transactions on Fundamentals, Letter, Vol. E101-A, No.12, pp.- , Dec. 2018.

2. Dinh-Dung Le, Duc-Phuc Nguyen, Thi-Hong Tran, Yasuhiko Nakashima; "Joint polar and run-length limited decoding scheme for Visible Light Communication"; IEICE Communication Express, Vol.7, Issue 1, pp. 19-24, Jan. 2018.

3. Duc Phuc Nguyen, Thi Hong Tran, Yasuhiko Nakashima; "A Multi-mode Error-Correction Solution based on Split-Concatenation for Wireless Sensor Nodes", Journal of Communications (JCM), Vol. 12, No. 2, pp. 130-136, 2017. Doi: 10.10720/jcm.12.2.130-136.

Peer review international conferences (C)

1. Duc-Phuc Nguyen, Dinh-Dung Le, Thi-Hong TRAN, Huu-Thuan Huynh, Yasuhiko Nakashima; "Hardware Implementation of A Non-RLL Soft- decoding Beacon-based Visible Light Communication Receiver"; International Conference on Advanced Technologies for Communications (ATC'18), pp.xxx-xxx, October 2018. (Accepted).

2. Tuan-Kiet Tran, Duc-Phuc Nguyen, Dinh-Dung Le, Thi-Hong TRAN, Huu-Thuan Huynh, Yasuhiko Nakashima; "Demonstration of A Visible Light Receiver Using Rolling-Shutter Smartphone Camera"; International Conference on Advanced Technologies for Communications (ATC'18), pp.xxx-xxx, October 2018. (Accepted).

3. Duc-Phuc NGUYEN, Dinh-Dung LE, Thi-Hong TRAN, Yasuhiko NAKASHIMA; "Non-RLL DC-Balance based on a Pre-scrambled Polar Encoder for Beacon-based Visible Light Communication Systems"; International

Conference and Exhibition on Visible Light Communication 2018 (ICEVLC 2018), pp. 1-4, Yokohama, Japan, March 16, 2018 [Oral Presentation].

4. Thi Hong Tran, Duc Phuc Nguyen, Yasuhiko Nakashima; "PER Evaluation of K-min Viterbi Decoder for Wireless Sensors"; in Proceedings of 10th IEEE International Conference on Sensing Technology (ICST-2016), pp. 1-6; Nanjing, China, November 11-13, 2016 [Oral Presentation].

5. Duc Phuc NGUYEN, Thi Hong TRAN, Yasuhiko NAKASHIMA; "A High Coding-Gain Reduced-Complexity Serial Concatenated Error-Control Coding Solution for Wireless Sensor Networks"; IEEE International Conference on Signal and Image Processing (ICSIP), pp. 694-698, Beijing, China, August 13-15, 2016 [Oral Presentation].

6. Thi Hong Tran, Soichiro Kanagawa, Duc Phuc Nguyen, Yasuhiko Nakashima; "ASIC Design of MUL-RED Radix-2 Pipeline FFT Circuit for 802.11ah"; 19th IEEE Symposium on Low-power and High-speed Chips (Cool Chips XIX), pp. 1-3, Yokohama, Japan, April 2016 [Oral Presentation].

Workshops (W) (Technical reports)

1. Nguyen Duc Phuc, Le Dinh Dung, Tran Thi Hong, Nakada Takashi, Nakashima Yasuhiko; "A Compact Low-latency Pipeline Systematic Successive Cancellation Polar Decoder for Visible Light Communication Systems"; in IEICE technical report, vol. 117 (issue 44), pp. 3-7, CPSY-HotSPA, 2017.

2. Le Dinh Dung, Nguyen Duc Phuc, Tran Thi Hong, Nakashima Yasuhiko, Nguyen Son Kiet, Huynh Huu Thuan; "A Prototype of Dimmable Visible Light Communication System on FPGA"; in IEICE technical report, vol. 117 (issue 45), pp. 9-13, CPSY-HotSPA, 2017.

3. Duc Phuc Nguyen, Thi Hong Tran, Shinya Takamaeda, Yasuhiko Nakashima; "BER/PER Performance of 802.11ah K-best Viterbi Decoder on Fading Channel"; in IEICE technical report, vol. 115 (issue 369), pp. 93-98, RCS, 2015.

Other workshops (OW) (Brief abstracts)

1. Duc-Phuc Nguyen, Dinh-Dung Le, Tuan-Kiet Tran, Thi-Hong Tran, Huu-Thuan Huynh, Yasuhiko Nakashima; "Indoor Localization based on Led-to-photodiod and Led-to-camera communication - Promises and Challenges"; 1st International Workshop on Frontiers in Computing Systems and Wireless Communication, Nara, Japan, March 12-13th, 2018 [Oral Presentation].

2. Dinh-Dung Le, Duc-Phuc Nguyen, Thi-Hong Tran, Yasuhiko Nakashima; "Log-likelihood Ratio Calculation using 3-bit Soft-Decision for Error-Correction in Visible Light Communication Systems"; 1st International Workshop on Frontiers in Computing Systems and Wireless Communication, Nara, Japan, March 12-13th, 2018.

3. Duc Phuc Nguyen, Dinh Dung Le, Thi Hong Tran, Yasuhiko Nakashima; "Non-RLL DC Balance based on Non-systematic Polar Code for Visible Light Communication"; 10th Vietnam-Japan Scientific Exchange Meeting (VJSE 2017); Tokyo, Japan; September 9th, 2017 [Peer-review][Oral Presentation].

Posters (P)

1. Duc-Phuc Nguyen, Dinh-Dung LE, Dai Long Hoang, Satoya Yoshida, "A Precise Indoor Localization System with Fixed Visible Light Communication LEDs for Smart Shopping"; Creative and International Competitiveness Project (CICP Workshop 2017), December 10-11th, 2017, Boscovilla, Nara, Japan.

2. Duc-Phuc Nguyen, Dinh-Dung Le, Dai Long Hoang, Satoya Yoshida, Thi-Hong Tran, Yasuhiko Nakashima; "A Beacon-based Visible Light Communication System applied in Precise Indoor Localization for Smart Shopping"; International Conference for Top and Emerging Computer Scientist (ICTECS 2017); December 21-24; Taipei, Taiwan, 2017.

3. Dinh Dung Le, Son Kiet Nguyen, Duc Phuc Nguyen, Thi Hong Tran, Huu Thuan Huynh, Yasuhiko Nakashima; "A Research on Dimming Issue of

Visible Light Communication System"; 10th Vietnam-Japan Scientific Exchange Meeting (VJSE 2017); Tokyo, Japan; September 9th, 2017.

Awards

1. Nguyen Duc Phuc, Best oral presentation award at 1st International Workshop on Frontiers in Computing Systems and Wireless Communications (FOSCOM 2018), March 12,13th, Nara, Japan, 2018.

2. Nguyen Duc Phuc, Best oral presentation award at 9th International Conference on Future Computer and Communication (ICFCC 2017), April 21-23, Nagoya, Japan.

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1 Introduction

1.1 Background

1.1.1 Convergence and hybrid of wireless networks

The future fifth-generation (5G)-and-beyond systems are a vast network which includes various small networks inside it. Hence, this requires the collaboration of all wireless networks to achieve targets of 5G-and-beyond communications. Besides challenges of coexistence, interoperability and seamless transfer of wireless networks, one of key ideas of 5G communication systems is the outdoor and indoor separation, in which penetration loss through building walls can be avoided [1]. Specifically, statistic shows that wireless users spend almost 80 percent of time indoor, while in traditional cellular architecture, an outdoor base station communicates with users no matter they are in outdoors or indoors. Consequently, the data rate, energy efficiency and spectral efficiency of wireless transmission are damaged by the penetration loss caused by building obstacles.

Visible Light Communication (VLC) systems employ visible light for communication that occupy a frequency spectrum of 430 THz to 790 THz. VLC is selected to apply in indoor communication scenarios because the VLC receiver can only receives signal from the transmitter when it resides in the same room with the transmitter [12]. Recently, VLC was considered as a member of the small-cell family of the heterogeneous 5G networks to complement the Radio Frequency (RF) wireless communication systems. Also, VLC offers significant traffic offloading, which is potential in highly crowded radio frequency (RF) scenarios [2]. Moreover, hybrid systems of VLC and RF wireless communication have been introduced at [3, 4, 5], in which VLC is used for downlink while RF communication is used for uplink. In particular, data are transmitted from overhead luminaries to VLC receivers, and RF communication with its omnidirectional characteristic was exploited for uplink transmission. In this model, the use of VLC helps reduce the congestion caused by the RF uplink and downlink.

Generally, RF and optical wireless systems have different characteristics in transmission channels. Recent trends on convergence and hybrid of RF and optical wireless networks may lead to hybrid RF-optical transceivers in the future.

1

RF Wireless Communication

LoRa

Sigfox

WiFi

Bluetooth

802.15.4 Zigbee

Dash7

Transceiver

FEC

Optical Wireless Communication (OWC)

FSO

LiDAR

LiFi

OCC

Visible Light Communication (VLC)
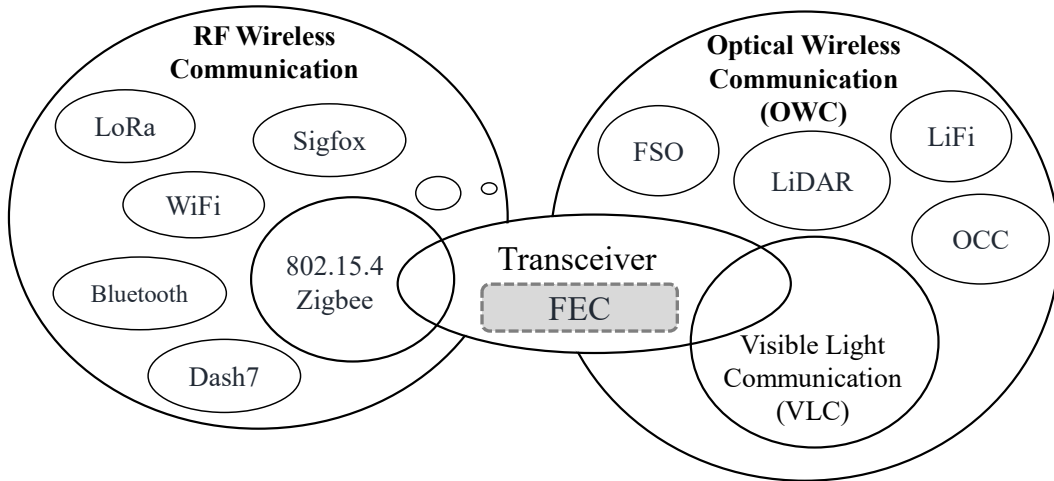
Figure 1. Our research scope which is covered in this thesis.

In this thesis, we have conducted the survey on forward error correction (FEC)-based transceivers which are currently applied in optical and RF wireless systems in heterogeneous wireless networks. An overview of our research scope is described in Fig.1, in which WSN's transceivers which based on Zigbee or 802.15.4 standards are selected for evaluation because of its wide simulation platforms. On the other hand, VLC is selected as a research object between many candidates in optical wireless communication (OWC) systems.

1.1.2 Forward Error Correction (FEC) algorithms

Forward Error Correction (FEC) algorithms can detect and correct errors appearing in received bit stream caused by a noisy channel, consequently FEC helps enhance the channel reliability as can be seen in Fig.2. The basic idea of such FEC algorithms is to add redundant bits or symbols to the original data with constraint equations; then the transmitted messages are rediscovered at the receiver side [14]. Because of error-correction characteristics, in RF wireless systems, FEC algorithms helps lower required transmitter power by increasing the channel reliability; hence, transmission range of RF wireless sensors can also be extended. On the other hand, in VLC systems, FEC helps improve transmission distance while LED light's flicker mitigation should be carefully considered. Some
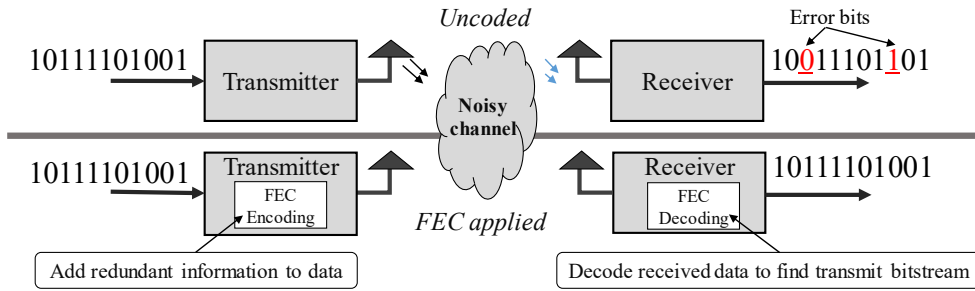
Figure 2. A communication scenario that FEC helps increase the channel reliability.
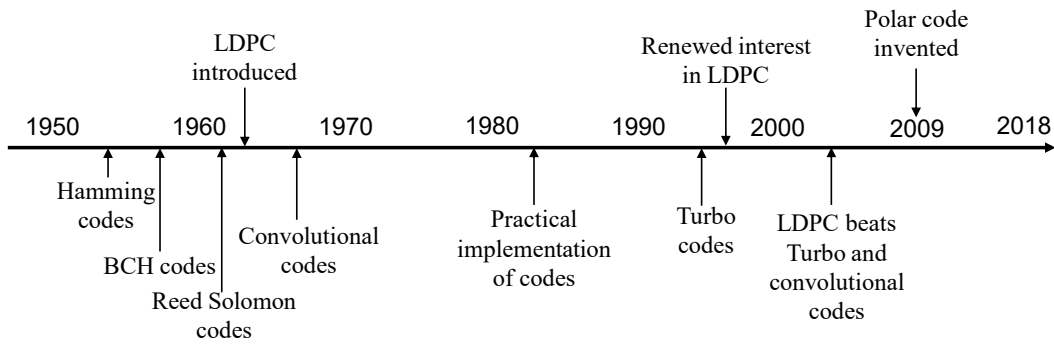
Figure 3. Timeline of appearances of some popular FEC codes.

popular FEC algorithms includes Hamming Codes, Reed Solomon, BCH, Turbo, Convolutional Code, LDPC, Polar code and so on. Each method has typical characteristics in error correction, and they are selected considerately to apply in various applications. Besides, robust codes can provide better error-correction performances with lower transmitted power requirements [15]. Therefore, superior BER performances and energy-efficient are essential criteria in many pieces of research about FEC codes.

Fig.3 presents the development timeline of common FEC codes. Gallager first introduced LDPC codes in 1960s [16]; however, they were forgotten at that time because they were impractical to be implemented. Recently, due to the superior error-correction performances, LDPC have received much attention again. Besides, Arikan invented a method for constructing capacity-achieving codes called *Polar code* in 2009 [17]. Channel polarization and Polar code are widely considered as breakthroughs in coding theory because they have shown promising features for future wireless standards. In this thesis, we consider LDPC code, Convolutional code and Polar code for the proposals which will be explained in later sections.

1.1.3 FEC-based Transceivers in Wireless Sensor Networks

A WSN could be defined as a network which includes many small devices that gather data from the environment, and communicate with each others. Compared with traditional wireless networks, WSN has a distinct design with some resource constraints. Specifically, short communication ranges and low-bandwidth are typical features of the wireless link. WSN nodes have limited energy and computing resources, they are small and inexpensive compared to conventional sensors [6]. WSNs cover many applications in target tracking and remote environmental monitoring. Nowadays, WSNs are available in health care systems, environment, agriculture, public safety, military, industry and in transportation systems [6].

Energy-constrained sensors are expected to run automatically for long periods without replacing batteries. Fig.4 shows a typical architecture of a wireless sensor node [7]. Generally, a common wireless sensor consists of some basic blocks such as a processor or micro-controller, some sensors, a RF transceiver, an external memory and a power source [8]. Also, wireless transceiver is considered as the

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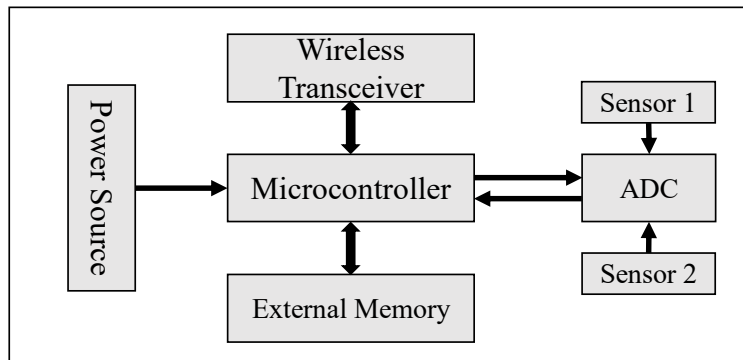
Figure 4. The typical architecture of a wireless sensor node.

component which consumes the most power-consumption in a wireless sensor node [9], especially when it's in transmission mode. Because of the trade-off between the channel reliability and transmission efficiency, FEC is an optional mode in most WSN tranceivers in which the firmware program can control FEC-setting registers to be enabled or disabled. Specifically, Section 2 provides further information of problems in FEC solutions for current WSN transceivers, then we introduce our FEC proposal afterwards.

1.1.4 FEC-based Transmitters and Receivers in Visible Light Communications (VLC)

In recent years, due to advantages of low-cost, high data-rate, unlicensed spectrum, high security, and immunity to radio frequencies, visible light communication (VLC) is getting many attentions from researchers to market interests. Indeed, VLC is considered as one of promising candidates in 5G wireless technologies [1]; specifically, VLC will be a potential complement and an alternative for the existing indoor RF systems [10]. Moreover, the global VLC/ Light Fidelity (Li-Fi) market was valued at 454.8 million USD in 2015, and Grand View Research Inc. has also given a forecast about the VLC market which will exponentially increase from 2016 to 2024 [11].

The VLC transmitter and receiver are not often located on the same package due to VLC is used for downlink communication in most cases, although there

are still some efforts which recently integrate VLC transmitter and receiver in the same node for full-duplex communication. Hence, through out in this thesis, instead of using the term: VLC transceiver; we use the terms: VLC transmitter and receiver separately. The definition, applications, standardization and research challenges of VLC have been clearly presented in [12, 13]. In particular, there are several open research issues have been shown in these works. In gereral, while FEC solutions for RF wireless transceivers gave more attentions in BER performances, code-rate or implementation complexity; researches on FEC solutions for VLC transmitters/receivers always consider the flicker mitigation and dimming control in evaluation. Particularly, performances of FEC codes cooperating with run-length limited (RLL) codes in VLC transmitters/receivers are well investigated in this thesis. Chapter 3 and Chapter 4 discuss details of our proposal.

1.2 Contributions

Our contributions in this thesis are summarized as follows.

1. **A Multi-mode FEC Solution based on Splitting-Concatenating FEC codes for Wireless Sensor Nodes:** In this thesis, we propose a multi-mode error-correction solution which bases on separating or concatenating the low-constraint convolutional code and truncated-iterative layered-decoding LDPC (TILD-LDPC) block code. The proposed FEC solution can offer four operational modes with four levels of error-correction performance which correspond to four transmit-power reductions. Besides guaranteeing superior BER performances without burst errors and error floors; the proposed FEC approach also provides different code-rates which are suitable for WSN transceivers. Furthermore, the proposal uses a low-constraint convolutional code for the inner code which potentially reduces hardware complexity compared with the high-constraint one. Chapter 2 describes our proposal and simulation results in details. Our contributions in Chapter 2 has been published in [J3, C5, C4, W3].

2. **VLSI Architectures of Non-RLL Soft-decoding Beacon-based Visible Light Communication Transmitter and Receiver:** Visible Light

Communication (VLC)-based systems are now applied widely in indoor positioning systems (IPS) in which VLC-based LED-beacons are assigned with fixed position identifications. In IPS, massive installation efforts of microcontrollers or programmable oscillators for VLC-LED beacons will be cut down if the VLC-specialized hardware is applied. Unfortunately, hardware implementations of VLC transmitters and receivers are not investigated until now; and encoding/decoding of run-length limited (RLL) codes and forward error correction (FEC) codes are processed purely on the firmware of embedded processors. However, recent works on soft-decoding of RLL have shown that they are bulky and time-consuming computations. This could be an obstacle, especially in low-end microcontrollers (MCUs) or system on chips (SoCs). In this thesis, we introduce a couple of hardware implementations of compact VLC transmitter and receiver. Compared with related works, our VLC transmitter is non-RLL one, that means flicker mitigation can be guaranteed even without RLL codes. In particular, we have utilized a centralized bit probability distribution of a pre-scrambler and a Polar encoder to create a non-RLL flicker mitigation solution. Moreover, at the receiver, a 3-bit soft-decision filter is proposed to analyze signals received from real VLC channel to extract log-likelihood ratio (LLR) values and feed them to the FEC decoder. Therefore, soft-decoding of the Polar decoder can be implemented to improve the bit-error-rate (BER) performance of the VLC system. Finally, we introduce a novel very large scale integration (VLSI) architecture for the compact VLC transmitter and receiver; and synthesis of our design under FPGA/ASIC synthesis tools. Due to the non-RLL basic, our system has a good code-rate and a reduced-complexity compared with other RLL-based receiver works. Also, we present FPGA and ASIC synthesis results of the proposed architecture with evaluations of power consumption, area, energy-per-bits and so on. The details of this proposal and simulation results are discussed in Chapter 3. Our contributions to Chapter 3 has been published in [J1, J2, C1, C3, W1, W2, OW2, OW3, P3].

3. **An FPGA-based centralized visible light beacon network** Indoor localization systems based on Visible Light Communication (VLC) have

shown promising advantages compared with systems based on other wireless technologies. In these systems, many VLC light-emitting diode (LED) anchors are employed in an indoor space in which location identification messages are sent to user devices in small packets. In normal beacon network models, a microcontroller (MCU) or low-end system-on-chip (SoC) is often the coordinators which configure messages for one or many VLC-LED bulbs. In this thesis, we discuss processing overload, and implementation cost of the two typical models of VLC beacon network in scenarios that hundreds of VLC-LED anchors are taken into account. Finally, an FPGA-based centralized VLC transmitter and its aided Nios II-based system have been introduced to enhance the performance of the VLC beacon network. Besides, due to the centralized processing, our system model is considered to be more cost-efficient than the dedicated-processor-based models. The details of this proposal and simulation results are discussed in Chapter 4. Our contributions of this research have been partly published in [J2, C2, OW1, P1, P2].

1.3 Structure of the thesis

The thesis is structured as follows.

In Chapter 1, we start an introduction of our research motivation. We introduce some research challenges in 5G-and-beyond wireless networks with a highlight on the convergence and hybrid of radio frequency and optical wireless communications. Motivation of the FEC-based transceivers in both systems, and preliminaries are also introduced in this chapter.

In Chapter 2, we present some FEC algorithms which are currently applied in WSNs transceivers. Then, we introduce a multi-mode FEC solution which based on splitting or concatenating of LDPC code and convolutional code. Besides, we also present some evaluation results of the proposed method on both AWGN and Rayleigh fading channels.

In Chapter 3, we present the motivation for the hardware implementation of VLC transmitter and receiver. Next, we introduce related works of non-RLL FEC-based VLC transmitters and receivers. Also, in this chapter, we introduce a non-RLL flicker mitigation method which concatenates a pre-scrambler with a

Polar encoder. Experimental results of flicker mitigation, run-length reduction, error-correction, and hardware implementation are extensively presented at the end of this chapter.

In Chapter 4, we evaluate critical processing delays of two beacon network models which are currently applied in VLC-based indoor positioning systems. Consequently, we introduce an FPGA-based centralized VLC transmitter and a Nios-II-based system which can accelerate the performance of embedded-processor-based models. Results related to synthesized resource, and processing time of the proposed design are also presented in this section.

In Chapter 5, we summarize all contributions of this thesis. Also, in this chapter, we present the outline of future works that we will conduct in near future.

2 A Multi-mode FEC Solution based on Splitting-Concatenating FEC codes for Wireless Sensor Nodes

2.1 Motivation

Providing a reliable communication channel with a reduced power consumption seems to be a critical problem in any wireless sensor nodes in which their batteries need to remain for a long time. Indeed, wireless sensor nodes do not often transmit information at high transmitted-power configurations. On the other hand, transmitting information at a low transmit-power while retaining a transmission reliability is the main target of any FEC-based WSN transceivers. Particularly, power-constrained is considered to be more important than bandwidth-constrained [23]. Therefore, to achieve the power efficiency, the sensor nodes accept transmitting information at a lower code-rate. Beside, coding gain is used as a parameter to evaluate the transmit-power efficiency of a FEC solution. The coding gain of a coding scheme at a given bit error rate (BER) is defined by the difference in decibels between the SNR required to obtain that BER with coding and without coding [23]. We assume that the transmitted powers to achieve the desired BER for an uncoded system and coded system are $P_{TX,U}$ and $P_{TX,FEC}$ respectively. As following [18], relationship between the coding gain and the transmitted power could be given by equation (1).

$$P_{TX,FEC}[W] = \frac{\eta_C B_C}{\eta_U B} \frac{P_{TX,U}}{10^{FEC_{gain}/10}} = \frac{P_{TX,U}}{10^{FEC_{gain}/10}} \qquad (1)$$

Where, η_U, η_C are the spectral efficiencies of the uncoded and coded systems respectively. Whereas, B and B_C are the bandwidths of the uncoded and coded systems. Note that $\eta_C B_C = \eta_U B = R$ in which R is the transmission rate. The equation (1) demonstrates that applying FEC helps lower the required transmitted-power because $FEC_{gain}/10$ is always larger than 1; this means improving FEC coding-gain (FEC_{gain}) could result in lowering transmitted power. Our error-correction solution provides different options for coding gains in different code-rates. Besides, our concatenating mode can provide a powerful error-

correction performance; however, in this mode, transmission efficiency reduces due to the incident low code-rates of the serial concatenating of FEC codes.

2.2   Related works

It seems that flexibility and scalability are current trends for researches related to FEC [19, 20]. To create a powerful error-correction code, a super coder/decoder could be created by serial concatenating FEC codes. This method is to combine an inner code with an outer code in both transmitter and receiver to take advantages of each FEC algorithms, as shown in Fig.5. Recently, many researches have introduced several concatenated FEC solutions for WSNs applications [15, 21, 22, 23]. They could be the combination of LDPC, Turbo code, Reed-Solomon, BCH or other FEC codes at various code rates, in serial or parallel architectures. Current works on concatenation-based FEC codes focuses on the optimization of architectures, scalability, or they introduced competitive races of BER performances [19, 20].
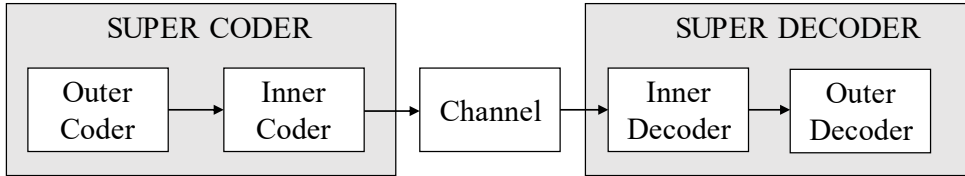
Figure 5. The concept of concatenating FEC codes.

WSN consists of a set of small devices which have limited capacities of battery, trivial performances, and limited transmitted power of RF front-ends [23]. Applying FEC for WSN transceivers needs to take care about the required transmitted power, and power dissipation of the FEC decoder circuits. Many researchers have proposed various methods for FEC-based WSN transceivers. Specifically, Moataz et al. combined LDPC with Turbo code for WSN [15], this approach could remove error floor of Turbo code by concatenating with LDPC; but their BER performance decreases remarkably in concatenating mode; and high-complexity of this FEC solution was unavoidable due to the iterative decoding of LDPC and Turbo code. Besides, Quassim et al. introduced a modified version of Reed Solomon

(RS) code [14] which can reduce power consumption; however, the BER/PER performances of this solution was not impressive even in AWGN channel. Nashat et al. proposed an adaptive parallel-concatenation of Turbo code in various interleave sizes for wireless sensor nodes, forwarding nodes and base stations [22]. This approach helps reduce power consumption of wireless sensor nodes; however, Turbo code at code-rate 1/3 is really poor, and BER performances at small sizes of interleaved memory is unimpressive. Furthermore, Ravanesh. M et al. also introduced a flexible parallel-concatenated Turbo codes for WSN transceivers in [21]. This work evaluated BER performances of Turbo code in many communication hops, and at different interleaver sizes. However, error floors appeared clearly even in low-SNR area, this drawback potentially reduce the channel reliability in high-SNR areas. In general, related works have shown some evaluation criteria for our FEC solution; in particular, some targets of our FEC solution for WSNs transceivers should be high coding-gain, reduced-complexity, no error-floor, and flexible code-rates which can adapt to many operational scenarios in WSNs. In this thesis, we propose a multi-mode FEC solution which is based on splitting-concatenating of QC-LDPC and low-constraint convolutional code. Our approach provides some levels of error-correction performances, transmitted-power efficiency with a reduced complexity. Also, flexible code-rates of the proposed FEC solution is suitable for different operational scenarios of WSNs.

2.3 System model

2.3.1 Description of the proposed method

Fig.6 shows the block diagram of the proposed method. The proposed solution includes four modes of operation:

1. *Uncoded (M01):* Channel coding is not selected in this mode. In normal cases, Automatic Repeat Request (ARQ) technique may be applied in this mode to increase the reliability of channel; however, this technique is not covered in this thesis. This mode is suitable for scenarios in which sensor nodes are required to transmit information in near distance, and in a low-noisy environment; many errors in the received bitstream are still accepted in this mode. This mode is often supported in low-power sub-1Ghz RF
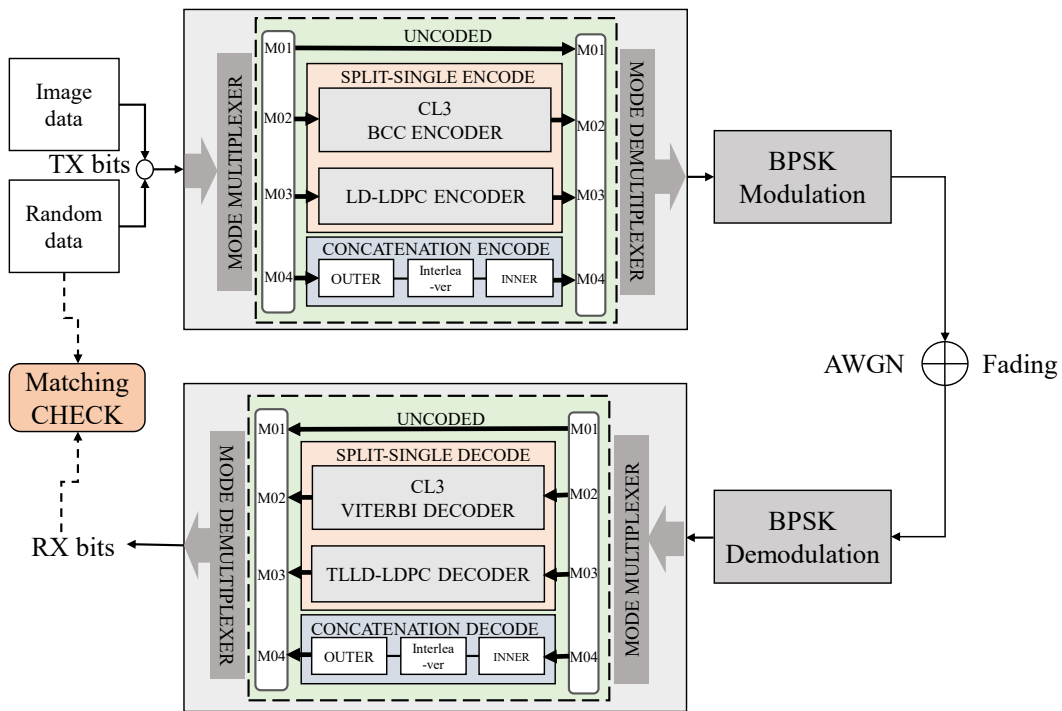
Figure 6. Block diagram of the proposed FEC solution in multi-modes which are based on spliting-concatenating of FEC codes.

front-ends such as TI's CC1100, CC1150 which are applied in small-area WSNs. Code-rate of this mode is 1.

2. *Low-constraint convolutional code (M02):* high-constraint convolutional codes are often applied in wireless standards such as IEEE 802.11.a,b,g,n, and in low-power sub-1Ghz RF transceivers [20]. We propose using a low-constraint convolutional code which has low-complexity and an accepted performance of error-correction. This mode is suitable for scenarios in which sensor nodes need to transmit information in medium distances, and in a low-noisy environment; however, the error-correction performances of WSN transceivers in this mode could be limited. Code-rate of this mode is 1/2.

3. *Truncated-Iterative Layered-Decoding of QC-LDPC (TILD-LDPC) (M03):* Due to the iterative decoding of TILD-LDPC, this mode could achieve good error-correction performances. Therefore, TILD-LDPC is selected as the main FEC code and located at "Outer" position in concatenating mode. The $M03$ mode is suitable for scenarios in which wireless sensor nodes need to transmit information in far distances through a noisy environment. Code-rate of this mode is 1/2.

4. *Concatenated FEC (M04):* Concatenating mode provides high error-correction performance with free burst-error. However, this mode potentially adds more redundant data in the transmitted data. Hence, this mode is suitable for scenarios in which wireless sensor nodes need to transmit information in far distances. Code-rate of this mode is 1/4.

2.3.2 Truncated-Iterative Layered Decoding of QC-LDPC (TILD-LDPC)

LDPC has shown benefits such as error-correction performances which can approach the Shannon limit. Also, LDPC is low-complexity in hardware implementation, and suitable for many wireless standards. Moreover, LDPC has better error-floor performances compared with the Turbo code. In the proposed method, Quasi-cyclic LDPC (QC-LDPC) [24] is selected as the main error-correction block and it works as "Outer" code in concatenation mode. Layered decoding technique with offset-min-sum (OMS) algorithm is also implemented to improve the conver-

gence speed and performance of the universal QC-LDPC. Also, through our simulation with a different number of iterations, we found that BER performances of the layered decoding QC-LDPC improves unremarkably when the iteration number is larger than five (Fig.7). Therefore, we selected five as the iteration limit for the iterative layered decoding QC-LDPC. In common multi-processor architectures of layered decoding QC-LDPC, an iteration is represented by one processing processor. Therefore, using the truncated-iterative method helps reduce remarkably the implementation complexity of the layered decoding of QC-LDPC.
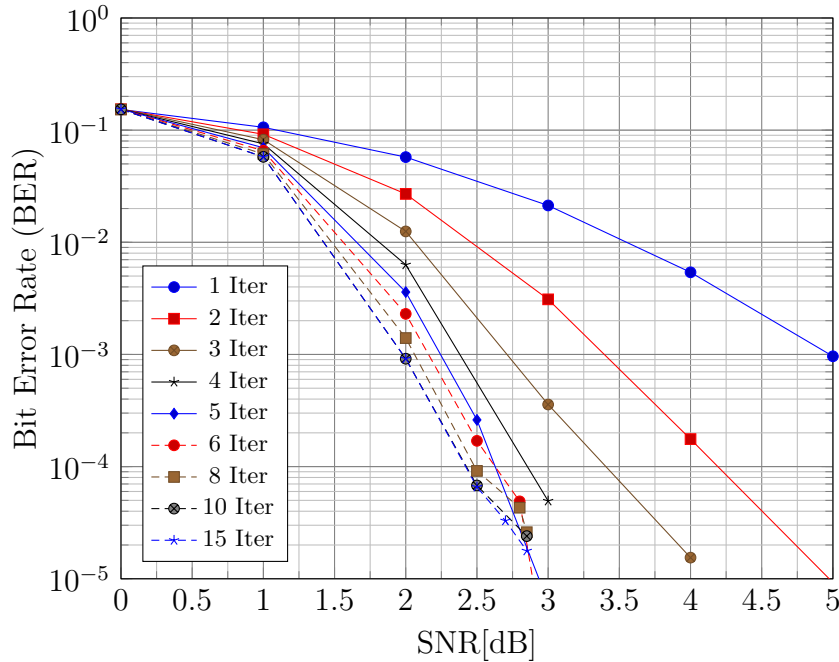
Figure 7. BER performances of layered-decoding of QC-LDPC at different values of iteration number.

2.3.3 Low-constraint Convolutional Codes

Convolutional codes (CC) are used as FEC solutions in many wireless transceiver [20]. Convolutional codes are often characterized by code rates and constraint lengths (n, k, K). The code rate is typically given as n/k where n is the input data, k is the output symbol and K is the constraint length (CL). We have

conducted the simulation in both AWGN and fading channel, as well as in hard- and soft-decision decoding of the convolutional code. Although in single FEC mode, the high-constraint convolutional code shows better performance compared with the low-constraint candidate. However, we found that concatenating low-constraint ($K = 3$) convolutional code (code rate 1/2) with TILD-LDPC (code rate 1/2) always gives better BER performances compared with high-constraint cases. Ioannis et al. introduced the relationship of the constraint lengths and the complexity of convolutional codes [25]. He found that the complexity of convolutional code increases exponentially when the constraint length increases. By using the low-constraint (e.g. CL = 3), the convolutional code reduces up to 1300 equivalent additions compared with the high-constraint one (e.g. CL = 7) [25]. For a low-complexity FEC solution, our proposed method has selected the low-constraint convolutional code for the inner code.

2.3.4 Influence of Inner and Outer Coder/ Decoder to Super Encoder/ Decoder's Performance

We have evaluated BER performances in four scenarios to give decisions about which FEC algorithm is more suitable for the outer code, and for the inner code.

1. *Scenario 01*: the Outer is TILD-LDPC with parity-check matrix 324×648; the Inner is BCC Encode/Viterbi Soft-Decision Decoding.

2. *Scenario 02*: the Outer is BCC Encode/Viterbi Soft-Decision Decoding; the Inner is TILD-LDPC, matrix 324×648.

3. *Scenario 03*: the Outer is TILD-LDPC with parity-check matrix 324×648; the Inner is BCC Encode/Viterbi Hard-Decision Decoding.

4. *Scenario 04*: the Outer and Inner are both TILD-LDPC with parity-check matrix 324×648.

Fig.8 shows BER performances of four scenarios, compared with TILD-LDPC at code rate 1/2. As a results, the scenario 01 (Outer = TILD-LDPC, Inner = BCC/Viterbi Soft Decision) shows the best BER performance. If we assume the name "stronger code" for TILD-LDPC and "weaker code" for the BCC/Viterbi,

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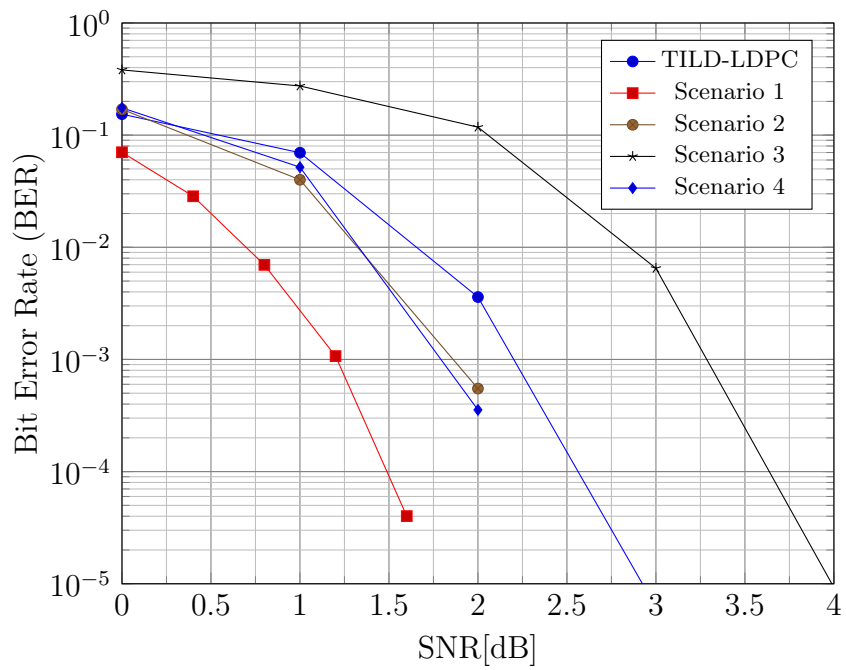
Figure 8. Influence of positions of inner and outer codes to the BER performances of concatenated codes.

we can conclude that serial concatenation of a "stronger code" with another "stronger code" does not always give better BER performances than concatenating a "stronger code" with a "weaker code" (scenario 04 and scenario 01). Moreover, the "stronger code" should be at Outer's position, and the "weaker code" should be at Inner's position (scenario 01 and scenario 02). Besides, concatenating TILD-LDPC with Viterbi Decoder in Hard Decoding gives worse BER performances than if only TILD-LDPC is implemented (scenario 03).

2.3.5 A free burst-error FEC solution with an internal interleaver

One of the main drawbacks of the convolutional code is burst errors exist in the decoded data. We have recognized burst errors in the received information by using digital images as the transmited data, together with random input data when we run the simulation model on MATLAB. It can be seen from the received images, concatenating convolutional code with TILD-LDPC does not remove definitely the burst errors which can be detected easily by eye. Therefore, an internal interleaver is implemented between the convolutional code and LDPC to provide a free burst-error FEC solution.

2.4 Evaluation results

Table 1. Simulation Parameters.

Software	MATLAB 2015a
Channel	AWGN, Fading
Modulation	BPSK
TILD-LDPC	Matrix size 324×648, Layered Decoding, Offset Min-Sum, Iteration number = 5
Convolutional Code	Hard Decision, Soft Decision, Code rate 1/2, Constraint Length (3,4,5,7)
Packet size	324 bits
Number of packets	1000, 10000

To evaluate the error-correction performances of the proposed method, we have built a simulation model on MATLAB, which is shown in Fig.6. Table.1 sum-

marizes all simulation parameters that we have used in the simulation model. The QC-LDPC with a 324×648 parity-check matrix is implemented, and it is assigned as the outer code. Whereas, the low-constraint convolutional encoder/ decoder are assigned at the position of the inner code. BPSK is used as the modulation type. Also, we have implemented two types of transmitted data: random data and digital images. By using image data, burst errors can be recognized quickly, and eye could find the effectivity of the internal interleaver. Fig.9 shows BER performance of the proposed method compared with some references on all modes (Uncoded, convolutional code, TILD-LDPC and concatenated mode). We see that the BER performance of TILD-LDPC (code rate 1/2) outperforms the BER performances of related works. Whereas, the error-correction performance of the soft- and hard-decoding of the convolutional code are not good. However, due to the low-complexity in hardware implementation of convolutional codes, they can be selected in some cases as we have mentioned in Section 2.3.1 and Section 2.3.3. Finally, concatenating mode of the TILD-LDPC and convolutional code provides the best BER performance compared with the reference works [14, 15, 22, 23]. Besides achieving a preeminant error-correction performance, the concatenating mode also introduces a free error-floor solution without burst errors. However, the proposed concatenating mode has a low code-rate (1/4), it means that more redundant data will be attached to the original data at the transmitter. In Section 2.1, we look back the theoretical points about the importance of power-constraint in WSNs compared with the bandwidth-constraint. Although transmitting encoded data in concatenating mode reduces effective transmission and may cause some extra energy consumption; however, achieving a higher coding-gain in noisy environment causes reduction of transmitted power, and increase transmission distance between sensor nodes.

Besides, we have evaluated the coding-gain and efficiency of reducing transmited-power of the proposed FEC approach. In particular, Fig.10 and Fig.11 show BER performances of four proposed modes in both AWGN and Fading channels. Some typical convolutional codes are also implemented for evaluation; these versions include convolutional codes in low-constraint (CL3) and high-constraint (CL7), which use the soft- and hard-decision as decoding methods. In this thesis, BER $= 10^{-5}$ is selected as the BER-performance limit for all FEC algorithms, and

this limit is also used for measuring coding-gain values. Fig.10 and Fig.11 show the effectivity of concatenating TILD-LDPC with low-constraint convolutional code in AWGN and Fading channels. We found that although high-constraint convolutional code gives better performances compared with the low-constraint candidates; however, the low-constraint convolutional code always show better performance when it is concatenated with TILD-LDPC. From this unexpected discovery, we propose using low-constraint (CL3) convolutional code for the spliting model and in concatenating mode with TILD-LDPC. In Section 2.3.3, we have also mentioned about the complexity reduction of using low-constraint convolutional codes compared with high-constraint convolutional codes [25]. Therefore, due to the reduced-complexity of low-constraint convolutional code, and high-performance of TILD-LDPC, our proposed method is expected to create a robust error-correction solution with a reduced-complexity for WSNs transceivers.

Transmitted-power reductions in four operational modes in AWGN channel are shown in Fig.12 and Fig.13. We have selected the low-power sub-1Ghz RF transceiver (CC1100) (Fig.12) and 2.4 GHz low-power Zigbee transceiver (CC2591) (Fig.13) to evaluate the reduced transmitted-power. Also, various output-power settings which are in low-to-high dBm ranges representing for different transmitted powers of RF front-ends. We have estimated the power efficiency of the four proposed method from achieved coding-gains and the equation (1). Besides, coding gain performance and transmitted power gain of spliting and concatenating modes are also summarized in Table 2. The proposed solution provides four modes with different levels of:

- Error-correction performances: Coding gains of four operational modes in AWGN channels are 0 (mode M01), 5.5 (mode M02), 9.2 (mode M03) and 10 (mode M04) respectively. Whereas, coding gains are much greater in Rayleigh Fading channel: 0 (M01), 27.4 (M02), 34.2 (M03), 37.8 (M04).

- Required transmitted-power: The uncoded mode requires the high transmitted power to retain the channel reliability. In AWGN channel, transmitted-power reduction of low-constraint convolutional code, TILD-LDPC, and concatenated mode are 71.8%, 88%, 90% respectively. We do not evaluate the transmitted-power gain of proposed modes in Fading channel due to the lack of theoretical foundations and related works.

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Table 2. Coding gains and transmitted-power gains of the proposed error-correction modes.

Proposed algorithms for multi-mode FEC solution		Code rate	Coding Gain (dB)		Transmitted-Power Gain (AWGN)
			AWGN Channel	Fading Channel	
Splitting	Low-constraint Soft-Decision Convolutional Code	1/2	5.5	27.4	3.55
	TILD-LDPC	1/2	9.2	34.2	8.32
Concatenating	Outer	Inner			
	TILD-LDPC	Low-constraint Soft-Decision Convolutional Code	1/4	10	37.8	10

- Scalability: Uncoded, splitting and concatenating modes bring out an integrated FEC solution which inherits effective FEC solutions of popular wireless standards such as Zigbee, Wi-Fi, WiMAX, Bluetooth etc. The complexity of each constitutive FEC block varies from low-complexity (low-constraint convolutional code) to higher complexity (TILD-LDPC) and highest complexity (serial concatenation mode).

- Code-rate: 1, 1/2, 1/4; when code-rate gets smaller, more redundant data will be added to original data to make encoded data more robust so that a higher transmitted-power gain can be achieved. Whereas in case of code-rate equals '1', which is in uncoded mode (M01), this mode can be set up for sensor nodes to operate in a low-noise environment, or near distance transmission, without redundant data in transmitted data.

Table 3 summarizes evaluation results of the proposed method compared with some related works which have been mentioned earlier. In particular, presented results of coding gains, code-rates, error-floor and complexity have shown that the splitting and concatenating mode of low-constraint convolutional code and TILD-LDPC is a scalable high-performance FEC solution. The proposed FEC solution could adapt flexibly to different operational scenarios in wireless sensor networks.
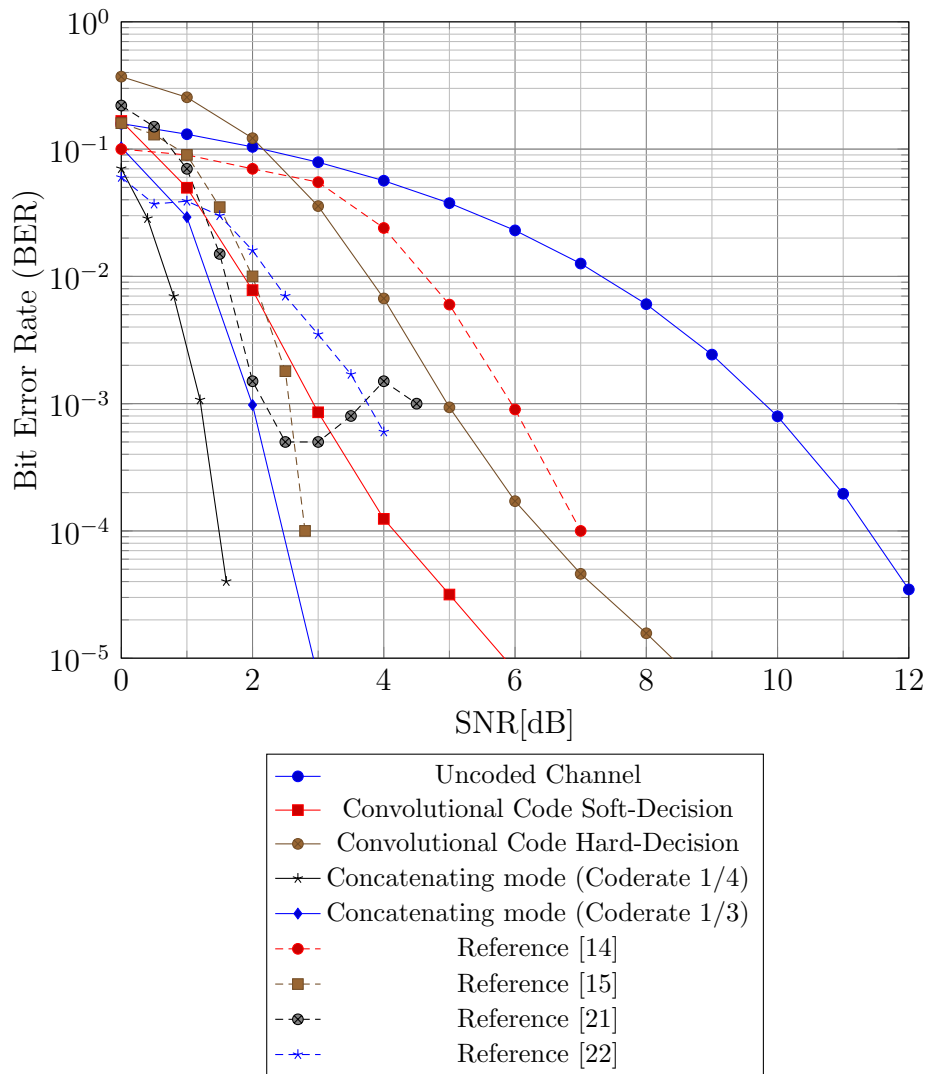
Figure 9. BER performances of serial concatenating mode (TILD-TILD, Convolutional Code) compared with some related works.
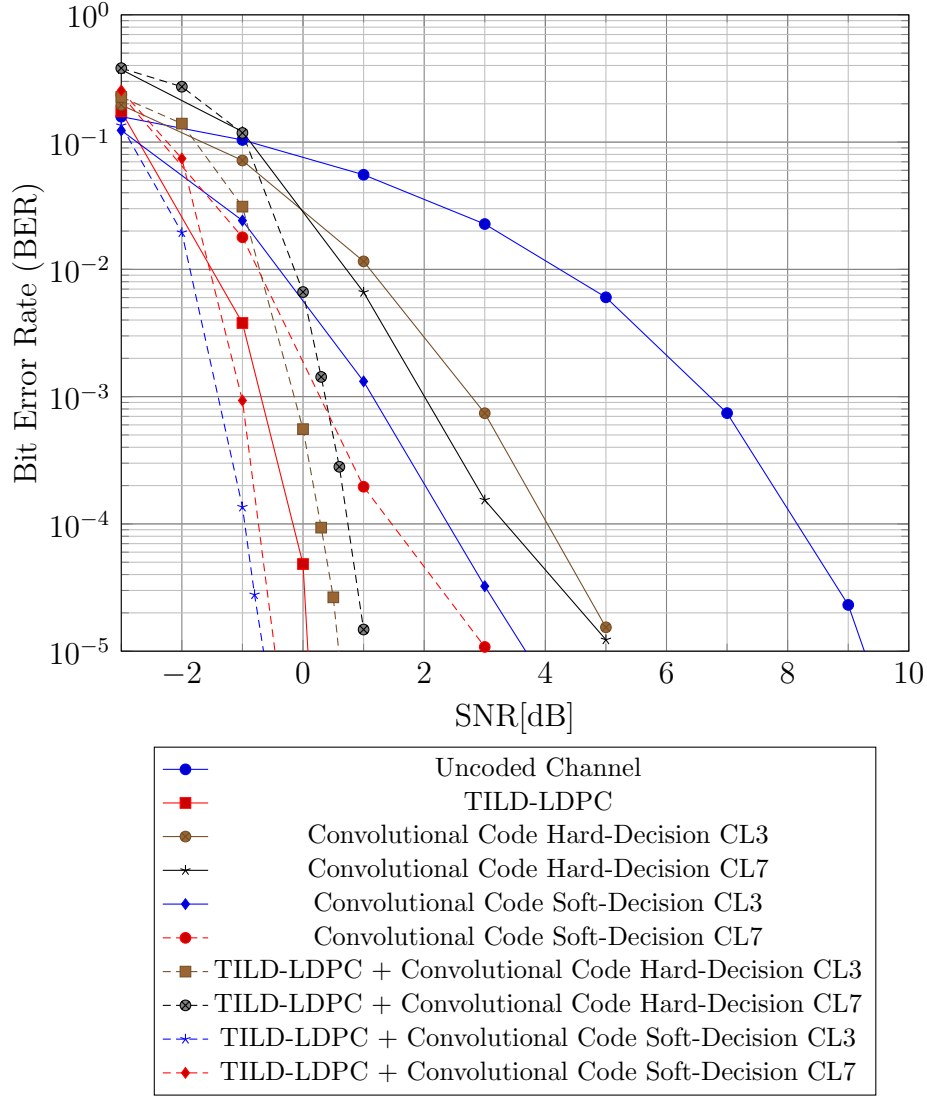
Figure 10. BER performances of the proposed modes in AWGN channel.

Table 3. Evaluation table of the proposed work compared with related works in some criteria.

Criteria	Ref.[14]	Ref.[15]	Ref.[21]	Ref.[21]	This work
Error floor	No	No	Yes	Yes	No
BER performance (Coding gain 10E-4)	4.3	8.5	N/A (Limited at 10E-3)	N/A (Limited at 10E-3)	5.5, 9.2, 10
Code-rate	0.6	0.42	0.33	0.33	1, 0.5, 0.25
Complexity	Low	High	High	High	Reduced
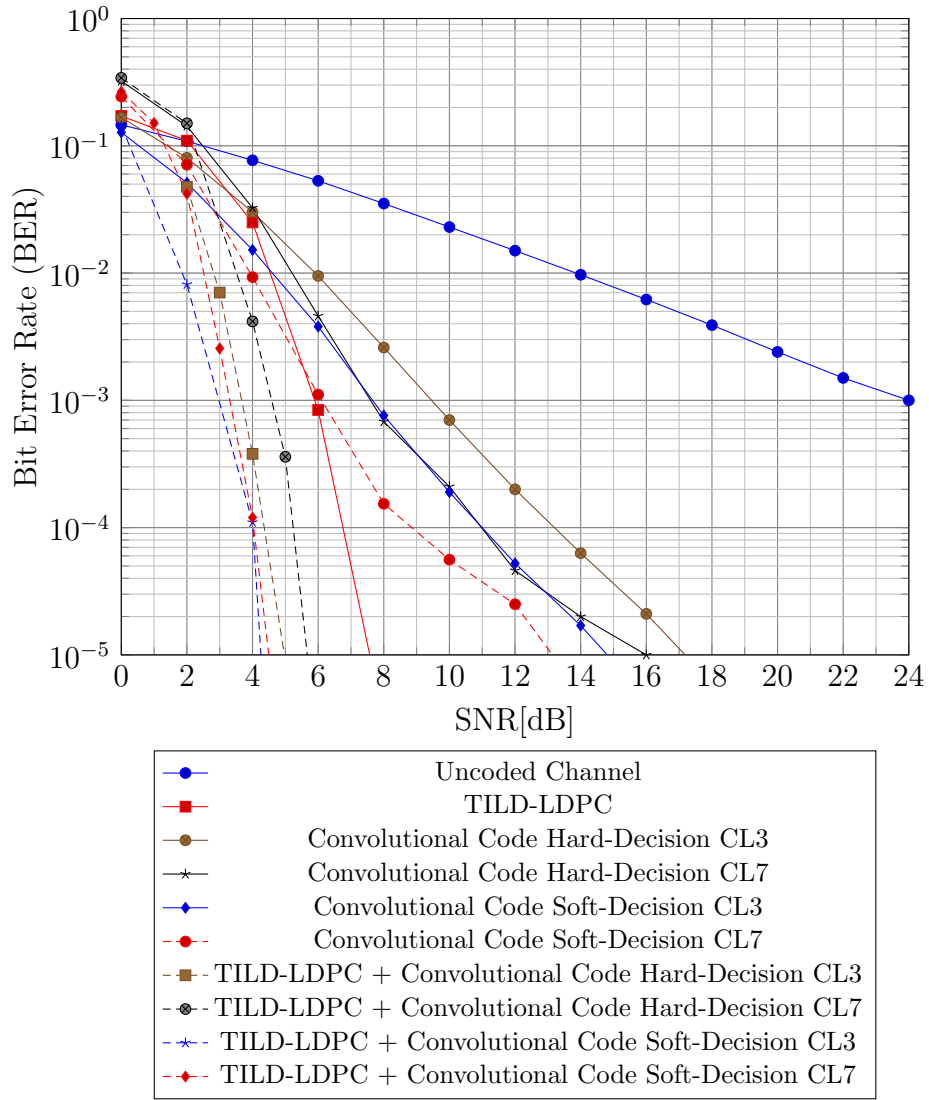
Figure 11. BER performances of the proposed modes in Fading channel.
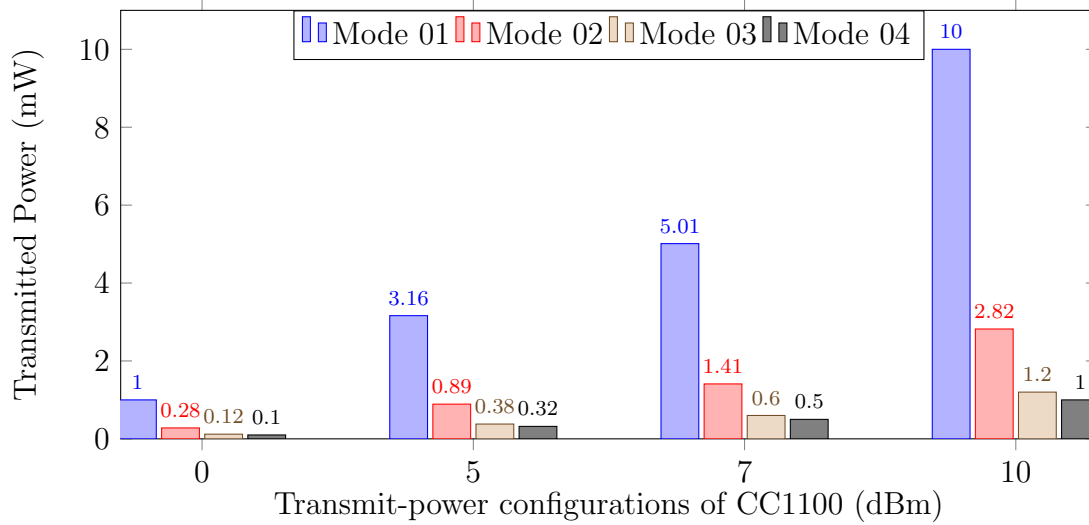
Figure 12. Transmitted power reduction of the proposed modes on Texas Instruments' wireless transceivers CC1100 in AWGN channel.
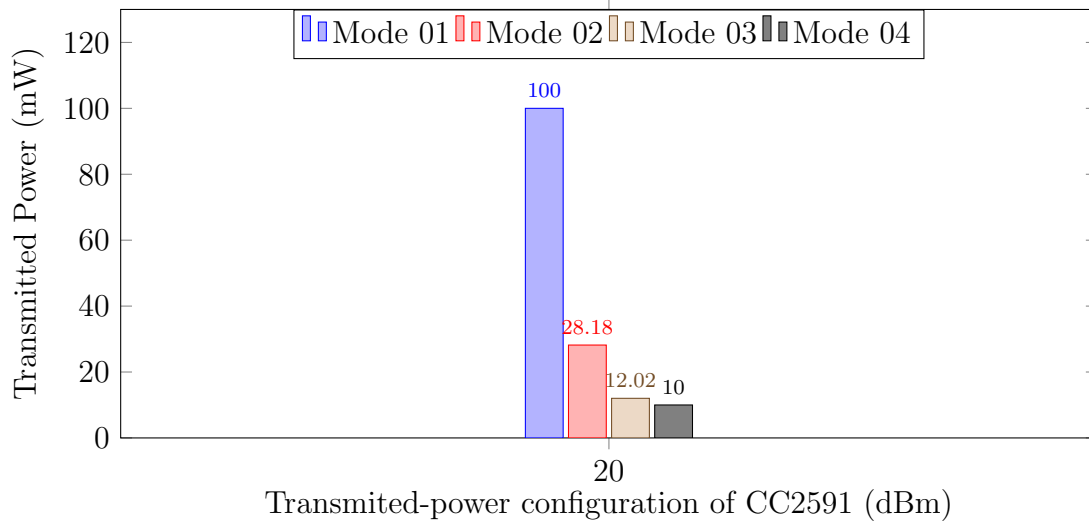
Figure 13. Transmitted power reduction of the proposed modes on Texas Instruments' wireless transceivers CC2591 in AWGN channel.

3 VLSI Architectures of Non-RLL Soft-decoding Visible Light Communication Transmitter and Receiver

3.1 Introduction

3.1.1 VLC-beacon-based indoor positioning systems (IPS)

VLC simultaneously provides both illumination and communication services. Specifically, VLC systems currently utilize visible light for communication that occupies the 380nm-750nm spectrum [26, 12]. Some modulation schemes have been introduced for VLC systems, e.g. Variable Pulse Position Modulation (VPPM), On-off Keying (OOK), or Orthogonal Frequency Division Multiplexing (OFDM) and so on [12, 27]. The VLC transmitter modulates the digital information to light signals through a transmit (TX) front-end and a light-emitting diode (LED).

Generally, indoor localization applications which show users' locations in indoor buildings are getting more attention from researchers and industry in recent years [27]. Several statistics show that human spend almost 80% time of a day indoor where global positioning systems (GPS) could not work [28]. Accordingly, indoor localization is the key to open a wide range of location-based service (LBS) applications. Indeed, mobile indoor positioning in retail is estimated up to $5 billion in 2018 [27]. Current approaches in indoor positioning which are often based on Wi-Fi, Ultra-wideband (UWB), Radio-Frequency Identification (RFID), or other RF wireless techniques [27]. These approaches often meet problems related to high cost of installation and management; or cannot be used in Radio Frequency (RF) banned areas such as hospitals, planes or gas stations [27]. VLC-based indoor positioning solutions have promising characteristics such as low cost, high security, high spatial reuse, low co-channel interference, high-precision and so on [28, 27]. VLC-based solutions, therefore are considered widely as suitable candidates for indoor positioning. In VLC-beacon-based indoor localization systems, unique ID information is transmitted from VLC-LED bulbs for purposes such as identifying objects and locations [29]. Furthermore, beacon-based frames

have been introduced in some publications with the sizes of 158-bit [29], 56-bit [30] or 34 symbols (0.96ms) [31]. We found that the 158-bit beacon-based frame which is defined by Standard of Japan Electronics and Information Technology Industries Association (JEITA) [12, 31] should be considered because an association confirms this work. Particularly, the structure of the JEITA's beacon-based frame includes three parts: start of frame (SOF), payload, and the end of frame (EOF). The SOF contains 6-bit preamble indicating the beginning of the frame, and another 8-bit defines the frame type. The payload includes 128-bit ID data. Finally, 16-bit cyclic redundancy is reserved for error correction [29].

There is one fact that beacon broadcasting of VLC-based indoor localization systems does not require a high-speed link. Therefore, throughout this thesis, we consider the OOK modulation because of its simplicity and smooth implementation. Also, we favor in setting a low frequency for the proposed system to evaluate its performance.

Figure 14. Run-length, bit probability distribution and flicker mitigation.

3.1.2 Flicker mitigation problem

The brightness and stability of the light are strongly affected by the distribution of the 1's and 0's in the data frames. RLL coding is indispensable to avoid LED's flicker and guarantee the direct current (DC) balance in visible light communication systems. Therefore, many DC-balance solutions are introduced to maintain approximately equal numbers of zero and one bits in the data frames. As a result, flicker mitigation which based on DC-balance techniques is considered as one of the essential concerns in any VLC systems. Moreover, when the light source is

modulated for data communication, run-length of the data codewords should be carefully controlled to mitigate the potential flickers. To avoid flicker, the changes in brightness must be faster than the maximum flickering time period (MFTP), which is defined by the maximum time period that light intensity can change without being perceived by human eyes [32]. In normal cases, a MFTP which is faster than 5 ms is considered safe for a non-flicker guarantee. Fig.14 shows an illustrative example to introduce how run-length and bit probability distribution affect to the flicker of VLC systems in case of light is modulated by OOK method. When Manchester coding modulates data, the maximum run-length is limited to 2 while the ratio of bit-0 and bit-1 are always equal in all cases. On the contrary, bit-distribution and run-length of non-RLL instances are arbitrary. Therefore, non-RLL approaches potentially cause flickers which could be recognized at the LED bulbs. As a result, whenever the non-RLL scheme is considered for VLC systems, the run-length and centralized bit probability distribution should be carefully investigated. Also, the lowest transmit frequency that can guarantees flicker mitigation should be considered in such non-RLL OOK VLC systems.

3.2   Related works

Table 4 summarizes proposals related to FEC and flicker mitigation for VLC. The conventional solution is defined in the IEEE 802.15.7 standard, which employs Reed-Solomon (RS) codes, Convolutional Codes (CC) and RLL codes with hard-decoding of RLL codes (hard-RLL) [33]. However, hard-RLL methods of inner RLL codes limit to hard-decoding of outer FEC codes [33, 34, 35]; consequently, the error-correction performance of the entire VLC system is restricted. Recently, soft-decoding RLL (soft-RLL) solutions have been proposed in [36, 37, 38, 39]. These techniques permit soft-decoding FEC algorithms to be applied to improve the bit-error-rate (BER) performance of the VLC system, but they also require heavy computational efforts, with many additions and multiplications.

Zunaira *et al.* have proposed replacing the classic RLL codes with a recursive Unity-Rate Code (URC) or an Unary-Code as the inner code, and a 17-subcode IRregular Convolutional Code (IRCC) is selected for the outer code [40, 41]. Although these methods can achieve different dimming levels with good BER performances; however, the system latency is increased with the iterative-decoding

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schemes. Besides, the reported codeword length is rarely long, which ranges from 1000 to 5000 bits, reduces the compatibility of this proposal to VLC-based beacon systems [29, 30] in which beacon-based frame sizes are always small. As an alternative approach, Kim *et al.* have proposed a coding scheme based on modified Reed-Muller (RM) codes [35]. Although this method can guarantee DC balance at precisely 50%, it has the inherent drawbacks of a deducted code rate and an inferior error-correction performance compared with turbo codes, low-density parity-check (LDPC) codes or polar codes. Also, Lee and Kwon have proposed the use of puncturing and pseudo-noise sequence scrambling with compensation symbols (CS) [42]. This proposal can achieve excellent BER performance; however, puncturing with CSs will lead to redundant bits in the messages, thereby reducing the transmission efficiency. Another coding scheme based on the fountain code, which has dramatically improved the transmission efficiency, is mentioned in [43]. However, this scheme requires feedback information and thus is not suitable for broadcasting scenarios in VLC-based beacon systems. Xuanxuan Lu *et al.* have reported a new class of enhanced Miller codes, termed eMiller codes which is a class of RLL codes known for high-bandwidth efficiency [44]. Besides, she also proposed an improved version of the Viterbi algorithm, termed *mnVA* to further enhance the performance of her proposed eMiller code. It can be seen from her simulation results that eMiller helps improve the performance of the whole VLC system, and this code seems to be a promising candidate for VLC applications. However, we have found two main drawbacks of this approach are the unoptimized code-rate = 1/2 of the eMiller code (Table 5), and an increase in computational complexity.

Advantages of Polar code are exploited intensely together with soft-decoding of RLL codes have been introduced at [38, 39]. According to these publications, Manchester and 4B6B codes are used as RLL solutions for the VLC system. As a result, their BER performances have been improved remarkably with a flexibility of Polar code's code-rate. However, we found that the code-rate = 1/2 of Manchester code, or code-rate = 0.67 of 4B6B (summarized at Table 5) are also not the best optimization solution for channel efficiency enhancement, if compared with non-RLL approaches. Fang *et al.* have recently proposed a non-RLL polar-code-based solution for dimmable VLC systems [32]. This approach has shown

Table 4. Overview of FEC algorithms and flicker mitigation solutions for VLC.

FEC solution	Flicker mitigation
RS, CC [33]	Hard-RLL
Multi-RS hard-decoding [34]	Hard-RLL
LDPC [45]	Hard-RLL
RS soft-decoding [36, 37]	Soft-RLL
Polar code [38, 39]	Soft-RLL
Irregular CC [40]	Unity-Rate Code
Irregular CC [41]	Unary-Rate Code
Reed-Muller [35]	Modified original code
Turbo code [42]	Puncture + Scrambling
Fountain code [43]	Scrambling
Convolutional code, Viterbi [44]	Enhanced Miller code
Polar code (N=2048) [32]	Flicker-free
Proposed method (K=158, N=256)	Flicker-free
(JEITA's beacon frame size)	

promising results in weight distribution and run-length distribution. Moreover, this solution also shows an improved transmission efficiency while achieving a high coding gain compared with RS and LDPC codes. We have found that this solution can overcome most of the drawbacks of the related works mentioned until now. Specifically, it offers the non-iterative decoding with a low-complexity. Also, it has a flexible code-rate and a high BER performance without requiring any feedback information. However, we found that the biggest obstacle of this proposal is the equal probabilities of short runs of 1's and 0's can only be achieved with a long codeword length; as chosen to be N=2048. Indeed, long data frames are rarely applied in low-throughput VLC systems, for instances, VLC-based beacon ones [29, 30]. It can be found that the non-RLL solution based only on a polar encoder [32] might not be applicable in such VLC-based beacon systems because DC balance is not guaranteed for short data frames.

In the later parts of this thesis, we point out the unsolved problems of non-RLL flicker mitigation in VLC-based beacon systems. Additionally, we introduce a couple of non-RLL beacon-based VLC transmitter and receiver and their VLSI

architectures. In summary, our contributions include:

1. First discussion on the importance of FPGA and ASIC implementations of VLC transmitters and receivers in VLC-based beacon systems.

2. A non-RLL flicker mitigation method based on a prescrambled Polar encoder (Section 3.3).

3. Two proposed hardware architectures of beacon-based VLC transmitter and receiver (Section 3.4).

4. A 3-bit soft-decision filter which can support soft-decoding of FEC decoders in real prototypes of VLC receivers (Section 3.4.2).

3.3 Flicker mitigation based on a non-RLL prescrambled Polar encoder

It follows from the Section 3.2, due to the small size of beacon-based data frames, a non-RLL DC-balance solution which dedicated for the VLC-based beacon systems seems still to be an unsolved problem. In this section, we introduce a non-RLL flicker mitigation solution which is designed for VLC-based beacon systems. Particularly, our flicker mitigation solution is the combination of a simple pre-scrambler placed at the outer code, with a (256;158) polar encoder set at an inner code's position. Fig.15 briefly introduces our proposal in style of a block diagram.

Table 5 summarizes a code-rate comparison of RLL and non-RLL solutions. It can be noticed that non-RLL solutions keep the system rate unchanged while removing the heaviness of RLL encode/decode blocks. Furthermore, FEC decoders also inherit from the removing RLL codes because soft-decoding of them can be implemented without difficulties in achieving LLR values. However, DC-balance and run-length should be controlled strictly in such non-RLL VLC systems.

In a digital transmission system, a data scrambler plays a vital role because it causes energy to be spread more uniformly. At the transmitter, a pseudorandom cipher sequence is modulo-2 added to the data sequence to produce a scrambled data sequence.

Table 5. Code-rate comparison of non-RLL and RLL solutions.

Code	Code-rate
Manchester	1/2
FM0/FM1	1/2
Conventional Miller	1/2
eMiller [15]	1/2
4B6B	0.67
8B10B	0.8
non-RLL (our work)	1 (No changed)

Describe the generating polynomial P(x) as:

$$P(x) = \sum_{q=0}^{N} c_q.x^q \tag{2}$$

where $c_0 = 1$ and is equal 0 or 1 for other indexes.

We have found that the output bit probability distributions of pre-scramblers in different generating polynomials seem to differ slightly. Therefore, we propose a simple generating polynomial presented in equation (3) to reduce the number of shift registers required for a pre-scrambler.

$$P(x) = x^4 + x^3 + 1 \tag{3}$$

Meanwhile, polar codes can be classified into two types: non-systematic and systematic codes. Typically, a polar code is specified by a triple consisting of three parameters: *(N, K, I)*, where N is the codeword length, K is the message length, and I is the set of information bit indices. Let d be a vector of N bits, including information bits. The generator matrix is defined as $G = (F^{\otimes n})_I$. Then, given a scrambled message u of K bits in length, a codeword x is generated as given in (4).

$$x = u.G = d.F^{\otimes n} \tag{4}$$

A Polar encoder is formed of many layers of XOR gates, with a complexity of $\frac{N}{2}log_2 N$ XORs. There is one fact that systematic polar codes were introduced to achieve better error-correction performances compared with non-systematic
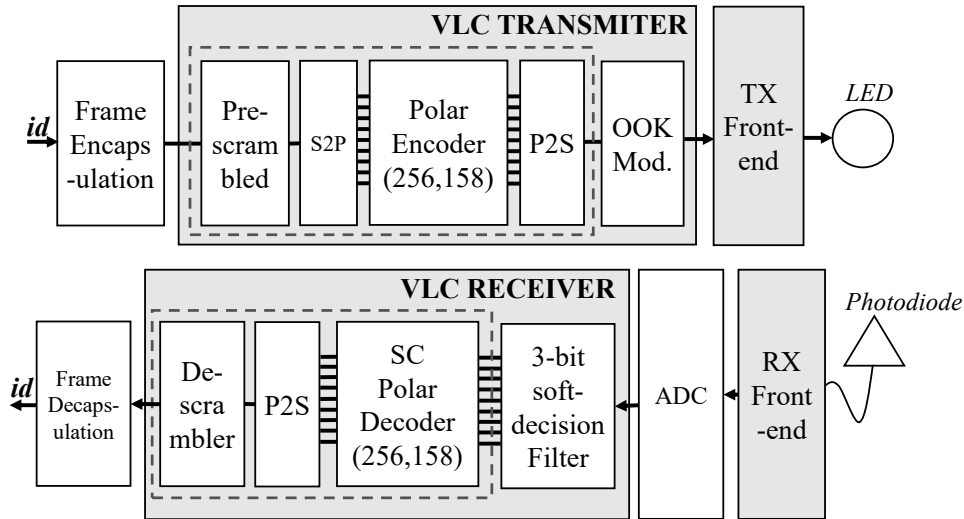
Figure 15. Block diagram of the proposed VLC transmitter/receiver.

codes [46]. However, due to the information bits transparently appear as a part of the codeword, we have found that the output bit-probability distribution of a systematic Polar encoder (SPE) is not well centralized. On the other hand, the output bit probability distribution of a non-systematic Polar encoder (NSPE) naturally becomes centralized approximately 50% 1's and 50% 0's when the codeword length is long enough [32].

In summary, we have selected the Polar code as the main FEC scheme for our VLC-based transmitter/receiver due to several reasons:

1. The encoder's output bit probability distribution is naturally centralized when long codewords are applied in the system.

2. Unusual code rates are supported. Specifically, a (256;158) polar code, which has a code rate of 0.617, is suitable for a beacon-based frame size of $K=158$.

3. High error-correction performance can be achieved with a low hardware complexity [47].

4. The inherently short run lengths of a polar encoder can be useful in mitigating the lighting flicker [32].

A pre-scrambler can help to ensure the fast convergence of the output probability distribution of an inner (256;158) Polar encoder. As a result, DC balance in a VLC-based beacon system can be guaranteed by the proposed transmitter depicted in Fig.16.

3.4 Hardware architecture of the proposed VLC transmitter and receiver

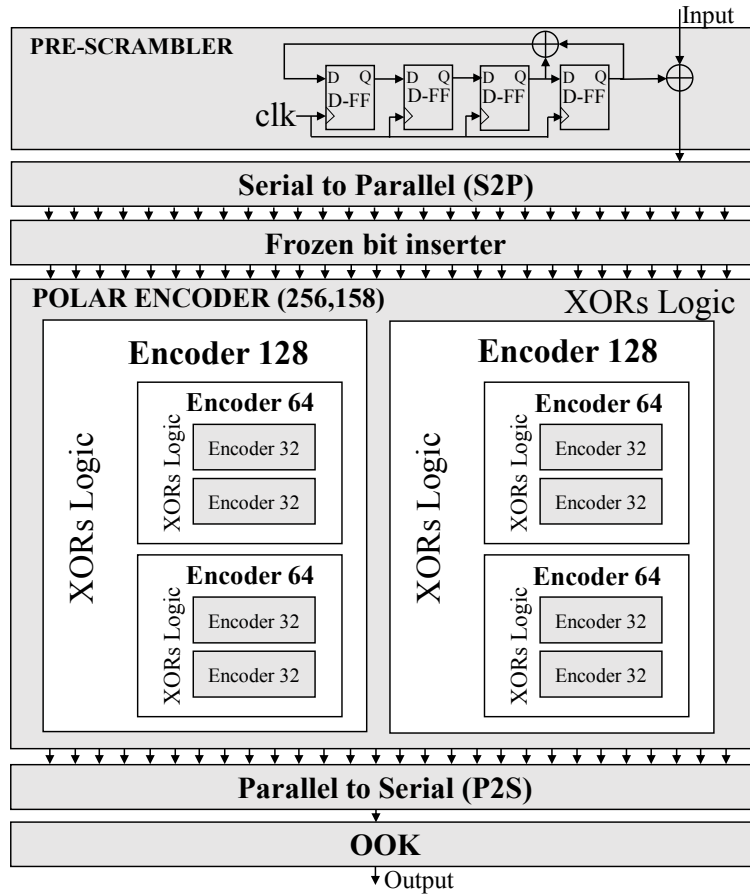### 3.4.1 Hardware architecture of the VLC transmitter

Figure 16. The hardware architecture of proposed non-RLL VLC transmitter.

Block diagram of the proposed VLC transmitter is shown in Fig.16. As mentioned in Section 3.2, it seems that Polar code is an optimal candidate for an

FEC solution in VLC receivers [32, 39]. In Section 3.3, we have also introduced a pre-scrambled Polar encoder as non-RLL flicker mitigation in case of beacon-sized codewords which defined by JEITA are applied in the VLC-based beacon systems. In fact, the IEEE 802.15.7 standard has stated that Reed-Solomon (RS) and convolutional codes are preferred over low-density parity check (LDPC) codes to support short data frames, hard-decoding with low complexity [33]. We found that flexible code-rates of the Polar code can support any sizes of data frames [46]. Also, its soft-decision decoding can improve the reliability of the VLC systems compared with RS and convolutional codes. Moreover, the inherent low-complexity characteristic of Polar code's encoding and Successive-Cancellation (SC) decoding is suitable for being applied in VLC receivers.

In the proposed VLC transmitter described in Fig.15 and Fig.16. Firstly, 128-bit ID information data is wrapped by a frame encapsulation procedure to form a 158-bit beacon-based frame [29]. Next, the 158-bit frame is scrambled by a pre-scrambler. Due to a simple generating polynomial (3) is applied, only four registers and one XOR gate are required to create a pre-scrambler. The frozen bit inserter plays a role of inserting $N - K$ frozen bit indices into different positions of a 256-bit frame. In particular, in case JEITA's 158-bit beacon-based frame is applied, 98 frozen-bits are inserted at positions defined at the Polar code construction stage. After frozen bits are inserted, the pre-scrambled 256-bit frame is encoded by a Polar encoder (256;158) to create a bit stream in which the DC-balance can be guaranteed even without any RLL codes. Regarding with the Polar encoder, we have implemented a recursive combinational architecture for the Polar encoder, in which 2^N-code-length encoders are created by $N/2$ XOR gates and two 2^{N-1}-code-length encoders Fig.16. Due to the block encoding characteristic of the Polar encoder, the Serial-to-Parallel (S2P) block is implemented to prepare the pre-scrambled serial bit-stream to a 256-bit register. This register is the input register of the Polar encoder. Also, Parallel-to-Serial (P2S) block converts parallel Polar encoded bits to serial bit stream before being modulated by the OOK block. Finally, the VLC TX front-end converts the OOK-modulated signals to light signals and broadcast them to the air. Specifically, we have also assembled a VLC TX front-end that successfully transmit information through a normal 5V LED with a transmit frequency up to 2.5 MHz.
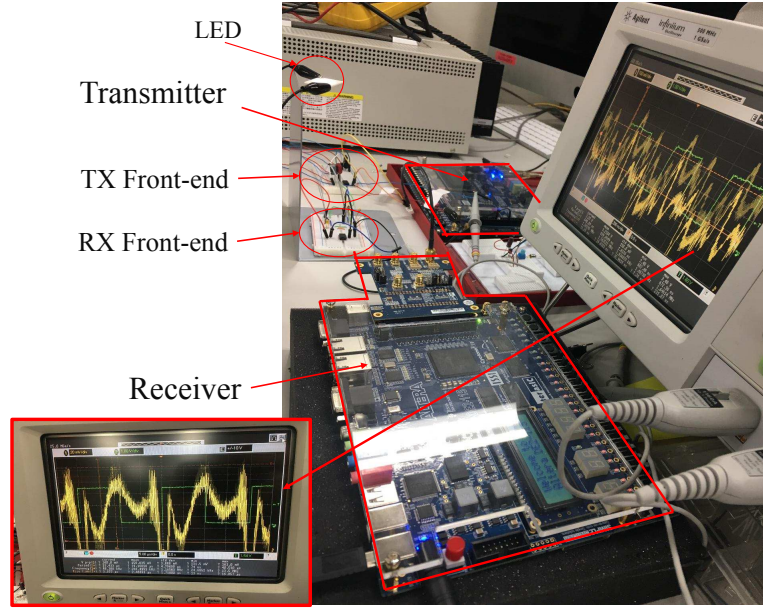
Figure 17. Distorted received signals due to the bad channel settings.

3.4.2 Hardware architecture of the VLC receiver

3-bit Soft-Decision Filter   Fig.17 shows our FPGA-based VLC demonstration system in which distorted signals are received at the VLC RX front-end, then it is displayed on the oscilloscope. Specifically, we have found that distortions appear in two experimental scenarios. Firstly, when the transmit frequency is higher than the maximum rate that RX front-end can receive. Secondly, when the distance between TX LED and RX front-end increases in space, distortions of the received signals also appear with shrunken peak-to-peak voltages (Vpp). Distorted received signals are usually the cases cause reliability of the VLC system deducted because hard-decoding of RLL and FEC are often the default selections in most VLC receivers [33]. In this thesis, we introduce a 3-bit soft-decision filter which is implemented at VLC receiver to support soft-decoding of RLL and FEC decoders in real VLC receiver prototypes.

Specifically, in the case of VLC AWGN channel, a sequence of the LLR values which is necessary for soft-decoding of FEC decoder, are expressed by Eq.5.

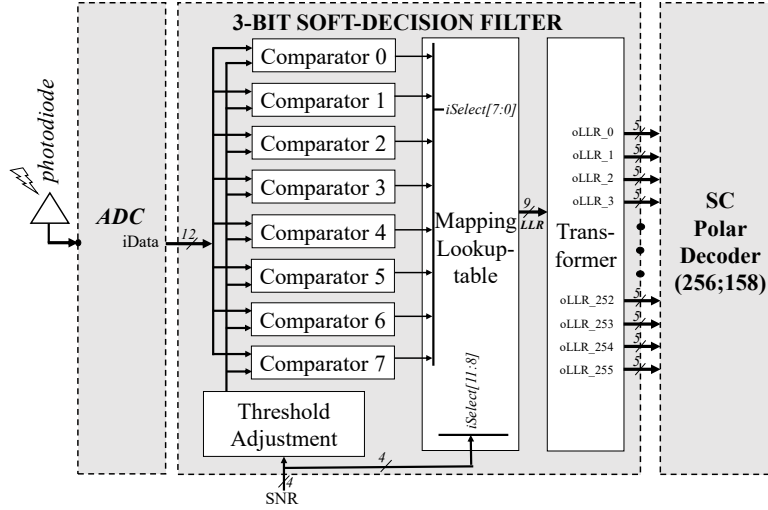$$LLR(y_i) = \ln \frac{P(x_i = 0|y_i)}{P(x_i = 1|y_i)} \tag{5}$$

Figure 18. Hardware architecture of the 3-bit soft-decision filter.

where y_i is the received sample and the conditional probability is generally calculated as Eq.6.

$$P(x_i|y_i = \Delta) = \frac{1}{\sqrt{2\pi\sigma_\Delta^2}}e^{-\frac{(y_i-\mu_\Delta)^2}{2\sigma_\Delta^2}} \tag{6}$$

where μ_Δ and σ_Δ are the mean value and standard deviation for $\Delta = 0, 1$. However, when making a real prototype of the soft-decoding VLC receiver, we found that it is unfeasible in estimating the LLRs using such equations (5) and (6) due to μ_Δ and σ_Δ cannot be estimated in real optical wireless channels. Therefore, in this thesis, we propose applying a soft-decision filter which is first introduced in optical communication systems for our VLC receiver prototype [48].

Fig.18 shows the proposed hardware architecture of 3-bit decision filter that we have implemented. Firstly, an analog-to-digital converter (ADC) converts analog signals received from the RX front-end to digital signals. The 3-bit soft-decision filter analyses these digital signals and calculate LLR values to feed to the soft-decoding Polar decoder. The soft-decision filter includes 2^{N-1} decision thresholds to compare with the incoming received signal, where N is the number of quantization bits. Previous research on the soft-decision filter in optical communication systems has shown that 3-bit soft decision was the optimum solution [48]. In the case of $N=3$ for 3-bit soft decision, we established seven threshold voltages from V_{t+3} to V_{t-3} which are calculated from equations given in equa-
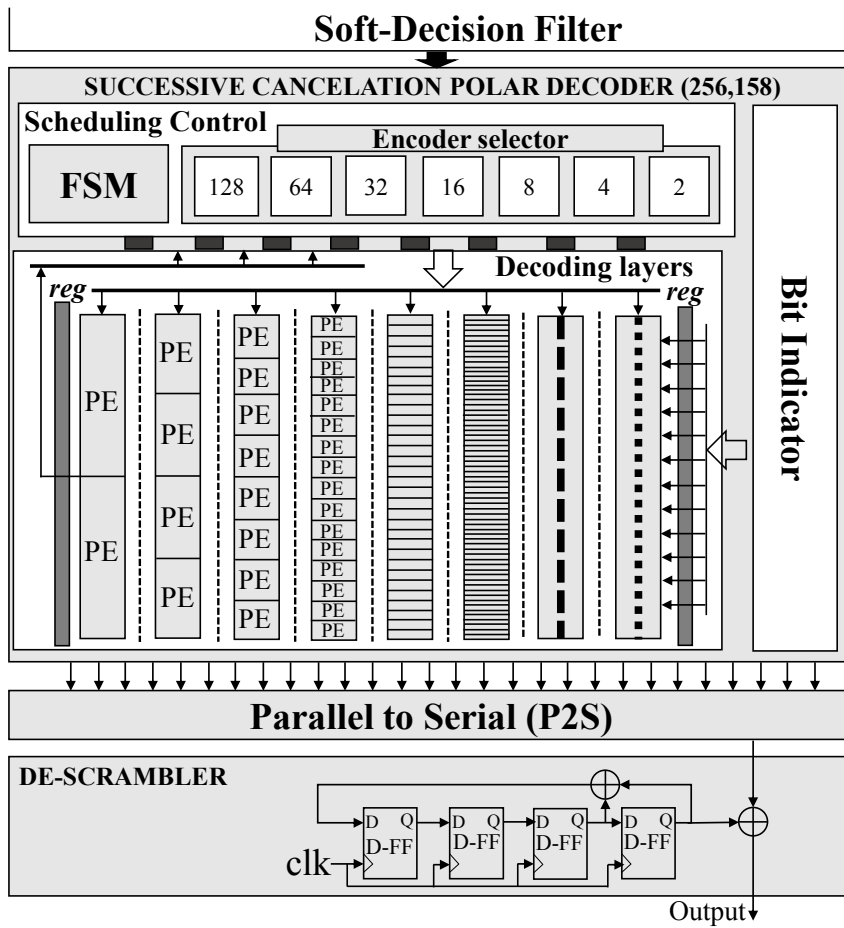
37

Figure 19. The hardware architecture of our non-RLL VLC receiver.

tion (7). We have defined a mapping table with output LLR values are carefully chosen from training simulation results on MATLAB. Table 6 shows ranges of comparison and their output LLR values. The sequence of 9-bit LLR results of mapping lookup-table is buffered and quantized by a block named *Transformer*, before passing them to the Polar decoder.

$$
\begin{aligned}
V_t &= \frac{V_{peak+} + V_{peak-}}{2} \\
V_{t-1} &= V_t - \frac{V_{peak+} - V_t}{4} \\
V_{t-2} &= V_t - 2\frac{V_{peak+} - V_t}{4} \\
V_{t-3} &= V_t - 3\frac{V_{peak+} - V_t}{4} \\
V_{t+1} &= V_t + \frac{V_{peak+} - V_t}{4} \\
V_{t+2} &= V_t + 2\frac{V_{peak+} - V_t}{4} \\
V_{t+3} &= V_t + 3\frac{V_{peak+} - V_t}{4}
\end{aligned}
\tag{7}
$$

Table 6. The mapping table of 3-bit soft-decision filter.

Comparator	Range	Output LLR values
0	$[V_{peak+} \; ; V_{t+3}]$	1.2017
1	$[V_{t+3} \; ; V_{t+2}]$	0.3630
2	$[V_{t+2} \; ; V_{t+1}]$	0.2185
3	$[V_{t+1} \; ; V_t]$	0.0656
4	$[V_t \; ; V_{t-1}]$	-0.0702
5	$[V_{t-1} \; ; V_{t-2}]$	-0.2116
6	$[V_{t-2} \; ; V_{t-3}]$	-0.3547
7	$[V_{t-3} \; ; V_{peak-}]$	-1.1943

Successive cancellation (SC) Polar decoder and descrambler Fig.19 shows the proposed hardware architecture of our non-RLL VLC receiver. Firstly,

as explained in Section 3.4.2, the proposed 3-bit soft-decision filter enables applying a soft-decoding Polar decoder at the VLC receiver to increase the reliability of the system. Indeed, the soft-decision filter passes 256 LLR values to the parallel inputs of the SC polar decoder. Fig.20 shows the hardware architecture that we have implemented for the non-systematic SC Polar decoder, and Fig.21 describes the architecture of one processing element (PE). Compared with the conventional architectures of the Polar decoder, our implemented Polar decoder (256;158) has three unusual features. Firstly, eight layers of processing elements (PEs) are purely processed by the combinational logic, because we have removed all intermediate registers to reduce the decoding latency. Secondly, the last stage's PE is modified to output two decoded information bits every each clock cycle. Thirdly, we have implemented a partial sums generator (PSG) based on Polar encoders with various code-length sizes, and integrate the PSG into the scheduling control block of the SC Polar decoder. The decoded data is converted to a serial form and is descrambled by a descrambler. Finally, the frame decapsulation block removes the SOF and EOF fields to extract the ID data.

3.5 Results and discussion

3.5.1 Flicker mitigation results

In the previous non-RLL solution work based only on a polar encoder [32], the authors have demonstrated the fluctuation of the code weight distribution around the 50% dimming level. Specifically, in the case of a polar encoder with 2048-bit codewords, the percentage of one bits was reported to fluctuate in the range of (42.1875%, 57.8125%).

However, we have found that this fluctuation range can only be achieved when the proportions of 1's and 0's in the input data (before the FEC encoder) are both equal to approximately 50%. Unfortunately, the bit ratio of the input data is unknown beforehand because of the randomness of these data, and this input bit ratio dramatically affects the output bit ratio of the FEC encoder. In this thesis, we evaluate our proposed method using a worst-case input bit ratio corresponding to 10% zero bits and 90% one bits. A simulation was performed using 10,000 158-bit data frames. If the minimum and maximum bit ratios are included, the real
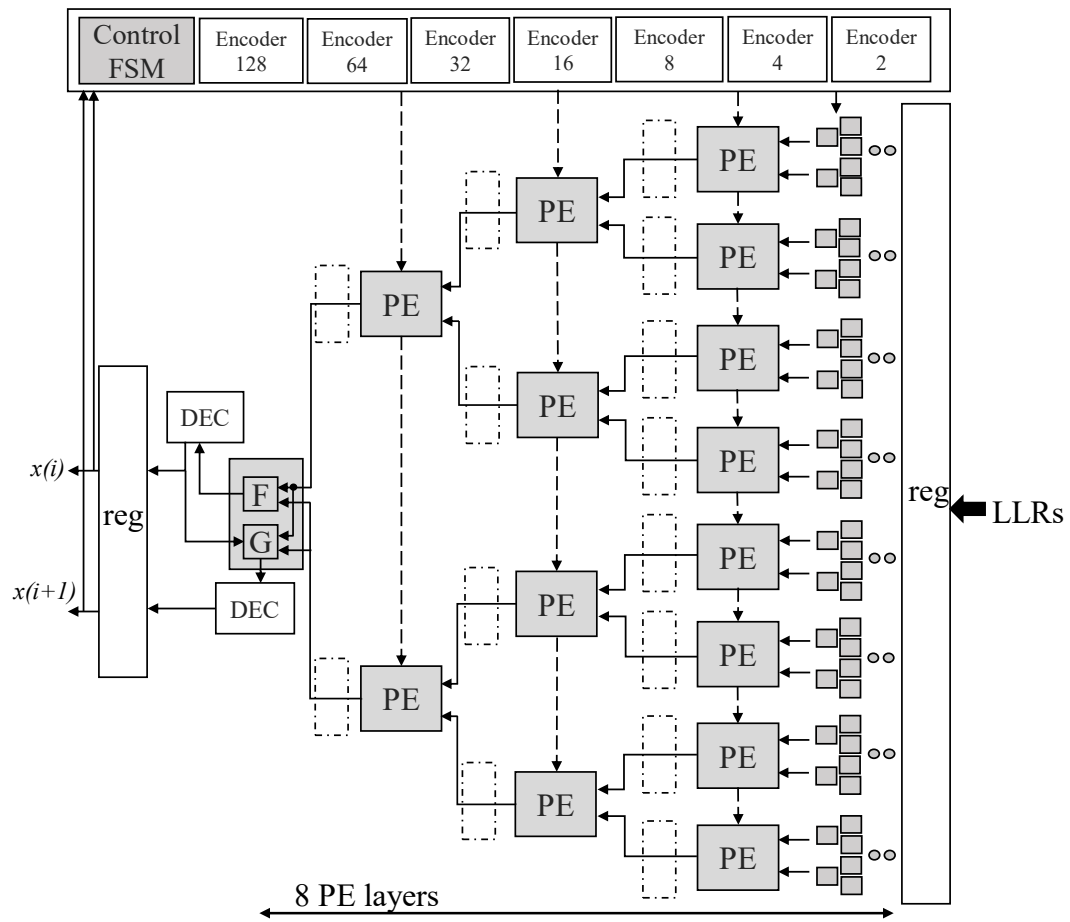
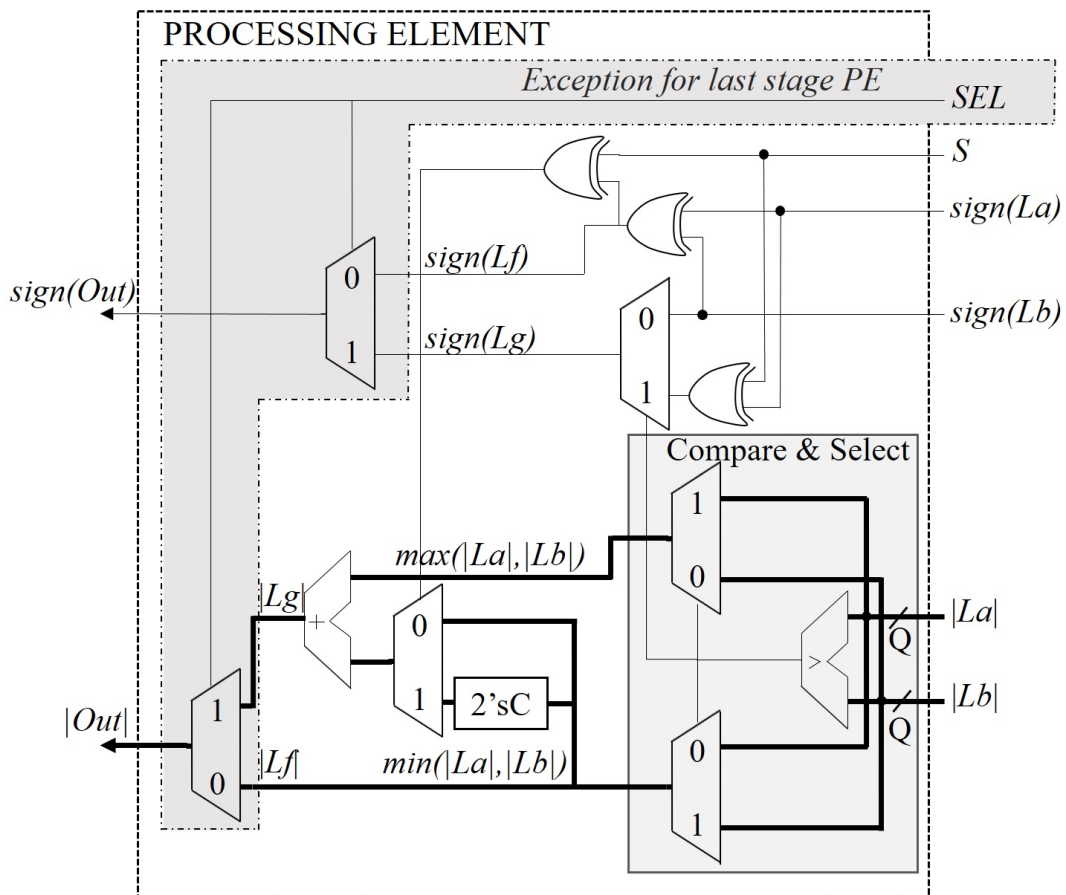Figure 20. The hardware architecture of our Polar decoder.

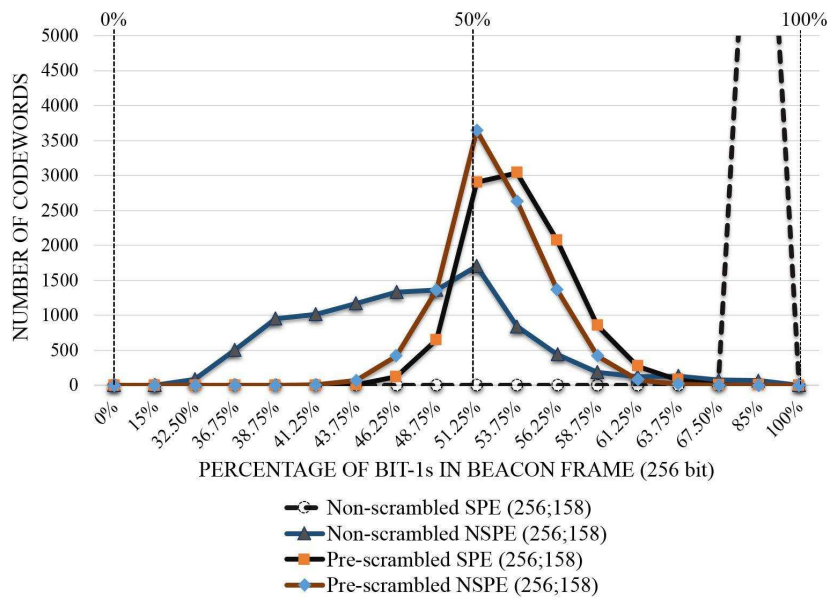Figure 21. The hardware architecture of a processing element.

Figure 22. Output bit probability distributions of non-scrambled/ pre-scrambled NSPE and SPE.
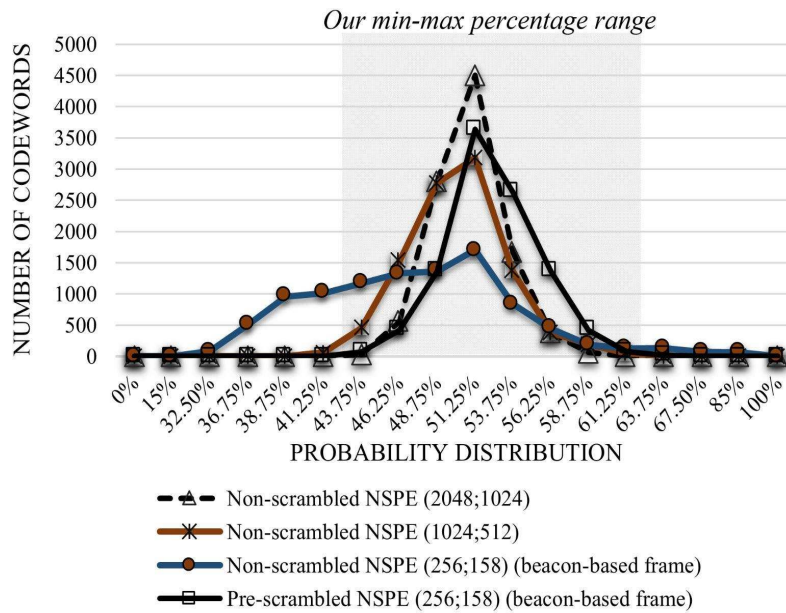
Figure 23. Output bit probability distributions of pre-scrambled and non-scrambled NSPEs with long and short codeword lengths.

fluctuation range of the output bit probability distribution of a polar encoder with 2048-bit codewords is (41.25%, 61.25%). From the experimental results presented in Fig.22, we can also see that the bit distribution of an NSPE shows a little bit more centralized than that of a SPE regardless of whether pre-scrambling is applied. Especially when a pre-scrambler is not used, the probability distribution of the SPE tends toward 85% one bits because it is significantly affected by the input bit probability distribution. Fig.22 shows the impact of a pre-scrambler on the output bit probability distribution of the NSPE and SPE. Notably, DC balance is not guaranteed in the case of a (256;158) polar code if a pre-scrambler is not applied because the encoder's output bit probability distribution is spread over a broad range of percentages (32.5%, 85%). However, when a pre-scrambler is used, the output fluctuation range of the pre-scrambled (256;158) polar encoder is (41.25%, 63.75%), whereas the fluctuation ranges of polar encoders with codeword lengths of 2048 and 1024 are (41.25%, 61.25%) and (38.75%, 67.5%), respectively, which is shown in Fig.23. Thus, pre-scrambling causes the output bit probability distribution of a (256;158) NSPE to be approximately equal to those of (1024;512) and (2048;1024) encoders.
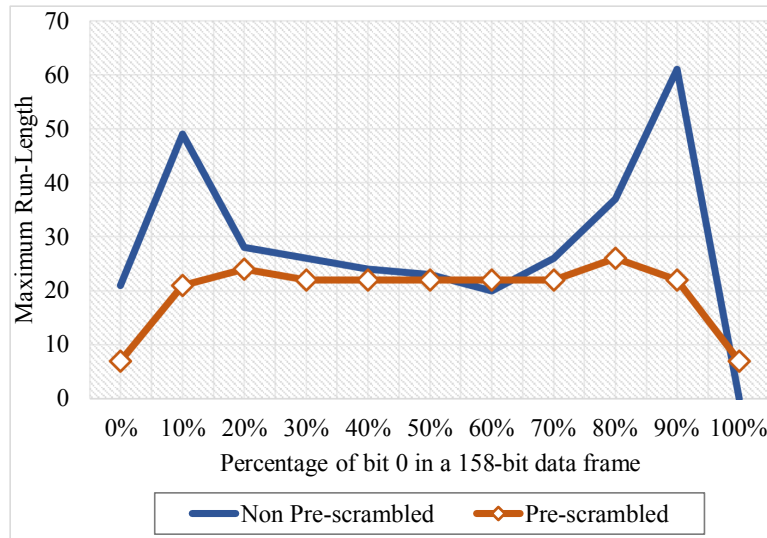

Figure 24. Run-length reduction performance of the pre-scrambled NSPE.

The bit-probability distribution results presented in Fig.22 and Fig.23 demonstrate that a pre-scrambler combined with a Polar encoder is useful for ensuring
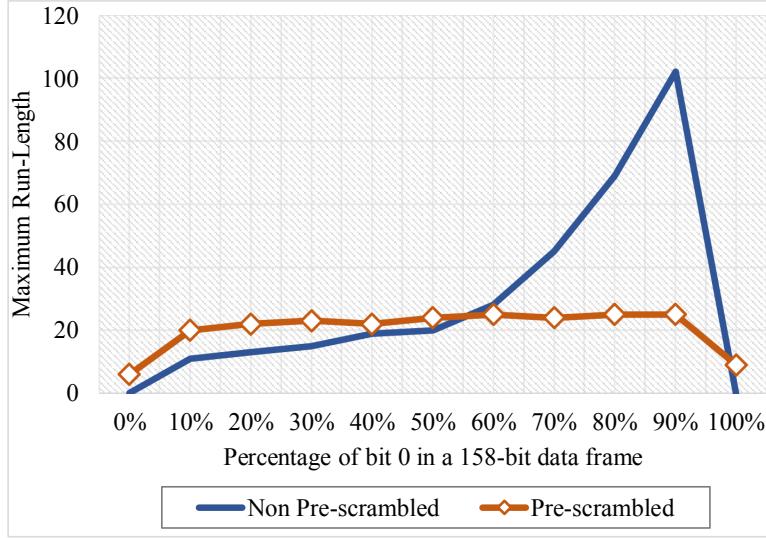
Figure 25. Run-length reduction performance of the pre-scrambled SPE.

faster convergence to a centralized output bit probability distribution. Accordingly, DC balance can be guaranteed in VLC-based beacon systems with a short data frame length of 158 bits. Compared with the non-RLL DC-balance solution based only on a polar encoder with 2048-bit codewords presented in [32], the proposed method can achieve the same output bit probability distribution with a codeword length that is shorter by a factor of 8.

Evaluating the flicker mitigation also requires consideration on run-length of all packets. In the MATLAB simulation model, we have sent 10000 frames with the percentage of bit-0 in each 158-bit data frame changes from 0% to 100%. The results have been presented in graphs at Fig.24 and Fig.25. Accordingly, the maximum run-lengths are reduced remarkably in case of the pre-scrambled technique is applied for Polar encoders. Specifically, the maximum run-length reduction that NSPE can achieve is 2.9; while an even better effect that SPE has achieved is the gain of 4.08 when 90% of bit-0 appears in a data frame. About the relationship between maximum run-length and minimum flicker mitigation frequency, we introduce a simple equation (8) that may be useful to estimate the minimum transmit frequency. Specifically, F_{minFM} is the minimum frequency that flicker mitigation is guaranteed; $maxRL$ is the maximum run-length and $MFTP$ is stated around 5 ms [32]. Hence, the minimum frequency that the

flicker mitigation in our proposed system is guaranteed is 2.5 kHz, which is still much smaller than the minimum frequency defined in [33].

$$F_{minFM} = \frac{1}{\text{MFTP . maxRL}} \tag{8}$$

Table 7 summarizes some evaluation results of the flicker mitigation using the prescrambled Polar encoder. Compared with related works, our work shows advantages in code-rate, with an acceptable range of DC balance in short codewords (256 bits). Finally, as mentioned earlier, the max run-length 27 could guarantee the flicker mitigation when the system frequency is larger than 2.5 kHz.

Table 7. Evaluation table of the proposed work compared with related works in some criteria.

Evaluation criteria	Unity-rate [40]	Unary code [41]	Pun, Scram. [42]	Polar code [32]	Prescrambled Polar (this work)
Code-rate	FEC*0.89	0.4, 0.333	0.333	0.5 (FEC*1)	0.617 (FEC*1)
Codeword	1000, 5000	1000, 5000	1024	2048	256
Max run-length	N/A	N/A	N/A	260	27
Bit-0-1 distribution	44%-56% (Dim 50%)	74%-82% (Dim 78%)	48.63% - 51.37%	42.18%-57.81%	41.25%-63.75%

3.5.2 Hardware implementation results

Table 8. FPGA synthesys results of our VLC transmitter and receiver.

	Transmitter	Receiver
Device	Cyclone IV	Cyclone IV
Model	1200mV 0C	1200mV 0C
Fmax	382.85 MHz	29.31 MHz
LE/LUT	1896/114480 (1.65%)	12134/114480 (10.6%)
Registers	1879	3109
Memory bits	0	1152

The block diagram of the proposed architectures of the VLC transmitter and receiver are presented in Fig.15, Fig.16, Fig.17. Verilog HDL language describes the proposed hardware architecture before Quartus II software synthesizes it. The

Table 9. Resource summary of our VLC transmitter and its function blocks.

Instance	Logic Cells	Register	LUT/Reg.LCs
Polar encoder	1437 (160)	1292 (158)	712(75)
Frozen Inserter	158 (158)	158 (158)	712 (149)
Parallel to Serial	259 (259)	258 (258)	193 (193)
Prescrambler	5 (5)	4(4)	5(5)
Serial to Parallel	178 (178)	167 (167)	168 (168)
Total	**1896 (0)**	**1879 (0)**	**946 (0)**

Table 10. Resource summary of our VLC receiver and its function blocks.

Instance	Logic Cells	Register	Mem. bit	LUT/Reg.LCs
Soft-dec. Filter	1341 (1341)	1301 (1301)	1152	1300 (1300)
Polar Decoder	10519 (3192)	1545 (1537)	0	2748 (1522)
Parallel to Serial	267 (267)	258 (258)	0	249 (249)
Descrambler	7 (7)	5 (5)	0	5(5)
Total	**12134 (0)**	**3109 (0)**	**1152**	**4302 (0)**

selected targeted device is Cyclone IV EP4CE115F29C7 FPGA. FPGA synthesis results of our VLC transmitter and receiver are given in Table 8. It can be seen that the consumed resource of the receiver is much more than the transmitter one. The consumed LE/LUT of our transmitter takes only 1.65% of the Cyclone IV FPGA. This result implies that there are around 60 VLC transmitters can be implemented on the same FPGA. Regarding this result, we expect that multi-VLC-transmitters could be implemented on one FPGA to reduce the cost and enhance the performance of the VLC system.

Table 9 and Table 10 summarize the logic resource that components of our transmitter and receiver have consumed. At the transmitter, the Polar encoder is the biggest block which takes around 76% of the whole VLC transmitter. On the other hand, the pre-scrambler only takes less than 1% resource of the whole transmitter, but it provides an effective solution in centralizing bit-probability distribution (Section 3.5.1). At the receiver, the Polar decoder block is the heaviest one. Specifically, it takes more than 85% resource of our receiver. Whereas the soft-decision filter occupies around 11%, and the descrambler only takes an unno-

ticeable amount of logic cells. The maximum frequency of the VLC transmitter can be up to more than 382 MHz because the polar encoder is created mostly from modulo-2 computations which are simple elements. On the contrary, the receiver's maximum frequency is reported at 29.31 MHz. The reason for this relatively low frequency is as we mentioned in Section 3.4.2; due to the nature of VLC-based beacon systems, high-throughput is not a high-priority criterion in VLSI architecture design. Therefore, we have implemented an architecture based on combinational logic for the network of PEs; hence, this causes an increase in delay of PEs-network and a deduction of frequency. Moreover, the synthesis results of consumed LEs/LUTs of transmitter and receiver are strongly affected by the code-length of Polar encoder/decoder. Specifically, We have noticed that the amount of consumed LEs/LUTs almost duplicates when the code-length increase two times. Table 13 introduces some ASIC synthesis results of our VLC transmitter and receiver. Specifically, we have utilized the Synopsys' Design Compiler RTL synthesis tool in which the VDEC's Rohm technology library 180nm is selected. Besides results of power consumption and area are reported, we also evaluate the throughput, energy-per-bit and hardware efficiency of implemented transmitter/receiver based on equations given in this thesis's appendix (9, 10, 11) [49].

Table 11. Logic-resource consumption of the proprosed VLC transmitter compared with related works.

	Manchester-based	4B6B-based	Proposed
Model	Cyclone IV	Cyclone IV	Cyclone IV
Code length	256	256	256
FEC	Polar code	Polar code	Polar code
Code rate	0.308	0.411	0.617
Logic Cells	1825	1855	1896
Memory bits	53	6201	0

Table 11 shows that the proposed VLC transmitter does not use any memory bits in logic synthesis compared with related works. Besides, Table 12 shows a complexity reduction of the proposed receiver compared with related works. Due to not using soft-decoding for any RLL codes, our works could reduce remarkably

Table 12. An estimation of complexity reduction of the proprosed VLC receiver compared with some related works.

Computation	Complexity reduction of proposed receiver compared with		
	Soft-decoding Manchester RLL-based	Soft-decoding 4B6B RLL-based	Soft-decoding 8B10B RLL-based (estimation only)
Power	2	2	2
Square root	1	1	1
Exponentiation	1	1	1
Division	2	5	9
Multiplication	2	80	1280
Addition	2	56	896
Logarithm	1	4	8

Table 13. ASIC synthesis results of our VLC transmitter and receiver.

	Transmitter	Receiver
Technology $[nm]$	180	180
Voltage $[V]$	1.8	1.8
Area $[\mu m^2]$	48761.39	573724.56
Frequency $[MHz]$	25	25
Power $[mW]$	1.3137	3.5022
Throughput $[Mb/s]$	15.38	16.58
Energy-per-bit $[pJ/b]$	85.42	211.2
Hardware Efficiency $[Mb/s/mm^2]$	315.41	28.75
Latency $[clocks]$	160	386

heavy computation efforts such as multiplication, division, logarithm, etc., which had been a big obstacle in hardware implementation of soft-decoding-based VLC receiver.

3.5.3 Bit error rate (BER) and frame error rate (FER) performances

Fig.26 shows the BER performances of our proposed VLC system in which both systematic and non-systematic Polar codes are applied to evaluate the BER per-
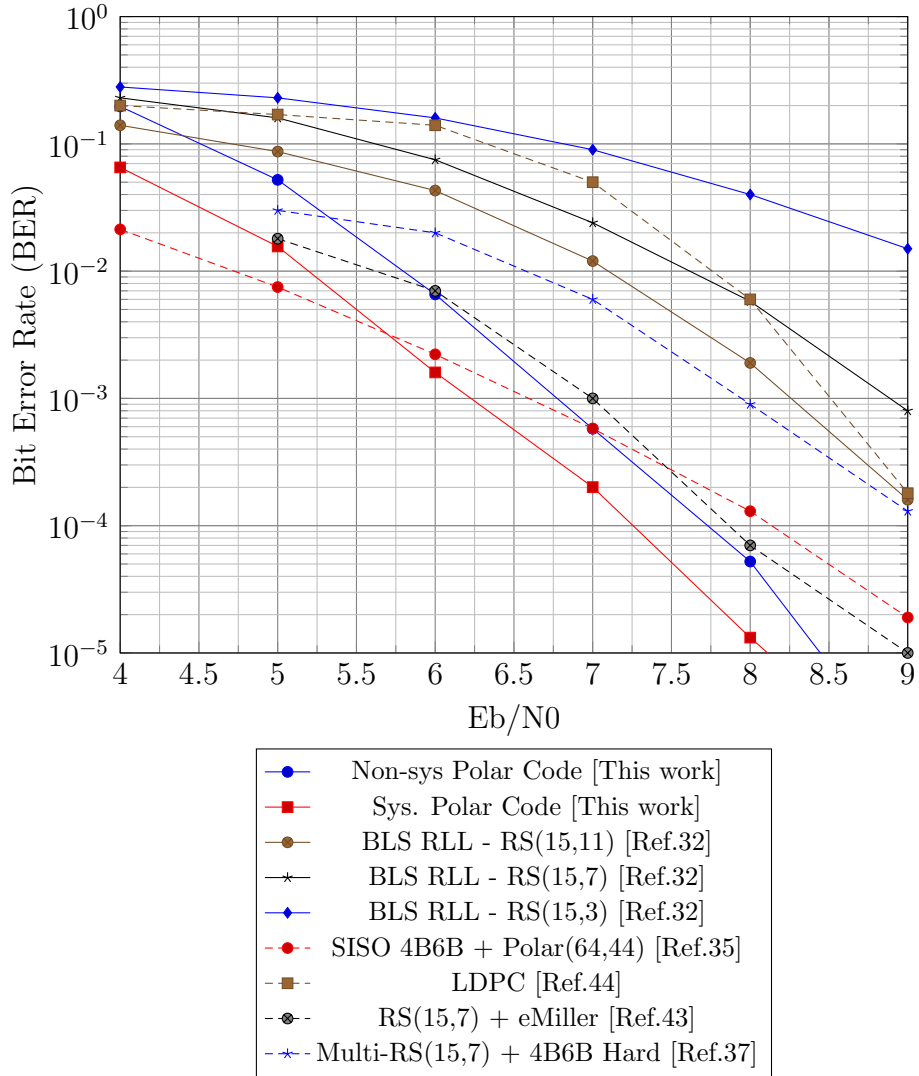
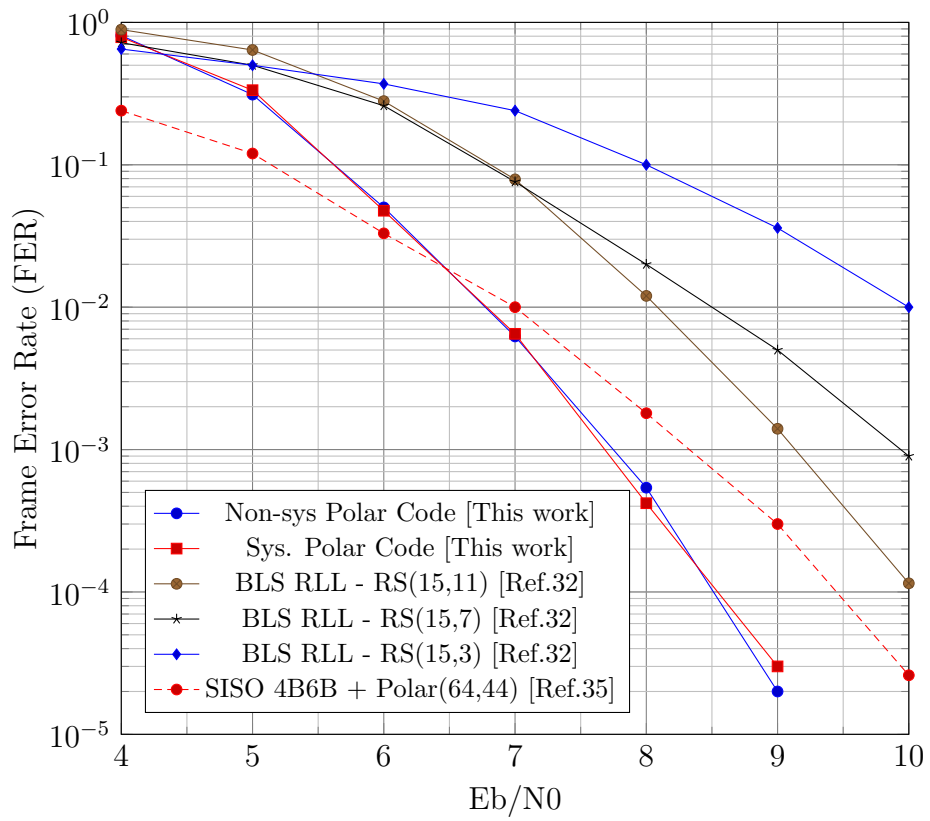Figure 26. BER performances of the proposed VLC system with some comparisons in real VLC-AWGN channel.

Figure 27. FER performances of the proposed VLC system and some related works in real VLC-AWGN channel.

formances. We have selected some typical joint FEC-RLL and non-RLL FEC solutions for comparison. It can be seen that the BER performances of our proposed system outperform current related works. Specifically, Fig.26 shows that at a code-rate = 0.62, our non-RLL Polar-code-based system outperforms RS-code-based ones at code-rates 0.49 (11/15 * 4/6), 0.31 (7/15 * 4/6) and 0.13 (15/3 * 4/6) which are mentioned in [36, 39]. Also, in Fig.26, we also put BER performances of other related works mentioned in [39, 34, 44, 45] into the same graph with our BER performance lines. It can also be noticed that our pre-scrambled non-RLL Polar code-based solutions have preeminent BER performances although their little code-rates compared with the related works. Furthermore, an evaluation of frame error rate (FER) has been presented in Fig.27 in which our non-RLL solutions also surpass related works introduced in [36, 39]. However, although systematic Polar decoder always shows a better BER performance than the non-systematic decoder does; the FER performance of these two decoders are always equal in all cases. This is not a strange discovery because it has been mention in previous systematic Polar decoder work [50].

$$\text{Thoughput [b/s]} = \frac{N \ [\text{b}]}{D_N \ [\text{sec}]} \tag{9}$$

$$\text{Energy-per-bit [J/b]} = \frac{\text{Power [W]}}{\text{Thoughput [b/s]}} \tag{10}$$

$$\text{Hardware Efficiency } [\text{b/s}/m^2] = \frac{\text{Thoughput [b/s]}}{\text{Area } [m^2]} \tag{11}$$

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4 An FPGA-based centralized transmitter for visible light beacon network

4.1 Introduction

Indoor Location-Based Services (ILBS) are getting more attractions from researchers and industry due to their practical applications. Generally, there are many wireless technologies applied in current ILBS such as WiFi, Bluetooth, Ultrasound, radio frequency identification (RFID), Zigbee and so on [51, 52]. Recently, visible light communication (VLC)-based indoor positioning systems (IPS) which possess promising characteristics of high bandwidth, energy-efficient, long lifetime and cost-efficient, are becoming strong candidates in ILBS market [52, 13, 53, 54]. Consequently, VLC-based IPSs now appear in indoor public spaces, factories, logistics, shopping and healthcare facilities [54]. Recently, Japan Electronics and Information Technology Industries Association (JEITA) has standardized the visible light beacon system in which unique identification (ID) messages are transmitted from each VLC-LED bulb for purposes such as identifying objects and locations [55]. At the user's device, photodiode-based or smartphone camera-based receivers decode the received light signals to retrieve the transmitted information [54]. Finally, localization algorithms (e.g., proximity and triangulation) are executed by the firmware of user's portable devices to estimate the location of the receiver.

Fig.28a and Fig.28b shows two typical models of VLC-based IPSs. In beacon network presented at Fig.28a, each VLC-LED anchor is controlled by one control unit which we called dedicated-processor-based model [56, 57, 58]. Whereas, Fig.28b shows a beacon network in which LED array is controlled by one central processor, we called this model as central-processor-based model [54, 59]. In these two beacon network models, VLC transmitter's procedures which including forward error correction (FEC) and run-length limited (RLL) encoding [53], are mainly processed by a firmware program on a low-end embedded processor. Besides, due to multiple LEDs are installed in an indoor space, the *Signal Modulation* block is required to execute multiplexing protocols, such as frequency division multiplexing (FDM) and time division multiplexing (TDM); this block

ensures that signals from different LEDs can be differentiated at the receiver [59]. Furthermore, an optional part of the VLC transmit (TX) package is the wireless programmer which helps configure the firmware on the micro-controller or low-end SoC remotely [56, 57]. At the receiver, signal demultiplexing and positioning algorithms are processed by a firmware program on user's portable device.

4.2   Problem and related works

According to [54], system implementation cost is the priority when considering the commercial availability of a VLC-based IPS design. In the dedicated-processor-based model (Fig.28a), considering this model is applied in a large building with hundreds or thousands of roof VLC-LED bulbs. In this scenario, the implementation cost increases linearly because each control board is dedicated for only one VLC-LED anchor [56, 57, 58]. Moreover, each VLC-LED anchor takes more space to integrate the control board and TX front-end into the same VLC-LED package. Due to these reasons, the dedicated-processor-based model should be further considered to be applied in real commercial systems.

On the other hand, considering the central-processor-based model is applied with hundreds of LED anchors, and long wires are required to route from the central control board to LED bulbs via VLC TX front-ends (Fig.28b). In this scenario, transmitter's essential procedures include encoding of FEC and RLL codes [53] are processed sequentially at the central control board's firmware. Next, encoded messages are modulated and be forwarded to VLC TX front-ends. Although, FEC and RLL encoding are often not heavy computations. However, computation efforts increase when more LED anchors are installed in the beacon network. Hence, the central-processor-based model potentially causes critical delays in processing time of FEC, RLL or modulation routines. Moreover, due to the limited storage capacity of most of the low-end embedded processor, the network scalability could be restricted.

To confirm the statement, we have evaluated the consumed memories and processing delays of sequentially executing VLC transmitters' procedures on Arduino Uno and Raspberry Pi 3 boards which are such two representatives between many low-end, low-cost MCUs and SoCs available on the market. Indeed, Reed-Solomon (RS) and convolutional codes (CC) are defined as FEC solutions in three
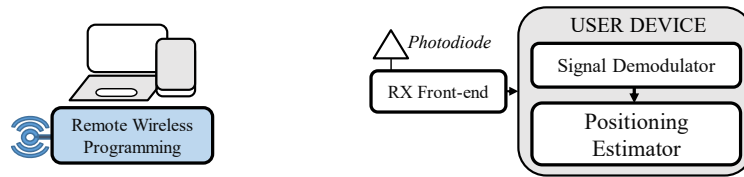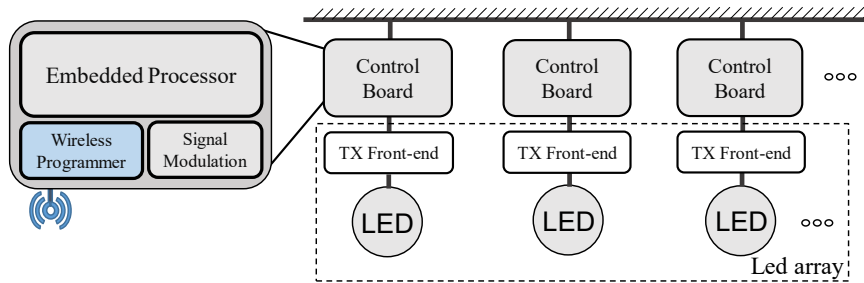
(a) VLC beacon network based on dedicated control boards
(dedicated-processor-based).
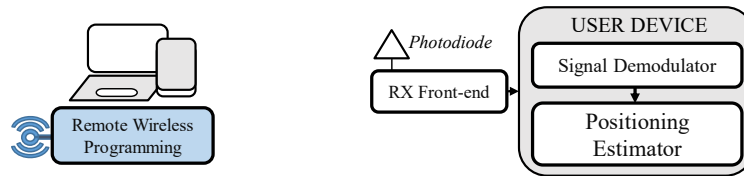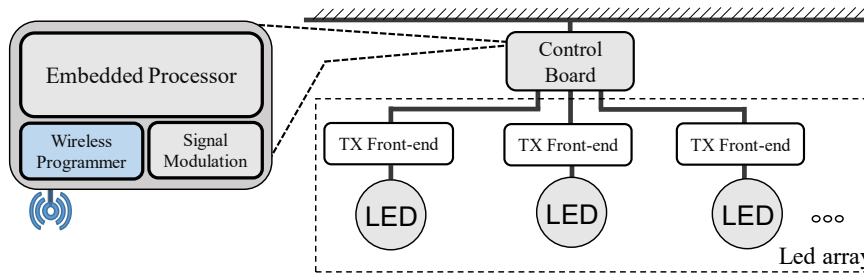
(b) VLC beacon network based on a central control board (central-processor-based).

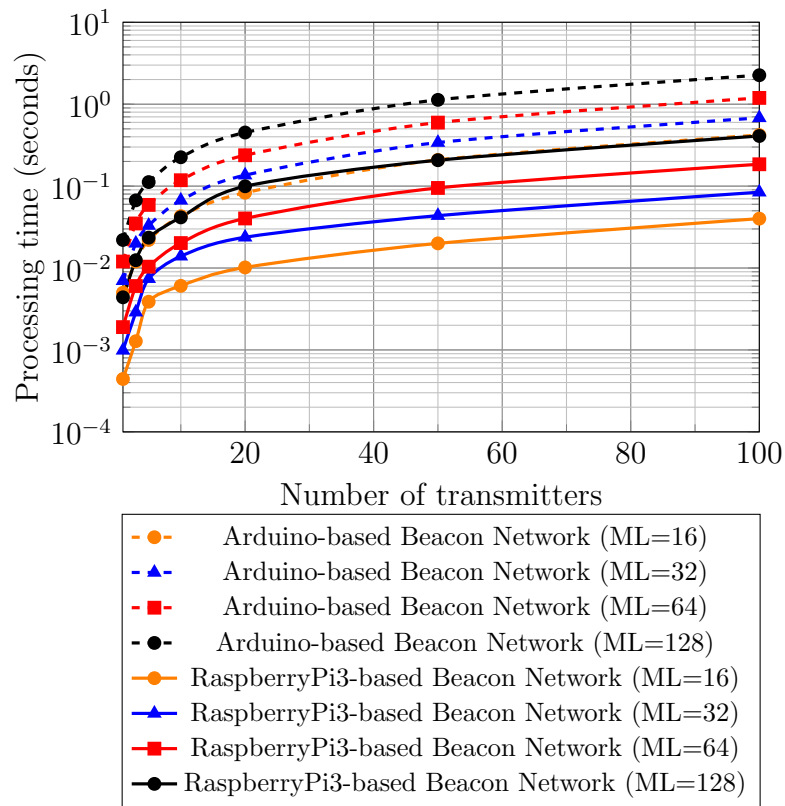Figure 28. Two typical models of VLC-based IPS

Figure 29. Evaluation of processing delay of central-processor-based beacon networks. Arduino Uno and Raspberry Pi 3 boards are selected for evaluations.

Algorithm 1 The algorithm used in the evaluation of central-processor-based beacon network. The transmitter's procedures include Polar encoding and Manchester RLL encoding; or Polar encoding and 4B6B RLL encoding.

Input: message array $mes[0 : K - 1]$, Frozen bit location index array $d[]$

Output: $outMan[0 : 2N - 1]$ (Manchester encode); or $out4b6b[0 : 2N/3 - 1]$ (4B6B encode)

    Initialisation :

    $+ k$: the number of transmitters in beacon network.

    $+ N$: codeword length, $N = 2^n$

    $+ bitIndex = 0; x = 0$

1: **for** $num = 0$ to $k - 1$ **do**
2:    **for** $c = 0$ to $N - 1$ **do**
3:       **if** $d[c]$ is a frozen bit **then**
4:          $polarEn[c] \leftarrow 0$
5:       **else**
6:          $polarEn[c] \leftarrow mes[bitIndex]$
7:          $bitIndex \leftarrow bitIndex + 1$
8:       **end if**
9:    **end for**
10:    **for** $i = 0$ to $n - 1$ **do**
11:       $b \leftarrow 2^{n-i}$
12:       $nb \leftarrow 2^i$
13:       **for** $j = 0$ to $nb - 1$ **do**
14:          $base \leftarrow j * b$
15:          $bdiv2 \leftarrow b/2$
16:          **for** $t = 0$ to $bdiv2 - 1$ **do**
17:             $polarEn[base + t] \leftarrow modulo_2(polarEn[base + t] + polarEn[base + t + bdiv2])$
18:          **end for**
19:       **end for**
20:    **end for**
21: **end for**

1:	**for** $z = 0$ to $2N - 1$ **do**
2:	**if** $polarEn[z/2] = 1$ **then**
3:	$outMan[z] \leftarrow 1; outMan[z + 1] \leftarrow 0$
4:	**else**
5:	$outMan[z] \leftarrow 0; outMan[z + 1] \leftarrow 1$
6:	**end if**
7:	$z = z + 2$
8:	**end for**
9:	**for** $z = 0$ to $2N/3 - 1$ **do**
10:	$out4b6b[z + 5, z + 4, z + 3, z + 2, z + 1, z] = 4B6BLookuptable($ $polarEn[x + 3], polarEn[x + 2], polarEn[x + 1], polarEn[x])$
11:	$z = z + 6 \ ; \ x = x + 4$
12:	**end for**
13:	**return** $outMan[0 : 2N - 1]$; or $out4b6b[0 : 2N/3 - 1]$

operating modes of VLC transmitters [60]. Besides, Manchester and 4B6B codes are also described as primary candidates for RLL codes in low-speed PHY I operating mode [60]. Recently, Polar-code-based FEC solutions and soft-decoding theories of RLL codes have been introduced to increase the performance of VLC systems [61, 62, 63, 64]. In this thesis, two Polar-code-based transmitters are selected to evaluate in two beacon network models. In the first transmitter, Polar encoding concatenated with Manchester RLL encoding is implemented. Whereas, 4B6B is selected as the RLL encoding solution for the second transmitter. Also, On-off keying (OOK) is selected as the modulation scheme because of its simplicity; and dimming support functions are not covered in the evaluation.

The Polar-code-based VLC transmitters' procedures are described in Algorithm 1. We have implemented two VLC transmitters on Arduino Uno and Raspberry Pi 3 boards to evaluate the processing delays in different message lengths (ML) (ML = 16-bit, 32-bit, 64-bit, 128-bit), corresponding to different codeword lengths (CL) of Polar code (CL = 32-bit, 64-bit, 128-bit and 256-bit). The evaluation results are shown in Fig.29. We have found that processing delay increases linearly when the number of transmitters increases in the beacon network; this is a critical point in any ILBS where users always expect real-time

Table 14. Amount and percentages of global variables consumed to execute one transmitter's routines on Arduino Uno.

	Polar + Manchester (Code rate = 1/4)	Polar + 4B6B (Code rate = 1/3)
ML=16, CL=32	452 bytes (22%)	422 bytes (20%)
ML=32, CL=64	644 bytes (31%)	582 bytes (28%)
ML=64, CL=128	1028 bytes (50%)	902 bytes (44%)
ML=128, CL=256	1796 bytes (87%)	1542 bytes (75%)

responses. Besides, Table 14 summarizes the amount of consumed global variables of transmitter's procedures. Due to the limited dynamic memory of 2048 bytes, Arduino Uno consumes 22%, 31%, 50%, 87% of memory resource to storage all global variables (GV) of Manchester-based transmitter's routines; with codeword lengths vary from 32, 64, 128 to 256 respectively. Also, in case 4B6B RLL encoding is applied with Polar encoding, smaller percentages of dynamic memory consumption are reported. However, in case of ML = 128 and CL = 256, the memory consumption rates of 87% and 75% might cause some instabilities when the system is in operation.

Evaluation results of processing time and consumed memory of central-processor-based VLC-LED beacon network (Fig.28b) have shown a critical processing delay when the number of transmitters increases in beacon network. Besides, limited storage capabilities of low-end MCUs create barriers for this model to be applied in reality. On the other hand, due to the high-cost of implementation, the dedicated-processor-based VLC beacon network (Fig.28a) is also not an effective solution for real commercial systems. Therefore, in this thesis, we introduce an FPGA-based centralized transmitter and its aided on-chip system, which can solve problems of processing delay and memory overload; and this solution is expected to support for a more massive VLC beacon network.

Recently some high-speed VLC networks which uses optical fiber and power line communication (PLC) as backbone networks have been introduced [65, 66]. For indoor positioning beacon networks, FPGA-based centralized node speed up the processing time of VLC transmitters. When beacon network is in maintenance, or being installed in a new indoor environment, the proposed work helps

speed up the operation of whole network without long delays. Especially, in high-speed hybrid VLC networks, delay in processing time at each VLC node should be avoid. Although high-speed VLC systems are not covered in this thesis; however, FPGA-based VLC transmitter could be one of promising solutions for speeding up the VLC networks.
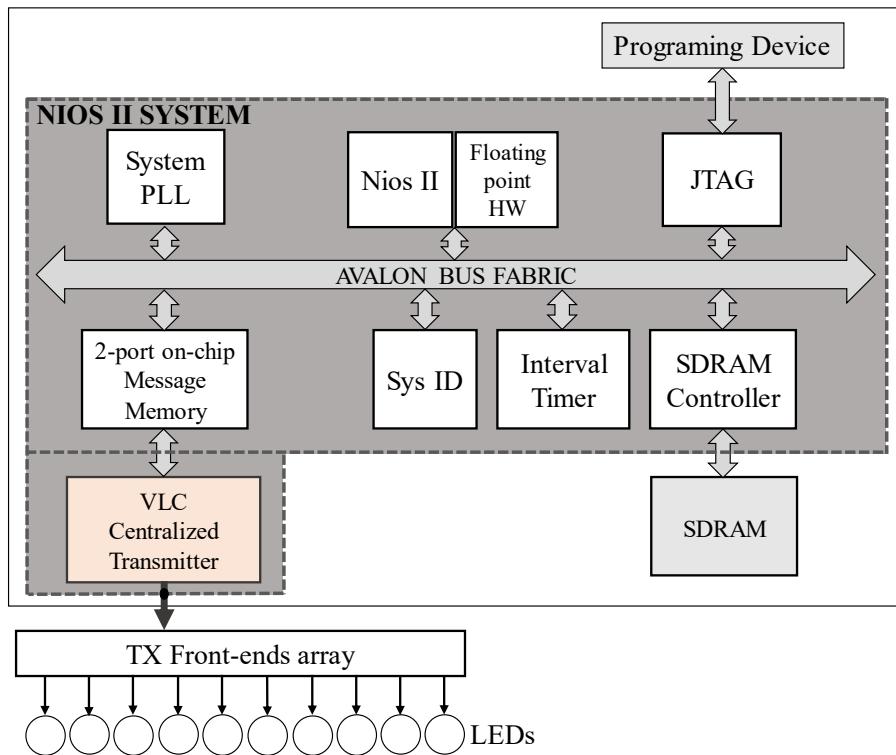
4.3   Proposed system

Figure 30. VLC centralized transmitter and the aided Nios-II-based system.

To solve problems mentioned in Section 4.2, we have proposed a beacon network based on a centralized VLC transmitter and its aided Nios II system on FPGA. Specifically, FPGA-based centralized beacon network enables all messages could be processed at the central FPGA-based transmitter before encoded signals are passed to TX front-ends. Altera DE2-115 board which features Cyclone IV FPGA chip is selected to implement our system. Indeed, due to the
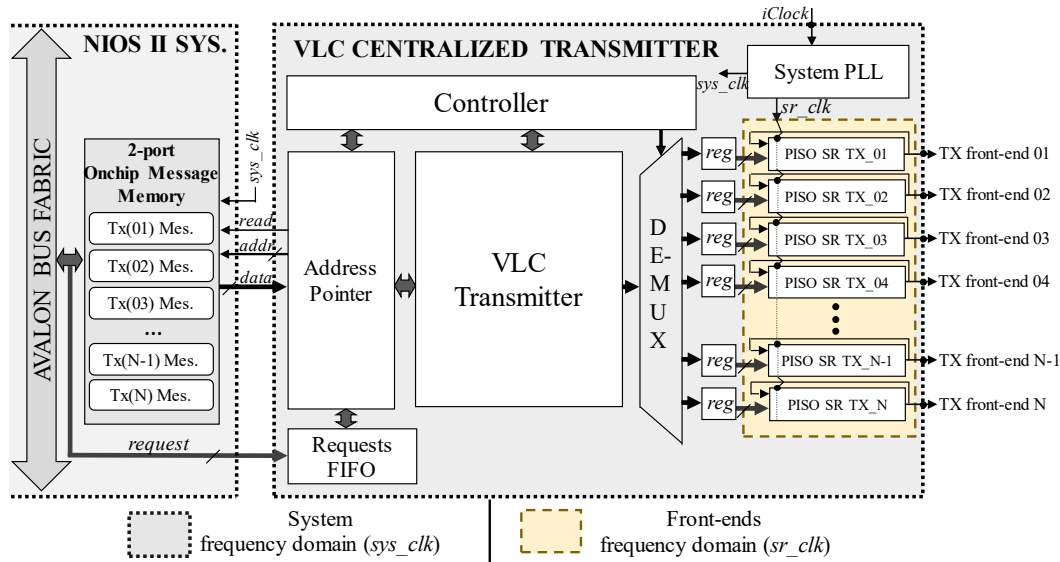
Figure 31. Hardware architecture of the proposed centralized transmitter.

parallel operating capabilities of the FPGA-based logic circuits and many pins are available on common FPGA devices. Our FPGA-based central processing node can cover many VLC front-ends.

4.3.1 A Nios II system for re-configuration

An overview of reconfiguration system is presented briefly in Fig.30. The Nios II system includes some basic blocks of any typical system on programmable chip (SoPC). Specifically, the system includes one Nios II soft-processor with specialized hardware for floating point calculations; a JTAG block which connects to programming, debug and monitoring device. Besides, a 64MB SDRAM off-chip is used to store the firmware; an interval timer helps measure the processing time of the program. Moreover, 2-port on-chip memory is proposed to storage all uncoded messages of all front-ends in beacon network. In our system, 128-bit is the maximum size of each message, while 100 is the number of front-ends selected for evaluation. Therefore, the 2-port message memory with 1600 bytes can be extended to serve a larger beacon network because of plentiful availability of FPGA's on-chip memory bits. In addition, the system is configured to operate

at a frequency of 50 MHz (*sys_clk*) which is created from internal phase-locked loop (*System PLL*).

4.3.2 VLC centralized transmitter

Fig.31 describes the hardware architecture that we have implemented for the centralized transmitter. An explanation of this architecture can be divided into five parts.

Clock domains There are two clock domains in the design: system clock (*sys_clk* = 50 MHz), and clock for shift registers (*sr_clk* = 100 Khz). These two clocks are created from the *System PLL* with the reference clock (*iClock* = 50 MHz). In addition, the VLC TX front-ends transmit information at the same frequency with shift registers' frequency (*sr_clk*), and this frequency could be adjusted following requirements of the expected VLC system.

Requests FIFO and Address Pointer In general cases, the VLC-based IPS initially configures new ID messages for all LED bulbs when IPS is first settled in some indoor spaces. However, there are some scenarios that messages are determined to send to some appointed LED bulbs. In these scenarios, there is no need to update messages for all LED anchors. Therefore, our centralized transmitter stores all write requests sent to 2-port message memory. Each request is a combination of signals: write request, address, and data to write. In our design, each request is a 136-bit signal which includes 128-bit of the message. A (first-in-first-out) FIFO buffer is used to storage requests. The *Address Pointer* checks the busy status of the *VLC Transmitter*; then it reads one request stored in FIFO and execute the request. The requests are executed by issuing read request (*read*) and address signal (*addr*) to the second interface of the 2-port on-chip message memory (Fig.31). Next, when *Address Pointer* achieves message from the memory interface (*data*), the acquired message is forwarded to VLC transmitter for FEC and RLL encoding procedures.

VLC Transmitter In Section 4.2, we have introduced two VLC transmitters that we have implemented for evaluation. Particularly, the first transmitter

includes procedures of Polar and Manchester RLL encoding; while the second transmitter procedures are the concatenation of Polar encoding with 4B6B RLL encoding. These two transmitters are recently mentioned in [61, 62, 63, 64]. In these two transmitters, the Polar encoders are implemented with architecture inherited from our previous work [67]. As mentioned earlier, dimming control function is not implemented in these two transmitters. The reason is, although puncturing and compensation symbols (CSs) are purely simple routines; however, these procedures require many storage bits on variable memory, which has been demonstrated about its limitation in Section 4.2. Hence, dimming control block is neglected in our hardware implementation for a fair comparison with the Arduino-based model.

De-multiplexer and registers   After the message is processed by *VLC transmitter* block, it is expected to be distributed to appointed front-end. Therefore, a de-multiplexer (*DE-MUX*) determines the front-end registers that the message should be passed, and the (*DE-MUX*) is controlled by a memory-read address that *Address Pointer* has issued. Also, we have implemented loop parallel-input serial-output shift-registers (*PISO SRs*) which can repeat the encoded messages while there are no new messages come to front-ends. *PISO SRs* are operated in front-end frequency domain (*sr_clk*). Besides, buffering registers (*reg*) are inserted between *DE-MUX* and *PISO SRs* to buffer the message.

Controller   The *Controller* block handles the operation of the VLC centralized transmitter. Precisely, it controls the start and finish of the *VLC Transmitter*; acquires the memory-read address from the *Address Pointer* and gives control signals to *DE-MUX*.

4.4   Experimental results

Synthesizable *Verilog HDL* language describes the proposed architecture of VLC centralized transmitter. *ModelSim* is used as the verification tool. The Nios II system is created with the help of *Platform Designer* tool. *Nios II Software for Eclipse* is used for firmware programming and debugging. Our system is synthesized by *Intel's Quartus II*. Table 15 summarizes the synthesis report of Nios II

system on Cyclone IV FPGA device. It can be noticed that the Nios II system only consumes 1% of memory bits of Cyclone IV FPGA; this means that on-chip message memory can be further extended to serve for a larger number of TX front-ends in a larger beacon network. Besides, Table 16 shows the synthesis report of the Manchester-based and 4B6B-based VLC centralized transmitters. In particular, due to a better code rate, the transmitter based on Polar and 4B6B RLL encoding consume fewer logic elements (LE), look-up tables (LUT) and registers than the Manchester-based transmitter does. However, due to the storage of 4B6B mapping tables, amount of consumed memory bits of the 4B6B-based transmitter is larger than the Manchester-based one. Besides, our FPGA-based centralized transmitters occupy 102 pins in the total of 529 pins of Cyclone IV FPGA (19%). Indeed, we have just implemented an architecture which only supports 100 front-ends for evaluation; however, the availability of unused pins enables more front-ends can be supported. Additionally, both transmitters can achieve maximum throughputs higher than 600 Mbps; therefore, our FPGA-based centralized transmitter could be potentially applied in high-speed VLC systems. Furthermore, Table 17 shows resource summary of the centralized transmitters and their components. It can be seen that the de-multiplexer, buffering registers and PISO shift registers occupy most of the logic cells in both centralized transmitters. However, instead of using logic cells to implement shift registers, we can utilize embedded memory bits which are still abundant in Cyclone IV FPGA to reduce the total logic cells of the system.

Table 15. FPGA synthesis report of the Nios II system.

	Nios II System
Device	Cyclone IV FPGA
Model	1200 mV, 0^oC
Fmax	80.25 MHz
LE/LUT	12166/114480 (11%)
Registers	7479
Memory bits	54713/3981312 (1%)
Embedded Multiplier	15/532 (3%)
Total PLLs	1/4 (25%)

65

Table 16. FPGA synthesis report of the FPGA-based centralized transmitters.

FEC, RLL	Polar, Manchester	Polar, 4B6B
Device	Cyclone IV FPGA	Cyclone IV FPGA
Number of front-ends	100	100
Model	1200 mV, 0^oC	1200 mV, 0^oC
Fmax	76.13 MHz	69.69 MHz
Code length	256	256
Code rate	1/4	1/3
LE/LUT	91518/114480 (80%)	78823/114480 (69%)
Registers	91004	78274
Memory bits	277/3981312 (<1%)	6425/3981312 (<1%)
Total pins	102/529 (19%)	102/529 (19%)
Total PLLs	1/4 (25%)	1/4 (25%)
Latency (sys_clk domain)	14 clock cycles	14 clock cycles
Maximum throughput	694.8 Mbps	630.8 Mbps

Fig.32 shows the processing delay evaluation of our FPGA-based centralized beacon network. Besides, Table 18 summarizes the processing delay improvement of FPGA-based beacon network. Specifically, improvements of maximum 4610 times and 966 times are reported for processing delay of the FPGA-based solution compared evaluation results on Arduino Uno and Raspberry Pi 3, respectively (Fig.29 and Fig.32).
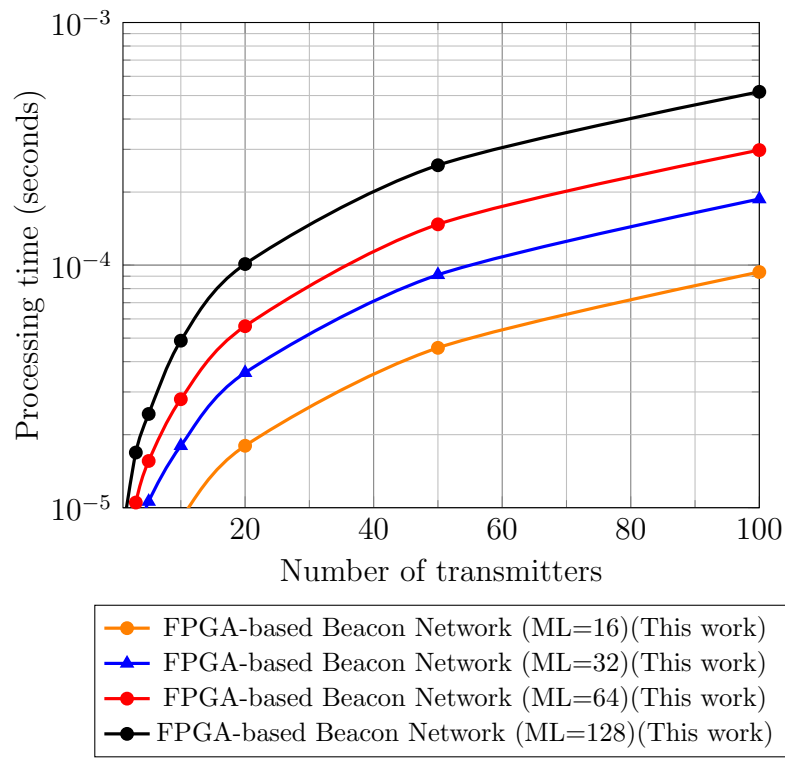
Figure 32. Processing time of proposed FPGA-based centralized beacon network.

Table 17. Resource summary of component blocks of the FPGA-based centralized transmitters; Manchester-based transmitter (left index) and 4B6B-based transmitter (right index).

Instance	Logic Cells	Registers	Mem.‡	LUT/Reg.†
Request FIFO	55|54	40|40	224|224	31|30
Address Pointer	11|11	11|11	0|0	11|11
Controller	17|17	15|15	0|0	15|15
VLC Transmitter	1388|1418	1338|1408	53|6201	908|714
De-multiplexer				
Front-end regs				
PISO Shift reg.	90062|77326	89600|76800	0|0	54759|41849
Total	91518|78823	91004|78274	277|6425	55708|42615

†LUT/Registers Logic Cells

‡Embedded memory bits

Table 18. Processing delay enhancement (at ML = 128).

No. of Transmitter	FPGA/Arduino Gain	FPGA/Raspberry Gain
1	2729	548
3	3969	738
5	4609	966
10	4610	850
20	4465	985
50	4375	802
100	4359	789

5 Conclusion and Future Works

5.1 Conclusions

In this thesis, we have introduced a multi-mode error-correction solution which is based on split-concatenation of TILD-LDPC with low-constraint soft decision convolutional code. The proposed solution has reduced-complexity, scalability, free burst-error, configurable error-correction performances, and four transmit-power-reduction options. Thus, the proposed approach could be adaptive for different transmission scenarios in WSNs applications. Moreover, good BER performance of concatenating reduced-complexity TILD-LDPC with low-complexity convolutional code (low-constraint) give a potentiality for designing low-complexity concatenated FEC encoders/ decoders.

Also, in this thesis, we have introduced a non-RLL flicker mitigation solution which consists of a pre-scrambler based on a simple generating polynomial combined with a Polar encoder. The proposed method has a centralized bit probability distribution with the distribution range is determined in (43.75% - 63.75%). Moreover, the maximum run-length is reduced up to 4.08 times when pre-scrambler is applied with an SPE; and up to 1.9 times when it is applied with an NSPE. Therefore, DC-balance can be maintained even with the short data frames used in VLC-based beacon systems. Moreover, the non-RLL nature of the proposal reduces the complexity of both VLC transmitter/receiver with significant improvements on information code-rate. Besides, we have introduced a soft-decision filter which can help the soft-decoding of polar code is implemented in real VLC receiver prototypes to enhance the error-correction performance. As a result, BER and FER performances of the proposed system have outperformed current approaches while remaining a good code-rate (0.62). Also, we have introduced a couple of hardware architectures for the proposed non-RLL VLC transmitter and receiver which their FPGA and ASIC synthesis results are given in details.

Finally, we have introduced an FPGA-based centralized beacon network. Our proposal includes a hardware architecture for the centralized VLC transmitter which can process messages for all TX front-ends in beacon network and a Nios

II-based system to control the messages and operation of the beacon network. Experimental results have shown that our system can improve the processing delay of the central-processor-based beacon networks remarkably. Besides, our FPGA-based model can be extended to serve for a large beacon network which includes many VLC-LED bulbs due to the abundant availability of embedded memory bits and FPGA's pins. Moreover, compared with beacon networks which based on dedicated embedded processors, our FPGA-based centralized system is expected to reduce the implementation cost of the commercial VLC-based positioning systems.

5.2   Future works

There are some future works that we plan to conduct as the next steps for proposals mentioned in Chapter 2, 3, 4. Specifically:

- Firstly, as presented in Chapter 2, our multi-mode FEC solution based on split-concatenation of LDPC and Convolutional codes are currently evaluated under simulation tools such as Matlab, eSimu, WSim. Therefore, only results of transmit-power reduction are introduced in this thesis. Next steps for this proposal should be evaluated on software-defined radio (SDR) devices. Besides, hardware implementation could be conducted by Verilog HDL, and synthesized by ASIC tools to assess the hardware-complexity and power consumption of this proposal.

- Secondly, in Chapter 3, we have introduced the proposed VLSI architectures for the non-RLL Polar code-based VLC transmitter and receiver. Although FPGA and ASIC synthesis results of the proposed transmitter and receiver have been presented; however, we have currently evaluated a fixed size of beacon frames, which is 158-bit. In fact, there are some scenarios that smaller frame sizes are defined for VLC transmitters. Therefore, we plan to build more flexible transmitters/receivers in which smaller data-frame sizes could be supported in operation.

- Finally, we have proposed an FPGA-based centralized beacon network in Chapter 4. Besides, we have shown the motivation of innovating current

embedded-processor-based network by bringing out evaluations of processing delays. Indeed, due to the low-latency and high-throughput features of the FPGA-based centralized transmitter, we found that this transmitter might also be applied in high-speed VLC systems; in which demands of transferring data at high-speed are more critical than in indoor localization applications. Consequently, our future works will be evaluations of the FPGA-based transmitter on high-speed VLC applications.

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