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Study on Neuromorphic Systems using Thin-Film Devices

Mutsumi Kimura

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Thesis Committee:

Professor Yasuhiko Nakashima	(Supervisor)
Professor Kazushi Ikeda	(Co-supervisor)
Professor Yukiharu Uraoka	(Graduate School of Materials Science)
Associate Professor Takashi Nakada	(Co-supervisor)
Assistant Professor Tran Thi Hong	(Co-supervisor)
Assistant Professor Renyuan Zhang	(Co-supervisor)

Study on Neuromorphic Systems using Thin-Film Devices *

Mutsumi Kimura

Abstract

Artificial intelligences have been used for various applications and are promising in future societies, but because the conventional neural networks are software on hardware, the size is bulky, and the power is huge. Neuromorphic systems are biomimetic systems from hardware level and have the same advantages as living brains, especially, compact size, low power, and robust operation. On the other hand, thin-film semiconductor electronic devices can be fabricated on large areas, and three-dimensional layered structure can be acquired.

Neuromorphic systems using thin-film devices will be studied in this doctoral dissertation. First, a neuromorphic system will be investigated, where a neuron element is simplified to three simple circuits and a synapse element is simplified to one variable resistor or capacitor, and a tug-of-war method and modified Hebbian learning will be proposed, whose advantage is that the synaptic connection strength is automatically controlled using the local electrical conditions. Next, low-temperature poly-Si (LTPS) device, amorphous In-Ga-Zn-O (α-IGZO) device, and amorphous Ga-Sn-O (α-GTO) device will be examined, where it is confirmed that the electrical conductance gradually decreases when electric current flows, which is available as a synaptic connection strength. Finally, Hopfield neural networks using crosspoint-type devices and cellular neural networks using separated architecture, surfaced architecture, layered architecture, and planar-type devices will be investigate, and the correct operations of simple logic learning and letter reproduction is confirmed. It will be believed that these results will be theoretical bases to realize ultra-large scale integration for neuromorphic systems. In this doctoral dissertation, the correct operations will be confirmed using Hopfield neural

networks and cellular neural networks, which are historical neural networks and have contrastive properties. According to the history of neural networks, individual parts can be implemented to new parts and the peculiar functions of the new parts can be obtained. Therefore, it is expected that this study can be adapted to the advanced technologies of neural networks.

Neuromorphic systems using thin-film devices have great potentials that the size can be compact, the power can be low, and the operation can be robust. Energy crisis can be avoided, and artificial intelligence on everything (AIoE) may be realized. Although integration of an astronomical number of processing elements with three-dimensional layered structure will not be achieved, the research results will suggest that it is possible in the future.

Keywords:
neuromorphic system, thin-film device, artificial intelligence, neural network, neuron element, synapse element, variable resistor, variable capacitor, tug-of-war method, modified Hebbian learning, low-temperature poly-Si (LTPS) device, amorphous In-Ga-Zn-O (α-IGZO) device, amorphous Ga-Sn-O (α-GTO) device, Hopfield neural network, cellular neural network, separated architecture, surfaced architecture, layered architecture, logic learning, letter reproduction

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Publications

Journal Papers (Peer reviewed)

1. Mutsumi Kimura, Yuki Koga, Hiroki Nakanishi, Tokiyoshi Matsuda, Tomoya Kameda, and Yasuhiko Nakashima, "In-Ga-Zn-O Thin-Film Devices as Synapse Elements in a Neural Network", IEEE J. Electron Devices Society, vol. 6, pp. 100-105, Dec. 2017.
2. Mutsumi Kimura, Ryohei Morita, Sumio Sugisaki, Tokiyoshi Matsuda, Tomoya Kameda, and Yasuhiko Nakashima, "Cellular Neural Network formed by Simplified Processing Elements composed of Thin-Film Transistors", Neurocomputing, vol. 248, pp. 112-119, Mar. and July 2017.
3. Mutsumi Kimura, Hiroki Nakanishi, Nao Nakamura, Tomoharu Yokoyama, Tokiyoshi Matsuda, Tomoya Kameda, and Yasuhiko Nakashima, "Simplification of Processing Elements in Cellular Neural Network", J. Electrical Engineering and Electronic Technology, vol. 6, issue 1, Apr. 2017.

Conference (Reviewed)

1. [Invited] Mutsumi Kimura, to be determined, ICDT 2018, Apr. 2018, to be presented.
2. [Invited] Mutsumi Kimura, Tomoya Kameda, and Yasuhiko Nakashima, "Brain-like Integrated System using Thin-Film Devices", NOLTA 2017, pp. 95-98, Dec. 2017.
3. [Keynote] Mutsumi Kimura and Yasuhiko Nakashima, "Neuromorphic Hardware using Simplified Elements and Thin-Film Semiconductor Devices", CANDAR '17, pp. 56, Nov. 2017.
4. [Keynote] Mutsumi Kimura, Tokiyoshi Matsuda, and Yasuhiko Nakashima, "Brain-type Integrated System using Thin-Film Devices", IC-TECS 2016, Dec. 2016.
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1 Introduction

Artificial intelligences have been used for various applications and are also promising in future societies. Neural networks are representative technologies, and the advantages are self-organization, self-learning, parallel distributed computing, fault tolerance, etc. However, because the conventional ones are software on hardware, the size is bulky, and the power is huge. Moreover, some of the advantages are not acquired, because they are executed on Neumann-type computers. Neuromorphic systems are biomimetic systems from hardware level and have the same advantages as living brains, especially, compact size, low power, and robust operation. Although some neuromorphic systems are well known, because they are hybrid systems, the abovementioned advantages are only partially obtained. On the other hand, thin-film semiconductor electronic devices are widely used, and the advantages are that they can be fabricated on large areas and three-dimensional layered structure can be acquired, whereas the unavoidable disadvantages are low performance and low yield. Neuromorphic systems are interesting applications for thin-film devices, because the advantages are available and the disadvantages are acceptable.

In this doctoral dissertation, we study neuromorphic systems using thin-film devices. First, we investigate a neuromorphic system, where we simplify processing elements and propose neural networks and a novel learning method, modified Hebbian learning. By using such processing elements and learning method in neuromorphic systems, it is expected that the size can be further compact, power can be low, and the operation can be robust. Next, we examine some kinds of thin-film devices, whose characteristics are available to the learning rule. By using such thin-film devices in neuromorphic systems, it is expected that the size can be further compact. Finally, we investigate Hopfield neural networks and cellular neural networks and confirm the correct operations. Although we have not yet succeeded in integration of an astronomical number of processing elements with three-dimensional layered structure, the research results suggest that it is possible in the future.

1.1 Artificial Intelligence

Artificial intelligences are thinking machines that mimic biological brains [1-5]. They have been already used in present world for various applications, such as, letter recognition [6], image recognition [7,8], medical diagnosis [9], face recognition [10], information guide [11], language translation [12], summary extraction [13], caption generation [14], expert system [15,16], autonomous driving [17], robot brain [18], etc., and are also promising as key technologies in future societies.

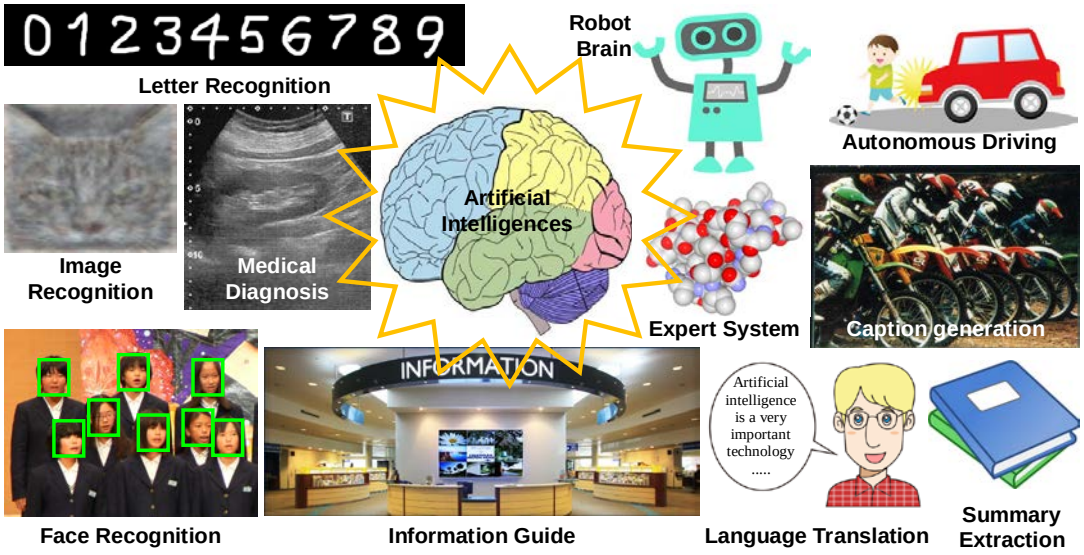
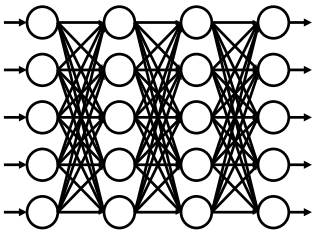
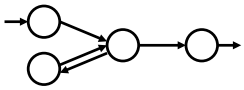
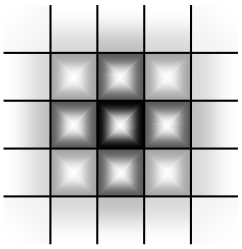


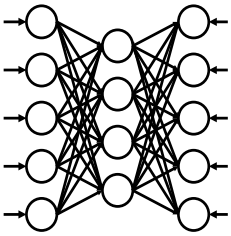
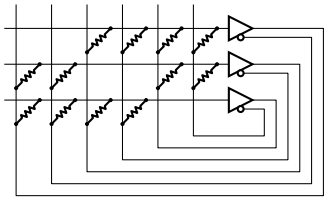
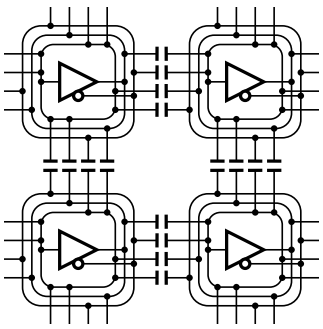
Fig. 1-1. Artificial intelligences for various applications.

Neural networks are representative technologies that realize artificial intelligences [19-23]. The outstanding advantages of the neural networks are self-organization, self-learning, parallel distributed computing, fault tolerance, etc. These advantages are obtained by connecting a large number of processing elements, namely, a large number of neuron elements and a much larger number of synapse elements, to imitate human brains, where more than 10^{11} neuron elements and 10^{15} synapse elements exist.

However, because the conventional neural networks are complicated software executed on high-spec hardware, the machine size is very bulky, and the power

consumption is unbelievably huge for not only hardware operation itself but also air conditioners to cool it, and so on. Moreover, some of the aforementioned advantages, such as parallel distributed computing and fault tolerance, are not acquired, because they are executed on conventional Neumann-type computers [24], which sequentially handle processes and stop only if a physical device is broken. Furthermore, the computing architecture is not optimized for the neural networks, and therefore extra circuits occupy a large area and consume large power.

Supervised Learning		
		
Feedforward Neural Network Perceptron	Recurrent Neural Network Feedback Neural Network	Convolutional Neural Networks
General Purpose	natural Language Processing	Letter Recognition Image Recognition

Unsupervised Learning		
		
Auto-encoder Deep Learning	Hopfield Neural Network	Cellular Neural Network
Almighty		

The detailed explanation is written in a prior article [5]. The Hopfield and cellular neural networks are explained later in this doctoral dissertation.

Fig. 1-2. Neural networks with various architectures.

1.2 Neuromorphic System

Neuromorphic systems are hardware buildups that realize neural networks, which are real hardware instead of virtual software [25-31]. It should be noted that technical approaches to enhance computation performance of multiply–accumulate operation using graphics processing unit (GPU) chips [32] and field-programmable gate array (FPGA) chips [33] based on the conventional Neumann-type computers are different from neuromorphic systems. The neuromorphic systems are biomimetic systems from hardware level, and therefore they have the same advantages as living brains. First, the machine size can be very compact. It is known that a machine size of a conventional neural network, Watson [34], which is one of the most famous cognitive computing system as a winner in a television quiz show, is the same as that of ten refrigerators, whereas a size of a human brain is only 1.4 ℓ. Next, the power consumption can be very low. It is known that a power consumption of Watson is roughly 100 kW, whereas a power consumption of a human brain is only 20 W. Finally, the robustness can be improved. It is known that a human brain loses 100,000 neurons each day, but it can keep the needed functions. It is not certain that neuromorphic systems can catch up the abovementioned advantages of human brains, but it can be expected that neuromorphic systems can have more excellent performances than the conventional neural networks from the

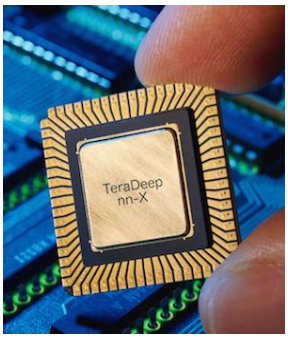
Conventional Neural Network				Neuromorphic System
Complicated Software on High-spec Hardware		Architecture		Biomimicry from Hardware Level
Sequentially and Synchronized	×	Operation	○	Parallel and Distributed
High	○	Generality	×	Low
Bulky	×	Size	○	Compact
High	×	Power consumption	○	Low
Low	×	Robustness	○	High
Limited Targets	×	Integration	○	AIoE (AI on Everything) Autonomous AI

Fig. 1-3. Neuromorphic system compared with conventional neural networks.

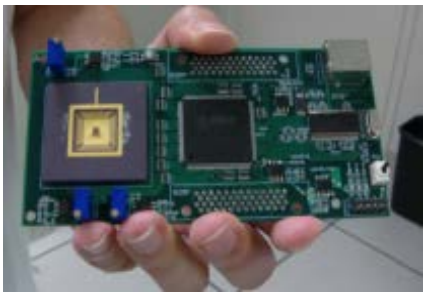
viewpoints of the aforementioned advantages. We named them "brain-type integrated system", because we expect that they can be integrated on everything in future life [35-41].

Some neuromorphic systems are well known, such as, Zeroth Processor from Qualcomm [42], nn-X from TeraDeep [43], SyNAPSE from DARPA [44], True North from IBM [45], brain-type integrated system from Kyushu Institute of

Zeroth Processor, Qualcomm

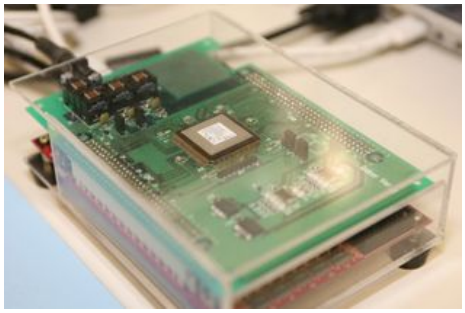


nn-X, TeraDeep



SyNAPSE , DARPA

True North, IBM



Brain-type Integrated System, Kyushu Institute of Technology

Fig. 1-4. LSI chips for neuromorphic systems.

Technology [46], etc. These large scale integration（LSI) chips are hybrid systems of Neumann-type computers and neuromorphic systems. For example, only a few neuron elements are actually prepared and a large number of neuron elements are virtually emulated using time-sharing algorithms, discrete values are actually saved in digital memory and continuous values are virtually approximated like analogue memories, etc. Therefore, the abovementioned advantages are only partially obtained. Moreover, because conventional technologies of the semiconductor fabrication are used, only two-dimensional structure can be acquired in principle, whereas three-dimensional structure is utilized in living brains, where a large number of processing elements are prepared and it is easy to connect them each other, which is an essence of neuromorphic systems.

1.3 Thin-Film Device

Thin-film semiconductor electronic devices are widely used for flat-panel displays (FPDs) [47], solar cells [48], etc. The outstanding features of the thin-film devices are low-temperature fabrication and high material efficiency [49]. As a result, the notable advantages are that they can be fabricated on large areas and three-dimensional layered structure can be acquired. Actually, we developed active-matrix organic light-emitting diode displays (AM-OLEDs), which have a layered structure of thin-film transistors (TFTs) and OLEDs [50], and complementally metal-oxide semiconductor (CMOS) device using TFTs, which also

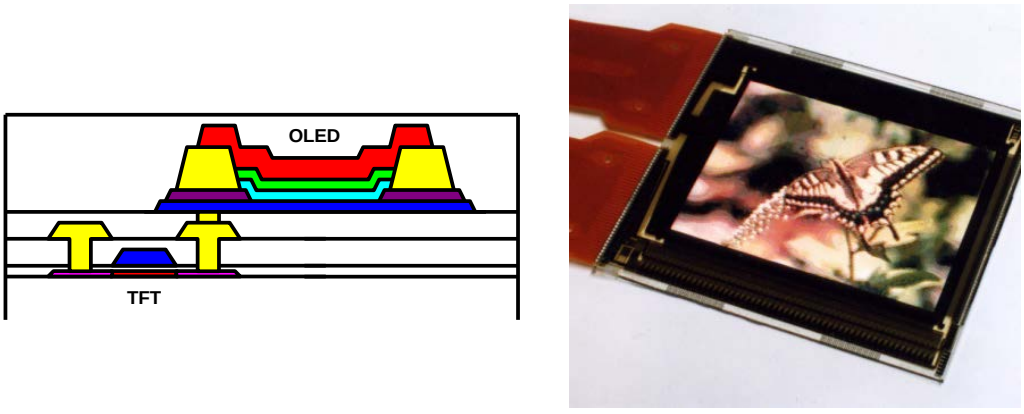


Fig. 1-5. AM-OLED with a layered structure of TFTs and OLEDs.

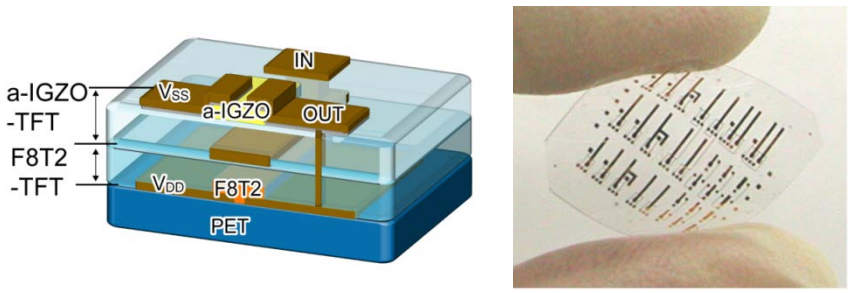


Fig. 1-6. CMOS device with a layered structure of AOS and organic TFTs.

have a layered structure of amorphous metal-oxide semiconductor (AOS) and organic TFTs [51]. On the other hand, the unavoidable disadvantages of the thin-film devices are low performance and low yield owing to the low-temperature fabrication.

Neuromorphic systems are interesting applications for thin-film devices. Because neuromorphic systems require an astronomical number of processing elements, the advantages of the thin-film devices, namely, they can be fabricated on large areas and three-dimensional layered structure can be acquired, are available. On the other hand, the disadvantages, namely, low performance and low yield, are acceptable, because the operation speed of neuromorphic systems do not have to be so fast and they are robust against the damage of processing elements.

Some thin-film devices are already used in neuromorphic systems [52]. However, the advantages of the thin-film devices are not employed well, namely, they are fabricated at high temperature and not uniform because they are poly-crystalline materials and have just a two-dimensional structure.

1.4 This Study

In this doctoral dissertation, we study neuromorphic systems using thin-film devices [35-41]. First, we investigate a neuromorphic system, where we simplify processing elements, such as, neuron elements and synapse elements, and neural network, to aim at integration of an astronomical number of processing elements. We propose a novel learning method, modified Hebbian learning, which does not need additional circuits to control synaptic connection strengths. By using such

processing elements and learning method in neuromorphic systems, it is expected that the machine size can be further compact, power consumption can be low, and the operation can be robust. Next, we examine some kinds of thin-film devices, such as, a low-temperature poly-Si device, amorphous In-Ga-Zn-O (IGZO) device, amorphous Ga-Sn-O (GTO) device, and SiN_x device, whose characteristics are available to the modified Hebbian learning. We can potentially acquire three-dimensional layered structure. By using such thin-film devices in neuromorphic systems, it is expected that the machine size can be further compact. Moreover, because amorphous IGZO and GTO devices can have extremely low leakage current, it is also expected that the power consumption can be further low. Finally, we investigate Hopfield neural networks and cellular neural networks by combining the aforementioned study and confirm the correct operations. Although it is pity that we have not yet succeeded in integration of an astronomical number of processing elements with three-dimensional layered structure, the research results suggest that it is possible in the future.

1.5 Contributions

Neuromorphic systems using thin-film devices have great potentials that the size can be compact, the power can be low, and the operation can be robust [53-55]. First, energy crisis can be avoided, while artificial intelligences will consumes 60 % of worldwide electricity in 2050 if effective countermeasure is not done. Next, artificial intelligence on everything (AIoE) may be realized, which is an extended version of internet of things (IoT). AIoE makes everything intelligent, and telecommunication is conducted only if necessary, which avoid information explosion. Finally, neuromorphic systems might be equipped in robot brains with common artificial intelligences as hybrid systems. The detailed explanation will be given in the last part of this doctoral dissertation. Although we have not yet succeeded in integration of an astronomical number of processing elements with three-dimensional layered structure, the research results suggest that it is possible in the future.

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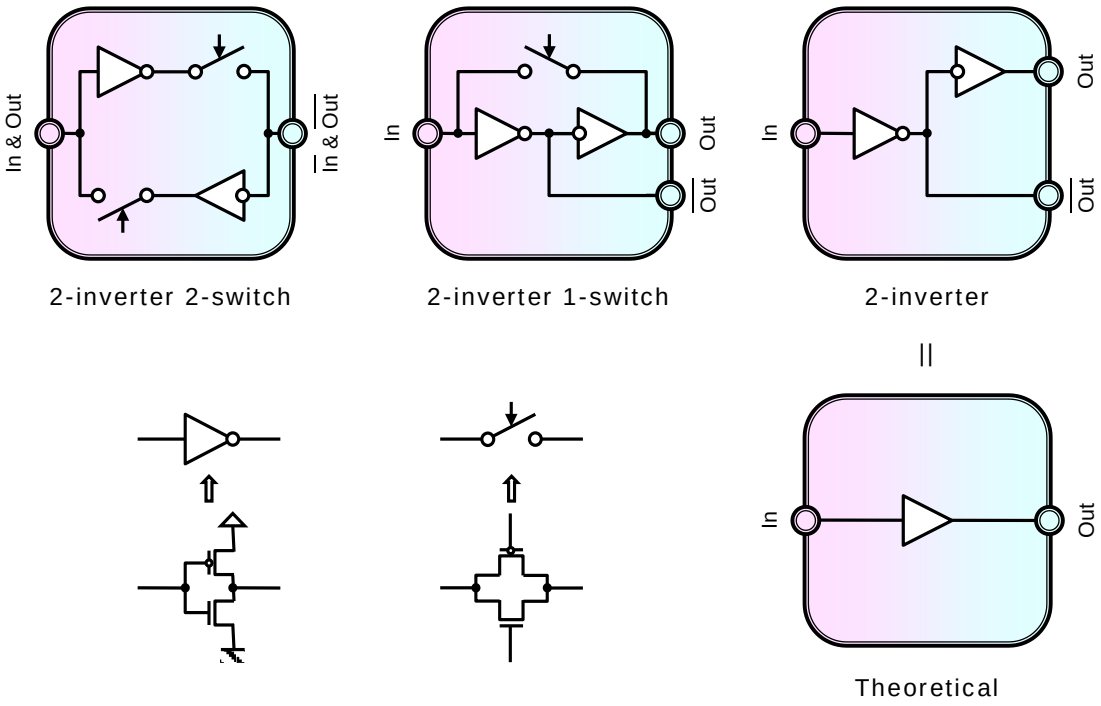
2 Neuromorphic System

Neuromorphic Systems require simplification of processing elements and neural networks, which is indispensable to aim at integration of an astronomical number of processing elements in neural networks, and some corresponding learning rule must be introduced. We have succeeded in simplification of processing elements, such as, neuron elements and synapse elements. First, we reduce a neuron element to "two-inverter two-switch circuit", "two-inverter one-switch circuit", or "two-inverter circuit", where the latter has the same functions as a theoretical model, namely, the simplest one. Next, we reduce a synapse element only to "one variable resistor" or "one variable capacitor". Moreover, we investigate network architectures and revise Hopfield neural networks and cellular neural networks, which are remarkably suitable for integration of electron devices. Because they are historical neural networks and have contrastive properties, once it is confirmed that they can operate correctly, it is also expected that all kinds of neural networks can operate correctly. Additionally, we investigate synaptic connections and propose a "tug-of-war method". Furthermore, the leaning rule is also modified to "modified Hebbian learning". The advantage is that the synaptic connection strength is automatically controlled using the local electrical conditions and any additional circuits are not needed. Therefore, it is also useful to simplify the processing elements and neural network from hardware level. Incidentally, this local behavior is possible by characteristics of electron devices, or, in other words, it is convenient for integration of electron device. Finally, we confirm the correct operations of the processing elements, network architectures, synaptic connection, and learning rule using logic simulation and a field-programmable gate array (FPGA) chip and trimmer resistors and capacitors arranged on printed circuit boards (PCBs). Although the current results are very fundamental, it can be expected that the neural network acquires various abilities. Our results will be theoretical bases to realize ultra-large scale integration for neuromorphic systems.

2.1 Neuron Element

We consider the operation of a neuron element and come to have an idea that the

requisite minimum functions for the neuron element are (1) generating a binary state, which is called fire and stable states, and (2) alternating the binary state according to the input signal [1,2]. We propose three-type neuron circuits. Figure 2-1 shows the neuron circuits, 2-inverter 2-switch circuit, 2-inverter 1-switch circuit, and 2-inverter circuit. Because the neuron circuits can be made using complementary metal-oxide-semiconductor (CMOS) circuit, an inverter consists of a pair of n-type and p-type transistors, and a switch also consists of a pair of the transistors. Some properties of each neuron circuit are compared in the table in Fig. 2-1.



	Number								Switching noise		Input signal level	
	Inverter		Switch		Transistor		Synapse per connected neuron					
2-inverter 2-switch	2	◎	2	△	8	△	2	◎	Some	△	Binary	◎
2-inverter 1-switch	2	◎	1	○	6	○	4	○	Some	△	Binary	◎
2-inverter	2	◎	0	◎	4	◎	4	○	No	◎	Analog	△

◎: Very good, ○: Good, △:Not good

Fig. 2-1. Neuron circuits and comparison of the properties.

The 2-inverter 2-switch circuit is literally a circuit where the two inverters and two switches are circularly connected. The inverters generate a binary state, and the binary state is maintained when the switches are on, whereas the binary state is alternated when the switches are off and some input signal is received. The two terminals are bi-directional, namely, simultaneously work as both input and output terminals. One terminal is that for positive logic, whereas the other terminal is that for negative logic. This neuron circuit consists of eight transistors. The number of the synapse element per connected neighboring neuron element is two, which is explained in detail later. Because the switching pulses are periodically applied to the switches, some switching noise exists. Because there is a feedback loop from the output terminal to the input terminal, the input signal is also set to a binary level.

The 2-inverter 1-switch circuit is also literally a circuit where the two inverters and one switch are circularly connected. In contrast to the 2-inverter 2-switch circuit, the three terminals are uni-directional, namely, constantly work as either input or output terminal. One terminal is an input terminal, whereas the other two terminals are output terminals. One output terminal is that for positive logic, whereas the other output terminal is that for negative logic. This neuron circuit consists of six transistors. The number of the synapse element per connected neighboring neuron element is four, twice of that for the 2-inverter 2-switch circuit, because a synapse element sending the signal from a neuron element to the neighboring neuron element and another synapse element sending the signal form the neighboring neuron element to the neuron element are necessary. Some switching noise exists, and the input signal is also set to a binary level, which is similar to the 2-inverter 2-switch circuit.

The 2-inverter circuit is a circuit where the two inverters are connected in series. The inverters generate a binary state, and the binary state is alternated whenever some input signal is received. The three terminals are uni-directional. This neuron circuit consists of four transistors. The number of the synapse element per connected neighboring neuron element is four. Because the switching pulses are not applied, no switching noise exists. Because there is no feedback loop, the input

signal remains analog, which is different from those for the other neuron circuits.

The theoretical model for the neuron element is just a buffer block, whose function is completely the same as the 2-inverter circuit. It should be noted that the 2-inverter circuit is at least necessary to get the buffer block actually.

2.2 Synapse Element

We consider the operation of a synapse element and come to have an idea that the requisite minimum functions for the synapse element are (1) sending the signal from a neuron element to the neighboring neuron element, (2) merging the signals from the multiple neuron elements for the neuron element to alternate the binary state following the majority rule, and (3) controlling the synaptic connection strength, namely, how the signal is effectively sent, on demand [1,2]. We propose two-type synapse devices. Figure 2-2 shows the synapse devices, namely, variable register and variable capacitor.

Variable resistor Variable capacitor

Fig. 2-2. Synapse devices using a variable resistor and capacitor.

The variable resistor sends the signal as an electric current. The conductance corresponds to the synaptic connection strength. The electric currents are easily added by bundling the variable resistors in parallel, which corresponds to merging the signals. The advantage of the neural network using the variable resistors is operation stability, because the constant dc electric currents surely settle all the conditions in the network circuit.

The variable capacitor sends the signal as a voltage shift through capacitive coupling. The capacitance corresponds to the synaptic connection strength. The voltage shifts are also easily added by bundling the variable capacitors in parallel. The advantage of the neural network using the variable capacitors is low power consumption, because there is no constant dc electric current.

2.3 Network Architecture

First, we investigate Hopfield neural networks. Hopfield neural networks are neural networks where all neuron elements are connected each other and synapse elements are located at all the connections [3,4]. As a result, in comparison with the neuron elements, a much larger number of the synapse elements exist, and connection wiring occupies large areas or volumes.

A Hopfield neural network with the simplification of processing elements is shown in Fig. 2-3. Here, synapse elements are crosspoint-type devices sandwiched between top and bottom electrodes corresponding to horizontal and vertical bar-electrodes. In comparison with the conventional Hopfield neural network, the vertical bar-electrodes are switched to not only the input but also the output of the neuron elements, which is necessary for the learning rules explained later.

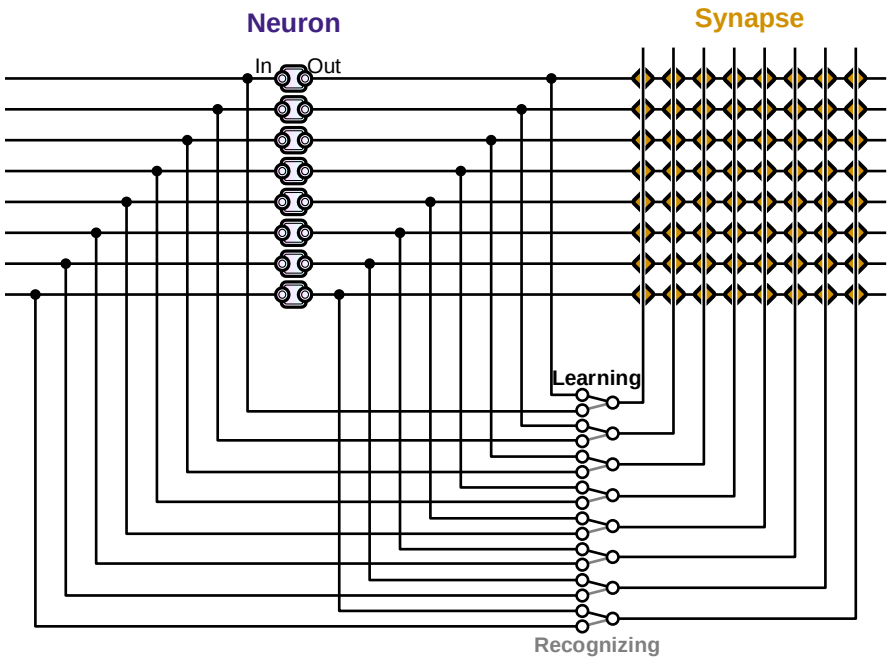


Fig. 2-3. Hopfield neural network with the simplification of processing elements.

Next, we investigate cellular neural networks [5-12]. Cellular neural networks are neural networks where a neuron element is connected to only neighboring

neuron elements, which are remarkably suitable for integration of electron devices. They are promising for image processing, pattern recognition, etc. As a result, in comparison with other neural networks, a relatively larger number of the neuron elements exist, and a large number of the synapse elements still exist, but connection wiring occupies little areas or volumes.

Cellular neural networks with the simplification of processing elements is shown in Fig. 2-4 [1,2,13-16]. Four-direction topology means that a neuron element is connected to four neighboring neuron elements, namely, upper, lower, right, and left ones, whereas eight-direction topology means that a neuron element is additionally connected also to four diagonal neighboring neuron elements.

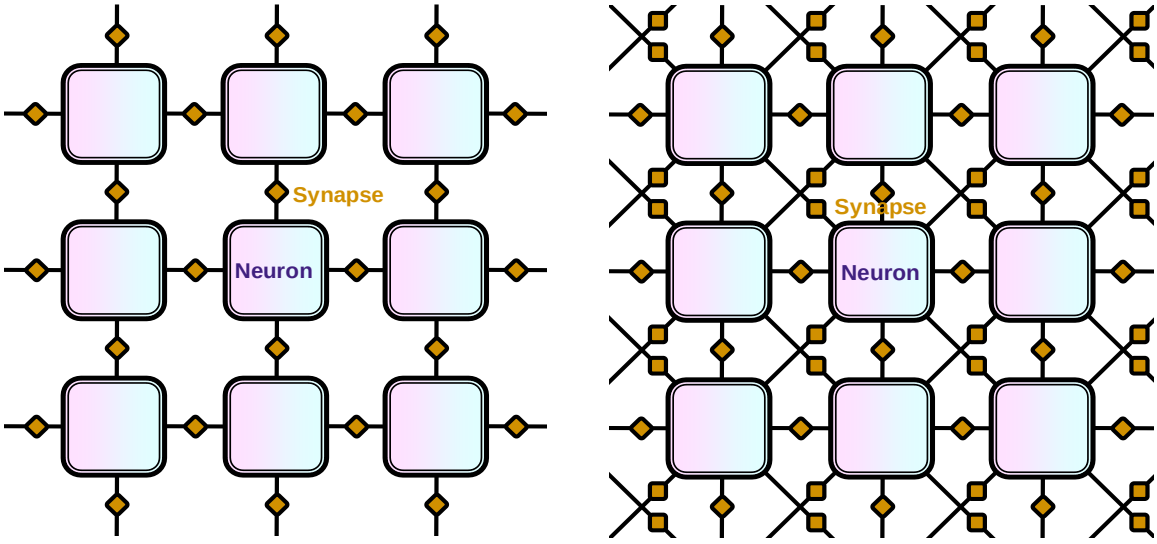


Fig. 2-4. Cellular neural networks with the simplification of processing elements.

Comparison between the Hopfield neural network and Cellular neural network is shown in Fig. 2-5. As aforementioned, in general, Hopfield neural networks have fewer neuron elements and more synapse elements, whereas cellular neural networks have more neuron elements and fewer synapse elements. It is checked that Hopfield neural networks can be used for various applications, whereas it is only checked that cellular neural networks can be mainly used for image recognition,

but this is just because systematic evaluation is not done very much. As aforementioned, Hopfield neural networks are not suitable for integration electron devices very much, because all neuron elements are connected each other and connection wiring occupies large areas or volumes, whereas cellular neural networks are remarkably suitable for integration of electron devices, because a neuron element is connected to only neighboring neuron elements and connection wiring occupies little areas or volumes. Because Hopfield neural networks and cellular neural networks are historical and typical neural networks described in all text books and they have contrastive properties, once it is confirmed that they can operate correctly, it is also expected that all kinds of neural networks can operate correctly.

Hopfield Neural Network				Cellular Neural Network
Single Layer All Connection		Architecture		Single Layer Neighboring Connection
Few		Neuron		Many
Many		Synapse		Few
Almighty	○	Application	×	Image Recognition ?
Difficult	×	Integration	○	Easy

Fig. 2-5. Comparison between the Hopfield neural network and Cellular neural network.

2.4 Synaptic Connection

We investigate synaptic connections and propose a tug-of-war method [1,2]. The tug-of-war method for synaptic connection is shown in Fig. 2-6. We prepare two-type synapse connections, concordant connection and discordant connection. The concordant connection connects the same logics of the two neuron elements, namely, positive and positive logics or negative and negative logics, and tends to make the states of the two neuron elements the same. On the other hand, the discordant connection connects the different logics of the two neuron elements, namely, positive and negative logics, and tends to make the states of the two neuron elements different. The reason why we prepare two-type synapse

connections is to obtain the same effect that the synaptic connection strength becomes both stronger and weaker even if the actual strength becomes either one. For example, the effect that the synaptic connection strength becomes stronger is gotten, if the discordant connection becomes weaker.

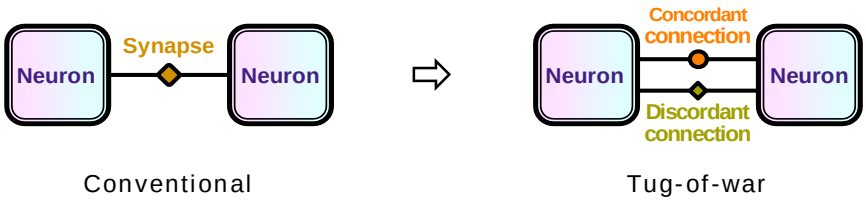


Fig. 2-6. Tug-of-war method for synaptic connection.

The tug-of-war method is more effective for cellular neural networks, because Hopfield neural networks have a much larger synapse elements whereas cellular neural networks have fewer synapse elements and the tug-of-war method partially compensates the disadvantage. Therefore, we show examples of the tug-of-war method using cellular neural networks. The tug-of-war method in cellular neural networks is shown in Fig. 2-7. Here, cellular neural networks with four-direction

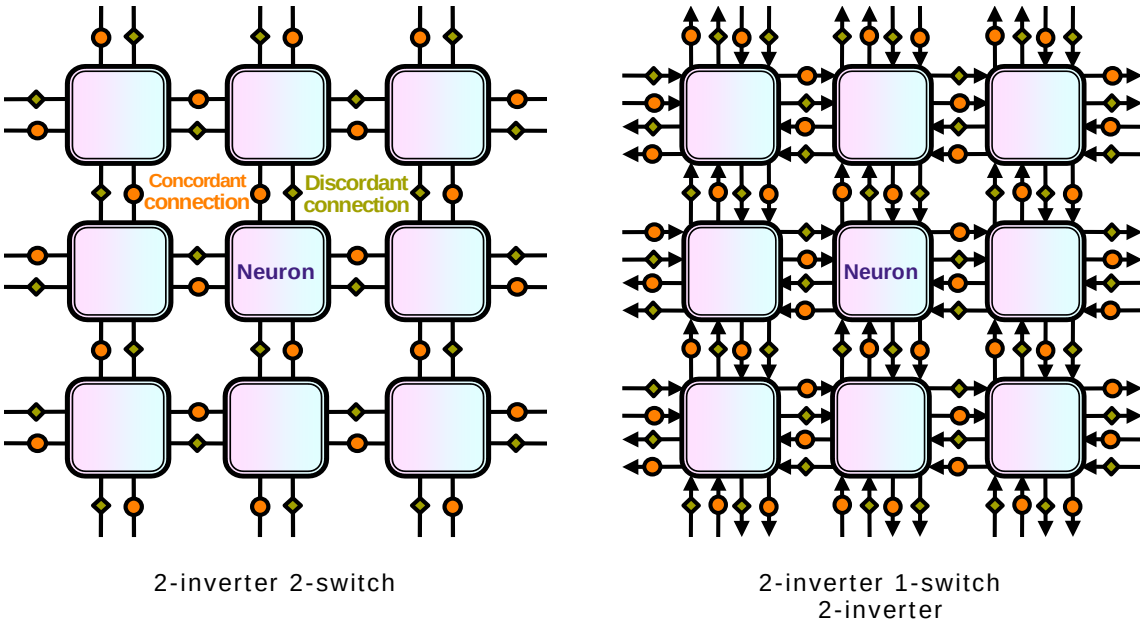


Fig. 2-7. Tug-of-war method in cellular neural networks.

topology are shown when the 2-inverter 2-switch, 2-inverter 1-switch, and 2-inverter circuits are used for neuron elements.

The cellular neural network for the 2-inverter 2-switch circuit has two synaptic connections, concordant and discordant connections, between a pair of the neighboring neuron elements. As a result, the cellular neural network having n neurons approximately has $8 \cdot n$ transistors and $4 \cdot n$ synapse devices by neglecting the exception of the connection at the peripheral neuron elements.

The cellular neural network for the 2-inverter 1-switch and 2-inverter circuits has four synaptic connections, forward and reverse connections in addition to the concordant and discordant connections, between a pair of the neighboring neuron elements. As a result, the cellular neural network for the 2-inverter 2-switch circuit having n neuron elements approximately has $6 \cdot n$ transistors and $8 \cdot n$ synapse devices, and the cellular neural network for the 2-inverter circuit approximately has $4 \cdot n$ transistors and $8 \cdot n$ synapse devices. Because the structure of the transistors is usually more complicated than that of synapse devices if the synapse devices are made using simple devices, the 2-inverter circuit is more suitable to realize ultra-large scale integration.

2.5 Modified Hebbian Learning

Hebbian learning is a typical learning rule in biological and artificial neural networks [17]. The synaptic connection strength is enhanced, when both neuron elements connected to the synapse connection are in the fire state, but impaired otherwise. Since the processing elements, such as, neuron elements and synapse element, are dramatically simplified, the leaning rule is also modified. Modified Hebbian learning is shown in Fig. 2-8 [1,2]. Here, "F" means the fire state, whereas "S" means the stable state. As an example, consider the NOT logic. The left and right neuron elements are assigned to the input and output elements, respectively. Initially, in the initial recognizing stage, a stable state is applied to the input element, and a stable state arises from the output element, and vice versa, because the synaptic connection strength of the concordant connection is accidentally slightly stronger than that of the discordant connection, which is not the NOT logic.

Next, in the first learning stage, a stable state is applied to the input element, and a fire state is applied to the output element. Since the concordant connection connects the two terminals for the same logic in the two neuron elements and the binary states at both terminals in the two neuron elements are different, some voltage occurs through the concordant connection, or the electric current flows through the concordant connection due to the voltage, but any voltage does not occur through the discordant connection, or the electric current does not flow through the discordant connection. If the synapse elements are designed so that the synaptic connection strength is continuously impaired when some voltage occurs or the electric current flows, only the synaptic connection strength of the concordant connection gradually weakens. In the second learning stage, a fire state is applied to the input element, and a stable state is applied to the output element. Similarly, only the synaptic connection strength of the concordant connection gradually weakens. Finally, in the final recognizing stage, a stable state is applied to the input element, and a fire state arises from the output element, and vice versa, because the synaptic connection strength of the concordant connection becomes slightly weaker than that of the discordant connection, which is the NOT logic.

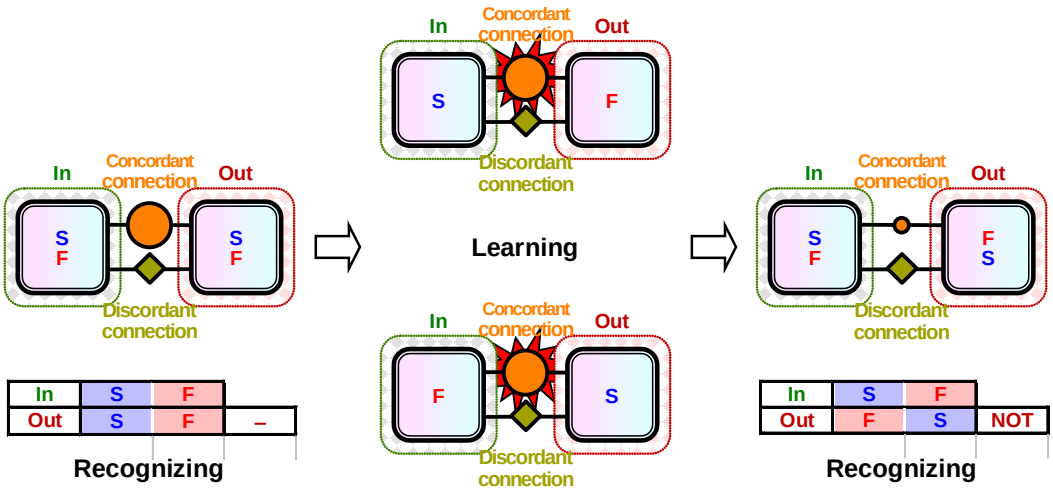


Fig. 2-8. Modified Hebbian learning.

The outstanding advantage of the modified Hebbian learning is that the synaptic connection strength is automatically controlled using the local voltage or electric

current and any additional circuits are not needed to control synaptic connection strengths. Therefore, it is believed that the modified Hebbian learning is also useful to simplify the processing elements and neural network from hardware level. Incidentally, this local behavior is possible by characteristics of electron devices, or, in other words, it is convenient for integration of electron device, which is explained in detail in the following chapers. On the other hand, the minor disadvantage of the modified Hebbian learning is that because the synaptic connection strength usually changes in the direction that it is impaired, the synaptic connection strength cannot be enhanced even if both neuron elements connected to the synapse connection are in the fire state. However, the relative values of the synaptic connection strength can be enhanced. In any case, by employing modified Hebbian learning and the characteristic change of the synapse devices, we successfully create a synapse device that consists of just one variable resistor or variable capacitor.

2.6 Operation Confirmation

We confirm the operations of the abovementioned processing elements, such as, neuron elements and synapse elements, network architectures, especially, cellular neural network, because it is revised more than the conventional ones, synaptic connection, namely, tug-of-war method, and learning rule, namely, modified

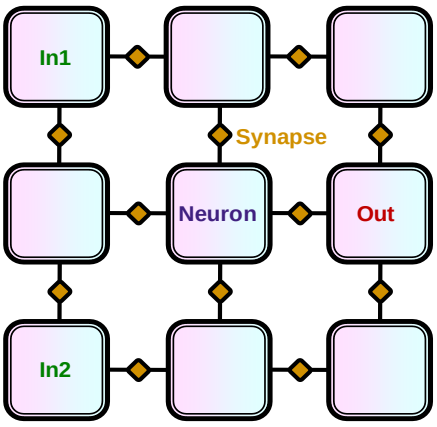


Fig. 2-9. Trial example for the operation confirmation.

Hebbian learning, using logic simulation and an FPGA chip and trimmer resistors and capacitors arranged on PCBs [1,18]. A trial example for the operation confirmation is shown in Fig. 2-9. Here, a cellular neural network, which has 3×3 neuron elements, four-direction topology, tug-of-war method, and modified Hebbian learning are used. Arbitrary two-input one output logics, such as, AND, OR, and XOR, are learnt, where two input neuron elements and one output neuron element are assigned, namely, the left upper neuron element is that for In1, the left lower neuron element is that for In2, and right middle neuron element is that for Out.

We execute logic simulation to determine the entire pattern of the synaptic connection strength. First, we apply In1, In2, and Out to the neuron elements for them. Next, we calculate a steady pattern for the states of the neuron elements based on the normal theory of the dynamics of the neural network and by repeating calculation of alternating the state. After that, the synaptic connection strength of the concordant connection is kept the same when both neuron elements connected to the synapse element are in the same states, and is impaired otherwise, whereas the synaptic connection strength of the discordant connection is kept the same when both neuron elements connected to the synapse element are in the different states, and is impaired otherwise. Finally, we obtain the entire pattern of the synaptic connection strength. Figure 2-10 shows the entire pattern of the synaptic connection strength for AND, OR, and XOR logics.

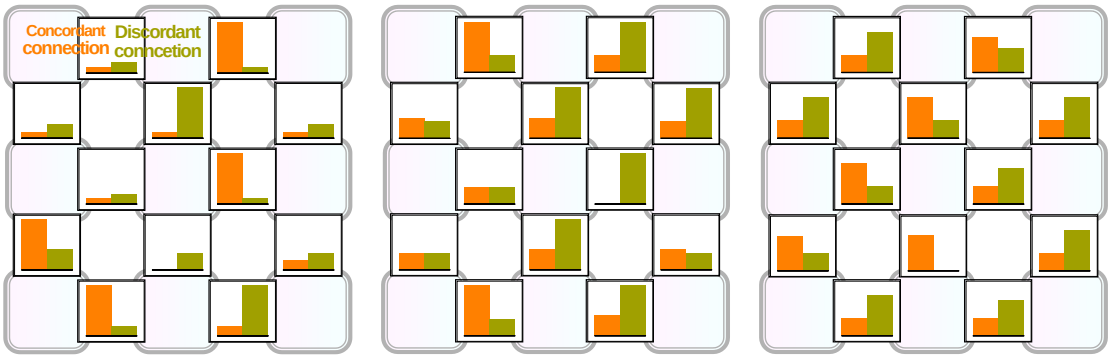
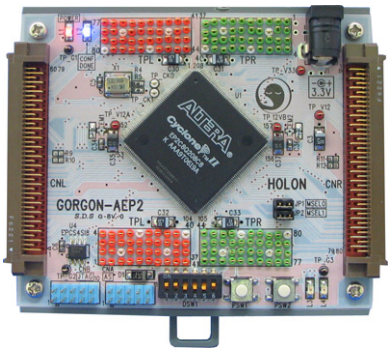
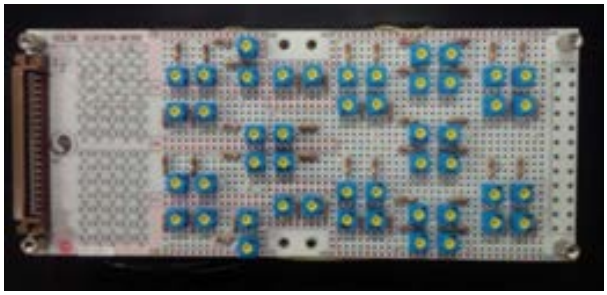


Fig. 2-10. Synaptic connection strength calculated using logic simulation.

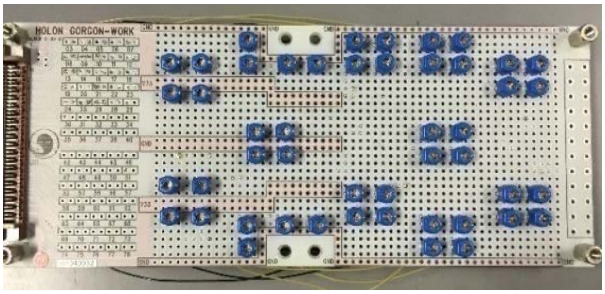
We compose the neuron elements in an FPGA chip and compose the synapse elements by trimmer resistors and capacitors arranged on PCBs. Figure 2-11 shows the actual hardware for the operation confirmation, namely, FPGA, trimmer resistors, and trimmer capacitors. Here, in addition to the conditions in the logic simulation, neuron elements, such as, two-inverter two-switch circuit, two-inverter one-switch circuit, and two-inverter circuit, synapse elements, such as, variable registers and capacitors, are used. It should be noted that although discrete parts, such as, trimmer resistors and capacitors, are used as variable registers and capacitors, this approach is only for the evaluation, and they should be undoubtedly replaced by some actual electron devices, such as, memristors and ferroelectric capacitors, to realize ultra-large scale integration. The entire patterns of the resistances and capacitances in the trimer resistors and capacitors are set to the entire patterns of the synaptic connection strength calculated using the logic simulation.



FPGA



Trimmer Resistors



Trimmer capacitors

Fig. 2-11. Actual hardware for the operation confirmation.

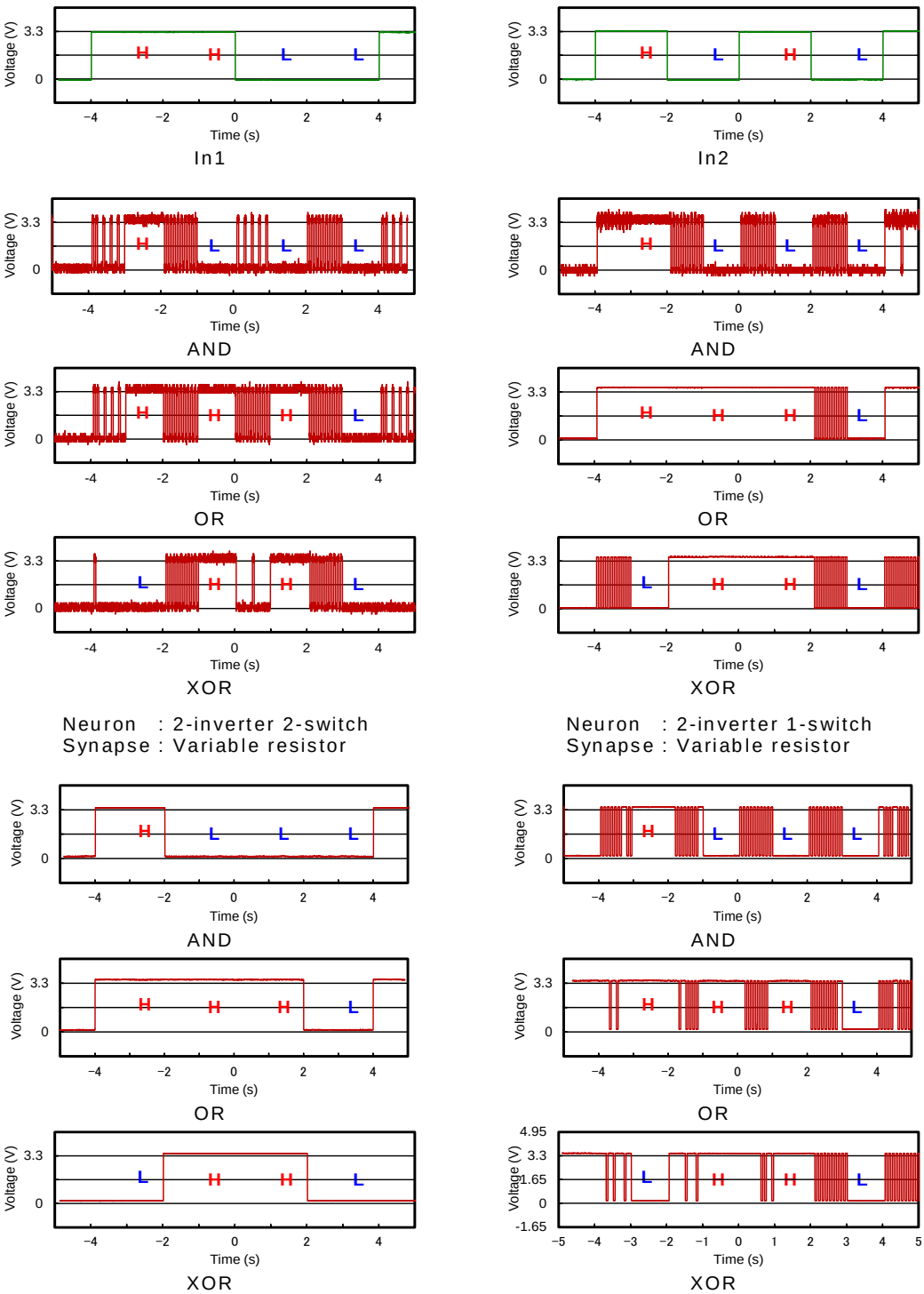


Fig. 2-12. Input and output waveforms of the actual hardware.

Figure 2-12 shows the input and output waveforms of the actual hardware. In1 and In2 are periodic rectangle pulses, which make all four combinations of high voltage (H) and low voltage (L), and applied to the input terminals of the neuron elements for In1 and In2. Out is measured at the output terminal of the neuron elements for Out. It is confirmed that the correct operations are achieved for all logics, namely, AND, OR, and XOR, all neuron circuits, namely, 2-inverter 2-switch, 2-inverter 1-switch, and 2-inverter circuits, and all synapse elements, namely, variable resistor and capacitor. For the 2-inverter 2-switch and 2-inverter 1-switch circuits, although some switching noise exists, after the switching pulses are off and states are settled, the correct operations are achieved. For the 2-inverter circuit, no switching noise exists. For the variable capacitor, only the 2-inverter 1-switch circuit is used, because the input terminals become floating if the 2-inverter circuit is used and unexpected behavior is unavoidable if some electric charges are accumulated in the input terminals during the network operation. In any case, it is confirmed that the correct operations are achieved for all logics, neuron elements, and synapse elements.

Although the current results are very fundamental, it can be expected that the neural network acquires various abilities, if a lot of processing elements are provided, which is possible because we succeeded in simplification of processing elements. In summary, our results will be theoretical bases to realize ultra-large scale integration for neuromorphic systems. Although we need great effort to develop actual electron devices having the requisite minimum functions especially for the synapse elements, our results indicates that the researchers solely focus on the development of the circuits and devices having the requisite minimum functions, because the correct operation of the neural networks has been already guaranteed once such circuits and devices are realized.

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3 Thin-Film Device

Thin-film devices may be suitable devices for neuromorphic systems from some viewpoints. First, the outstanding features of the thin-film devices are low-temperature fabrication and high material efficiency. As a result, the notable advantages are that they can be fabricated on large areas and three-dimensional layered structure can be acquired. Therefore, an astronomical number of processing elements may be integrated, when thin-film devices are used for neuromorphic systems. Next, the unavoidable disadvantages of the thin-film devices are low performance and low yield owing to the low-temperature fabrication. However, they may be acceptable, because the operation speed of neuromorphic systems do not have to be so fast and they are robust against the damage of processing elements. In this chapter, we enumerate some kinds of thin-film devices available for neuromorphic systems, such as, low-temperature poly-Si (LTPS) device, amorphous metal-oxide semiconductor (AOS) devices, namely, amorphous In-Ga-Zn-O (α-IGZO) device and amorphous Ga-Sn-O (α-GTO) device, and Ta_2O_5 device. In any case, it is confirmed that the electrical conductance gradually decreases when electric current flows, which is available as a synaptic connection strength based on an operation theory of the modified Hebbian learning. By using such thin-film devices in neuromorphic systems, it is expected that the machine size can be further compact. Moreover, because amorphous IGZO and GTO devices can have extremely low leakage current, it is also expected that the power consumption can be further low.

3.1 Low-Temperature Poly-Si Device

LTPS devices are widely used as thin-film transistors (TFTs) [1-3] for flat-panel displays (FPDs), such as, high-resolution liquid-crystal displays (LCDs) and light-emitting diode displays (OLEDs). These FPDs are mainly used for mobile applications because they are very tough ageist rough handling.

A transistor-type LTPS device is shown in Fig. 3-1. First, an amorphous-Si thin film is deposited using low-pressure chemical-vapor deposition (LPCVD) of Si_2H_6

and crystallized using XeCl excimer laser to form a poly-Si thin film. The thickness of the poly-Si thin film is 50 nm, and the grain size is 500 nm or less. Next, a SiO_2 thin film is deposited using plasma-enhanced chemical-vapor deposition (PECVD) of tetraethyl orthosilicate (TEOS) to form a gate-insulator thin film. The thickness of the gate-insulator thin film is 75 nm. Next, phosphorous ions are pseudo-selfalignedly implanted and thermally activated to form source and drain regions, and a gate-metal thin film is deposited and patterned to form a gate terminal. Finally, a SiO_2 thin film is deposited and patterned to prepare an interlayer-insulator thin film, and a source-drain metal thin film is deposited and patterned to form source and drain terminals. Consequently, top-gate, coplanar, and n-type poly-Si TFTs are fabricated. Here, the gate width (W) / gate length (L) = 5 / 5 μm. The field-effect mobility (μ) ≅ 90 $cm^2 \cdot V^{-1} \cdot s^{-1}$, and threshold voltage (V_{th}) ≅ 4.0 V.

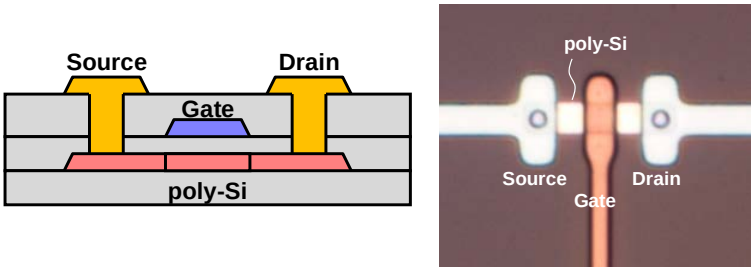

Fig. 3-1. Transistor-type LTPS device.

The degradation characteristics of the LTPS device are investigated to find a suitable condition for the modified Hebbian learning. The degradation characteristics of the LTPS device is shown in Fig. 3-2 [4]. First, initial transfer and output characteristics are measured. Next, stress tests are executed by applying Vgs = 0 ~ 15 V and Vds = 0 ~ 12 V during 0 ~ 3 hr. Afterward, normal transfer and output characteristics are measured, where the normal characteristic is defined as the transistor characteristic when the source and drain terminals for the measurement are the same as those for the stress test. Next, reverse characteristics are also measured, where the reverse characteristic is defined as the transistor characteristic when the source and drain terminals for the measurement are

opposite to those for the stress test. Here, since the grain size is as small as 500 nm or less as aforementioned, it can be assumed that the grains are uniformly distributed within the poly-Si thin film and there is little unbalance between the normal and reverse characteristics from the viewpoint of the number and location of the grain boundaries.

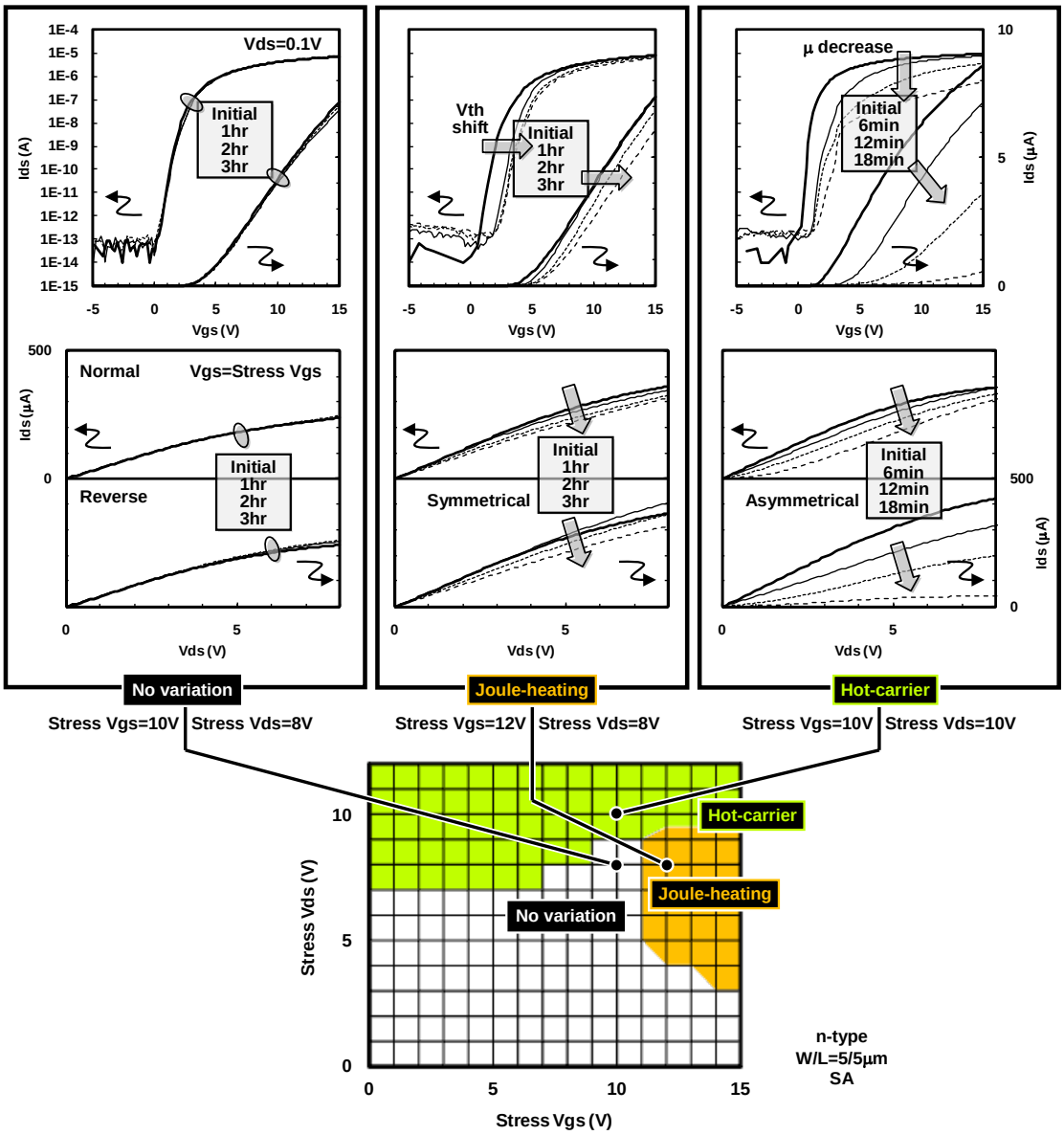

Fig. 3-2. Degradation characteristics of the LTPS device.

The Joule-heating and hot-carrier degradations are indicated in Fig. 3-2. Here, logarithmic and linear graphs of the transfer characteristics are shown to observe V_{th} shifts and μ decreases, whereas normal and reverse characteristics of the output characteristics are shown to check whether they are symmetrical or asymmetrical. The symmetrical characteristics are defined when the degradation in the normal characteristics are similar to the degradation in the reverse characteristics, whereas the asymmetrical characteristics are defined when the degradation of the normal characteristics are less than halves of the degradation in the reverse characteristics. First, no degradation is observed for low V_{gs} and V_{ds}. On the contrary, V_{th} shifts are mainly observed during the range of hours for high V_{gs} and medium V_{ds} as shown by yellow areas in Fig. 3-2. It is supposed that Joule-heating degradation occurs because the power consumption is large in the poly-Si thin films but the lateral electric fields are not strong near the drain junctions [5,6]. The Si-H bonds are broken in the poly-Si thin films and at their interfaces, and the dangling bonds are generated there. In addition, the normal and reverse output characteristics are symmetrical because the entire poly-Si thin films are uniformly heated and degraded. Therefore, it is suggested that the symmetrical normal and reverse characteristics indicate the Joule-heating degradation. On the other hand, not only V_{th} shift but also μ decreases are observed during the range of minutes for high V_{ds} as shown by green areas in Fig. 3-2. It is supposed that hot-carrier degradation occurs because the lateral electric fields are strong near the drain junctions [7,8]. The charges are injected into the gate-insulator thin films, and traps are generated in the poly-Si thin films and at their interfaces. In addition, the normal and reverse output characteristics are asymmetrical because the poly-Si thin films, gate-insulator thin films, and their interfaces only near the drain junctions are locally degraded. Therefore, it is suggested that the asymmetrical normal and reverse characteristics indicate the hot-carrier degradation. Although the hot carrier degradation and Joule-heating degradation are expected to simultaneously occur especially for high V_{gs} and V_{ds}, the hot carrier degradation rapidly occurs as aforementioned and is therefore dominant. Since the symmetrical normal and reverse characteristics indicate the Joule-heating degradation whereas the

asymmetrical characteristics indicate the hot-carrier degradation, they can be clearly and easily classified as shown in Fig. 3-2. It qualitatively coincides with the previous report [6]. Since electric currents flow in alternating directions through the synapse elements in the neural networks, it is preferable to use the Joule-heating effect because the characteristic variations are symmetrical.

3.2 Amorphous In-Ga-Zn-O Device

AOS devices are promising because they have excellent and uniform performances even when they are deposited at low temperature and in amorphous phase [9]. Moreover, AOS devices can be potentially formed using printing methods [10], which is convenient to realize three-dimensional layered structure for neuromorphic systems [11]. α-IGZO devices are representative devices [12] and recently used as TFTs for FPDs, such as, high-resolution LCDs and OLEDs [13-16].

Planar-type α-IGZO devices are shown in Fig. 3-3 [17]. First, a quartz glass substrate is used. The thickness is 1mm, and the size is 3×3 cm. Next, an α-IGZO thin film is deposited using radio-frequency (RF) magnetron sputtering. The sputtering target is an IGZO ceramic whose composition is In:Ga:Zn=1:1:1, and the sputtering gas is Ar. The α-IGZO thin film is patterned through a metal mask as shown by the dotted line in Fig. 3-3. The thickness of the α-IGZO thin film is

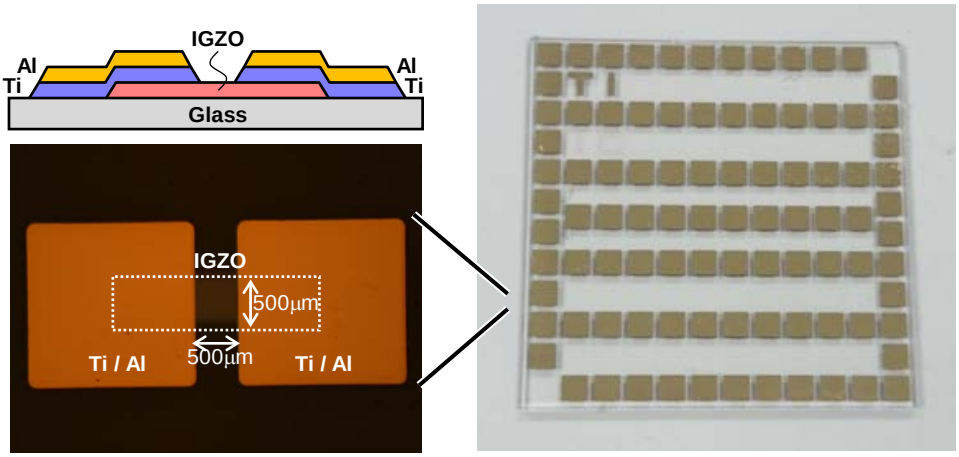

Fig. 3-3. Planar-type α-IGZO devices.

70nm. These fabrication conditions are the same as those for the TFTs having the best performance [18]. Finally, Ti and Au thin films are sequentially deposited using vacuum evaporation. Ti and Au thin films are also patterned through a metal mask as shown in Fig. 3-3. The thicknesses of Ti and Au thin films are 50nm each. Ti thin film is used to obtain ohmic contact to the α-IGZO thin film because it has a proper work function and improve adherence, and Au thin film is used to avoid the surface oxidation and make probing easy. No additional annealing is executed.

The electrical current through the planar-type α-IGZO device is shown in Fig. 3-4 [19]. Here, we apply 3.3 V between the right and left terminals of the Ti and Au thin films and measure the electrical current through the planar-type α-IGZO device. It is found that the electrical conductance continuously decrease when the electric current flows. The conductance decrease is irreversible. The modified Hebbian learning can be employed using this phenomenon. As shown in Fig. 3-4, the conductance decrease is not so fast. However, because the operation of the neural network is based on the delicate balance of the majority rule, the slow change is sometimes convenient also to avoid the excess learning.

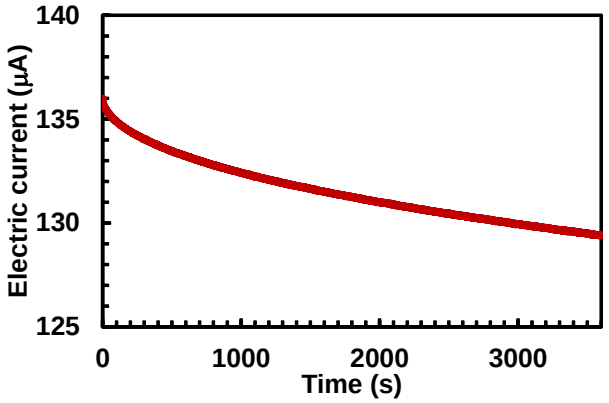

Fig. 3-4. Electrical current through the planar-type α-IGZO device.

The mechanisms for the conductance decrease are shown in Fig. 3-5. It is supposed that this phenomenon is caused by either the generation of trap states in the α-IGZO thin film or injection of the electric charge into the interface between the α-IGZO thin film and quartz glass substrate. In the case of the generation of

trap states, first, free electrons are accelerated and collide to the α-IGZO crystal. Next, trap states are generated and capture free electrons. Finally, free electrons decrease because of the fixed charge in the trap states and are simultaneously scattered by them, which induces the conductance decrease. On the other hand, in the case of the injection of the electric charge, first, free electrons are again accelerated near the interface and are casually injected into the interface between the IGZO thin film and quartz glass substrate. Next, the free electrons are captured at the interface. Finally, free electrons decrease because of the fixed charge of the injected electrons, which also induces the conductance decrease.

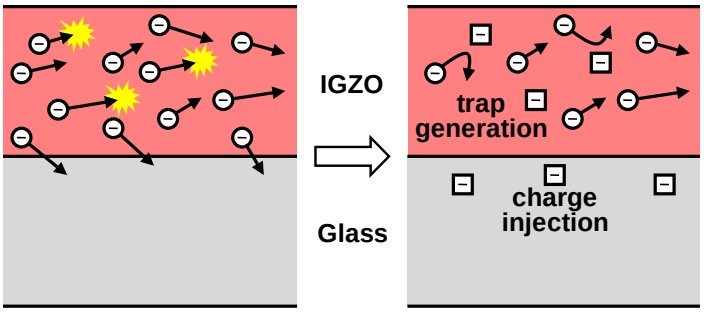

Fig. 3-5. Mechanisms for the conductance decrease.

The planar-type α-IGZO device is a kind of memristor, because the definition of the memristor is that the present value of electric current changes by the historical summation of flowing electric charges. However, in comparison with the conventional memristers used as resistive memories [20], the planar-type α-IGZO device shows the continuous change of the electric conductance, which is preferable for our neural network. Moreover, it does not need high temperature for fabrication process and can be potentially formed using printing methods. Furthermore, in comparison with the conventional floating-gate transistors [21], the device structure is quite simple, which is convenient to realize three-dimensional layered structure for neuromorphic systems.

3.3 Amorphous Ga-Sn-O Device

α-GTO devices are newcomer devices and expected to be gotten at low cost because they do not include In [22]. Therefore, α-GTO devices may be more suitable for neuromorphic systems, because a lot of material are consumed when three-dimensional layered structure are built.

Crosspoint-type α-GTO devices are shown in Fig. 3-6. First, a quartz glass substrate is used. Next, Ti thin film is deposited using vacuum evaporation. The Ti thin film is patterned through a metal mask, and fine multiple stripe patterns are formed as bottom electrodes. Next, an α-GTO thin film is deposited using RF magnetron sputtering. The sputtering target is a GTO ceramic, and the sputtering gas is Ar : O_2 = 20 : 1 sccm. The α-GTO thin film is patterned through a metal mask, and peripheral areas are exposed to contact the bottom electrodes. The thickness of the α-GTO thin film is 70nm. Finally, Ti thin film is again deposited. Fine multiple stripe patterns are again formed as top electrodes, which is perpendicular to the bottom electrodes. Post-annealing is executed at 350 °C for 1 hr.

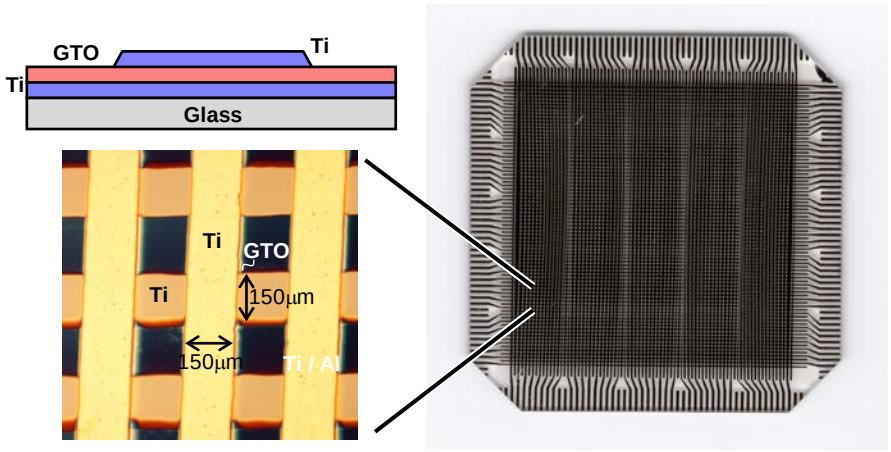

Fig. 3-6. Crosspoint-type α-GTO devices.

The electrical current through the crosspoint-type α-GTO devices is shown in Fig. 3-7. Here, we apply 3.3 V between the top and bottom terminals of Ti thin films and measure the electrical current through the crosspoint-type α-GTO device. It should be noted that the horizontal axis is a logarithmic axis in contrast with Fig.

3-4. It is found that the electrical conductance continuously decrease when the electric current flows and the decrease speed is faster than the planar-type α-IGZO device because the voltage is applied to the α-GTO thin film and strong. The modified Hebbian learning can be employed also using this phenomenon. It is supposed that the mechanism for the conductance decrease is the generation of trap states in the α-GTO thin film.

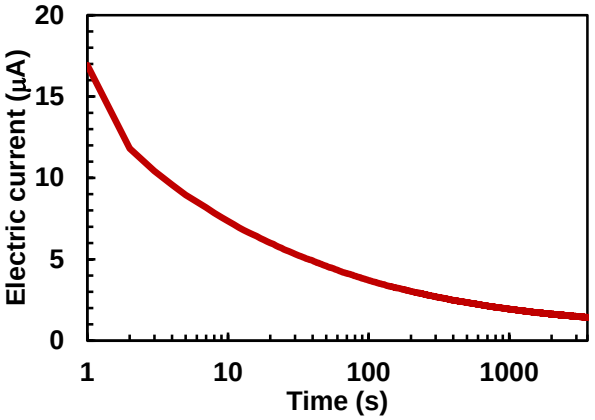

Fig. 3-7. Electrical current through the crosspoint-type α-GTO device.

3.4 Ta_2O_5 Device

Ta_2O_5 devices are begun to be used as resistive memories [23]. Because memristor devices are often considered to be used for neural networks [24], Ta_2O_5 devices are used also in this study. Crosspoint-type Ta_2O_5 devices are similar to crosspoint-type α-GTO devices, and the electrical current is also similar, namely, the electrical conductance continuously decrease. We will submit the results to some journal soon.

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4 Hopfield Neural Network

Hopfield neural networks are neural networks where all neuron elements are connected each other through synapse elements. Because a large number of the synapse elements exist, it is important to confirm the correct operations of the simplified synapse elements. Neuron elements are virtually composed in a field-programmable gate array (FPGA) chip, whereas synapse elements are actually composed of crosspoint-type devices. In the learning stage, voltages appear and electric currents flow in some crosspoint devices, and the synaptic connection strength, such as, the electric conductance, etc., is weakened. In the recognition stage, output signals are detected, which is the response from the Hopfield neural network. The electric conductance is weakened in the learning stage because the voltages are applied for a long time, whereas the electric conductance is not changed very much in the recognition stage because the voltages are applied for an instant. Letter reproduction is executed to confirm the operation of the Hopfield neural network. Crosspoint-type α-GTO devices is used as synapse elements. First, it is found that the standard patterns of two numeral letters can be completely reproduced in the revised patterns. However, an issue is that the success probability is not so high. Therefore, majority-rule handling is invented. It is found that the standard patterns of three alphabet letters can be reproduced in the revised patterns. Moreover, the success probability is high. This means that we have succeeded in letter reproduction. In addition, crosspoint-type Ta_2O_5 devices are used, and we have also succeeded in letter reproduction.

4.1 System Architecture

Hopfield neural networks are neural networks where all neuron elements are connected each other and synapse elements are located at all the connections [1,2]. As a result, in comparison with the neuron elements, a much larger number of the synapse elements exist, and connection wiring occupies large areas or volumes. Therefore, whereas various structures are usually acceptable for the neuron elements, it is important to simplify the synapse elements and confirm the

operations.

System architecture of a Hopfield neural network is shown in Fig. 4-1 [3]. Eighty neuron elements are virtually composed in a personal computer (PC), peripheral component interconnect (PCI) board, and FPGA chip using hardware description language (HDL), whereas 80 × 80 synapse elements are actually composed of crosspoint-type devices, and they are connected through a connection

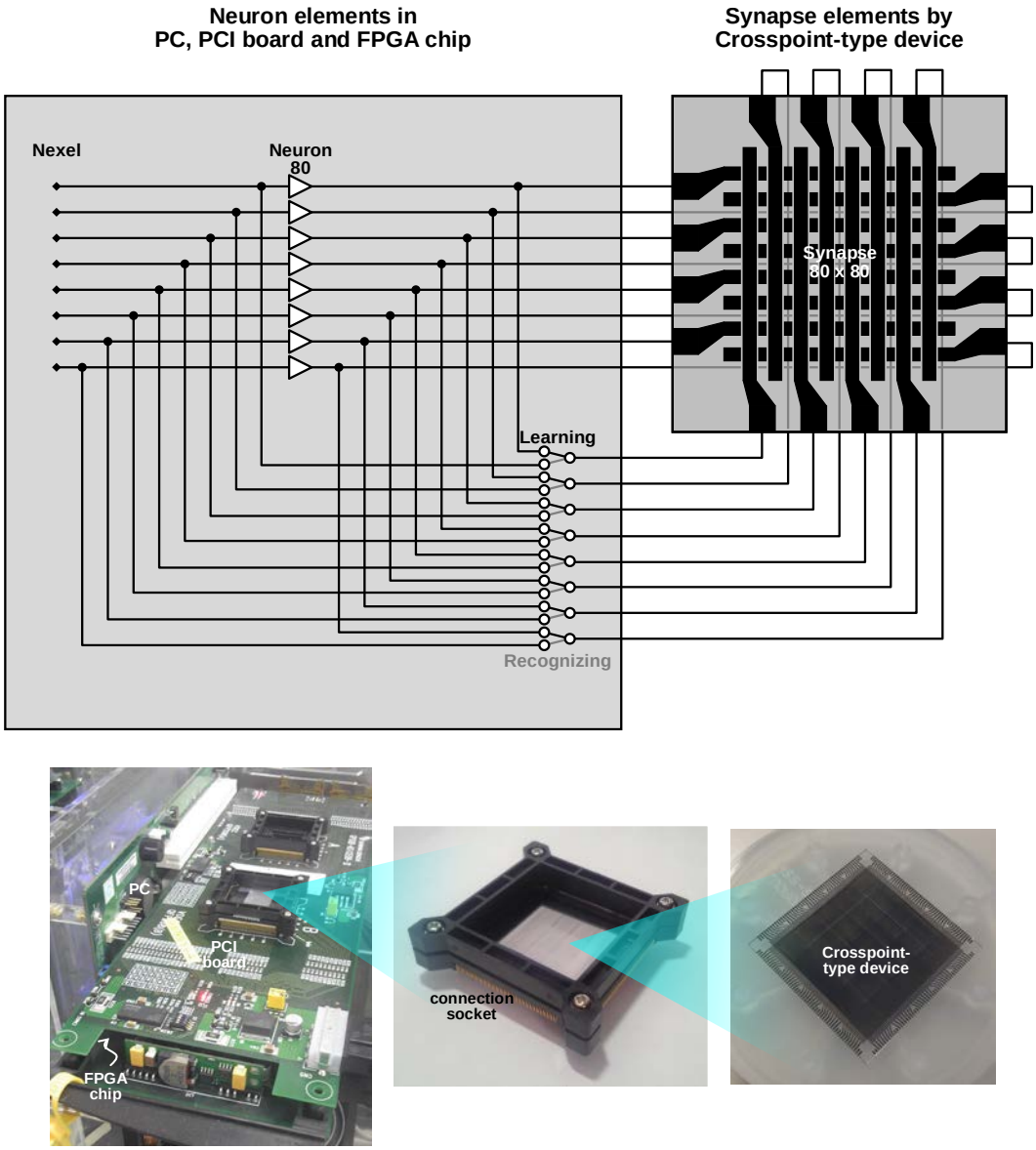

Fig. 4-1. System architecture of a Hopfield neural network.

socket to confirm operations of crosspoint devices with various materials by replacing them in the connection socket. The crosspoint-type devices have top and bottom electrodes as aforementioned, and they correspond to horizontal and vertical bar-electrodes. The bus groups of the horizontal and vertical bar-electrodes are each connected to the neuron elements. Output signals from the neuron elements are outputted to the bus group of the horizontal bar-electrodes, and they are also outputted to the bus group of the vertical bar-electrodes in learning stage. Output signals from the bus group of the vertical bar-electrodes are inputted into the neuron elements in recognizing stage. "Nexel" is an abbreviation of "neuron cell", which is similar to that "pixel" is an abbreviation of "picture cell", and in-out interface to a neuron element. In summary, a conventional architecture of the Hopfield neural network is used with the novel architecture of the crosspoint-type devices.

The operation principle of the crosspoint-type devices is shown in Fig. 4-2. First, in the learning stage, high voltage, for example, 3.3 V, is applied to the corresponding horizontal and vertical bar-electrodes for the neuron elements in the fire state, as shown in bright blue in Fig. 4-2, whereas low voltage, for example, GND, is applied to the bar-electrodes in the stable state, as shown in dark blue in Fig. 4-2. As a results, voltages appear in some crosspoint devices, and electric currents flow, as shown in bright brown in Fig. 4-2. After a while, the synaptic connection strength, such as, the electric conductance, etc., is weakened. Finally, in the recognition stage, high and low voltages are applied to the corresponding horizontal bar-electrodes, and high and low voltages are detected from the vertical

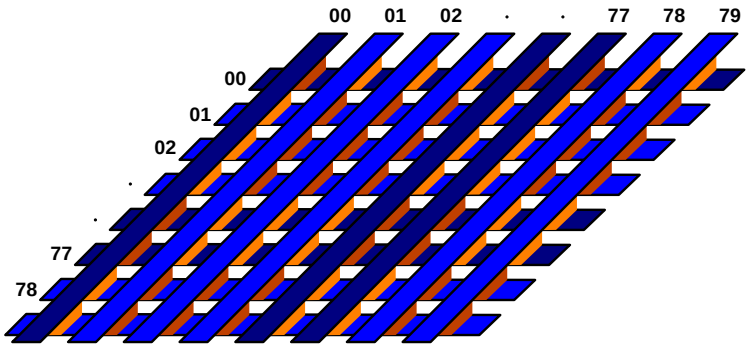

Fig. 4-2. Operation principle of the crosspoint-type devices.

bar-electrodes, which is the response from the Hopfield neural network. It should be noted that the electric conductance is weakened in the learning stage because the voltages are applied for a long time, whereas the electric conductance is not changed very much in the recognition stage because the voltages are applied for an instant.

Letter reproduction is executed to confirm the operation of the Hopfield neural network. The letter reproduction is a part of the letter recognition [4], where distorted letters is reproduced to standard letters, which is available for hand-writing reading, optical character recognition (OCR), etc., and also an often-used criterion to check neural networks [5]. Mapping from a two-dimensional pattern for image expression to a one-dimensional pattern for computer interface is necessary for the letter reproduction. Mapping from a two-dimensional pattern to a one-dimensional pattern is shown in Fig. 4-3. Although the two-dimensional pattern includes 9×9=81 units, because the one-dimensional computer interface includes only 80 units, one unit in the image description is neglected. In comparison with convolutional neural networks (CNNs) [6], the advantage of this study is that, whereas the CNNs need deep multiple layer neural networks, the Hopfield neural network needs an only single layer neural network, which is simple and speedy in both learning and recognizing stages.

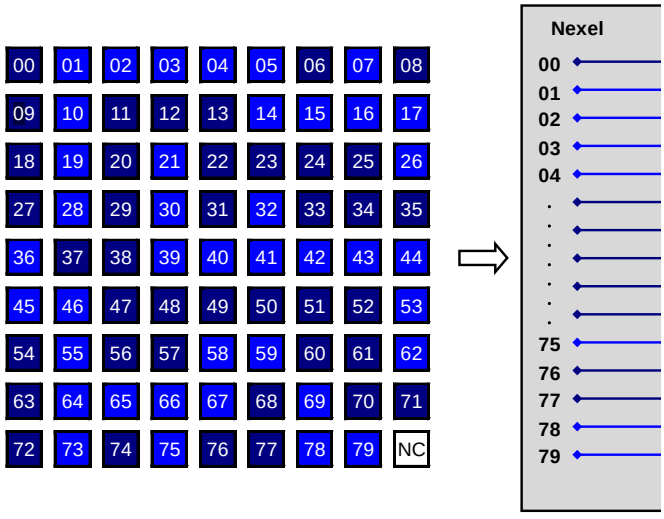

Fig. 4-3. Mapping from a two-dimensional pattern to a one-dimensional pattern.

4.2 Amorphous Ga-Sn-O Device

Crosspoint-type α-GTO devices are used as synapse elements. An experimental result of the letter reproduction is shown in Fig. 4-4. Here, the pixel pattern corresponds to the nexel pattern one to one. First, in the learning stage, standard

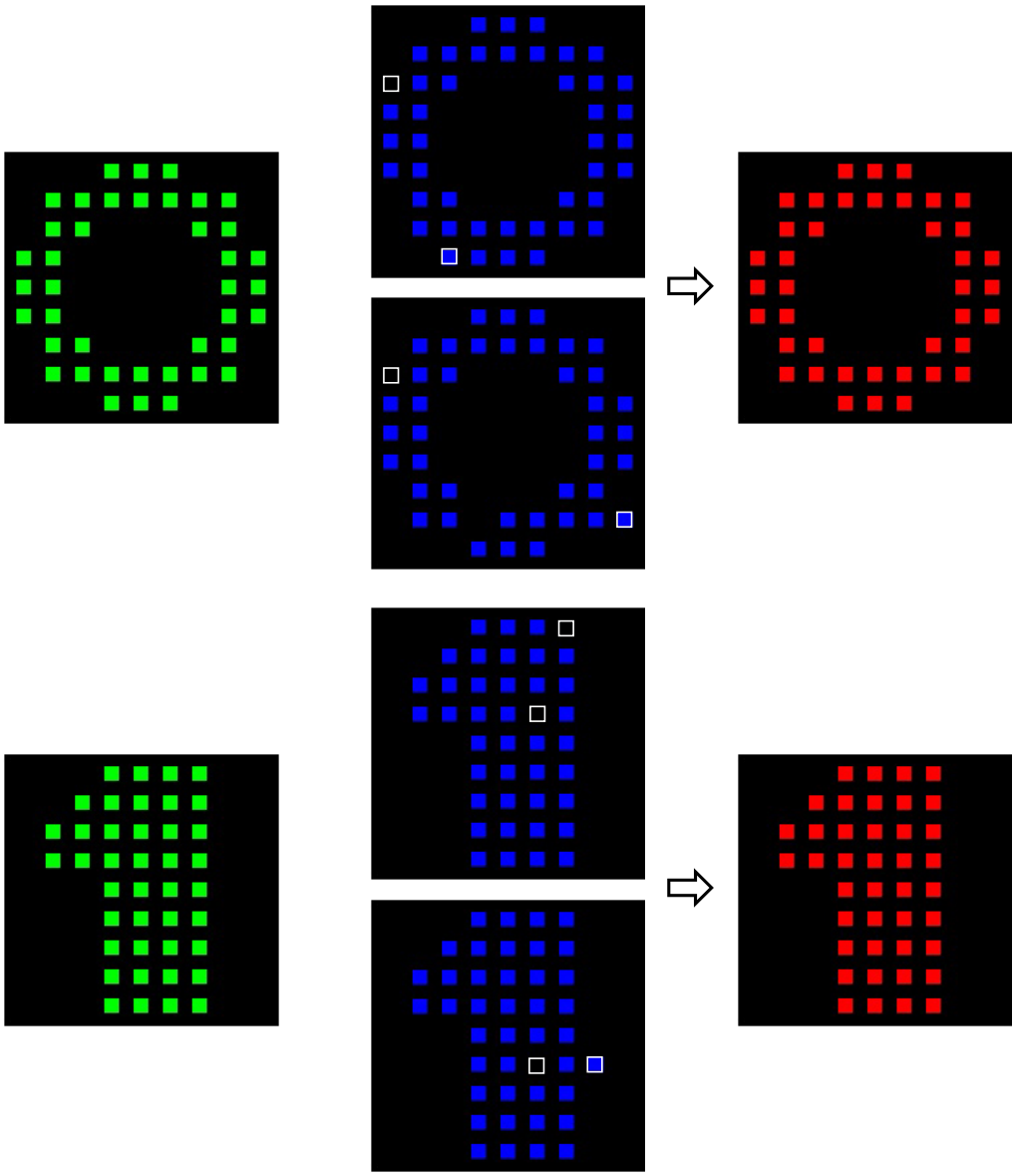

Fig. 4-4. Letter reproduction using complete matching.

patterns of numeral letters of "0" and "1" are prepared. These on-pixels, which is shown in green squares in Fig. 4-4, and off-pixels, which is shown in invisible squares in Fig. 4-4, are inputted into the neuron elements as binary states in several minutes multiple times. Next, in the recognizing stage, slightly distorted patterns of numeral letters of "0" and "1" are prepared, where the distorted pixels are indicated by white squares in Fig. 4-4. These on-pixels and off-pixels are inputted into the neuron elements in an instant. Next, revised patterns are outputted from the neuron elements immediately. As aforementioned, the electric conductance is weakened in the learning stage because the voltages are applied for a long time, whereas the electric conductance is not changed very much in the recognition stage because the voltages are applied for an instant and additionally the slightly distorted patterns are random. Finally, it is checked that the standard patterns of numeral letters of "0" and "1" are completely reproduced in the revised patterns. As shown in Fig. 4-4, it is found that the standard patterns can be reproduced in the revised patterns. This means that we have succeeded in letter reproduction. However, an issue is that the success probability is not so high, namely, the experimental result shown in Fig. 4-4 is indeed an only example. This is because the complete matching between the standard and revised patterns requires complete fabrication of all synapse elements and horizontal and vertical bar-electrodes, which is almost impossible from the viewpoint of our fabrication abilities.

Majority-rule handling is invented to solve the issue of the complete matching. Majority-rule handling is shown in Fig. 4-5. For the one-to-one handling in the complete matching, one pixel corresponds to one nexel. On the other hand, for the majority-rule handling, one pixel corresponds to multiple nexels, for example, 3 ×

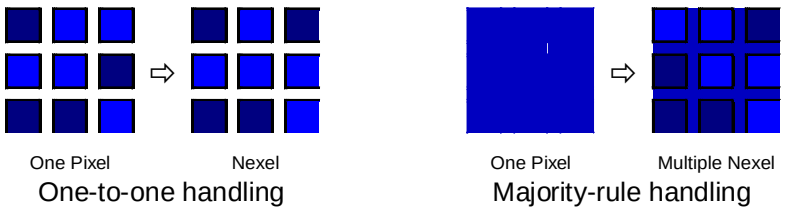

Fig. 4-5. Majority-rule handling.

3 nexels. First, when the distorted pattern is inputted, from the pixel pattern, the nexel pattern is generated. For the example of 3 × 3 nexels, in each on-pixel, five nexels are randomly selected and set to on-nexels, whereas the other nexels are set to off-nexels. On the other hand, in each off-pixel, five nexels are randomly selected and set to off-nexels, whereas the other nexels are set to on-nexels. These on-nexels and off-nexels are inputted into the neuron elements as binary states. Next, when the revised pattern is outputted, from the nexel pattern, the pixel pattern is generated. Either on-pixel or off-pixel is determined by the majority rule between on-nexels and off-nexels in the pixel. The majority-rule handling seems suitable for neural networks because it seems robust against the damage of processing elements.

An experimental result of the letter reproduction using majority-rule handling for two letters is shown in Fig. 4-6. First, in the learning stage, standard patterns of alphabet letters of "T" and "L" are prepared. Here, the majority-rule handling is not used, namely, in each on-pixel, nine nexels are set to on-nexels, and vice versa. These on-nexels and off-nexels are inputted into the neuron elements in several minutes multiple times. Next, in the recognizing stage, slightly distorted patterns of alphabet letters of "T" and "L" are prepared, where the distorted pixels are indicated by white squares in Fig. 4-6. Here, the majority-rule handling is used, namely, in each on-pixel, five nexels are randomly selected and set to on-nexels, and vice versa. These on-nexels and off-nexels are inputted into the neuron elements in an instant. Next, revised patterns are outputted from the neuron elements immediately. Here, the majority-rule handling is used again, namely, either on-pixel or off-pixel is determined by the majority rule between on-nexels and off-nexels in the pixel. Finally, it is checked that the standard patterns of alphabet letters of "T" and "L" are reproduced in the revised patterns. As shown in Fig. 4-6, it is found that the standard patterns can be reproduced in the revised patterns. This means that we have succeeded in letter reproduction using the majority-rule handling. Moreover, the success probability is high, namely, there is no failure.

Another experimental result of the letter reproduction using majority-rule

handling for three letters is shown in Fig. 4-7. The experimental method is the same as that for two letters except that alphabet letters of "T", "L", and "X" are used. As shown in Fig. 4-7, it is found that the standard patterns can be reproduced in the revised patterns also for three letters. This also means that we have succeeded in letter reproduction using the majority-rule handling.

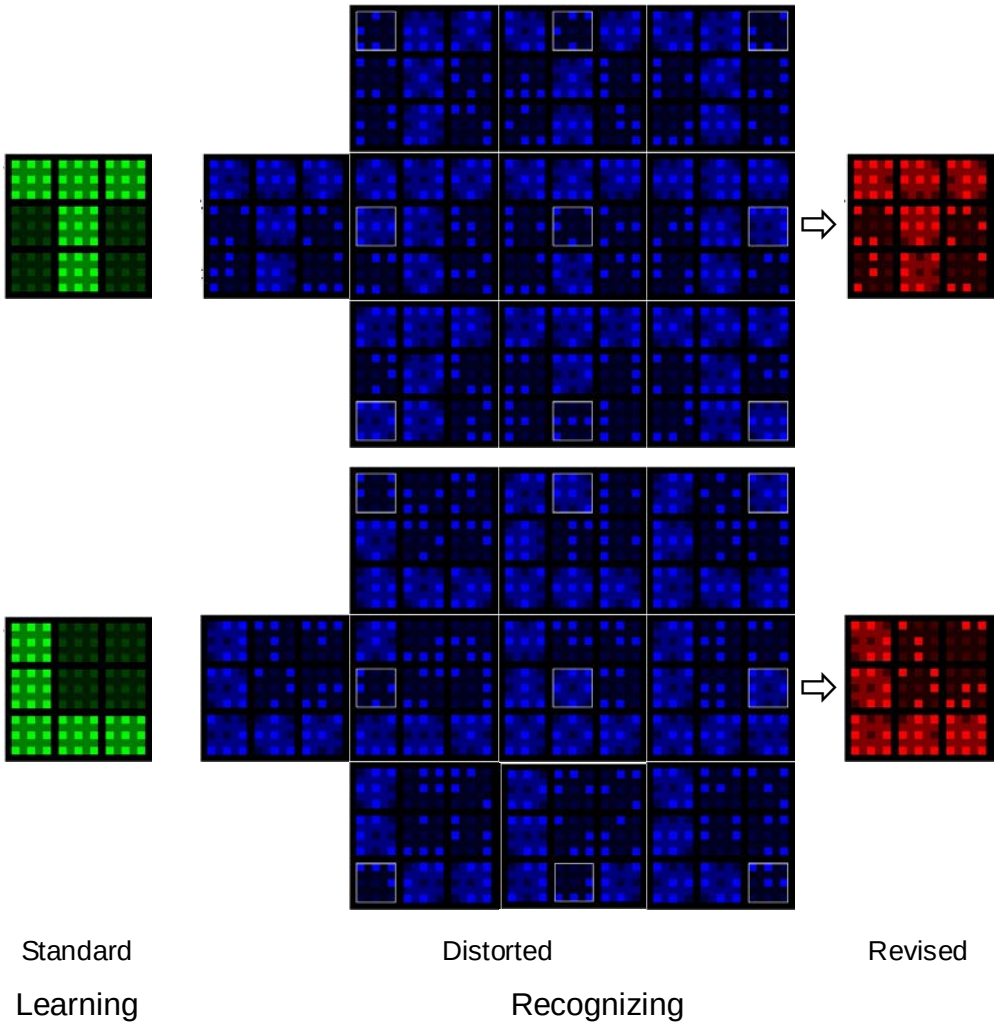

Fig. 4-6. Letter reproduction using majority-rule handling for two letters.

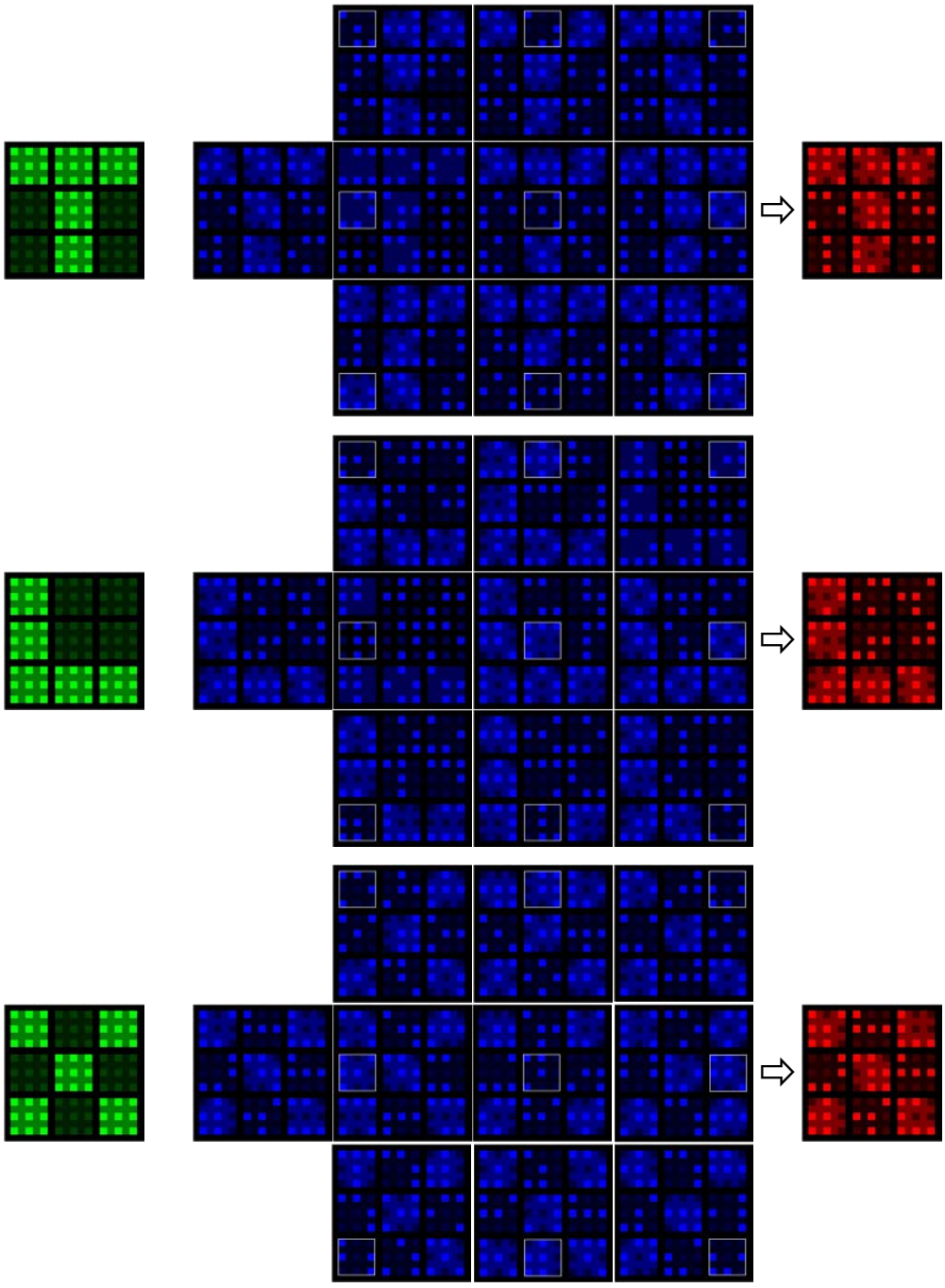

Fig. 4-7. Letter reproduction using majority-rule handling for three letters.

It is theoretically known that m = 0.14 × n [7] or m = n / 4 log n [8], where n is the number of units and m is the maximum of letters that can be learned in the Hopfield neural network. Although this Hopfield neural network is not a simple Hopfield neural network, because n = 9, number of pixel, ~ 80, number of nexel, m = 0.14 × 9 ~ 0.14 × 80 = 1.26 ~ 11.2 or m = 9 / 4 log 9 ~ 80 / 4 log 80 = 1.02 ~ 4.56. Therefore, it is good result that the standard patterns can be reproduced in the revised patterns for three letters.

4.3 Ta_2O_5 Device

Crosspoint-type Ta_2O_5 devices are used as synapse elements. An experimental result of the letter reproduction using the majority-rule handling for the two letters for the Ta_2O_5 devices is similar to that for the α-GTO devices. It is found that the standard patterns can be reproduced in the revised patterns. This means that we have succeeded in letter reproduction also for the Ta_2O_5 devices. We will submit the results to some journal soon.

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5 Cellular Neural Network

Cellular neural networks are neural networks where a neuron element is connected to only neighboring neuron elements and remarkably suitable for integration of electron devices. Because the cellular neural networks are quite different from the Hopfield neural networks, namely, a relatively larger number of the neuron elements exist, etc., it is again important to confirm the correct operations of the simplified processing elements, namely, both neuron and synapse elements, synaptic connection, and modified Hebbian learning. First, a separated architecture with the amorphous IGZO (α-IGZO) devices is evaluated, whose advantage is that either the neuron or synapse elements can be independently replaced from the viewpoint of practical use and respective evaluations. We have confirmed that the cellular neural network can learn simple logic functions. Next, a surfaced architecture with low-temperature poly-Si (LTPS) devices is evaluated, where flexible film substrate can be potentially used, which can be crumpled like brain wrinkles. We have again confirmed that the cellular neural network can learn simple logic functions. Moreover, another surfaced architecture with the LTPS devices is evaluated. We have succeeded in letter reproduction. Finally, a layered architecture with amorphous Ga-Sn-O (α-GTO) devices is evaluated, whose advantage is that a large number of processing elements can be potentially prepared and it is easy to connect them each other. We have partially succeeded in letter reproduction, although the success probability is not so high, which should be clarified in the near future.

5.1 Separated Architecture and Amorphous In-Ga-Zn-O Device

Cellular neural networks are neural networks where a neuron element is connected to only neighboring neuron elements [1-8], which are remarkably suitable for integration of electron devices. They are promising for image processing, pattern recognition, etc. As a result, in comparison with other neural networks, a relatively larger number of the neuron elements exist, and a large number of the synapse elements still exist, but connection wiring occupies little

areas or volumes. Therefore, it is again important to simplify the processing elements, namely, both neuron and synapse elements, verify the synaptic connection and modified Hebbian learning, and confirm the operations. We evaluate several architectures of cellular neural networks and thin-film devices for synapse elements

Separated architecture means that neuron elements are composed somewhere, synapse elements are separately composed elsewhere, and they are connected through peripheral wiring [9]. The advantage is that either the neuron or synapse elements can be independently replaced from the viewpoint of practical use and respective evaluations. Here, α-IGZO devices are used as the synapse elements.

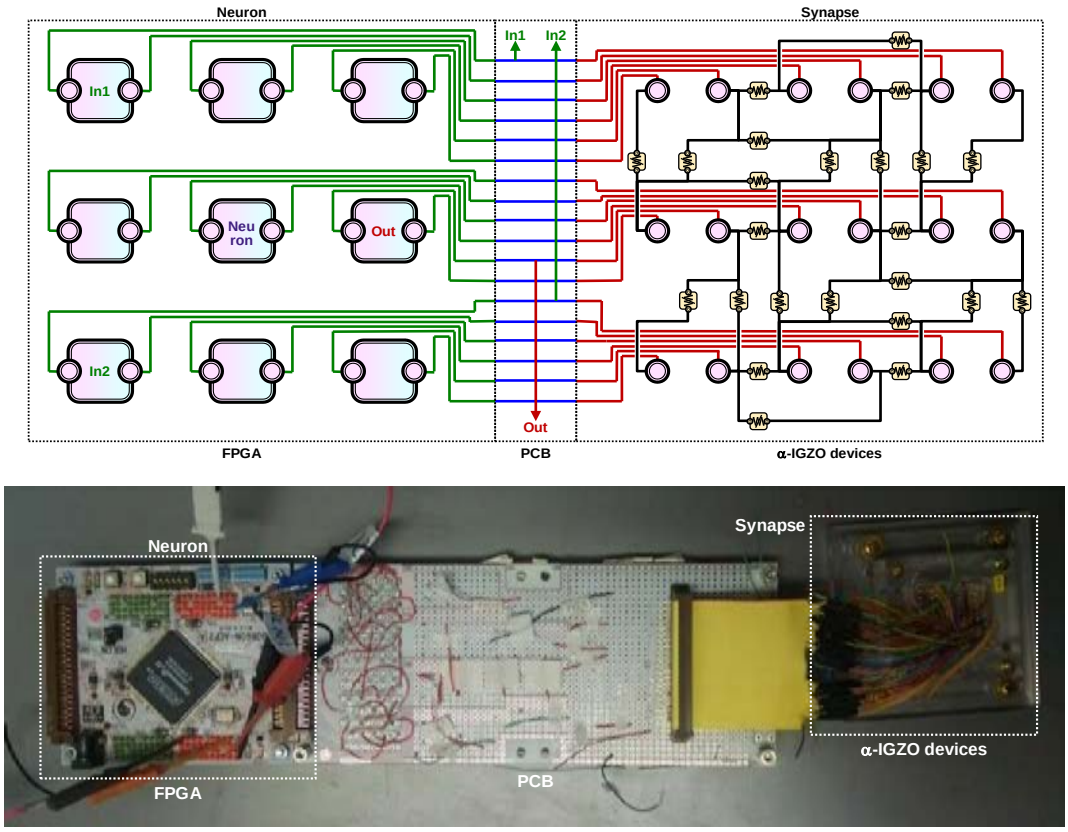

Fig. 5-1. Separated architecture with the α-IGZO devices.

A separated architecture with the α-IGZO devices is shown in Fig. 5-1. Here, the neuron elements are the abovementioned 2-inverter 2-switch circuits, which are composed in a field-programmable gate array (FPGA), Cyclone II FPGA supplied

from Altera and designed by hardware description language (HDL) [10], and they can be easily formed because they are general digital circuits. 3 × 3 neuron elements are formed because we believe that this is the minimum number for the simple logic learning explained later and it is also important to evaluate how small neural network can get the required functions. The synapse elements are planar-type α-IGZO devices. The neuron and synapse elements are properly connected through a printed circuit board (PCB), and a cellular neural network with four-direction topology and tug-of-war method is realized. Moreover, modified Hebbian learning is used by utilizing the conductance decrease of the planar-type α-IGZO devices.

We teach simple logic functions, such as, AND and OR, to the cellular neural network. First, we assign In1, In2, and Out as shown in Fig. 5-1. Next, we apply combinations of high voltage (H), namely, 3.3 V, and low voltage (L), namely, GND, to In1 and In2 and corresponding voltage to Out. As a result, the continuous change of the electric conductance occurs in each α-IGZO device. Finally, we apply the combinations of the voltages to only In1 and In2 and check the voltage at Out. Similar to the Hopfield neural network, the electric conductance is weakened in the learning stage because the voltages are applied for a long time, whereas the electric conductance is not changed very much in the recognition stage because the voltages are applied for an instant.

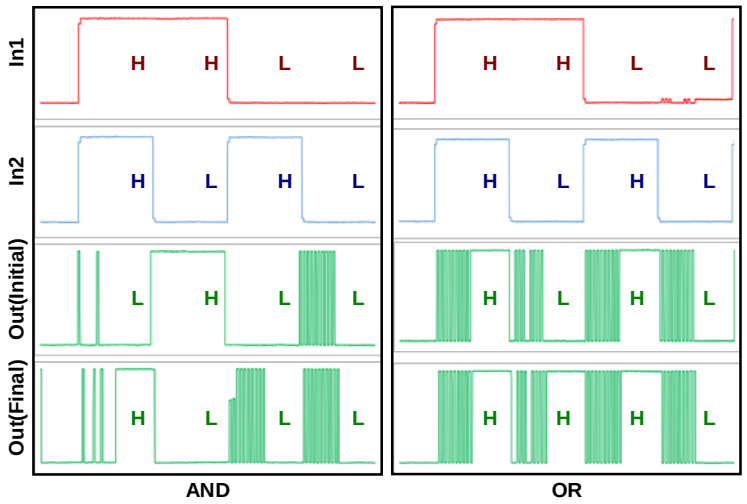

Fig. 5-2. Logic learning by the separated architecture with the α-IGZO devices.

The logic learning by the separated architecture with the α-IGZO devices is shown in Fig. 5-2. Because the fine oscillations are noises from the switching pulses to the switches, ignore them. It is found that although Out is initially not correct before the learning, Out becomes finally correct after the learning for both AND and OR. A problem is that it takes as long as one hour for the learning. We expect that this problem can be solved by optimizing the electrical characteristic of the α-IGZO devices and speeding up the conductance decrease. In any case, this means that we have confirmed that the cellular neural network can learn simple logic functions.

5.2 Surfaced Architecture and Low-Temperature poly-Si Device

Surfaced architecture means that all processing elements are composed and connected on flat surfaces [11,12]. Although rigid glass substrates are used in this study, flexible film substrate can be potentially used, which can be crumpled like brain wrinkles. Here, LTPS devices are used as the processing elements, namely, both neuron and synapse elements.

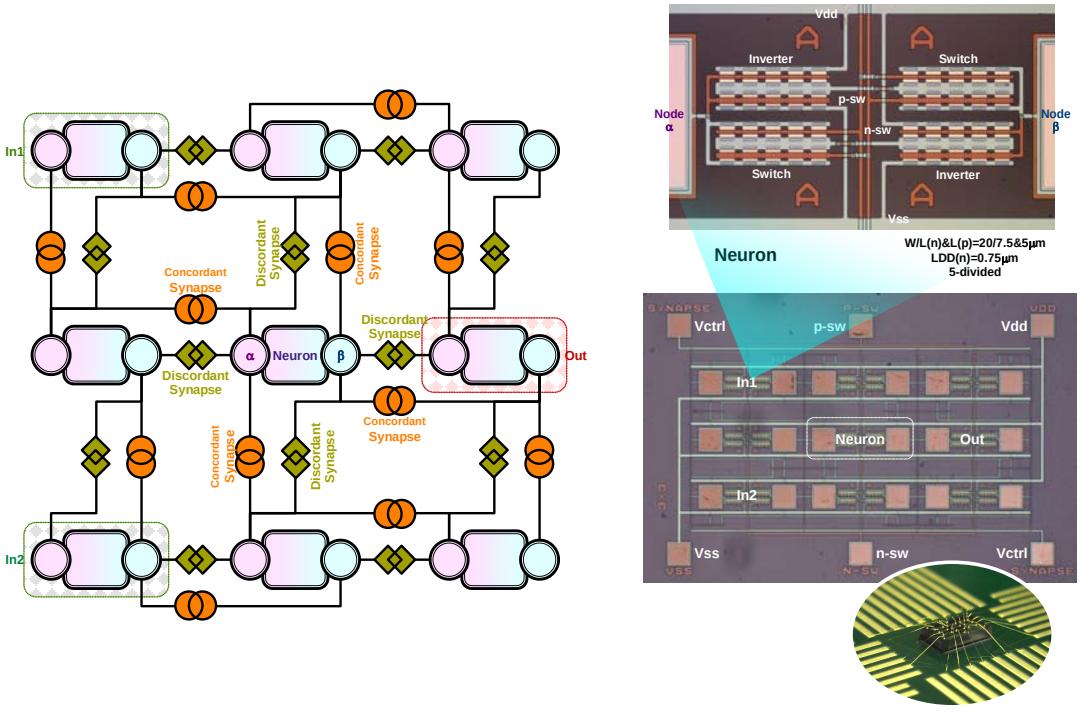

Fig. 5-3. Surfaced architecture with the LTPS devices.

A surfaced architecture with the LTPS devices is shown in Fig. 5-3. Here, the neuron elements are the abovementioned 2-inverter 2-switch circuits, which are composed by LTPS thin-film transistors (TFTs) [13-15], where the field effect mobility (μ) and threshold voltage (V_{th}) of the n-type transistors are 93 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and 3.6 V while those of the p-type transistors are 47 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and -2.9 V respectively, and they can be easily formed because they are general digital circuits. 3 × 3 neuron elements are formed. The synapse elements are transistor-type LTPS devices. The neuron and synapse elements are simultaneously fabricated on a flat surface, and a cellular neural network with four-direction topology and tug-of-war method is realized. Moreover, modified Hebbian learning is used by utilizing the conductance decrease of the transistor-type LTPS devices.

We teach simple logic functions, such as, AND, OR, and XOR, to the cellular neural network. The teaching sequence is the same as that for the separated architecture with the α-IGZO devices except that the driving voltages are ±5 V, the switching pulses are ±10 V, the control voltages to control the degradation characteristics are 15 and 10 V for the learning and recognizing stages, respectively, and the logic voltages are ±5 V for the H and L, respectively.

The logic learning by the surfaced architecture with the LTPS devices is shown in Fig. 5-4. It is found that although Out is initially not correct before the learning, Out becomes finally correct after the learning for all AND, OR, and XOR. This

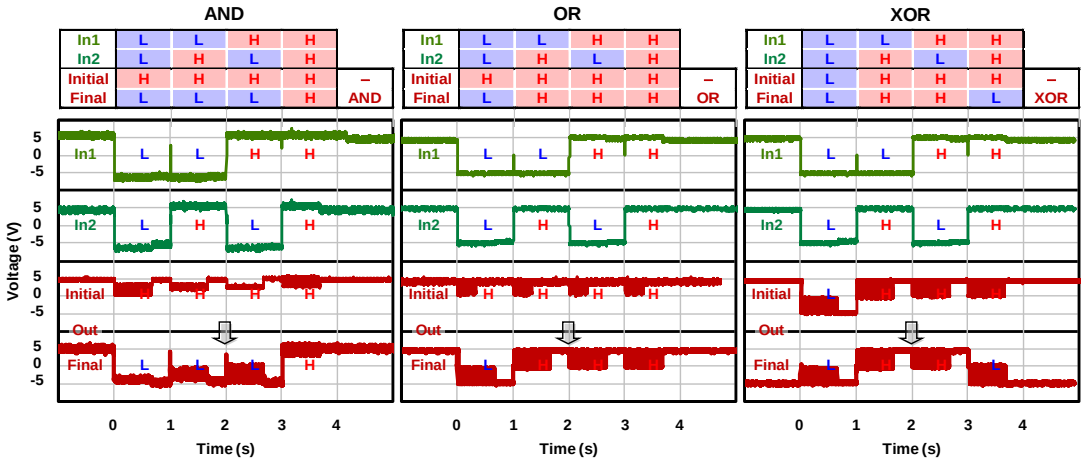

Fig. 5-4. Logic learning by the surfaced architecture with the LTPS devices.

means that we have confirmed that the cellular neural network can learn simple logic functions.

Another surfaced architecture with the LTPS devices is shown in Fig. 5-5 [16,17]. Here, an only difference is that 3 × 3 neuron elements are formed in Fig. 5-3, whereas 7 × 7 neuron elements and corresponding synapse elements are formed in Fig. 5-5.

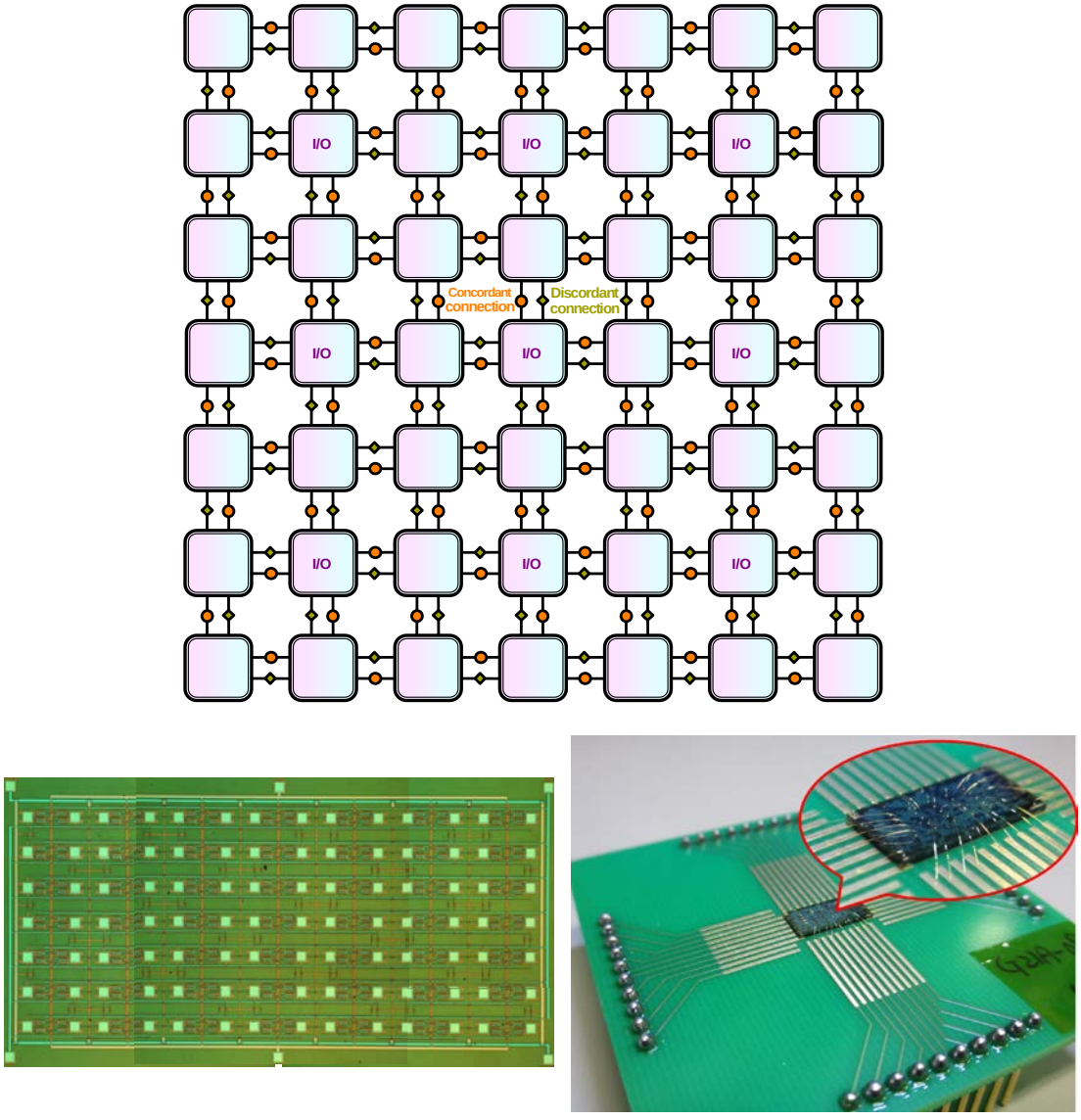

Fig. 5-5. Another surfaced architecture with the LTPS devices.

We teach letter recognition to the cellular neural network. The teaching sequence is similar to that for the Hopfield neural networks. We assign input and output (I/O) neuron elements as shown in Fig. 5-5. The cellular neural network has 7 × 7 neuron elements, including 3 × 3 I/O neuron elements, to which the standard patterns are inputted and from which the revised patterns are outputted, and hidden neuron elements between them. The driving voltages are ±8 V, and the control voltages are 15 and 10 V for the learning and recognizing stages, respectively. First, in the learning stage, standard patterns of alphabet letters of "T" and "L" are inputted into the I/O neuron elements. A steady pattern of the binary states is generated in the hidden neuron elements based on the normal theory of the dynamics of the neural network. After that, the synaptic connection strengths are changed, obeying modified Hebbian learning. Next, in the recognizing stage, slightly distorted patterns of alphabet letters of "T" and "L" are inputted into the I/O neuron elements and immediately released. Next, revised patterns are automatically outputted from the I/O neuron elements. Finally, it is checked the standard patterns of alphabet letters of "T" and "L" are reproduced in the revised patterns.

The letter recognition by the surfaced architecture with the LTPS devices is shown in Fig. 5-6. Only the standard, distorted, and revised patterns in the I/O neuron elements are shown, although steady patterns in the hidden neuron elements are between them. It is found that the standard patterns can be reproduced in the revised patterns. This means that we have succeeded in letter reproduction.

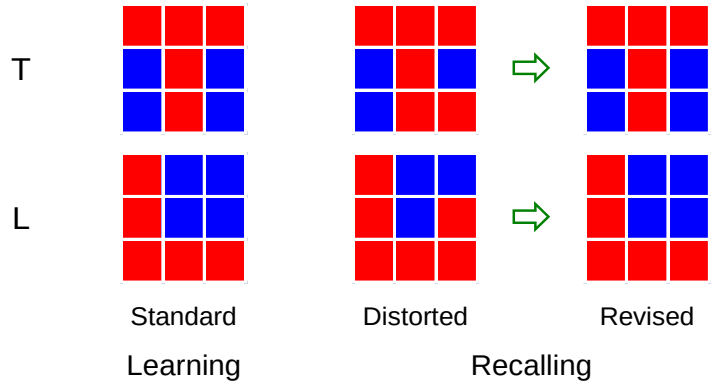

Fig. 5-6. Letter recognition by the surfaced architecture with the LTPS devices.

5.3 Layered Architecture and Amorphous In-Ga-Zn-O Device

Layered architecture means that processing elements are composed in three-dimensional layered structure [18-21]. The advantage is that a large number

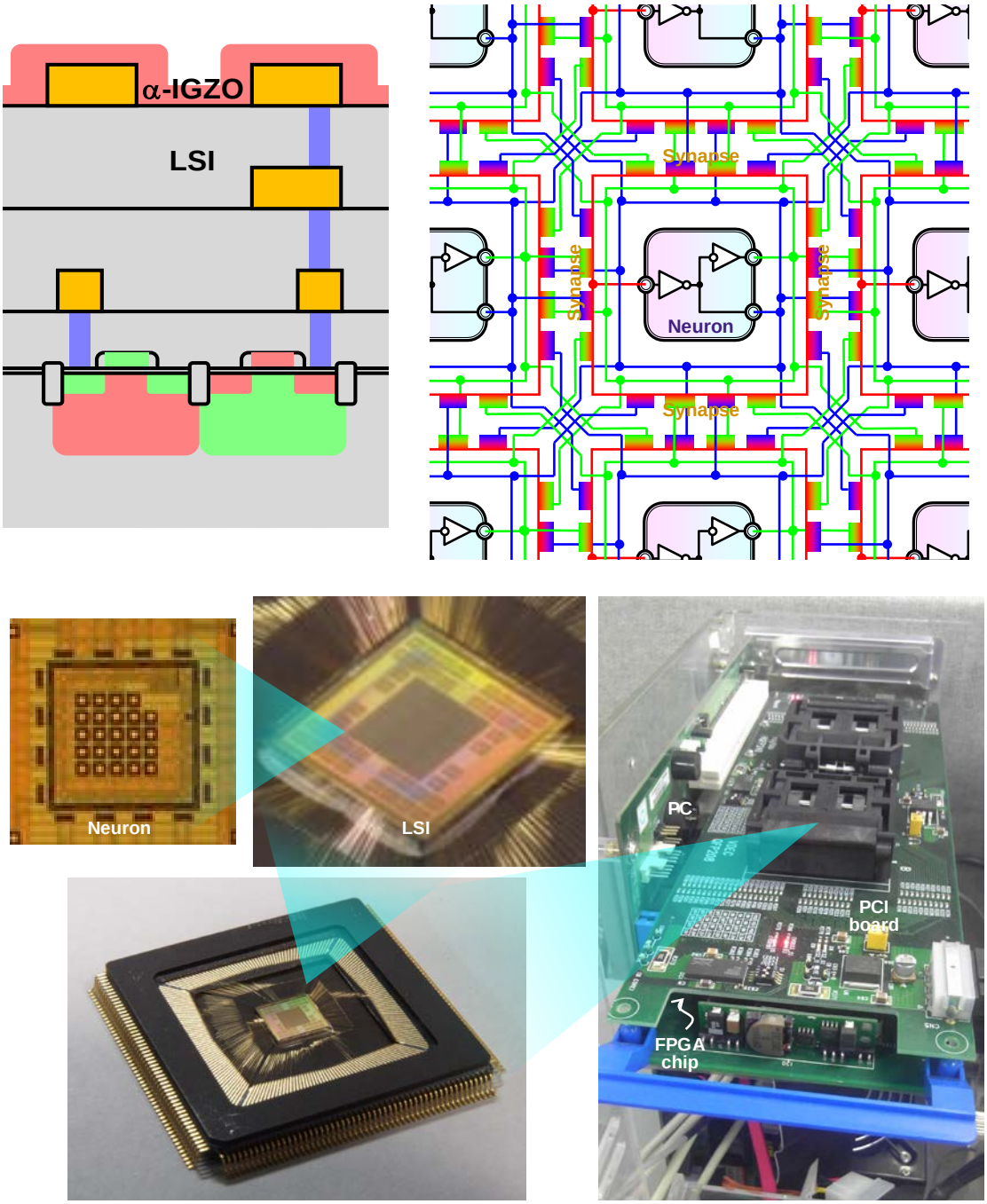

Fig. 5-7. Layered architecture with the α-IGZO devices.

of processing elements can be potentially prepared and it is easy to connect them each other, which is an essence of neuromorphic systems. Here, a large scale integration（LSI) chip is used as the neuron elements, whereas α-IGZO devices are deposited on the LSI chip and used as the synapse elements. Although this layered architecture has only two layers, it is potentially practicable that it has more layers by repeating the deposition of the thin-film devices.

A layered architecture with the α-IGZO devices is shown in Fig. 5-7. Here, the neuron elements are the abovementioned 2-inverter circuits, which are

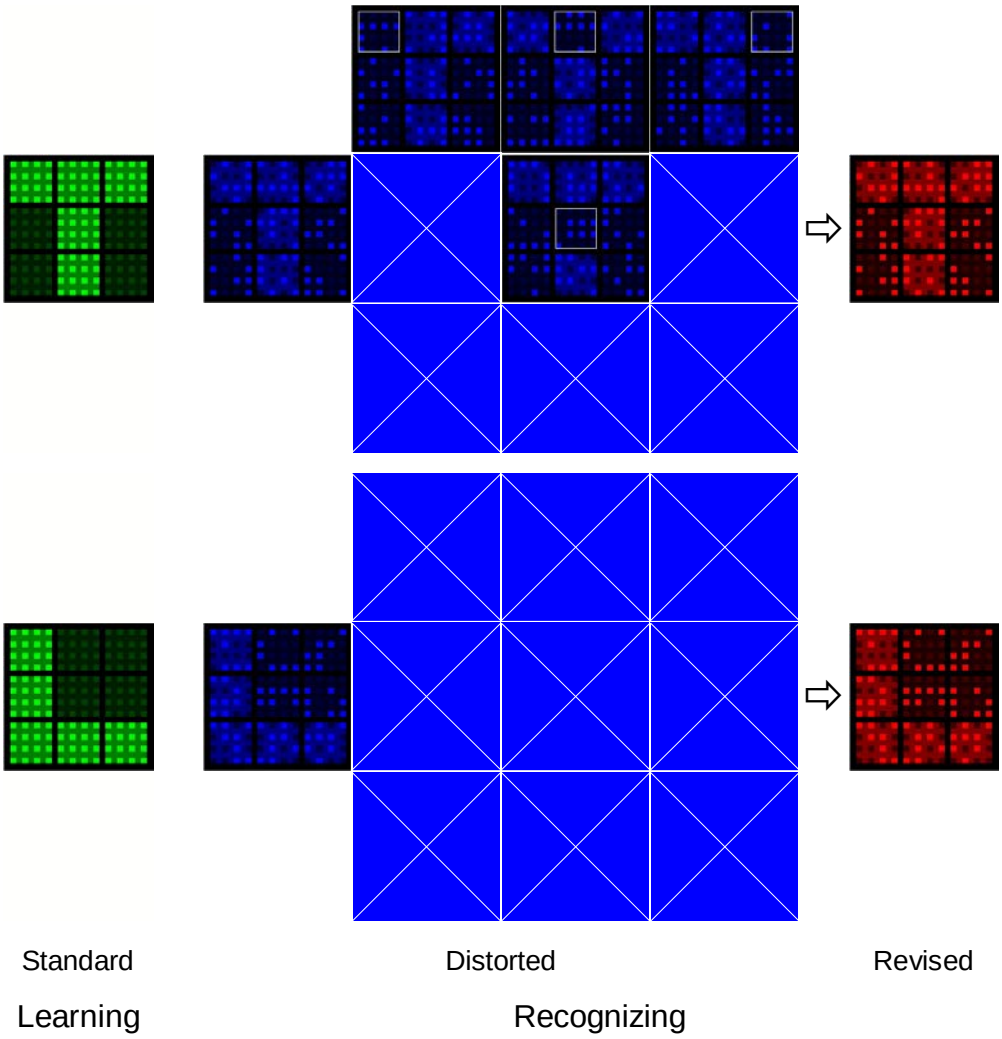

Fig. 5-8. Letter reproduction by the layered architecture with the α-IGZO devices.

manufactured by VLSI Design and Education Center (VDEC) [22], and they can be asily formed because they are general digital circuits. The synapse elements are planar-type α-IGZO devices, which are directly deposited on the LSI chip using radio-frequency (RF) magnetron sputtering. A cellular neural network with eight-direction topology and tug-of-war method is realized. Moreover, modified Hebbian learning is used by utilizing the conductance decrease of the planar-type α-IGZO devices. The total system is controlled using a personal computer (PC), peripheral component interconnect (PCI) board, and FPGA chip using hardware description language (HDL).

We teach letter recognition to the cellular neural network. The teaching sequence is similar to that for the surfaced architecture with the LTPS devices. The cellular neural network has 25 × 25 neuron elements, including 12 × 12 I/O neuron elements and hidden neuron elements between them. The majority-rule handling is similar to that for the Hopfield neural networks, namely, one pixel corresponds to 4 × 4 nexels.

The letter recognition by the layered architecture with the α-IGZO devices is shown in Fig. 5-8. It is found that the standard patterns can be reproduced in the revised patterns for some distorted patterns, although the success probability is not so high, which should be clarified in the near future.

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6 Conclusion

6.1 Conclusion

Artificial intelligences have been used for various applications and are promising in future societies, and neural networks are representative technologies. However, because the conventional ones are software on hardware, the size is bulky, and the power is huge. Neuromorphic systems are biomimetic systems from hardware level and have the same advantages as living brains, especially, compact size, low power, and robust operation. On the other hand, thin-film semiconductor electronic devices can be fabricated on large areas, and three-dimensional layered structure can be acquired.

In this doctoral dissertation, we studied neuromorphic systems using thin-film devices. First, we investigated a neuromorphic system, where we simplified a neuron element to three simple circuits and synapse element to one variable resistor or capacitor, and proposed tug-of-war method and modified Hebbian learning, whose advantage is that the synaptic connection strength is automatically controlled using the local electrical conditions. By using such processing elements and learning method in neuromorphic systems, it is expected that the size can be further compact, power can be low, and the operation can be robust. Next, we examined low-temperature poly-Si (LTPS) device, amorphous In-Ga-Zn-O (α-IGZO) device, and amorphous Ga-Sn-O (α-GTO) device, where, it was confirmed that the electrical conductance gradually decreases when electric current flows, which is available as a synaptic connection strength. By using such thin-film devices in neuromorphic systems, it is expected that the size can be further compact. Finally, we investigated Hopfield neural networks using crosspoint-type devices and cellular neural networks using separated architecture, surfaced architecture, layered architecture, and planar-type devices and confirmed the correct operations of simple logic learning and letter reproduction. It is believed that these results will be theoretical bases to realize ultra-large scale integration for neuromorphic systems.

6.2 Adaptation

In this doctoral dissertation, we confirmed the correct operations using Hopfield neural networks and cellular neural networks, which are historical and typical neural networks described in all text books and have contrastive properties, as abovementioned. According to the technological history of neural networks, individual parts can be implemented to new parts and the peculiar functions of the new parts can be obtained as they are. Therefore, it is expected that this study can be adapted to the advanced technologies, such as, multi-layer perceptrons [1], recurrent neural network [2], convolutional neural networks [3], auto-encoders [4], reservoir neural networks [5], spiking neural networks [6], chaotic neural networks [7], etc., except the Hebbian learning, which should be considered to be adapted for each case. Unfortunately, this study cannot be adopted to deep learning [8] as it is, because the layer re-construction is difficult for neuromorphic systems from hardware level, but it might be possible by revising three-dimensional layered structure. Moreover, this study can be adapted to analog output by outputting direct outputs from synapse connections and rectified linear units (ReLU) [9] by exchanging neuron elements.

6.3 Future

Neuromorphic systems using thin-film devices have great potentials that the size can be compact, the power can be low, and the operation can be robust [10-12]. Comparison of the hardware size and power consumption between a human brain and various neural networks is shown in Fig. 6-1. Rough estimations for this study in the future are listed. (This comparison is slightly unfair because current abilities of the conventional ones and future abilities of this study are listed.) It is again confirmed that neuromorphic systems using thin-film devices have great potentials that the size can be compact, the power can be low. As a result, the following contributions are promising in the future.

		Human Brain	Soft on Hard (Watson)	Conventional Neuromorphic (True North)	This study (R-type) in future	This study (C-type) in future
Element (Number in Unit)	Neuron	2×10^{10}	1.5×10^{13} (Memory)	1×10^{6}	2×10^{10}	2×10^{10}
	Synapse	2×10^{14}		3×10^{8}	2×10^{14}	2×10^{14}
Size (Assumption of Brain)		1.5 ℓ	10 Refrigerators	2×10^{4} CPUs	1 ℓ	0.2 ℓ
Power (Assumption of Brain)		20 W	85 kW	6 kW	30 W	20 W

Fig. 6-1. Comparison of size and power between a brain and various neural networks.

First, energy crisis can be avoided. If no effective countermeasure is done, it is forecasted that artificial intelligences will consumes 60 % of worldwide electricity in 2050. The future possibilities of the power in a neuromorphic system can be forecasted as follows. If variable capacitors are used as synapse elements, the electric capacitance is 10 fF, operation voltage is 0.1 V, and an average value of the operation frequency is 1 kHz, the dynamic current can be calculated by 10 fF × 0.1 V × 1 kHz = 10^{-12} A, and the power in a synapse element can be calculated by 0.1 V × 10^{-12} A = 10^{-13} W. If the number of the synapse elements is 2 × 10^{14}, which is the number of the synapse elements in a human brain, the power can be calculated by 10^{-13} W × 2 × 10^{14} = 20 W, which is similar to that in a human brain and 1 / 5,000 of that in Watson, as shown in Fig. 6-1.

Next, artificial intelligence on everything (AIoE) may be realized, which is an extended version of internet of things (IoT). AIoE makes everything intelligent, and telecommunication is conducted only if necessary, which avoid information explosion. The future possibilities of the size of a neuromorphic system can be forecasted as follows. If the device size of the synapse element is 1 μm^3 and the number of the synapse elements is 2 × 10^{14}, the system size can be calculated by 1 μm^3 × 2 × 10^{14} = 0.2 ℓ, which is 1 / 10 of that of a human brain, as shown in Fig. 6-1. Namely the same function can be realized with more compact size using neuromorphic systems than living brains.

Finally, neuromorphic systems might be equipped in robot brains with common artificial intelligences. Although mobile robots cannot carry heavy and high-power super computers, even if internet networks are disconnected, they have to work by

themselves. Therefore, it seems better that elementary functions are executed in the neuromorphic systems and advanced functions are executed through the internet networks, which is hybrid systems of the neuromorphic system and common artificial intelligences. It is also useful that the operation can be robust.

Although we have not yet succeeded in integration of an astronomical number of processing elements with three-dimensional layered structure, the research results suggest that it is possible in the future.

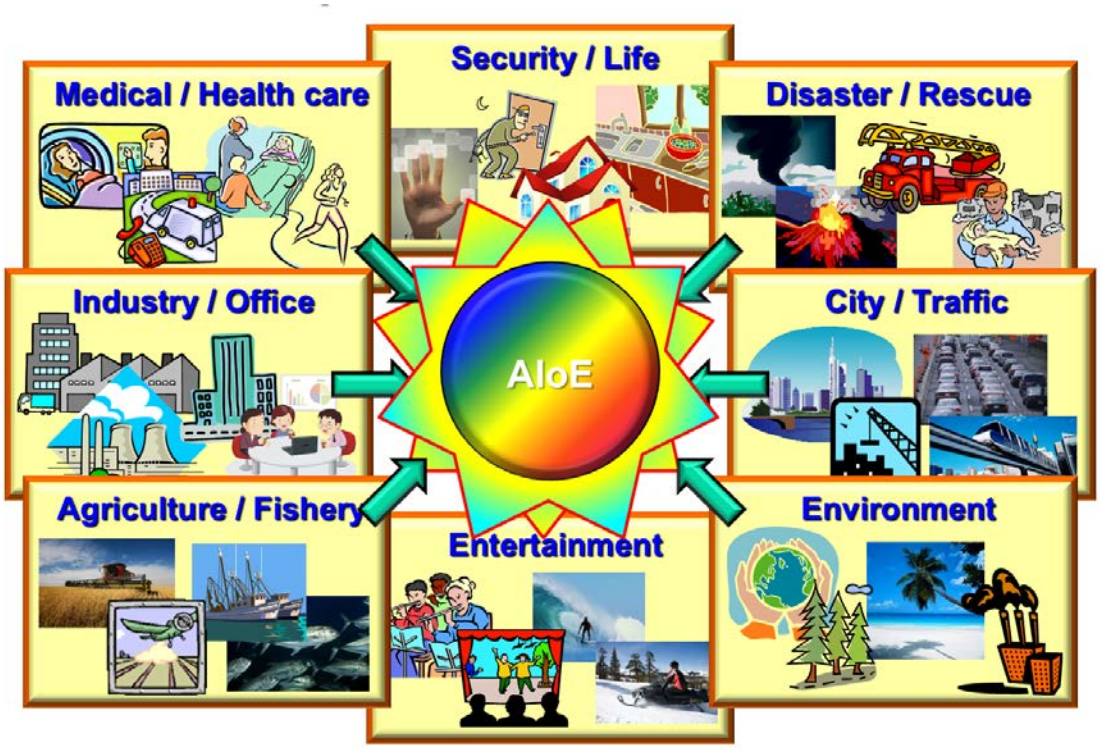

Fig. 6-2. Artificial intelligence on everything.

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