Crystalline silicon growth at low-temperature and its application to thin-film transistors and related devices

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Abstract

In the large-area electronics, such as active-matrix displays, printer heads, and image sensors, poly-Si based thin-film transistors (poly-Si TFTs) are indispensable to drive those functions.

In this thesis, the low-temperature growth techniques for crystalline silicon were studied in three different ways under gas, solid and liquid phase first. As the gas phase deposition method, epitaxial growth conditions were studied by employing hydrogen-radical enhanced chemical-vapor-deposition (HR-CVD). Supply of a large amount of atomic hydrogen to the growth surface certainly promotes two-dimensional crystalline growth at low-temperature around 350 °C even though increasing both thickness to be more than 1 μm and doping concentration. Electron Hall mobility of the epitaxially grown films was reached to be 115 cm^2/Vsec. Those results showed the potential of crystalline silicon growth even at low-temperature. As the solid phase crystallization, a grain boundary filtration technique was proposed and demonstrated with Ge films. Single large grain Ge films to be larger than 100 μm^2 were fabricated on amorphous substrates by using together selective nucleation and lateral solid-phase-epitaxy. In the case of Si, grain boundary filtration through the planer constrictions was not enough even though more than several micrometers of grain growth were successfully demonstrated, and its possible reasons were discussed. As the liquid phase crystallization, excimer laser crystallization was studied. The number of laser shots contributed to reduction of defects in grains/grain boundaries, differing from that the irradiation energy directly contributed to variations in grain-size. And also he found out that the maximum cooling rate must be maintained at less than 1.6×10^{10} °C/sec to avoid micro-crystallization.

Then, the excimer laser crystallization was chosen to fabricate poly-Si TFTs and was investigated details how should be applied for practical devices. Some attempts were studied to improve uniformity, to reduce photo-leakage current and to maintain stable performance, and some devices were demonstrated. Finally, an apparatus was developed to obtain location controlled large-grain Si films. By using the apparatus, lateral growth length up to 2.8 μm with single laser shot were demonstrated. The field effect mobility of 270 cm^2/Vsec for n-channel TFT and 230 cm^2/Vsec for p-channel TFT were demonstrated at predetermined positions by employing those films.

This series of study has contributed to develop the large-area electronics practically and resulted in generating the new industry based on poly-Si TFTs. Also it will be useful for further development of the large-area electronics devices.

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1. Introduction

The origin of current microelectronics devices widely used in the world goes back to the discovery of the transistor effect [1] as embodied in the point-contact transistor in 1948. Followed by, for example, the development for MOS (Metal-oxide semiconductor)-FETs (Field-effect transistors) [2] in 1960, the silicon-based large-scaled integrated-circuits (Si-LSIs) technology[3)4)], one of the most important stream to create current IT industry, was dramatically progressed. As well-known as Moore's law [5], history of the microelectronics devices has driven transistor feature size scaling from 10 μm to 10 nm on single-crystalline silicon substrate during the past 50 years [6].

The discovery of the transistor effect has also contributed to the "large-area electronics" that forms electronics devices with fine structures on a large-area substrate such as a glass substrate. They are applied to image input/output (I/O) devices, such as active-matrix information displays [7-12], printer heads [13] and image sensors [14-24]. In the large-area electronics, thin-film transistors (TFTs) have an important role to drive those I/O functions on such a large-area substrate. Those I/O applications have been developed since the 1960s, started for practical applications in the 1980s, and spread widely in the 1990s. In contrast to the microelectronics devices, history of the large-area microelectronics devices has driven size of glass substrate up-scaling from 300 × 300 mm to 3 × 3 m during the past 30 years [25].

This chapter provides overviews of previous research, the I/O devices and their functions (1.1), the TFTs to drive those I/O devices (1.2), and crystalline silicon films to be employed in TFTs as active layers (1.3). Then, the purpose of this thesis is described (1.4).

1.1 Target applications and technology trends

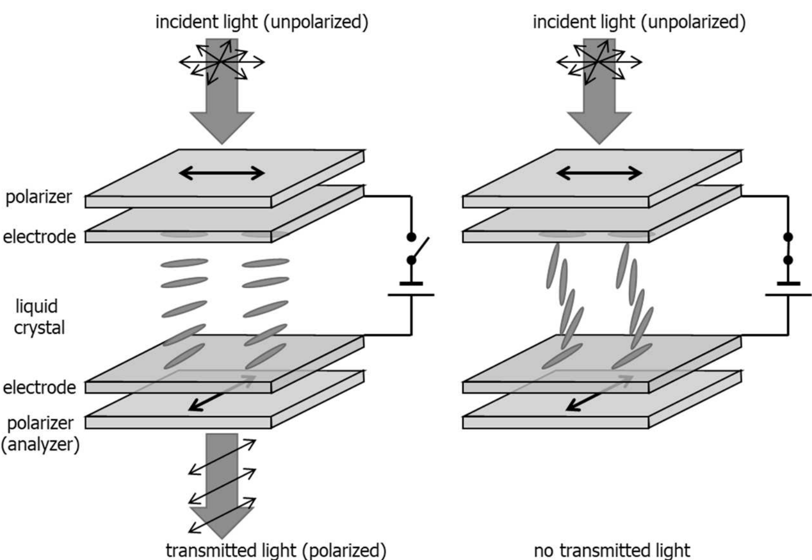
1.1.1 Active-matrix liquid crystal displays (AM-LCDs)

Information displays are the one of indispensable devices as an image output interface in this age of the information technology (IT). For example, large screen displays with more than 50-inch diagonal are widely used as television monitors. High resolution displays with more than 400 ppi (pixels per inch) are also commonly installed in smartphones. Today, there are two main technologies, liquid crystal and organic light-emitting diode, to reproduce images on those screens.

The information display devices have their origin gone more back to than that of the transistors described above. Since cathode-ray tube was embodied by Braun in 1897

[26], the cathode-ray tube had been dominant for information display devices, such as TVs and monitors for computers until the appearance of liquid-crystal displays [8)12)] in 1980's. There has been a long history also in liquid crystal technologies. In 1888, Reinitzer discovered a strange behavior of what would later be called liquid crystals [27]. However, it seemed to be very far from the practical use in those days. Eighty years later, the first research activities that contributed to the current AMLCD technology was the discovery of dynamic-scattering mode [28] by Heilmeier et al. in 1968, followed by the discovery of twisted-nematic (TN) mode [29] by Shadt and Helfrich in 1971.

In the typical TN mode cell, the liquid crystal is confined between two-crossed polarizers and its birefringence controlled by an electric field applied between two electrodes. It is designed that the nematic director undergoes a smooth 90° twist within the cell in the absence of an electric field. As shown in Figure 1.1 (a), unpolarized light enters the first polarizer and the twisted arrangement of the LC molecules then acts as an optical wave guide and rotates the plane of polarization by 90° turn so that the light which reaches the second polarizer can pass through it. When a voltage is applied to the electrodes, the light cannot pass through it because the liquid crystal molecules tend to align with the electric field E as shown Figure 1.1 (b) and the optical wave guiding property is lost.



(a) transparent state with no electric field. (b) dark state with electric field.

Figure 1.1 Typical TN mode cell.

Then, in 1980's, the liquid crystal related technologies remarkably progressed with development of thin-film transistor technologies employed silicon based active

layers. For example, Suwa Seikosya released a product of 2" color liquid crystal TV [8] in 1984 and Sharp shipped 14" LCD product [12] in 1988.

At this moment of 2020's we know that the TN mode liquid crystal technologies [29] combined with a-Si:H TFT [30] had created the first stage of LCD industry. They were applied to laptop style personal computers (PCs) and also assisted to create a new product category for mobile computers, such as current notebook-PC. Followed by the development for wide viewing-angle mode LC technologies, for example In-Plain Switching (IPS) mode in 1992 [30], the LCD became popular widely in not only the medium-size markets, such as the notebook-PC described above, but also both large and small-size displays markets that is represented by TVs and smartphone. Especially in the small-size displays, low-temperature poly-Si TFTs, so called LTPS [32], has been playing an important role t to expand the market of high resolution displays since the joint venture from Sony and Sanyo shipped the first LCD product in 1996 [33]. It has also contributed to create a new market for OLED described below.

1.1.2 Active-matrix organic light-emitting diode displays (AM-OLEDs)

Another display technology is organic light-emitting diode display (OLED). In 1953, Bernanose and Vouaux first observed electroluminescence in organic materials [34]. Ten years later, Pope et al. observed direct current (DC) electroluminescence under vacuum on a pure single crystal of anthracene [35]. However, it required more than 400 V. After a quarter century from Pope's report, Tang and VanSlyke successfully demonstrated high-efficiency light emission [36].

Figure 1.2 shows the double-layer type EL devices introduced by Tang and VanSlyke. They used a diamine derivative as a hole transport layer for hole injection from the anode into the emitting layer of aluminum complex and demonstrated the structure significantly improves the emission efficiency. It was considered that the hole transport layer plays an important role in transporting holes and blocking electrons. This demonstration inspired a study of the three-layer structure consisting of a hole transport layer, an emitting layer and an electron transport layer, and following many investigations for multilayer structure currently used in popular.

Other numerous important studies continued in the last ten years since Tang's report. In terms of luminous efficiency[37], the concept of charge balance [38] and the phosphorescent materials [39] were proposed and demonstrated. Then, it was in 2000's for OLED to be really practical used. The joint venture from Sanyo and Kodak shipped 2.16" OLED product in 2003 [40].

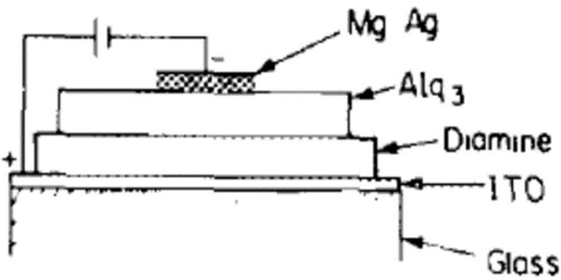


Figure 1.2 the double-layer type EL devices introduced by Tang and VanSlyke [36].

1.1.3 1D and 2D image sensors

Besides the use as an active layer in TFTs, a-Si:H films were expected for use in photoelectric conversion functions, such as solar cells and photo sensor. Photoconductive effect of a-Si:H was discovered by Chittick et al. in 1969 [41]. In 1975 and 1976, Spear et al. reported that the electrical properties of a-Si:H can be controlled by substitutional doping [42] and that p-n junctions [43] can be formed in a-Si:H. Carlson demonstrated a-Si:H solar cells with p-i-n structures in 1976 [44]. Then, in 1980's, much effort had been devoted to develop photo-sensors and photo-diodes employed a-Si:H films.

One of advantages of a-Si:H was that photo response-time was shorter than that of cadmium sulfide (CdS) based photo-sensors already developed in those days [17]. Figure 1.3 shows a structure of a-Si:H photo-sensor. In that figure, Al was selected as the lower electrode because of its better blocking characteristics than those of Cr-Au and Ni. There had been a lot of investigations for diode structures to reduce the dark current further, a-Si:H pin-diode structure became dominant in later [45].

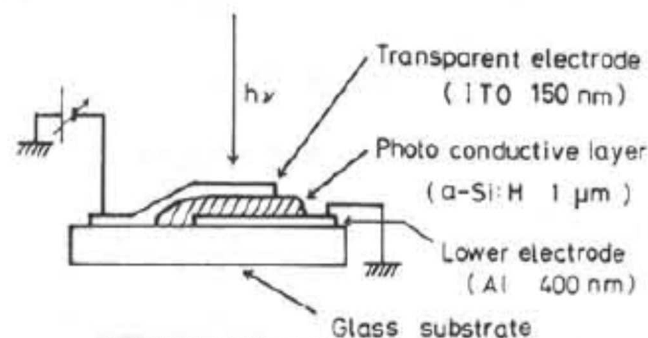
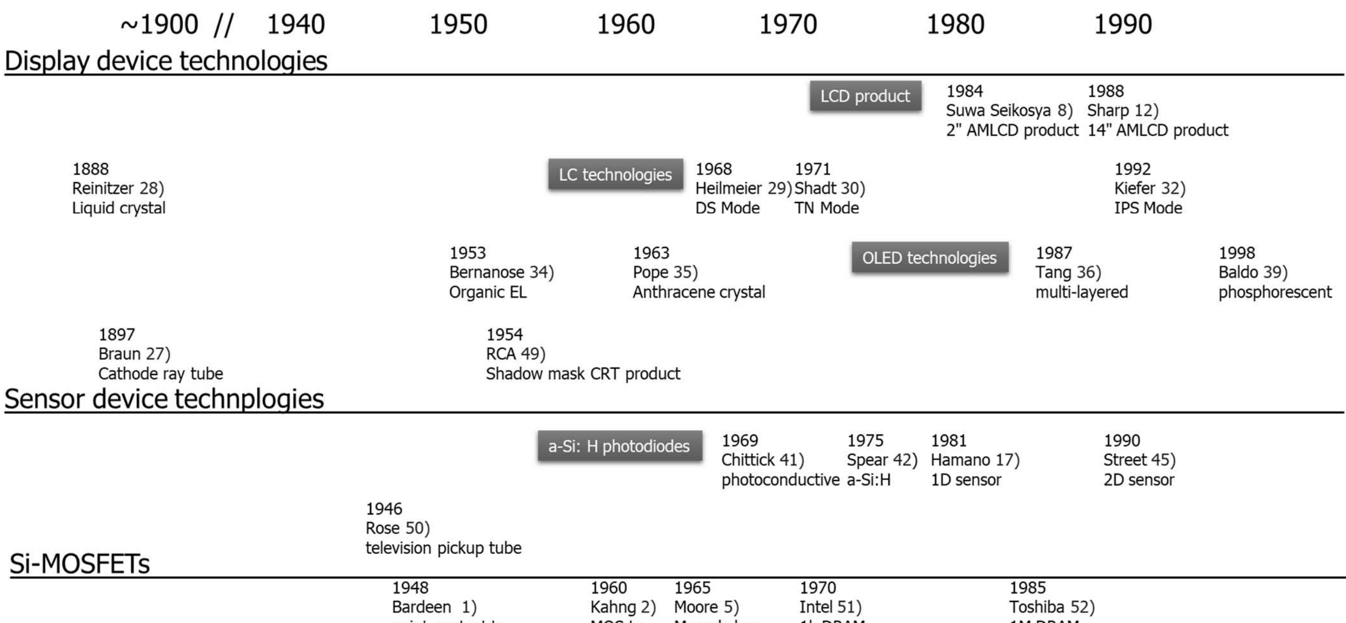


Figure 1.3 The a-Si:H photo-sensor with sandwich structure developed by Hamano et al. [17].

This photosensitive function of a-Si:H has been attracted much attention for use in not only linear (1D) image sensors [23][24] but also two dimensional (2D) ones [45-47]. The

most important advantage of this technology is that it can be fabricated image sensor arrays on glass substrate in size as same as that of target images. That is why it enables the volume of image reading scanner to be reduced compared with the Si-LSIs based scanners, such as the CCD and the CMOS sensors, because it does not need optical system to reduce the image. This image input device is less familiar than the information displays as image output devices described above. Today, however, this technology was already practically used in medical imaging systems as X-ray detector[48].

Table 1.1 Typical topics for each target application.



1.2 Thin-film transistors for large-area microelectronics

1.2.1 a-Si:H TFT

It is already described that the MOS transistors were demonstrated in 1960, and the concept of Moore's law was proposed in 1965. An idea for TFTs that is the main function for the current large-area microelectronics was also born in the same period. However, it may not be famous than the Si-MOSFETs. The first TFT proposed in 1961 by Weimer had a top-gate staggered type structure and consisted of polycrystalline CdS as a semiconductor layer and silicon monoxide as gate insulator [53]. About 10 years later, Brody et al. reported a design, fabrication and its performance for the AM-LCD that was consist of CdS-TFTs and nematic liquid crystals [7]. Epoch-making experiments for TFTs based on silicon thin films were done in 1979. LeComber et al. demonstrated TFTs by

using hydrogenated amorphous silicon (a-Si: H) on a glass substrate [30]. The a-Si:H related technologies were fortunate to have many opportunities studying its properties, fabrication process and its application, because it had not only switching functions but also photosensitive functions as described above. For example, the plasma-enhanced chemical vapor deposition (PE-CVD) as a fabrication tool was developed smoothly because it was able to be shared with development for solar cells [54]. A major disadvantage of a-Si:H TFTs was that its carrier mobility is relatively low to be 0.1 ~ 1 cm^2/Vsec. It was enough to drive liquid crystal in a pixel, but it was too small to integrate peripheral circuits with adequate clock frequency on a same substrate [55-57]. In order to overcome the low carrier mobility, poly-Si TFTs had been expected to be developed because poly-Si films might realize its mobility to be 1 ~ 100 cm^2/Vsec. Main purpose was integration of peripheral drivers for displays, printer heads and image sensors.

1.2.2 Poly-Si TFT

There were several approaches to develop poly-Si TFTs. Those approaches should be categorized first. One motivation was, as extensions of conventional microelectronics [58-62], to develop three-dimension integrated-circuits (3D-IC) on Si wafers and silicon-on-sapphire technology (SOS) based on the Si-MOSFET process, that were so called the high-temperature process in distinction to next one. It was resulted in the static random access memory (SRAM) with poly-Si transistor loads [63], for instance. The other one was, as the purpose of the large-area microelectronics [32][56][57], to develop I/O devices on conventional glass substrates based on the concurrently developing low-temperature process. Despite a lot of knowledge [64-66] and technical information [67-69] obtained in the former one were also contributed to the studies for the latter one, there still were many investigations required to develop poly-Si TFTs under low-temperature processes [10][70][71]. Therefore, the poly-Si TFTs under high-temperature process were also applied to specific, relatively small, I/O device applications. Actually, the first product for the AM-LCD stated in subsection 1.1.1 employed the poly-Si-TFTs on quartz substrate fabricated at high temperature [8]. These categories are easily explained by the kind of substrate material as summarized in Table 1.2. Several benefits are earned by using Si wafers, such as high resolution process and highly reliable transistor performance [72-74]. In contrast, applications must be limited because the Si wafers are not optically transparent. Quartz substrate are employed to solve the limitation [75][76]. Even though employed quartz, the applications are still limited because the material is highly expensive. In a view point of the material cost, conventional glass was suitable for large-size applications. That's why the poly-Si TFT was expected to be fabricated on the

conventional glass substrate at low-temperature.

Table 1.2 Several kinds of poly-Si TFTs categorized
by process temperature and substrate material.

Process	substrate	main application	example
High-temperature (Si-MOSFET compatible)	Si wafer	reflective type LCD [72,73] top-emission type OLED[74]	LCOS micro-display (typical < 2 inch)
	quartz	transparent type LCD[75,76]	light valve (for LCD projector)
Low-temperature	glass	direct-view type display	

1.2.3 Technical features and practical motivation for poly-Si TFTs

Figure 1.4 shows a typical configuration for active-matrix displays, (a) a TFT array driven by external driver ICs [77,78], (b) a pixel circuit for LCD [7], and (c) a pixel circuit for OLED [79]. The full high-definition (FHD), one of the standard display resolution, has the number of pixels for 1920 × 1080 × 3 (RGB), for example. In the case of LCD, the number of TFTs are as same as the one of pixels. In the case of OLED, the number of TFTs are at least as twice as the one of pixels.

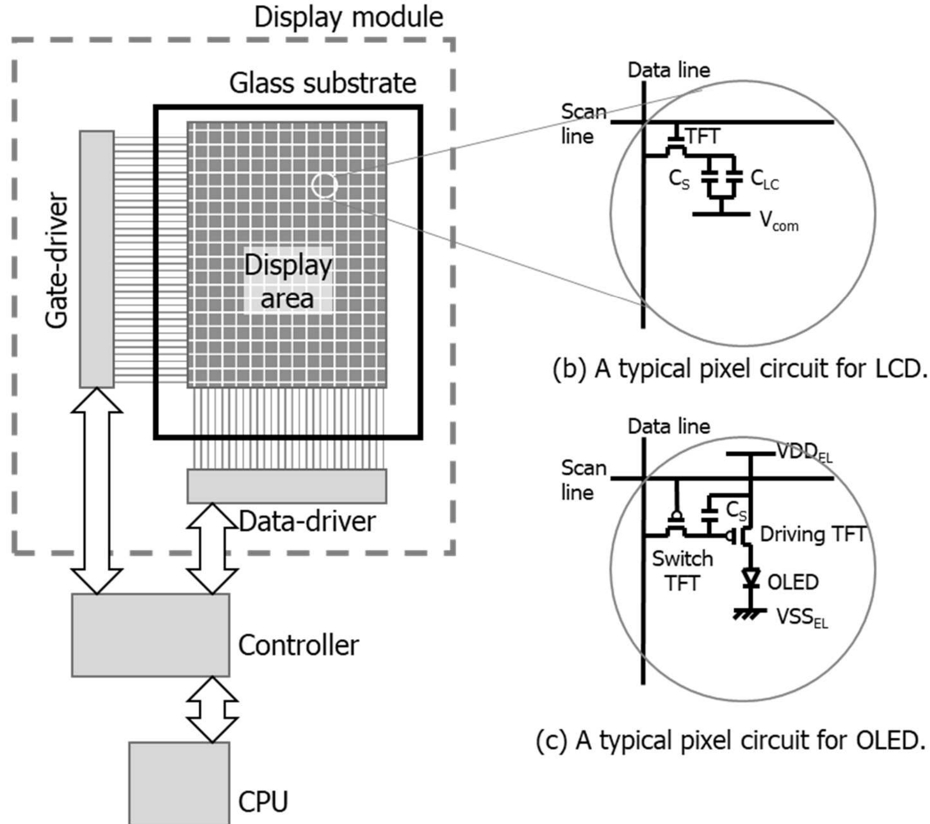


Figure 1.4 A typical configuration for active-matrix displays.

If it is applied to Figure 1.4 (a), there needs 1920 connections with the gate-driver and 1080 × 3 connections with the data-driver. Also it is found that the pitches of pixel and sub-pixel are very small to be about 80.6 μm and 26.8 μm, respectively, for example in the case of 7 inch diagonal FHD display. Thus, the larger numbers of pixels (or the smaller screen size), the more difficult to bond those connections physically. One of the remarkable benefits of the integration for the poly-Si TFT drivers is to solve this issues. The other is to reduce the size of display module, such as the volume and the space to assemble the driver ICs. Figure 1.5 shows a highly anticipated configuration for active-matrix TFT array driven by integrated poly-Si TFT drivers on the same substrate [57)80)].

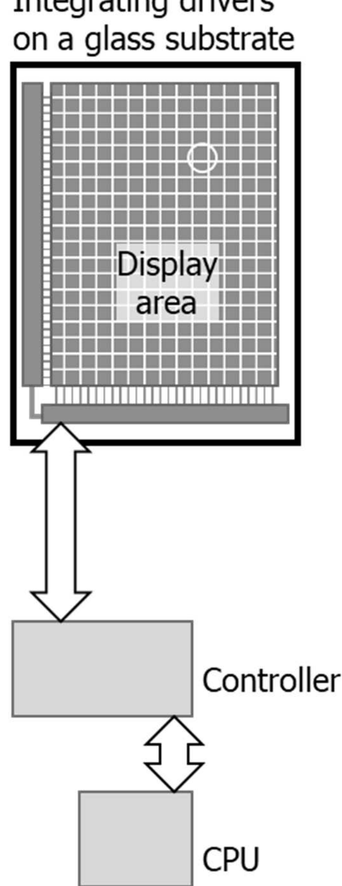


Figure 1.5 An expected configuration for active-matrix TFT array driven by integrated poly-Si TFT drivers on the same substrate.

1.2.4 Technical trends for TFTs compared with Si-MOSFETs

In this subsection, the evolution for substrate size and design rule in the FPD (Flat-panel display) industry is reviewed compared with that in Si-MOSFET. Figure 1.6 shows the increase in size of glass substrate for FPD and wafer for Si-MOSFETs [25]. The size of glass substrate increased about 10 times in ten years from 1990 to 2000. It was quite rapid, compared that the wafer size took about 25 years, from 1975 to 2000, to increase 10 times. There were two important reasons to evolve so fast. The one was that size of the applications also grew from middle-size PC-related monitors to large-size TVs. The other was to reduce cost through the manufacture of multiple display panels on a single mother substrate.

Figure 1.7 shows the decrease in feature size for FPD [81] and for Si-MOSFETs [6]. The feature size was substituted by the minimum resolution for photo-exposure tools in FPD here. The feature size for FPD reduced to be only half or one-third in thirty years

from 1990 to 2020. It was quite slow, compared that the feature size for Si MOSFET reduced one-hundredth in about 30 years from 1970 to 2000.

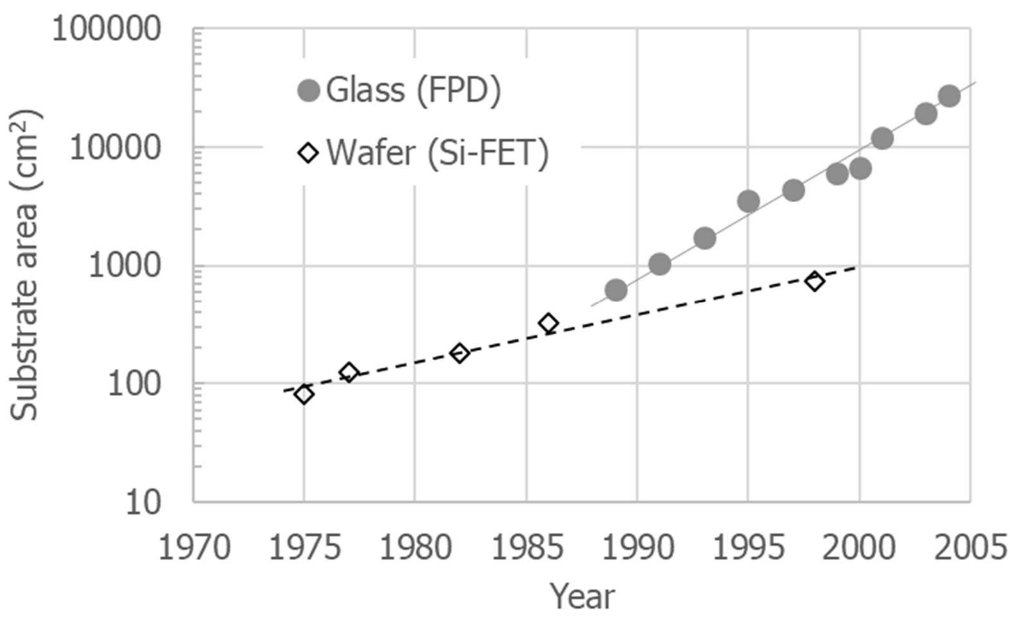


Figure 1.6 Increase in size of glass substrate for TFT-LCD and wafer for Si-MOSFETs [25].

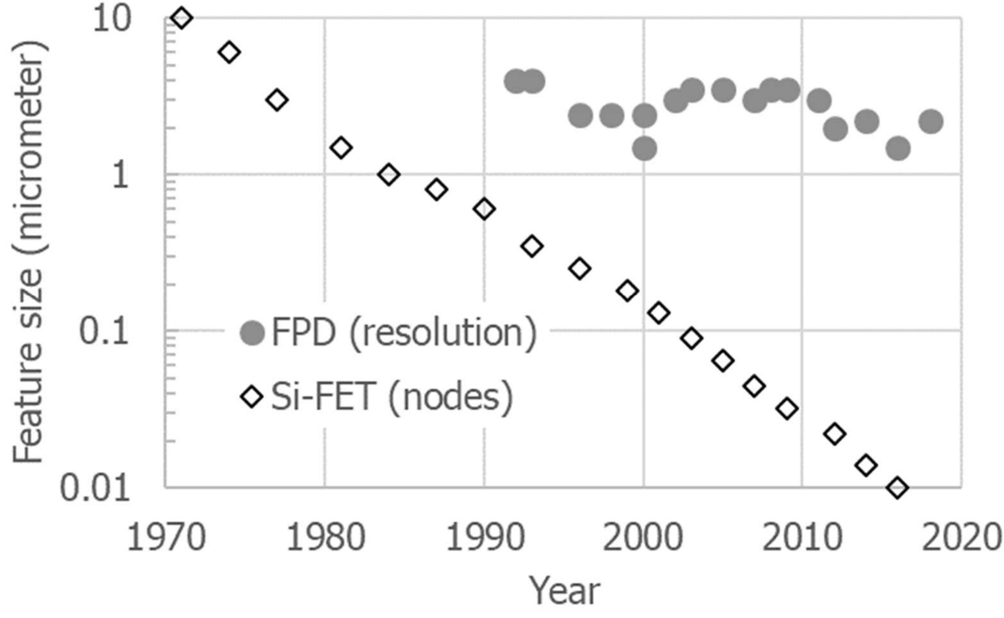


Figure 1.7 Decrease in feature size for FPD and for Si-MOSFETs [6][81].

As described above, it was found that the process evolution for FPD was quite different from the one for Si-MOSFET. However, it is also fact that there were two approaches in the FPD industry. Large-size displays, such as used in TV, have led the increasing the substrate size by employing a-Si:H TFTs. Moreover, they have not need to reduce the feature size, which is still about 4 micrometers. As the result, the substrate size reached to be almost 2.9 × 3.1 m, so called G10 (Generation 10) [82]. In contrast, small- and middle-size displays, such as used in smartphone, have required smaller feature size because they have been expected higher display resolution and driver integrations by employing poly-Si TFTs as discussed in the previous subsection. Therefore, the feature size is decreasing to be less than 2 micrometers, but the substrate size is still limited to be 1.5 × 1.8 m, named G6 [83].

1.3 Crystalline growth techniques for silicon thin-films

It is already described in section 1.2 that the one of approach for poly-Si TFT employed the low-temperature process. In this thesis, the formation techniques for crystalline silicon thin-films under the low-temperature are discussed, that is compatible with glass substrates, typically under 600 °C and preferably under 300 °C. There are mainly two ways to fabricate crystalline silicon thin-films at the low-temperature. The one is to deposit crystalline film directly on an amorphous substrate through gas phase [70)71)84-86]. The other is to crystallize films already deposit on a substrate. The latter technique is categorized in two ways, through solid [87-89] and liquid phases [55)90)91]. Those three crystallization methods, through gas, solid and liquid phases, are investigated in this thesis.

1.3.1 Gas-phase direct deposition

It is already described that Weimer proposed the first TFT in 1962 by employing polycrystalline CdS films [53], and that LeComber et al. demonstrated the first a-Si:H based TFT [30] in 1979. The pioneering research for the a-Si:H films preceded by Spear and LeComber [42] inspired many researchers to develop the fabrication method for poly-Si films [70)71)86] not limited to the a-Si:H films, that could enhance functions in large-area microelectronics device. Since then, direct deposition methods for silicon thin films has been investigated by many researchers. The objective for those was mainly how crystalline phase of silicon can be fabricated at low temperature below about 600 °C that is applicable for conventional glass substrate because the mobility for a-Si:H films are low to be around 1 cm^2/V sec. Higher mobility, more than 10 cm^2/Vsec for example, was

expected in order to integrate peripheral driver circuits into active-matrix devices, such as AM-LCDs.

There were two kinds of major way of direct deposition to obtain crystalline phase silicon thin films. The one was based on a thermal decomposition of source gases. Matsui et al. reported polycrystalline-silicon TFTs on conventional glass substrate by utilizing molecular beam deposition (MBD) method [10] in 1980. Morozumi et al. employed low-temperature chemical-vapor deposition (LP-CVD) method [32] to obtain polycrystalline silicon thin-films. In their report published in 1986, they already used a term "Low-Temperature processed poly-Si TFTs" that is the origin for the term "LTPS", which is currently used for indicating type of AM-LCDs. The other one was based on a plasma assisted decomposition of source gases, so called plasma-enhanced chemical vapor deposition (PE-CVD) method. Morin et al. reported poly-Si film formation at 450 °C of substrate temperature[70] in 1979. Matsuda et al. discovered to obtain crystalline phase silicon thin-films by optimizing deposition conditions under the similar conditions for deposition of a-Si:H at about 300 °C [71]. The former is a process under thermal equilibrium and the latter is a process under non-equilibrium. So it was considered the latter one was promising to obtain crystalline phase silicon thin-films more possibly than the former under the quite limitation for the deposition temperature, which must be applicable to conventional glass substrate.

1.3.2 Solid-phase crystallization

Behaviors for crystalline growth under solid phase had been started to study in 1970's for epitaxial growth on single crystalline substrate. One approach was to crystallize films without transport media that assist crystalline growth. In 1976, Csepregi et al. reported that thermal annealing at 500-600 °C produced epitaxial regrowth of amorphous layer in Si crystal produced by highly-dosed ion-implantation [92]. In 1977, Roth and Anderson demonstrated solid phase epitaxy (SPE) of deposited a-Si films on atomically clean Si (100) substrates by heating the a-Si films to temperature of 500-600 °C. The purpose was to obtain thin epitaxial layers with abrupt doping profiles because the diffusivity of common dopants and undesirable impurities could be reduced during growth at low-temperature [93]. As the results they indicated that crystalline growth of silicon can be obtained under solid phase at low-temperature at around 500-600 °C. Lateral solid phase epitaxy (L-SPE) of a deposited amorphous silicon film were intensively investigated in early 1980's to apply to the fabrication of three-dimensional large scale integrated circuits (3D-LSI's). The concept was that the epitaxial film first grows vertically in the regions directly contacted to the Si substrate as a seed and then

grows laterally on SiO_2 patterns until the epitaxial growth is stopped by random nucleation spontaneously occurred [94]. Then, polycrystalline silicon growth on a foreign substrate without any seed were studied in 1980's to apply to the fabrication of flat panel displays and solar cells. Noguchi et al. proposed a technique of Si+ ion implanted amorphization and subsequent solid phase growth, and applied it to fabricate TFTs [95]. Hatalis et al. investigated crystallographic properties for the films depending on the annealing temperature in 1988 [87]. Aoyama et al. reported the focused study for deposition temperature dependency under fixed annealing temperature of 600 °C in 1989 [89]. Those solid-phase-crystallized (SPC) poly-Si films were applied to TFTs and investigated by Panwar et al. in 1989 [88]. The electrical properties of poly-Si TFT are strongly dependent on the microstructure of the poly-Si film. Grain boundaries and defects inside grains are known that these act electrical potential barriers and scattering sites, which decrease the carrier transport mobility and also increase the leakage currents. Therefore, many efforts have been attempted to increase the grain size and to reduce the density of crystalline defects in the grains. If the grain size was achieved as large as the dimension of channel length, a technique to control location of the large grains were desired in order to avoid the grain boundaries being inside channel.

The other approach was to crystallize films with transport media that assist crystalline growth. Solid phase epitaxy, on single crystal germanium [96] or silicon [97], had already been discovered under employing transport media such as a metal or a compound prior to those researches without transport media. The transport media assisted to reduce the temperature for the crystalline growth happen. In those cases, however, there was a seed crystalline layer underneath in the initial stages. It was late 1990's for low-temperature crystallization of amorphous films with transport media to be again attracted attentions to. The concept was that the seed area is first selectively crystallized in the regions the metal layer locally patterned on and then crystalline grows laterally until the growth is stopped by random nucleation spontaneously occurred. Lee et al. applied selectively formed palladium (Pd) [98] and nickel (Ni) [99] films as seed regions on silicon films. Yang et al. employed Au, Cu, In, Co and Ni as the transport media for selective nucleation for germanium films [100]. Those techniques for the selective nucleation have achieved controlling the location for the grain. However, further techniques for controlling location for the grain boundary and reducing residual the defects inside grains have been desired to improve the electrical performance of TFTs.

1.3.3 Liquid-phase crystallization

One of the most typical way to form single-crystalline silicon is performed under

liquid phase, as widely known as Czochralski method [101]. A seed of single-crystalline silicon is placed on the surface of molten silicon in the quartz crucible, and gradually drawn upwards while simultaneously being rotated. This draws the molten silicon after it which solidifies into a continuous crystal extending from the seed. poly-Si ingot is also formed from molten silicon by cast method [102]. Those process temperature is required more than 1400 °C to melt silicon source. This kind of technology is not suitable for large-area microelectronics. In order to make it possible to use liquid phase crystallization in the large-area microelectronics, many researchers paid attention to the laser process.

While much effort has been devoted to the development of laser annealing techniques since middle of 1970's for epitaxial regrowth of ion-implanted amorphous layers on semiconductors. At the same time, development for large grained semiconductor films on foreign substrates has been started by using similar techniques. The initial study in this area can be found in the brief report by Laff and Hutchins [55] in 1974. They had already supposed these kinds of technique to be used in the active-matrix addressing of liquid-crystal displays. This work was extended by Fan and Zeiger using a continuous wave (CW) Nd-YAG laser to crystallize RF (radio-frequency) sputtered Si films on Al_2O_3 substrates [103] and by Gat et al. using CW argon laser to recrystallize poly-Si films deposited by LP-CVD on amorphous insulators [104]. Pulsed lasers were also attempt as well as CW lasers in those days. Young et al. applied Q-switched ruby laser [105] and excimer laser to the annealing [106] of ion-implanted Si. Also by Morin et al. the Q-switched ruby laser was also applied to fabricate poly-Si TFTs on glass [57].

In contrast to those attempts that several kinds of lasers were applied to silicon crystallization, there was a research groups investigating that crystallographic orientation might be controlled by means of artificial surface-relief structure underneath. Geis et al. demonstrated that crystallographic orientation of Si films on amorphous substrate was controlled by laser crystallization of a-Si deposited over a surface-relief grating in the substrate [90]. The same group also proposed and demonstrated another technique to eliminate sub-boundaries through planar construction during zone-melting recrystallization [107]. It is found there were the same challenges as in solid phase crystallization, that were to control location for the grain boundary and to reduce residual the defects inside grains to improve the electrical performance of recrystallized Si films.

Just after those approaches in both selecting the kind of laser apparatus and controlling crystallographic micro-structures, Sameshima et al. presented the potential of XeCl excimer laser (308 nm) to fabricate high quality poly-Si films on a plane glass substrate. They reported the channel mobility of n-channel TFTs employed poly-Si films crystallized by XeCl excimer laser reached to 180 cm^2/Vsec [91]. With this as a trigger,

there were many studies started to apply the excimer laser to the large-area microelectronics devices.

1.3.4 Comparison for three methods

As described above, there were mainly three kinds of approaches to obtain crystalline silicon thin-films for TFT applications in late 1980's. They are categorized below.

i) gas phase (direct deposition)
ii) liquid phase (laser irradiation)
iii) solid phase (thermal treatment)

In these days, 30 years later, those kinds of technologies are still being used in display industry as summarized in Table 1.3. i) Direct deposition technique, i.e. gas phase growth, is widely used for larger size displays, such as TVs and PC monitors, as the technology called a-Si TFT. ii) Laser irradiation technique, i.e. liquid phase growth, is employed for small and medium size displays with high resolution, such as smartphones and digital-camera monitors. In addition to those, iii) thermal treatment technique, i.e. solid phase growth, is also utilized for very small size and high pixel-density displays, such as a light-valve for LCD projectors, as the technology called HTPS (High-temperature poly-Si). i) Direct deposition technique is applicable glass substrate but, unfortunately, it still produces a-Si. Also iii) thermal treatment technique provides poly-Si but it requires quartz substrate because it needs higher temperature process, such as thermal oxidation for gate insulators. So current dominant TFTs for on conventional glass substrate employing crystalline phase silicon are manufactured by utilizing laser irradiation technique, that is called LTPS to distinguish with a-Si TFT technologies.

Table 1.3 Film properties, typical process temperature and their applications

	film property (typical)	process temperature (substrate)	technology name in industry
gas	amorphous (a-Si:H)	300 ℃ (glass)	a-Si TFT
liquid	crystalline (poly-Si)	500 ℃ (glass)	LTPS
solid	crystalline (poly-Si)	1000 ℃ (quartz)	HTPS

1.4 Purpose of this study

This thesis covers somewhat long period along the progress for technologies both of low-temperature growth of crystalline silicon and poly-Si TFTs. The low-temperature growth techniques for crystalline silicon were studied in three different ways under gas, solid and liquid phase. As they were at different time periods, those investigating objectives were adopted along each technical stage when they were studied. Then, the liquid phase crystallization by using excimer laser was employed to fabricate poly-Si TFTs. As there were still many challenges in order to apply it practically, some of critical issues to apply for specific applications were investigated and improved. The main purpose for this series of study is to make it possible for large-area microelectronics devices based on poly-Si TFTs to be used practically, i.e. to contribute generating a new industry. There had been many prior fundamental studies, and there are many subsequent developments in the stage of manufacture. The role of this series of study is to bridge from academic research to product business. The academic research sometimes aspires the highest numerical value or the world first achievement. In contrast, this work was focused on practical development, such uniformity and reliability. Thus, some of individual study were accompanied by the developments of novel apparatus to fabricate the poly-Si films and their TFTs.

In this thesis, the method to fabricate poly-Si films is discussed first. *The gas phase deposition method*, that is one step process as like a-Si deposition, had been expected. Actually, quite small grain Si called microcrystalline Si (μc-Si) films were formed on a glass substrate. As their electrical properties were not enough, however, the mechanism to promote crystalline silicon growth at low-temperature was required to be clear. *The solid phase crystallization* with combination of selective nucleation and grain boundary filtration method was studied as an alternative for laser crystallization, the mainstream technology in those days, in the viewpoint for enlargement of grain size. The goal of this study is to improve performance of the poly-Si TFTs and to result in expanding products range for those TFTs to be applied. As it was at relatively later stage during this series of study, the grain size was targeted to be more than micrometer that was as large as the channel length of TFTs. *The liquid phase crystallization* by utilizing excimer laser had a unique advantage to obtain high-mobility poly-Si films easily even on a glass substrate. As the crystallization process was being performed within quite short period to be several tenth nanosecond, however, it was still necessary to understand the growth mechanism during the laser irradiation. The objectives for those three methods are summarized in Table 1.4.

Table 1.4 The objectives for those three methods

	method	objective
gas	epitaxial growth by utilizing plasma enhanced CVD	- demonstrating to grow crystalline silicon at low-temperature. - studying how impurity doping effects on microstructures and electrical properties.
solid	grain boundary filtration under lateral solid phase epitaxy and selective nucleation	- demonstrating grain boundary filtration of germanium film by using planar constriction. - studying the potential to apply it to silicon film.
liquid	excimer laser crystallization	- understanding the growth mechanism during quite short period of the laser irradiation.

Then, in this series of study, excimer laser crystallization was chosen to fabricate poly-Si TFTs and was investigated details how should be applied for practical devices. First, some attempts were studied to improve uniformity for TFT characteristics. Next, a method to reduce photo-leakage current was demonstrated for the poly-Si TFTs to be applicable to LCDs under high-luminance. Further, a method to improve reliability in TFTs was investigated. Finally, the possibility to realize ultra-high mobility TFTs was investigated to integrate further functions and to expand products range for those TFTs to be applied. These challenges to improve characteristics in excimer laser crystallized poly-Si TFTs are summarized in Table 1.5.

Table 1.5 The challenges to improve characteristics
in excimer laser crystallized poly-Si TFTs

challenges	attempts to improve
uniformity	- selecting precursor film - controlling re-solidification process - dividing unit size of circuit design
photo-leakage current	- reducing thickness for poly-Si films
reliability	- controlling clean interface between gate-oxide and poly-Si channel
ultra-high mobility for integrating further functions	- extending the grain laterally

2. Low-temperature deposition of crystalline silicon thin-films

This chapter states on a new deposition technique called HR-CVD (Hydrogen-Radical-Enhanced Chemical Vapor Deposition) with assistance of chemical potential of atomic hydrogens for preparing crystalline silicon films epitaxially grown on single-crystalline silicon substrates (110) and (100) under the substrate temperatures at around 300 °C.

In this study, a coaxial microwave discharge system was used to generate precursors, SiFnHm (n+m ≤ 3), as a consequence of the plasma-induced decomposition of gaseous mixture of SiF_4 +H_2. So as to introduce additional atomic hydrogens into the growth area, a new apparatus termed "cavity" system was used to combine with the coaxial discharge system. Remarkable changes were found in the structure of Si-network by changing preparation parameters, i.e., the substrate temperature, film thickness, doping concentration of impurity, flow rate of atomic hydrogen and orientation of crystalline substrates. The optimum conditions for epitaxial growth were obtained at 300 °C on Si (110) and 350 °C on Si (100) substrates, respectively. Although the disorders in Si-networks tended to be apparent with increasing the thickness or raising the impurity concentration of P (phosphorous) or B (boron), modulating conditions with excessive hydrogens were highly effective on reducing those disorders. The highest electron Hall mobility was obtained to be 115 cm^2/Vsec with the carrier concentration of 2×10^{16} cm^{-3} in the epitaxially grown P-doped silicon film.

2.1 Previous research and objectives

It was already described that studies to form poly-Si films by using PE-CVD were started in late 1970's [70)], following the discovery of a-Si:H films [41-43)]. In 1980, Matsuda et al. reported detailed studies that polycrystalline silicon films can be deposited on a glass substrate by a glow-discharge technique using gas sources containing fluorine under high RF (radio-frequency) power conditions [71)]. In their article, it was also reported that P-doped those films revealed conductivities two order magnitude higher than those of amorphous film fabricated under low RF power conditions. Since then many researchers had investigated varieties of low-temperature deposition techniques for crystalline silicon, such as MBD [10)], LP-CVD [32)], photochemical vapor deposition [109)], PE-CVD [110)111)] and biased sputtering [112)]. Because it was considered that those crystalline films brought higher driving ability than amorphous films if those films applied to TFTs. It was fact, however, that there was no remarkable progress for growth of "high-quality" polycrystalline film on a glass substrate. That might be due to lack of information both

nucleation on a foreign substrate and crystalline growth at low-temperature. Thus, this study targeted to understand behavior in the “crystalline growth” on existing nuclei, i.e. epitaxial growth on a single crystalline substrate at low-temperature.

In the late 1980’s, there were some reports to refer silicon epitaxial growth at low-temperature by using techniques based on plasma decomposition that was similar with techniques for fabricating hydrogenated amorphous silicon (a-Si:H). Baert et al. demonstrated it by gas-mixture system of PH_3/SiH_4 under the substrate temperature at 250 °C [113]. Shibata et al. obtained it by SiF_4 based gas source with additional supply of atomic hydrogen at 300 °C [110]. However, these studies just referred kinds of discovery of epitaxial growth. Following the Shibatas’ work, the author was attempt to study epitaxial growth of silicon. Regarding the method employing plasma with SiF_4 based gas source and additional supply of atomic hydrogen, Shimizu and coworkers named Hydrogen-Radical-Enhanced Chemical Vapor Deposition (HR-CVD) [114] because in which the concentration of atomic hydrogen in the deposition process was strictly controlled. They reported the features of that method as follows [110]; i) The presence of atomic hydrogen is required for film deposition. ii) The fluorine content in the film is very low to be less than 1 at. % even though fluorides are employed as source gases. Fluorine evolution by formation of HF (hydrogen fluoride) accompanies the formation of three-dimensional Si networks, iii) The hydrogen content and the chemical structures such as Si-H and $Si-H_2$ bonds, in the film can be controlled by the hydrogen flow rate during deposition. iv) The polycrystalline film deposited on a glass substrate shows (220) orientation strongly preferred. A lot of effort was devoted by Shimizu and coworkers to investigate resulting film properties and their deposition mechanisms [114-116], but they were mainly focused on amorphous films and their depositions.

The purpose of this section was to understand behaviors for crystalline growth at low temperature under the technique of HR-CVD. Single crystalline substrates were employed to avoid the process for nucleation, as already described.

2.2 Apparatuses and experimental [117]

Two types of deposition system were adopted in this experiment to prepare silicon thin films on single-crystalline silicon substrates. A coaxial microwave discharge system was used in the first system as shown schematically in Figure 2.1(a). Hydrogen was pre-diluted in Ar (argon) gas, introduced into the outer tube, and then decomposed to hydrogen atoms by microwave plasma. SiF_4 gas was passed through the inner tube and exposed to the plasma only at the end of this tube, since the plasma was concentrated in the space close to the walls of the outer tube. Interaction between the resulting SiF_n ($n \leq$

3) radicals and the hydrogen atoms generate the precursors responsible for deposition. In the second system, additional microwave plasma reactor named "cavity" was combined with the first system as shown schematically in Figure 2.1(b). Hydrogen was pre-diluted in Ar gas, introduced into the cavity area, and then decomposed to hydrogen atoms by another microwave plasma system. Those two sets of H_2/Ar flows and microwave power supplies were able to be controlled independently. It means that excessive supply of hydrogen atoms onto growth surface could be achieved by the cavity discharge system that was independent on the coaxial discharge system. For the doping with substitutional impurities, either PH_3 or BF_3 was pre-diluted to 1 vol. % in helium and mixed with the SiF_4 gas to be predetermined concentrations prior to introducing into the reactor through the inner tube.

At the step for cleaning substrate surface, so-called "RCA clean" method [118] was employed to fabricate chemical oxide on the Si substrate. And, the oxide layer was removed by using 10% HF solution before introducing the substrate into the reactor. Films were prepared on the (100) or (110) oriented silicon wafers. Microstructures of the films were evaluated by using Raman scattering spectroscopy, RHEED (Reflection High Energy Electron Diffraction) and IR (Infrared) absorption spectroscopy [119]. The van der Pauw method [120] was used to evaluate electrical properties, such as Hall mobility and carrier densities. Typical deposition conditions are summarized in Table 2.1.

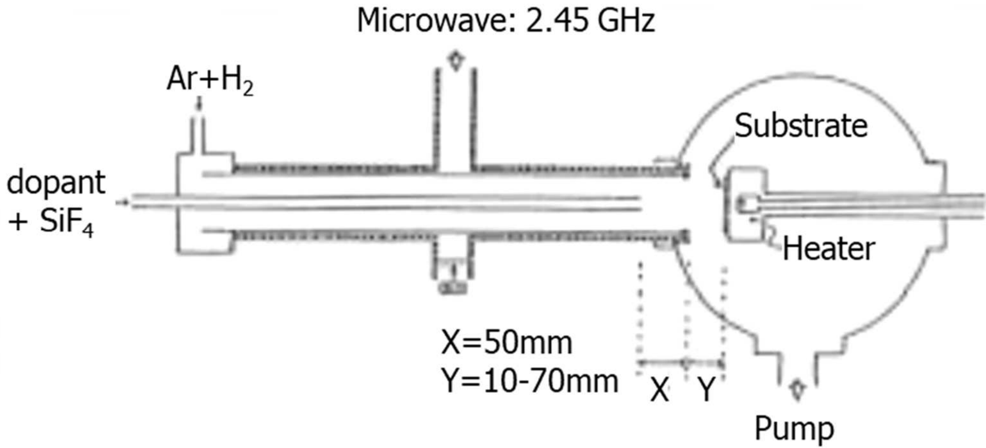


Figure 2.1 (a) A coaxial microwave plasma reactor.

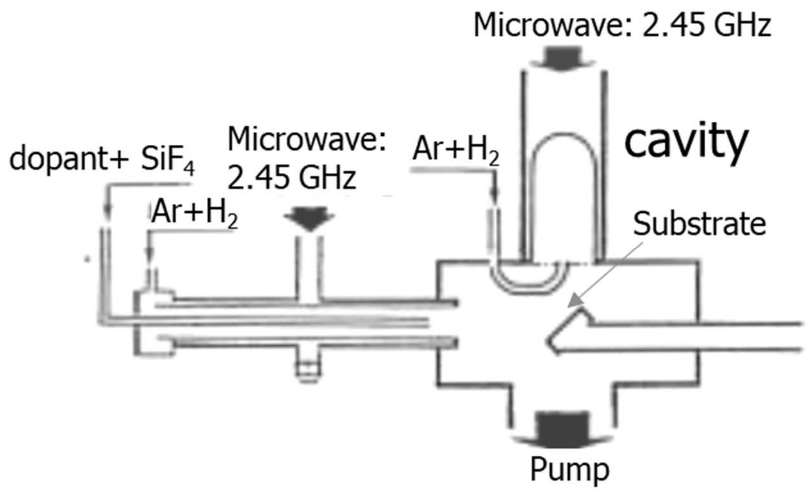


Figure 2.1 (b) A coaxial microwave plasma reactor combined with a cavity.

Table 2.1 (a) Typical deposition conditions for
Si (110) under the coaxial microwave plasma reactor.

Coaxial reactor

Flow rate for H_2: 30 sccm	Microwave power: 440 W
Flow rate for Ar : 76 sccm	Substrate temperature: 300 ℃
Flow rate for SiF_4: 76 sccm	Pressure: 440 mTorr

Table 2.1 (b) Typical deposition conditions for
Si (100) under the coaxial microwave plasma reactor.

Coaxial reactor

Flow rate for H_2: 30 sccm	Microwave power: 360 W
Flow rate for Ar : 76 sccm	Substrate temperature: 350 ℃
Flow rate for SiF_4: 76 sccm	Pressure: 100 mTorr

Table 2.1 (c) Typical deposition conditions under the coaxial and cavity microwave plasma reactor.

Coaxial reactor	
Flow rate for H_2: 30 sccm	Microwave power: 440 W
Flow rate for Ar : 76 sccm	
Flow rate for SiF_4: 76 sccm	
Cavity	
Flow rate for H_2: 10-100 sccm	Microwave power: 260 W
Flow rate for Ar : 76 sccm	Substrate temperature: 300 ℃
	Pressure: 400 mTorr

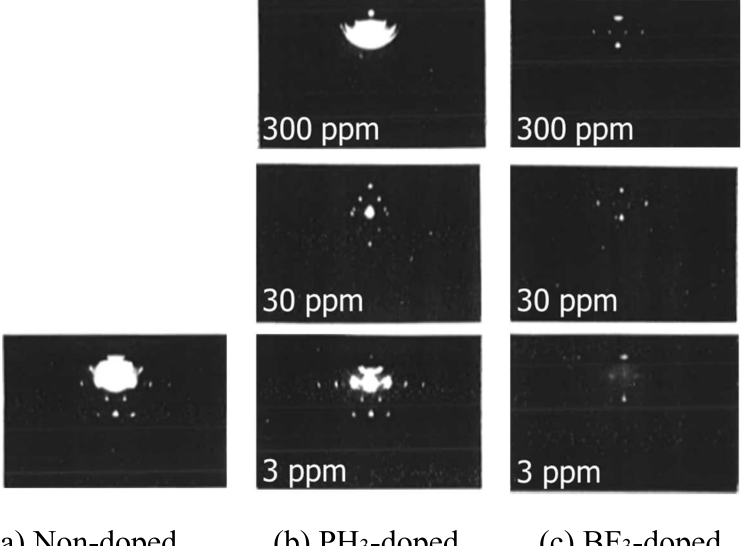
2.3 Impurity doping

The polycrystalline film deposited on a glass substrate by HR-CVD shows (220) preferred orientation as described above [110]. Therefore, epitaxial growth on Si (110) substrates was attempted at first, then those films were evaluated by using RHEED and Raman spectroscopy. After that microstructures and electrical properties were also evaluated in those non-doped films and doped ones with substitutional impurities, such as phosphorus and boron. The RHEED pattern for non-doped film of 300 nm thickness revealed that it was epitaxially grown on a Si (110) substrate as shown in Figure 2.2 (a). This condition was as same as the one to obtain the best polycrystalline film with strongly (220) oriented on a glass substrate. Deposition rate of this film was about 1.2 nm/sec, that is high rate relatively. The dilution ratio of SiF_4/Ar could control deposition rate. The epitaxial films were successfully grown also at the deposition rate of 0.5 and 1.5 nm/sec. Increasing the thickness, ring pattern became to dominates in RHEED image. It suggested that epitaxial growth was deteriorated at near surface. Based on those results, 300 nm thick samples are prepared in studies followed. Si substrates may affect the Raman scattering as same as the films deposited onto, but the affection can be negligible to study comparative values of films.

As shown in Figure 2.3 (a), the peak widths at around 520 cm^{-1} caused by crystalline Si in Raman scattering spectrum [121][122] increased with the concentration for PH_3. It suggests that the doped impurity promoted disordering during growth of

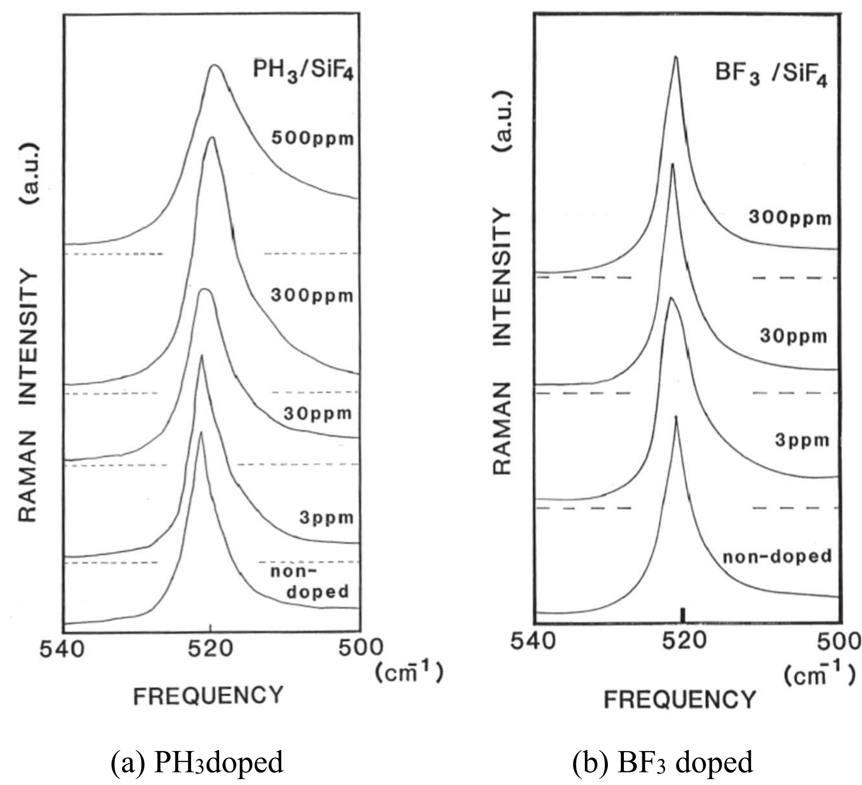
crystalline Si. As scattering intensity at lower frequency also increased with the concentration, formation of disordered phase, such as polycrystalline grain, grain boundaries and amorphous fraction, is suggested. These results supports that doped impurity obstructs the ideal growth of crystalline. RHEED patterns shown in Figure 2.2 (b) varied from "spot" to "ring" with concentration of doping. Spot-patters in diffraction caused by single crystalline phase were still observed in the films doped with 30 ppm, however ring-patterns originated by polycrystalline phase were observed in those doped with 300 ppm and more. It is considered that something assistance is required to coordinate "P" well into Si-networks because disorders were caused by impurities, such as P and PH_3, during chemical reactions at growth surface and those in gas phase.

Next, the results for boron doping by using BF_3 are shown in Figure 2.2 (c) for RHEED and in Figure 2.3 (b) for Raman spectroscopy. As different from PH_3, the peak widths at around 520 cm^{-1} were kept as almost same as the one for non-doped film even though the doping concentration reached at 300 ppm. The spot-patterns also maintained with doping concentration from non-doped to 300 ppm. It suggests that the BF_3/SiF_4 system affected less than PH_3/SiF_4 to chemical reactions both in gas phase and at growth surface. It was resulted in that boron can be coordinated into Si-networks easier than phosphorus here different from the previous study for fabricating doped μc-Si films by using HR-CVD [110]. Those films fabricated by using PH_3/SiF_4 or BF_3/SiF_4 systems with 300 ppm concentration in gas phase indicated 3 orders of magnitude higher than non-doped film in their conductivity. It meant that those impurities were electrically activated as substitutional dopants.



(a) Non-doped (b) PH_3-doped (c) BF_3-doped

Figure 2.2 RHEED patterns of (a) Non-doped, (b) PH_3-doped and (c) BF_3-doped epitaxial layers on Si (110) substrate.



(a) PH_3doped (b) BF_3 doped

Figure 2.3 Raman spectra of (a) PH_3doped and
(b) BF_3 doped epitaxial layers on Si (110) substrate.

The difference in epitaxial film qualities depending on doping concentration between PH_3 and BF_3 might be considered as follows. Table 2.2 shows silicon related binding energies [123)]. The decomposition of PH_3 is considered to be much easier than that of SiF_4 because the binding energy of the P-H, representing PH_3 gas, is smaller than that of Si-F, representing SiF_4. It means that a reaction originated from P-H system precedes another reaction originated from Si-F system and then the former reaction disturbs the epitaxy in silicon. In contrast, the binding energy of the B-F, representing BF_3 gas, is larger than that of Si-F. As the result, the species decomposed by BF_3 do not affect so much to the reaction originated from Si-F system during the epitaxial growth.

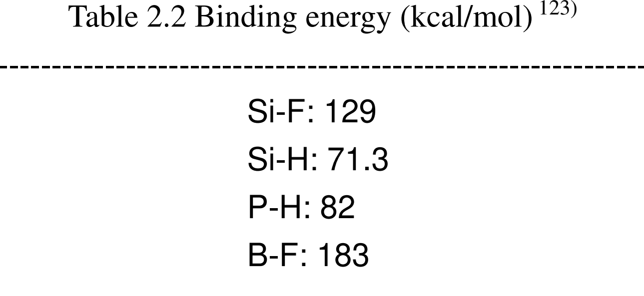
The epitaxial grown films as resulted in above have some features as described below;

i) High deposition rate: it was as high to be about 1.5 nm/sec as the one for μc-Si films.

ii) Thickness dependency: the epitaxial growth was deteriorated by increasing the deposition thickness. The spot pattern was observed within 300-400 nm of the maximum thickness through RHEED.

iii) p-n doping: Substitutional doping was possible. However, the crystallinity was deteriorated with increasing impurity concentration.

Table 2.2 Binding energy (kcal/mol) [123)]



Bond	Binding energy
Si-F	129
Si-H	71.3
P-H	82
B-F	183

The fact that the deposition rate is as almost same as the one for μc-Si suggest us those below. It is not limited by the reaction rate that Si atoms reach to the thermally equilibrium sites to form Si-Si bonds at the growth surface. There are variety of reactions within growth zone, such as bonding-debonding of Si atoms, debonding of H and F atoms, and etching caused by atomic hydrogen and decomposed SiF_4. They are almost same as those in the growth of μc-Si films. Thus, it is considered that Si atoms are introduced to the condition with thermal equilibrium by chemical reaction including etching promoted by F and H, even though the deposition was performed through non-equilibrium plasma. Simultaneously, however, the film quality become worse, i.e. resulting non-epitaxial growth by increasing defects, during the series of deposition because the condition for Si atom to bond to ideal site is very severe. Those facts also suggest that the crystalline growth process at low temperature is not determined only by simple selection of microscopic reactions, but also some structures, such as cluster type of precursors and morphology of growth surface.

2.4 Substrate temperature and growth orientation [†1]

Additionally, two important facts were obtained to discuss epitaxial growth mechanism at the surface. The one was that there was optimum range in temperature to obtain epitaxial film. Figure 2.4 shows RHEED patterns obtained by the 300 nm-thick films grown on Si (110) at several temperatures. Ring pattern was observed at 200 °C of the substrate temperature. With increasing the temperature, the spot patterns, evidence for the epitaxial growth, could be observed. And increasing the temperature further to be 400 °C, the ring pattern was observed again. It has been conventionally considered that

higher temperature promotes crystalline growth because that a lot of thermal energy supply can assist the migration of precursors at the growth surface. In this case, however, higher temperature rather obstructed the epitaxial growth. It could assume there was another factor to promote surface reaction instead of the temperature. Hydrogen was considered to be one of the potential candidate. In the study of μc-Si growth from SiH_4, for example, amorphous film was obtained at higher temperature. The reason was considered that excessive atomic hydrogen that originally covered the growth surface was desorbed and that then the migration of precursors at the growth surface was suppressed.

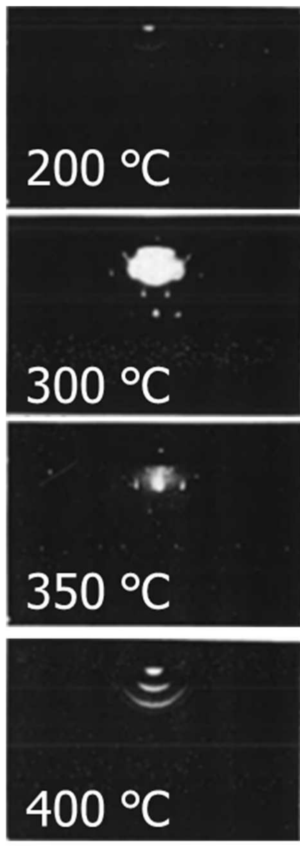


Figure 2.5 RHEED patterns obtained by the films grown on Si (110) at each temperature.

The other important fact was obtained by investigation to deposit films on Si (100). Typical deposition condition is referred in Table 2.1 (b). Figure 2.5 shows hydrogen content depending on deposition temperature obtained by IR spectroscopy with film quality obtained by RHEED pattern. The content of hydrogen in films decreased monotonically with substrate temperature. The optimum range in temperature was slightly shifted to higher temperature to be at 350 °C. Hydrogen content revealed to be 1-2 at. % in highly oriented samples observed Kikuchi-line [124] in that temperature range.

Remarkable difference in film quality compared with the experiments on Si (110) was that the epitaxial growth was achieved with 1 μm thickness of the films as shown in Figure 2.6 even though the deposition rate was maintained to be 1.2 nm/sec as same as the experiment on Si (110). Electrical properties for those epitaxial films on Si (100) are shown in Figure 2.9 later.

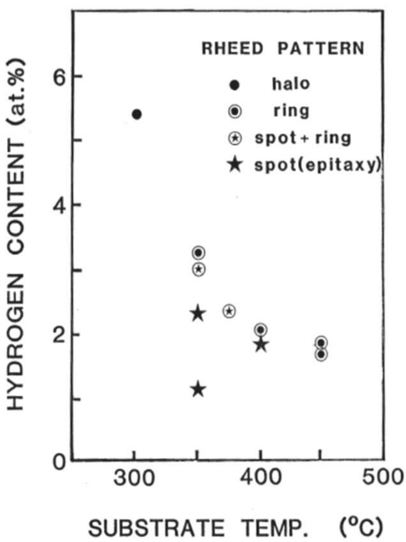


Figure 2.5 Hydrogen content depending on deposition temperature obtained by IR spectroscopy with film quality obtained by RHEED pattern.

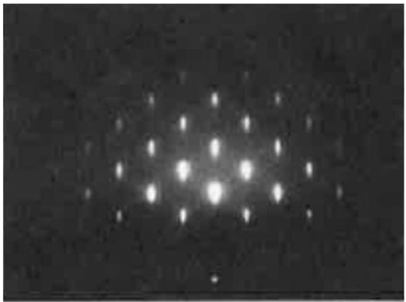


Figure 2.6 RHHED pattern of epitaxial layer on Si (100).

2.5 Additional supply of hydrogen

Turning the attention to the deposition conditions on Si (100), it was different, especially in pressure, from the one to obtain strongly Si (220) oriented polycrystalline film on a glass substrate, i.e., to obtain the epitaxial film on Si (110). It could mean that the precursors to contribute on Si (100) growth is different from those on Si (110) growth. Also the supply of atomic hydrogen might be promoted because the expanding the region

of hydrogen plasma was experimentally observed by lowering the pressure. Therefore, additional microwave plasma reactor named "cavity" was then employed to study how excessive supply of hydrogen atoms onto growth surface play during crystalline growth. The contribution of additional hydrogen to the epitaxial growth on Si (110) was verified in the three key parameters for i) film thickness, ii) substrate temperature, and iii) PH_3 doping. Because epitaxial growth was limited less than 0.5 μm in thickness on Si (110) in spite of that excellent epitaxial growth was observed more than 1 μm thickness on Si (100).

2.5.1 Film thickness

Figure 2.7 shows the thickness dependency on the films grown on Si (110) by utilizing additional microwave plasma reactor combined with the conventional system. The spot pattern was observed even if the film was deposited to be 1 μm in thickness. And strong orientation was observed even in the 1.5 μm thick film. They indicated the epitaxial growth was still maintained in those thick films. In contrast, the border to change from spot to ring in RHEED patterns was about 400 nm in thickness, in the case of conventional reactor, as described above. Thus, the additional hydrogen atoms contributed to reduce the formation of defects and to form stable Si-Si bonds at the growth surface.

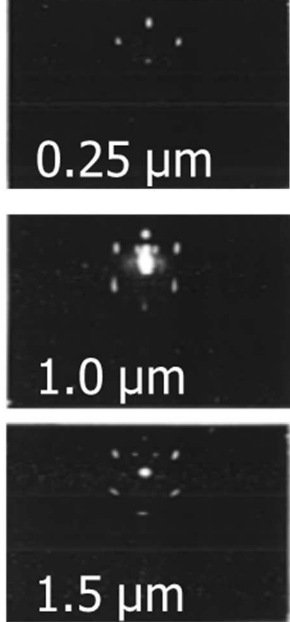


Figure 2.7 RHEED patterns depending on
the thickness of the films grown on Si (110).

2.5.2 Substrate temperature

Additional supply for hydrogen atoms promoted the epitaxial growth on Si (110) also in studying substrate temperature dependency. Figure 2.8 shows RHEED patterns obtained by the films grown on Si (110) at each temperature. The spot patterns were observed in the wide range of temperature from 300 °C to 400 °C. It was different from that ring pattern was observed at 400 °C by using the conventional reactor.

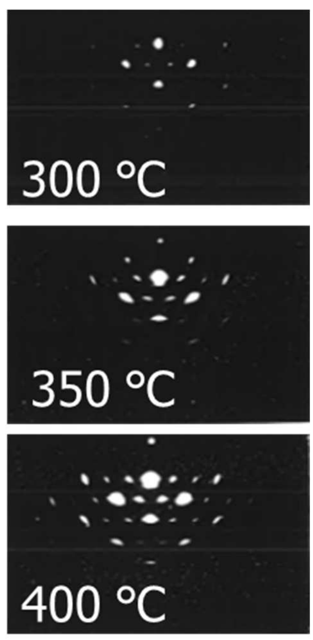


Figure 2.8 RHEED patterns obtained by the films grown on Si (110) at each temperature.

2.5.3 PH_3 doping

The spot patterns, the evidence of the epitaxial growth, were observed in the wide range of PH_3 concentration from non-doped to 300 ppm against SiF_4. It was also different from that ring pattern was observed at 300 ppm by using the conventional reactor. Figure 2.9 shows electron mobility and carrier concentration for PH_3 doped-epitaxial grown layers on Si (110) with comparison for the films grown on Si (100) by using the conventional reactor. The film with 30 ppm indicated the hall mobility to be 115 cm^2/Vsec and the carrier density to be 2×10^{16} cm^{-3}. They also showed that carrier density increased with keeping electron mobility in comparison with the film with 30 ppm deposited by conventional reactor. Substitutional doping was also confirmed by the fact that variation with 5 orders of magnitude in carrier density was observed in the film with 300 ppm, even

though those crystalline qualities were deteriorated as sharp drop in mobility was observed at the concentration of 300 ppm.

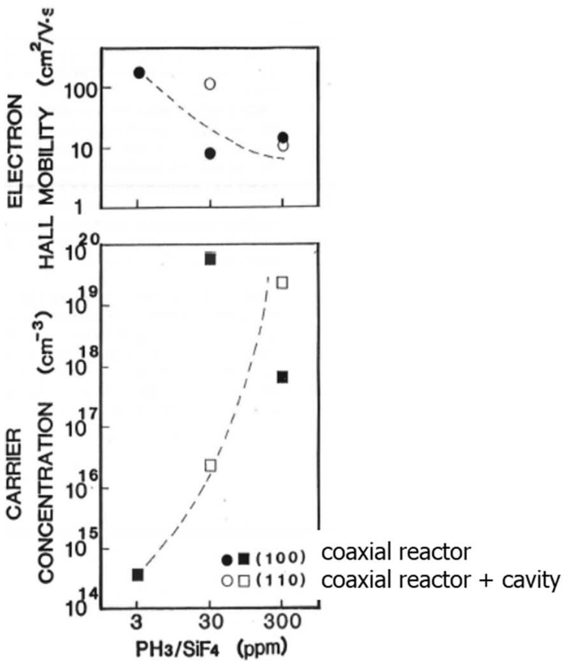


Figure 2.9 Electron mobility and carrier concentration for PH_3 doped-epitaxial grown layers on Si (100) with conventional reactor and Si (110) with cavity added.

2.6 Discussion [†1]

This chapter was described crystalline growth on single crystalline substrates by using gas phase deposition assisted by atomic hydrogen. This study had based on the concept that highly diffusible hydrogen could promote structural relaxation of Si-network at the growth surface. As the results, it was demonstrated that crystalline Si films could be grown epitaxially on Si substrates. Atomic hydrogen surely played an important role to promote reactions in making Si-network, and enabled to obtain higher concentration of impurity doping and thicker growth of epitaxial films. The reason is considered its strong chemical affinity for silicon. The behaviors in making Si-network observed from the precursors, SiH_nF_m, generated by the plasma-induced decomposition of SiF_4, fluorinated compounds, was known quite different from those observed from the other precursors, SiH_n, generated in the similar manner from SiH_4 [125)]. The chemical activity of those fluorinated radicals are supposed to be greatly reduced due to its strong electron negativity of fluorine. In fact, these precursors were able to be carried as the gaseous mixture to a rather long distance apart from the plasma region where they are generated, typically as shown in Figure 2.1 (a). Fluorine bound strongly with silicon is

predominantly released as the form of HF to make Si-Si bonds, and thus only hydrogen remains in the rigid Si-network. In a pre-examination for hydrogen content remained in films on a glass substrate as a function of the hydrogen flow rate, the hydrogen content was reduced monotonically with increase of the flow rate [126)]. And it was found that crystallization appears suddenly at around 5 at. % of the hydrogen content. An idea that quasi-chemical equilibrium is establishes in the vicinity of the growing surface by impinging atomic hydrogen is led by the evidence that there was a tight relationship between the hydrogen content and the crystallization. The reactions for making Si-Si bonds are considered to be equilibrated by the reverse reactions for initiated by the strain stored in the films resulting from reduction of the hydrogen content. This idea is also supported by the evidence that the disorder in the bond angle measured by the Raman scattering was systematically reduced with the reduction in hydrogen content in μc-Si films as shown in Figure 2.10.

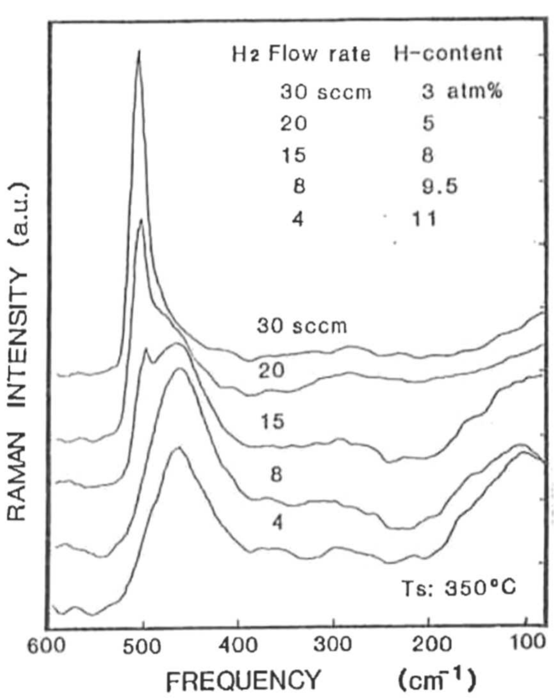


Figure 2.10 Raman scattering spectra for μc-Si films
with different hydrogen content

[†1] *Reproduced partially from "H. Tanabe, M. Azuma, T. Uematsu, H. Shirai, J. Hanna, and I Shimizu, Growth of crystalline silicon, microcrystalline and epitaxial at low substrate temperature, Mat. Res. Soc. Symp. Proc., vol. 149, pp. 17-22, (1989)," with the copyright permission of Cambridge University Press.*

2.7 Summary

In this chapter, the author demonstrated that the supply of a large amount of atomic hydrogen to the growth surface certainly promotes two-dimensional crystalline growth at low-temperature around 350 °C even though increasing both thickness to be more than 1 μm and doping concentration. The behaviors for crystalline growth at low temperature employing the HR-CVD are concluded as follows. By utilizing a conventional coaxial microwave plasma reactor;

- Epitaxial growth was demonstrated on the Si (110) and (100). The growth rate reached to be 1.5 nm/sec, that was almost equivalent to that of μc-Si films on a glass substrate.
- The crystalline structure was deteriorated as increasing thickness.
- Impurity doping was also demonstrated. However, the crystalline structure was also deteriorated as increasing impurity concentration.
- There was an optimum temperature range of about 300-350 °C in the epitaxial growth.

It was considered that not only the kinetic energy supplied from the substrate temperature but also the balances of the chemical reactions played an important role in this growth process. Therefore, an additional microwave plasma reactor named "cavity" was then introduced to supply atomic hydrogen into growth surface independently from the conventional coaxial microwave plasma reactor. As the results;

- The supply of additional hydrogen effectively promoted the epitaxial growth even increasing both thickness and doping concentration.
- The highest temperature for epitaxial growth was extended to be 400 °C and also the optimum temperature decreased to be 300 °C
- The highest electron Hall mobility was obtained to be 115 cm^2/Vsec with the carrier concentration of 2×10^{16} cm^{-3} in the epitaxially grown P-doped silicon film.

2.8 Future prospects

Two-dimensional epitaxial growth on single crystalline substrate were demonstrated as described above. Following this studies, several attempts employing fluorine based gas sources [127)128)] or high-density plasma [129)] were reported. However, they have not been practically used in industry yet. There still remain two major approaches in order to extend this technique to the large-grained crystalline film formation on a glass substrate resulting the large-area microelectronics.

The one is the microscopic aspect that another technique is necessary to control the nucleation process instead of crystalline substrates employed in this study. On the

glass substrate, the island-like growth may be a dominant in making films with the SiHnFm because of the strong terminating function of fluorine. In other words, quite a lot of islands are seeded on the glass surface simultaneously. Those behaviors limit the enlargement for the grain because the distance among islands could be very short and the crystalline orientation of those could be random. Thus, further approach is expected, either reducing the nucleation site, i.e. number of islands, or aligning the orientation of those island, in order to obtain the large-grained crystalline films on a glass substrate.

The other one is the macroscopic aspect that an equipment is necessary to deposit those films on a large substrate. In now days, large size substrates with more than meters square are utilized in production. The PE-CVD equipment is also popular, but it conventionally employs a plasma generator with radio-frequency (RF). In this study, a microwave generator was used as a plasma source because it could generate hydrogen radicals three orders of magnitude more than RF plasma [114]. The advantage of the microwave plasma to generate hydrogen radicals are that the gas is free of contamination from the electrodes and that high density of hydrogen atoms can be produced [130]. In contrast, there is a disadvantage to expand the size of plasma region. Therefore, a novel apparatus supplying hydrogen radicals to large area is anticipated to be developed.

3. Low-temperature crystallization of silicon thin-films

3.1 Solid phase growth: selective nucleation and grain-boundary filtration

This section states on a grain boundary filtration technique of Ge (germanium) and Si through planar constrictions for unseeded fabrication of single grain semiconductor films on amorphous substrates by using patterned amorphous films with metal-induced selective-nucleation and solid-phase-epitaxy (SNSPE). The concept is proposed as follows. The patters consist of a small island-like seed region including a metal induced selective nucleation site, a narrow seed selection region and a single grain region consisting of a main rectangular island. Lateral epitaxy initiates at the edge of the selective nucleation site and the grain selection process through the narrow seed selection region choose only one grain orientation at the entrance of the main island. Growth front of the lateral epitaxy goes into the main island region while competing with spontaneous nucleation. Single grain region as large as 100 μm^2 with only a few low-angle boundaries were demonstrated in the case of Ge. In contrast, in the case of Si, SNSPE of more than several micrometers of grain growth was successfully demonstrated, however, grain boundary filtration did not seem to be enough. It could be caused by less concentration of metal in the seed selection region and unique mechanism for crystalline growth.

3.1.1 Previous research and objectives

Pioneered study for the solid phase epitaxy (SPE) with transport media goes back to 1970's as described in subsection 1.3.2. In those days, variety of metal-semiconductor combinations, such Al-Ge, Al-Si, Ag-Si, Au-Si as eutectic systems and such Pd-Si, Ni-Si as compound forming systems, were already investigated [131]. As it had the feature that the transport media can reduce the temperature for the crystalline growth happen as reported by Liu and Fonash [132][133], it was attracted attentions again in late 1980's to apply it to low-temperature crystallization of amorphous films on foreign substrate. The advantage of solid phase crystallization (SPC) is to obtain large crystalline grains regardless of with/without transport media. On the other hand, electrical properties of grain boundary are quite less performance than that inside grains. Thus, location of the grains should be coincident with the region to form channel in order to obtain uniform performance of poly-Si TFTs. To control the location of the grains, Chen and Atwater proposed Pd induced selective-nucleation (SE) and SPE in Si films for photovoltaic applications [134]. And they successfully demonstrated to obtain location controlled grains

with sizes of 10 μm at 620 °C on thermally grown SiO_2. The SNSPE process, one of the techniques for controlling nucleation to obtain large grain crystalline films, exploits the thermodynamic barrier to nucleation whose origin lies in the size dependence of the surface and volume contributions to the crystal free energy. The existence of a nucleation barrier results in a temporal delay in growth of small crystals to macroscopic size. At the onset of the transformation, there will be a finite incubation time during which no crystal nucleation occurs before the onset of steady state nucleation as illustrated in Figure 3.1. If there are heterogeneous nucleation sites, i.e. selective nucleation sites, present, these can lower the thermodynamic barrier to nucleation. In this case, a growing small crystal will be enlarged by annealing during the incubation time without competition from random nucleation. Figure 3.2 illustrates the idea. The achievable grain size (R) can be estimated as the product of the incubation time (T_{inc}) and the lateral solid phase epitaxy rate (V_{SPE}) during SNSPE.

$$R = V_{SPE} \times T_{inc}$$

Ideally, the selective nucleation region would be a single crystal, but it is difficult to achieve in practice, Metal induced nucleation yields a large number of nanometer-scale crystalline grains in each seed region, and since lateral epitaxy starts at the periphery of each selective nucleation site, in general multiple grains are produced from each nucleation site [100].

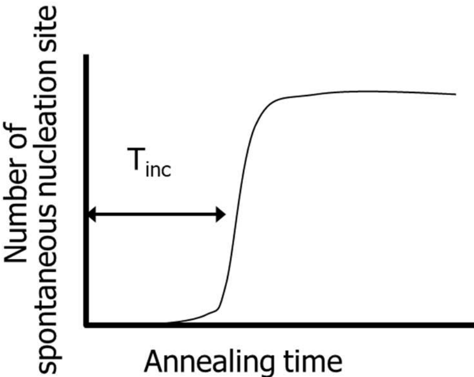


Figure 3.1 The number of spontaneous nucleation site depending on annealing time

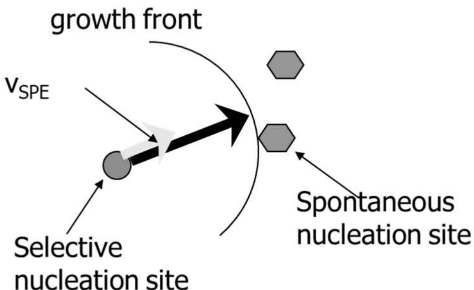


Figure 3.2 An illustration that crystalline growth from a selective nucleation site during the incubation time without competition from spontaneous nucleation

There were still scopes for improvement, however, to apply it to poly-Si TFTs. The one was simply to reduce process temperature to be able to apply conventional glass substrates. The other was to fabricate single crystal grains in order to obtain better electrical characteristics. Regarding the former one, besides Pd, Ni was a candidate to reduce the temperature for nucleation and growth of Si [135-138]. Selectively formed Ni films were reported to be effective as seed regions on silicon films [99] in addition to Pd [98]. $NiSi_2$, a formed compound as silicide, was also known to grow on Si with the lowest lattice mismatch of 0.4 % [138]. And regarding the latter one, grain boundary filtration techniques was demonstrated in the zone-melted solidification process in 1982 [107] and was also attempt to excimer laser crystallization of Si in 1996 [139].

The objective of this section was to demonstrate the grain boundary filtration technique under SNSPE, First, a grain boundary filtration technique by using planar constrictions in patterned films during SNSPE of Ge are proposed and demonstrated. Large grain polycrystalline Ge (Poly-Ge) may be a useful as a template for GaAs hetero-epitaxy in optoelectronic and photovoltaic devices, and it also serve as a model for similar techniques applied to Si films. Then, similar techniques are applied to Si films and discussed in this work.

3.1.2 Concept for grain boundary filtration technique †2

In the present study, the patterns consist of (i) a small Ge island seed region including metal-deposited selective nucleation site, (ii) a narrow seed selection region that connects the seed region and a following single grain region and (iii) the single grain region consisting of the main rectangular island, as illustrated in Figure 3.3. In region (i), lateral SPE of Ge starts at the edge of the selective nucleation site and SPE continues in all directions with a variety of orientations. The growth of almost all grains is terminated at the pattern edge of region (i), but a few grains survive to grow into the seed

selection region. Further grain selection occurs in the seed selection region (ii) and only one grain orientation is able to reach region (iii). Consequently, the main island has a single crystal seed and the region is crystallized laterally as shown in Figures 2.13 (a) and 2.13 (b).

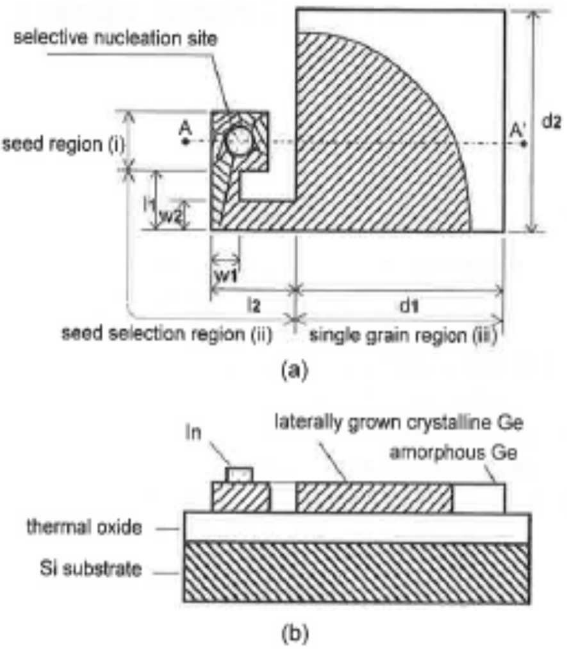


Figure 3.3 (a) Plan view schematic of the pattern employed for grain boundary filtration, and (b) Cross-sectional view od A-A’

3.1.3 Grain boundary filtration for Ge films †2

In this study for Ge, 100 nm-thick-amorphous Ge films were deposited by ultra-high vacuum electron beam evaporation onto cleaned, thermally-grown 100 nm silicon dioxide films on Si (100) substrates. Phosphorous doping by ion implantation at 50 keV to a dose of 2 x 10^{15} cm^{-2} yielded a calculated peak phosphorous concentration [140)] of 0.7 at. %. Then photolithography and wet etching with an $HF/HNO_3/H_2O$ (=1/20/40) solution were employed to define mesa islands of the a-Ge film on SiO_2. The size of the mesa islands was smaller than the mask pattern size because the islands were over-etched in the process. As shown in Figure 3.4, the seed selection region is typically 1.5 um in width (= w1 = w2) and 10 µm in length (= l1 + l2) and the main island was designed to be between 5 × 5 µm and 45 × 45µm in size (= d1 × d2). Indium was used for the study of Ge, referring to the prior work done by Yang et al. A 20-nm-thick In film, used for selective nucleation regions, was deposited by high vacuum evaporation onto the Ge films covered with patterned photo-resist. A lift-off process was performed to define In islands of 2 µm diameter. After those preparation steps, samples were annealed at

400 °C for several time steps. Lateral growth was investigated at each annealing step by using optical-microscopy or transmission electron microscopy (TEM). TEM specimens were prepared by back etching the Si substrate using an $HF/HNO_3/H_2O$ solution after the first annealing step.

Table 3.1 Preparation conditions for Ge samples

Semiconductor material	a-Ge
Deposition tool	MBD
Thickness (nm)	100
Dopant	P
Dose (cm^{-2})	2×10^{15}
Seed material	In, evaporated
Thickness (nm)	20
Anneal temp.(°C)	400

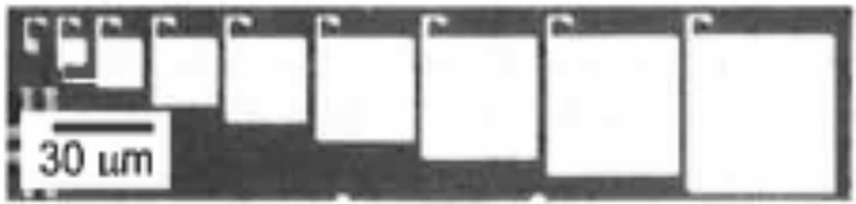


Figure 3.4 Optical micrograph of mesa patterns defined in amorphous Ge for grain boundary filtration.

Figure 3.5 shows a series of plan-view TEM photographs of Ge after 400 °C annealed for (a) 663, (b) 976 and (c) 1293 min. Also electron diffraction patterns are shown, of (d) selective nucleation site, (e) seed selection region, (f) seed area for single grain region, (g) center of single grain region, (h) growth front and (i) and (j) two corners. The location and area for the electron diffraction observations are shown as dotted circles in Figure 3.5 (c). The incident angle of the electron beam used for the diffraction patterns was approximately perpendicular to the sample, but it was not precisely aligned, owing to bending of the thin film specimen after back-etching. Figure 3.5 (a) reveals a large number of fine grains in the selective nucleation site and a ring-like electron diffraction pattern corresponding to Poly-Ge as shown in Figure 3.5 (d). Lateral grain growth in all directions with a variety of orientations started at the edge of the selective nucleation site and the number of grains was reduced in the seed selection region as shown in Figure 3.5

(e), which has no ring pattern. In this seed selection region, the fastest-growing orientation is selected. After the growth front passes through the seed selection region, it is able to expand into the single grain main island as shown in Figure 3.5 (b). The area indicated by the diffraction pattern of Figure 3.5 (f) acts as the seed for the single grain region. The diffraction pattern of Figure 3.5 (f) indicates successful demonstration for single grain seeding of the main island.

With further annealing, lateral seed growth must compete with spontaneous nucleation in the a-Ge film because SNSPE has to be completed within the incubation time for spontaneous nucleation. The lateral SPE rate at 400 °C estimated from Figure 3.5 (a), (b) and (c) is 2.9×10^{-4} μm/second. As shown in Figure 3.5 (c), no spontaneous nucleation was observed and the entire crystallized area was laterally grown continuously from the seed of the selective nucleation site. The electron diffraction patterns of Figure 3.5 (f), (g), (h), (i) and (j) also show the single grain region has no polycrystalline components. These results demonstrate that locally controlled large (> 100 μm^2) Ge single crystal films can be obtained by using the SNSPE through planar constrictions. For other patterns with different shapes and larger main islands than those illustrated in Figure 3.5, spontaneous nucleation competing with SNSPE was also observed, as shown in Figure 3.6. This suggests that the annealing time of 1293 min. is almost equal to the incubation time at 400 °C for amorphous Ge films. A maximum achievable grain size of 20 μm radius in this phosphorous doped Ge film can be estimated ideally by products of the SPE rate mentioned above and an incubation time of 1200 min.

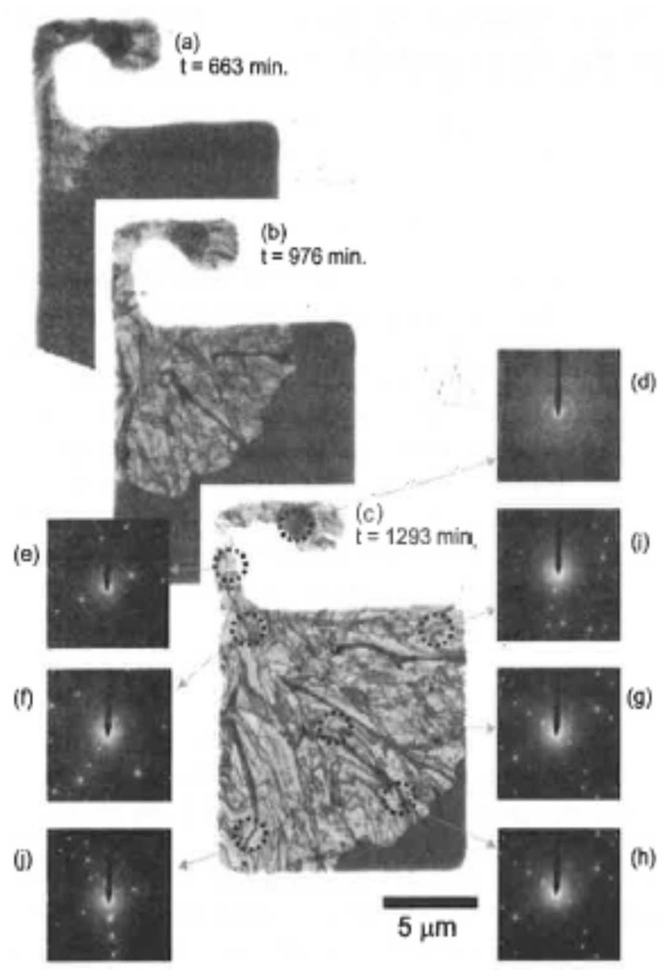


Figure 3.5 Plan view transmission electron microphotographs and selected area diffracted patterns for partially crystallized films after each 400 °C anneal.

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†2 *Reproduced from "Hiroshi Tanabe, Claudine M. Chen and Harry A. Atwater, Grain boundary filtration by selective nucleation and solid phase epitaxy of Ge through planar constructions, Applied Physics Letters, vol. 77, pp. 4325-4327, (2000)," with the permission of AIP Publishing"*

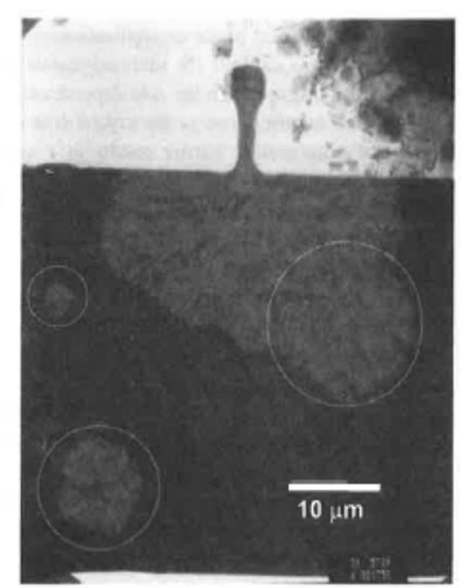


Figure 3.6 Example of spontaneous nucleation (circumscribed by dotted lines) and patterned selective nucleation in a larger Ge island following a 400 °C anneal for 1293 min.

3.1.4 Grain boundary filtration for Si films

In this another study for Si, 75 nm-thick-amorphous Si films were deposited by low-pressure chemical vapor deposition (LP-CVD) onto cleaned, thermally-grown 100 nm silicon dioxide films on Si (100) substrates. These films were not intentionally doped. Then photolithography and wet etching with an $HF/HNO_3/H_2O$ (=1/20/40) solution were used to define mesa islands of the a-Si film on SiO_2. Those samples were implanted in the selective nucleation region with nickel at an energy of 40 keV, with dose of 1×10^{16} cm^{-2}. Also for those samples, the implantation energy was chosen to give the peak of Ni atoms at depth of half the a-Si film thickness. One of the most important reason why Ni was employed for the study of Si was it has the lowest lattice mismatch with Si to be -0.4% among candidates to form silicide, such as Pd (100), Pt (200), Ni (200) and Co (350). It was also one of the reason why Ni was employed that lateral growth rate of Ni mediated crystallization was higher than that of In. Figure 3.7 shows lateral growth rate mediated with Ni and In. It was found that the rate with Ni is more than one order larger than that with In. To remove any organic and other metallic contaminants, all the samples were cleaned with adequate solutions, respectively. Annealing was then carried out in a vacuum furnace, operating at pressures of about 1×10^{-7} Torr, at temperatures ranging between 550 and 620 °C. Lateral growth was investigated at each annealing step, as with the study for Ge, by using optical-microscopy or transmission electron microscopy (TEM).

Table 3.2 Preparation conditions for Si samples

Semiconductor material	a-Si	a-Si
Deposition tool	MBD	LPCVD
Thickness (nm)	100	75
Dopant	undoped	undoped
Seed material	In	Ni
Concentration (cm^{-3})	4.7×10^{21}	1.3×10^{21}

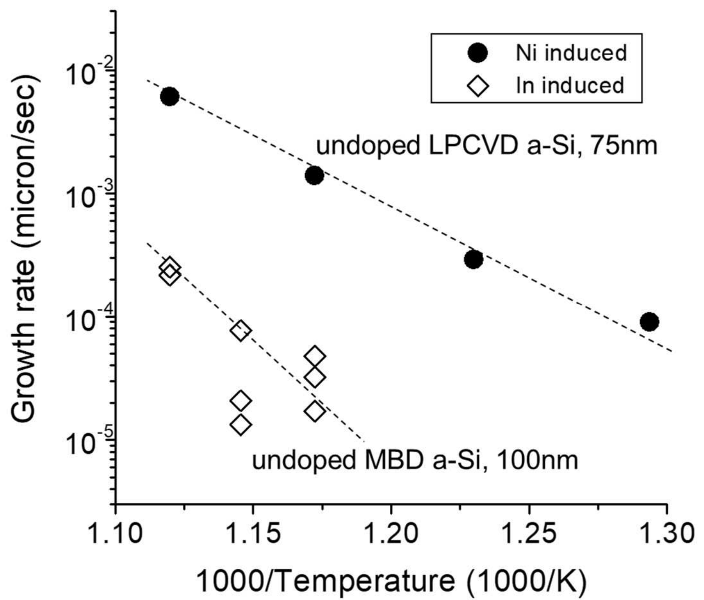


Figure 3.7 Lateral growth rate of Si mediated with Ni and In.

Crystallization of the Si films was first observed by optical microscopy. Figure 3.8 shows Optical micrographs of Si samples after annealing at (a) 500 °C, 787min, (b) 540 °C, 300min, (c) 580 °C, 127min, and (d) 620 °C, 30min, respectively. The patterns for planer constrictions was slightly different from the one used in Ge. The patterns consisted of two sets of a small Si island seed region including a Ni implanted selective nucleation site and a narrow seed selection region with straight shape, and a main rectangular island. The seed selection regions were connected to the upper and the bottom parts of the main island, respectively. The bright parts starting near each set of two seed

regions indicate the crystallized Si, while the dark parts the amorphous Si. Several micrometers of lateral growth were observed in the samples shown in Figure 3.8 (c) and (d). Figure 3.9 shows plan view TEM images after 620 °C anneals of (a) the seed selection region and (b) the main island region. The location for electron diffraction patterns are shown by arrows in Figure 3.9. Lateral grain growth started near the selective nucleation site, and as shown in Figure 3.9 (c) and (d), the similar spot patterns with each other were observed in the seed selection region. In contrast, the spot patterns were observed to be slightly blurred as shown in Figure 3.9 (e). There might be existence of disorders in crystalline even if it was not polycrystalline. Those results suggested that the "crystallinity" of the seed selection region was superior than that of the main island even though the grain selection occurred in the seed selection region. It may mean that the crystallinity was worsen during the grain growth process in the main region.

This is considered because there are two possible reasons. The one is that the concentration of Ni in the seed selection region is larger than that in the main island. Silicide mediated crystallization in the seed selection region was promoted by enough amounts of Ni supplied from seed region. It is considered that the concentration was not enough to promote the silicide mediated crystallization because the growth front was expanding wider after the lateral grain growth reached to main island. This idea is supported by the facts that the SPE rate and achievable grain size with SPE were enhanced with dosage of Ni into the seed region. The other reason is suggested by needle-like growth unique to Ni mediated crystallization. Small regions of a-Si embedded in the crystalline phase can be observed, consistent with a Ni mediated crystallization mechanism via migration of $NiSi_2$ precipitates, at the amorphous crystal interface, that catalyze the transition. Those precipitates migrate in the a-Si also for several micrometers during annealing at temperatures higher than 500 °C, leaving behind a narrow needle of c-Si. When two crystallized needles collide each other, the growth is stopped and results in leaving amorphous regions around the needle-like crystalline grains. This idea is also supported by the TEM image of the growth front consisting of the needle-like morphology shown in Figure 3.10.

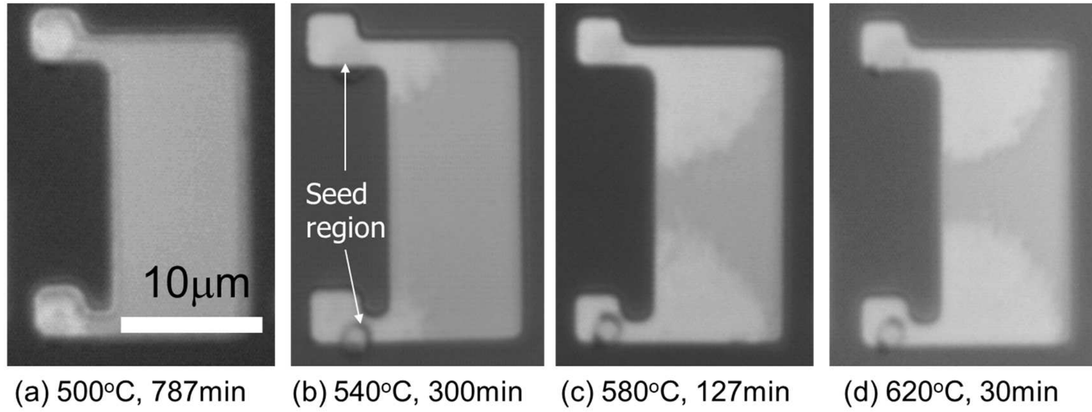


Figure 3.8 Optical micrographs of Si samples after annealing at (a) 500 ℃, 787min, (b) 540 ℃, 300min, (c) 580 ℃, 127min, and (d) 620 ℃, 30min, respectively. The bright parts starting near each set of two seed regions indicate the crystallized Si, while the dark parts the amorphous Si

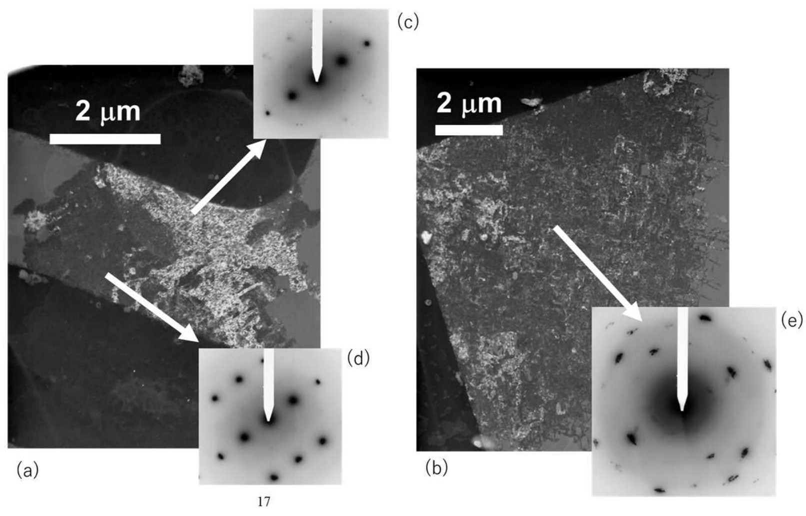


Figure 3.9 Plan view transmission electron microphotographs and selected area diffracted patterns for partially crystallized films after each 620 ℃ anneal. (a) Seed selection region, (b) main island region

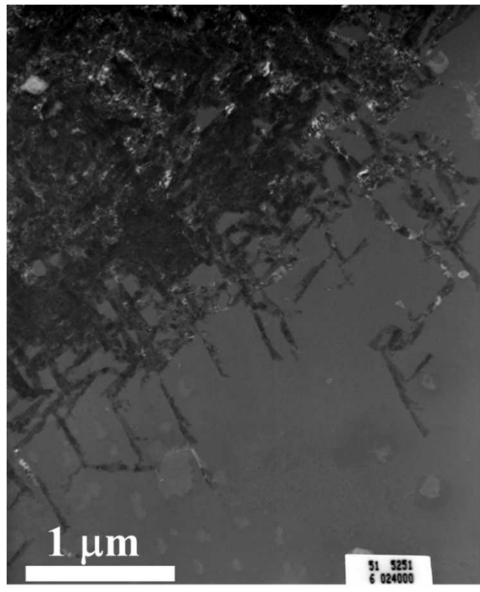


Figure 3.10 Plan view transmission electron microphotographs for the growth front.

3.1.5 Summary for the solid phase crystallization

In this section, the author proposed and demonstrated a grain boundary filtration technique for fabricating single large grain semiconductor thin films on amorphous substrates by using selective-nucleation and lateral solid-phase-epitaxy (SNSPE). In the study of Ge, the patterns consist of a small Ge island seed region including a metal-deposited selective nucleation site, a narrow seed selection region and a single grain region consisting of a main rectangular island. TEM photographs revealed that lateral SPE started at the edge of the selective nucleation site and the grain selection process produced only one grain orientation at the entrance to the main rectangular island. Moreover, TEM and electron diffraction analysis revealed the presence of only a few low-angle boundaries in the lateral SPE region. A single planar grain which is larger than 100 μm^2 was successfully crystallized at 400 °C in approximately 1300 min. without any occurrence of spontaneous nucleation. A maximum grain size of 20 μm radius can be achieved at 400 °C based on estimates of the product of the 2.9×10^{-4} μm/sec SPE rate and the 1200 min. incubation time for spontaneous nucleation. During these experiments, low annealing temperatures and long annealing times were chosen to optimize the maximum achievable grain size. Based on the previous work on SNSPE [100)], it is anticipated that the same grain boundary filtration process can be achieved with much shorter annealing times (< 60 min) for annealing temperatures in the range of 400-500 °C, although the maximum achievable grain size may be slightly smaller.

In another study of Si, Ni implantation was employed to form seed region and similar grain boundary filtration technique based on the SNSPE method was attempted. As a result of SNSPE, more than several micrometers of grain growth was successfully demonstrated at around 600 °C, that is applicable conventional glass substrates. As another result with the planer constrictions, however, grain boundary filtration did not seem to be enough. There were two possible reasons. The one is that the concentration of Ni in the seed selection region was not enough to promote the silicide mediated crystallization further because the growth front was expanding wider after the lateral grain growth reached to main island. The other is corresponding to the needle-like growth mechanism unique to Ni mediated crystallization. When two crystallized needles collide each other, the growth is stopped and results in leaving amorphous regions around the needle-like crystalline grains. It was found that the crystallinity was deteriorated near the growth front even if the grain boundary filtration could be successfully achieved.

3.1.6 Future prospects

There still remain some challenges to apply the grain boundary filtration technique to Si films because of unique feature of $NiSi_2$ mediated crystallization. Following this study, co-workers of the author investigated details of Ni-induced SNSPE. According to that results, relatively high-temperature was still necessary to obtain larger grain poly-Si films [141)142)]. Also, the needle-like growth-fronts branched to variety of angles might leave non-crystallized region in the film. It could be eliminated if a large amount of Ni was provided to SN site. However, in that case, behavior of high concentration of Ni as impurity could be concerned. In almost same period of this study, for instance, a research group was attempt to employ laser recrystallization for Ni-induced crystallized poly-Si films, and it suggested to need improvement of the crystalline quality [143)144)]. The group also reported that gettering process was necessary to reduce the residue of Ni, i.e. to suppress leakage current of TFTs originated from Ni as impurity [145)146)]. Those results suggest that an investigation for other metals to replace Ni is necessary to fabricate high-quality crystalline Si films through solid phase at low-temperature.

3.2 Liquid phase growth: excimer laser induced melt-solidification

This section describes investigation results for excimer laser crystallization of a-Si thin-films, especially for resulting microstructure as functions of both irradiation energy and the number of irradiation pulses, and for the influence of the use of such

polycrystalline films in thin-film transistors (TFTs). The microstructure in the films obtained was strongly depending on the irradiation energy. The results of microscopic observation and cooling rate simulation suggested that increase of grain size depending on irradiation energy was supported by the decrease of cooling rate at near melting point, and also that abrupt decrease of the grain size at high energy range was explained by the increase of cooling rate at maximum during solidification. The microstructure in the films obtained was strongly depending on the irradiation energy. In contrast, although the number of irradiation pulses did not affect grain size obtained by microscopic study, that promoted to decrease defects, including small grains, grain boundaries and defects inside grains.

3.2.1 Previous researches and objectives

As stated in subsection 1.3.3, the initial study in this area can be found in the brief report by Laff and Hutchins [55)] in 1974. While both CW and pulsed lasers had been used and investigated to form crystalline Si films since then. The turning-point was when Sameshima et al. reported TFTs by using excimer laser crystallization. The group presented the potential of XeCl excimer laser (308 nm) to fabricate high quality poly-Si films on a plane glass substrate. They reported the channel mobility of n-channel TFTs employed poly-Si films crystallized by XeCl excimer laser reached to 180 $cm^2/Vsec$ [91)]. With this as a trigger, there were many studies started to apply the excimer laser to the large-area microelectronics devices. Regarding laser sources, not only excimer lasers, such as XeCl [108)], KrF (249 nm) [147)148)] and ArF (193 nm) [149)], but also Ar laser [150)] were studied for fabrication of poly-Si films. In order to understand the phenomena during melt-solidification induced by nanosecond lasers, there were some approaches focused on transient-time measurements, such as transient thermometry [151)], transient conductance [152)] and transient reflectivity [153-155)] as well as other approaches focused on microscopic observation by Scanning Electron Microscope (SEM) and Transmission Electron Microscopy (TEM).

In those prior studies, much efforts were devoted to investigate the dependence of irradiation energy, but there were not so many studies focused on the dependency of the number of irradiation pulses [156)]. The quality of excimer-laser-crystallized Si film strongly depends on such crystallization conditions as energy density and the number of laser shots. The grain sizes of the Si films, in particular, increase with energy density, starting at the melting threshold of Si films and the size reaches a maximum value. Then the grain size sharply decreases in the excess energy range [157)158)]. This phenomenon is called amorphization [159)] or micro-crystallization, and it obstructs formation of over-

micrometer sized single-grain films. However, it still remains to be understand what factor might control the crystallization conditions, especially in micro-crystallization. While the effects of energy density on the melt-crystallization process (a process of temperature rise and fall) have been studied to a significant degree, especially to the microstructure obtained as the results, it also remains to be determined precisely what effects might be produced by a series of laser shots, i.e. what film properties might change, and just how they might change, as a function of the number of shots.

The objective of this section is to study details in concerning the effects, as a function of the number of laser shots as well as the energy density, on the properties of poly-Si film and on poly-Si TFT characteristics. Structural studies were made by means of Scanning Electron Microscope (SEM), Transmission Electron Microscopy (TEM), Raman spectroscopy and Secondary Ion Mass Spectroscopy (SIMS). TFT characteristics employed those films were also investigated to understand the relations with the process conditions resulted in those microstructures. In addition to those structural studies, this section also describes the studies for transient temperature during the excimer laser crystallization by using a finite element analysis system. The author focus on the cooling rate just before the solidification of the molten Si and discuss its correlation with consequent film properties.

3.2.2 Experimental procedures

Low-pressure chemical vapor deposited (LP-CVD) amorphous silicon (a-Si) films on quartz substrates were laser crystallized with an NEC excimer laser crystallization system XL-561, shown schematically in Figure 3.11. The system was equipped with an NEC XL-120B XeCl excimer laser having an energy output of 200 mJ at a wavelength of 308 nm. The laser beam, focused on the Si surface through a beam homogenizer, an aperture mask and an imaging lens, was 5×5 mm^2 on the surface of the sample and was clocked at 10 Hz. The films were crystallized in argon at room temperature. Figure 3.12 shows (a) a typical intensity profile, whose uniformity at the center of the beam was within ± 5%, (b) the waveform of the pulse actually measured. In this study, so-called beam-overlapping method [91)108)] wasn't employed in order to avoid the influence of the beam edge, which is a consideration in multiple-shot irradiation; i.e., the author evaluated the films that were crystallized by the flat-top area of the beam.

The electrical properties of these films were obtained from the TFT characteristics. The channel width/length were 6/6 μm. The fabrication process for the TFTs, which has a staggered-type structure, is described below. Figure 3.13 shows the fabrication process for an n-channel poly-Si TFT. The TFT was fabricated on a quartz

substrate at low temperature, below 600 °C. (a) A sputtered tungsten-silicide (WSi_2) layer was employed for source and drain metallization. The source/drain regions were n^+ poly-Si layers prepared by the ion implantation method. (b) The active layer was an a-Si layer deposited by LP-CVD and crystallized by XeCl excimer laser, as described above. (c) After crystallization, the poly-Si film was plasma etched to define the island pattern. The gate insulator was a SiO_2 film deposited by LP-CVD. (d) An aluminum layer was formed for gate and source-drain metallization. Grain boundary passivation was accomplished by using hydrogen plasma [160-162].

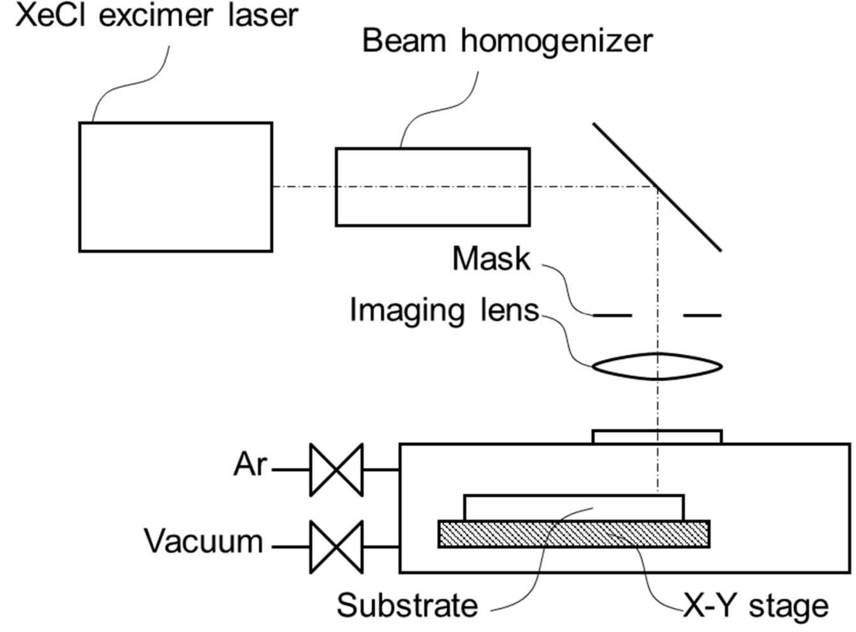


Figure 3.11 Schematic drawing of the excimer laser crystallization system

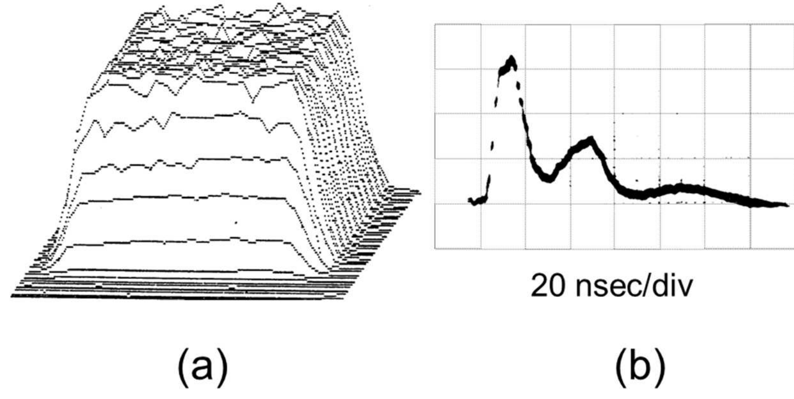
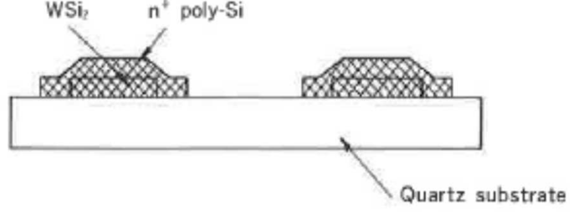
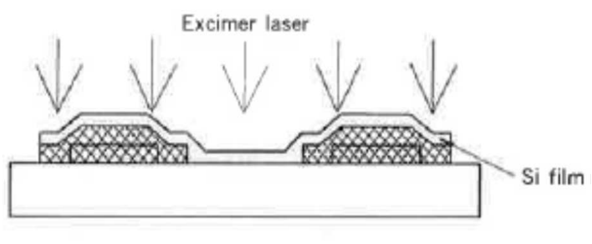


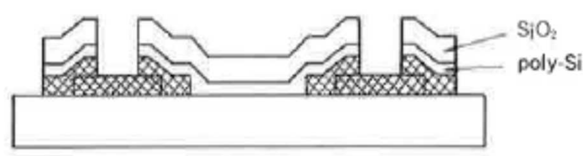
Figure 3.12 (a) A typical intensity profile, whose uniformity at the center of the beam was within ±5 %, (b) the waveform of the pulse actually measured



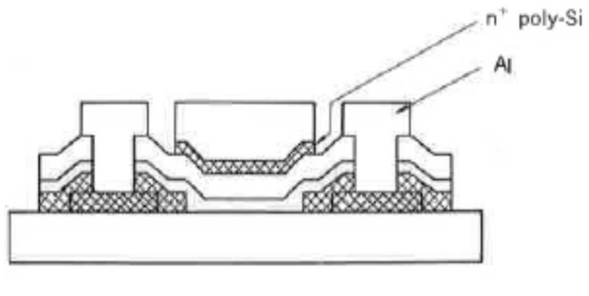
(a) Source/drain region.



(b) Active layer.



(c) Gate insulator/contact hole.



(d) Metallization.

Figure 3.13 Process sequence for n-channel poly-Si TFT fabrication by using excimer laser crystallization. (typical W/L = 6/6 μm)

3.2.3 Irradiation energy dependency

Figure 3.14 shows SEM microphotographs obtained from the Si films. Those

films were prepared by the laser irradiation of 1, 3, 10, 20 and 50 shots at energy densities of 339, 424 and 521 mJ/cm^2, respectively [163)164)]. In order to delineate the grain-boundary, a crystallographic etching process called "Secco-etch" [165)] was performed before the SEM observation. In the samples irradiated by the single shot, grain size increased with energy density; however, in the sample irradiated at 521 mJ/cm^2, we found that the grain size had greatly decreased and that some fractions of the film had been etched away. These results suggest that micro-crystallization occurred during irradiation at 521 mJ/cm^2. With respect to the samples irradiated by three shots, both large grains and micro-crystallized region were observed in the 521 mJ/cm^2 sample. In contrast, there were no significant differences between 1 and 50 shots at energy densities of 339 and 424 mJ/cm^2 except for that relatively larger grains were observed in the 521 mJ/cm^2 sample with 50 shots. The SEM observations suggested that the energy density affects dramatically on crystallographic variation in Si films more than the number of irradiations. Figure 3.15 plots grain size dependency on the irradiation energy density under the number of shot to be 20, that was estimated by SEM images [158)]. The grain size monotonically increased from 40 to 600 nm with the energy density, between 324 and 521 mJ/cm^2.

Figure 3.16 shows the variation in electron mobility versus the energy density at which the Si films were crystallized [166)167)]. The number of shots was three. The mobility, estimated from TFT (Id-Vg) characteristics, increased monotonically with energy density, with maximum mobility being obtained at about 450 mJ/cm^2. The increase in electron mobility corresponds to the enlargement of grain size. The mobility decreased dramatically in the higher energy region, even though larger grains were observed in the sample of 521 mJ/cm^2. It is considered that the existence of the micro-crystallized region prevented the carrier transport. The electrical properties were varied as a function of irradiation energy as described above. It was consistent with that the grain size increased with the irradiation energy as shown in Figure 3.14. An interest, however, has been remained in the mobility drop in higher energy range. In order to study the phenomena in that range, numerical thermal analysis was performed.

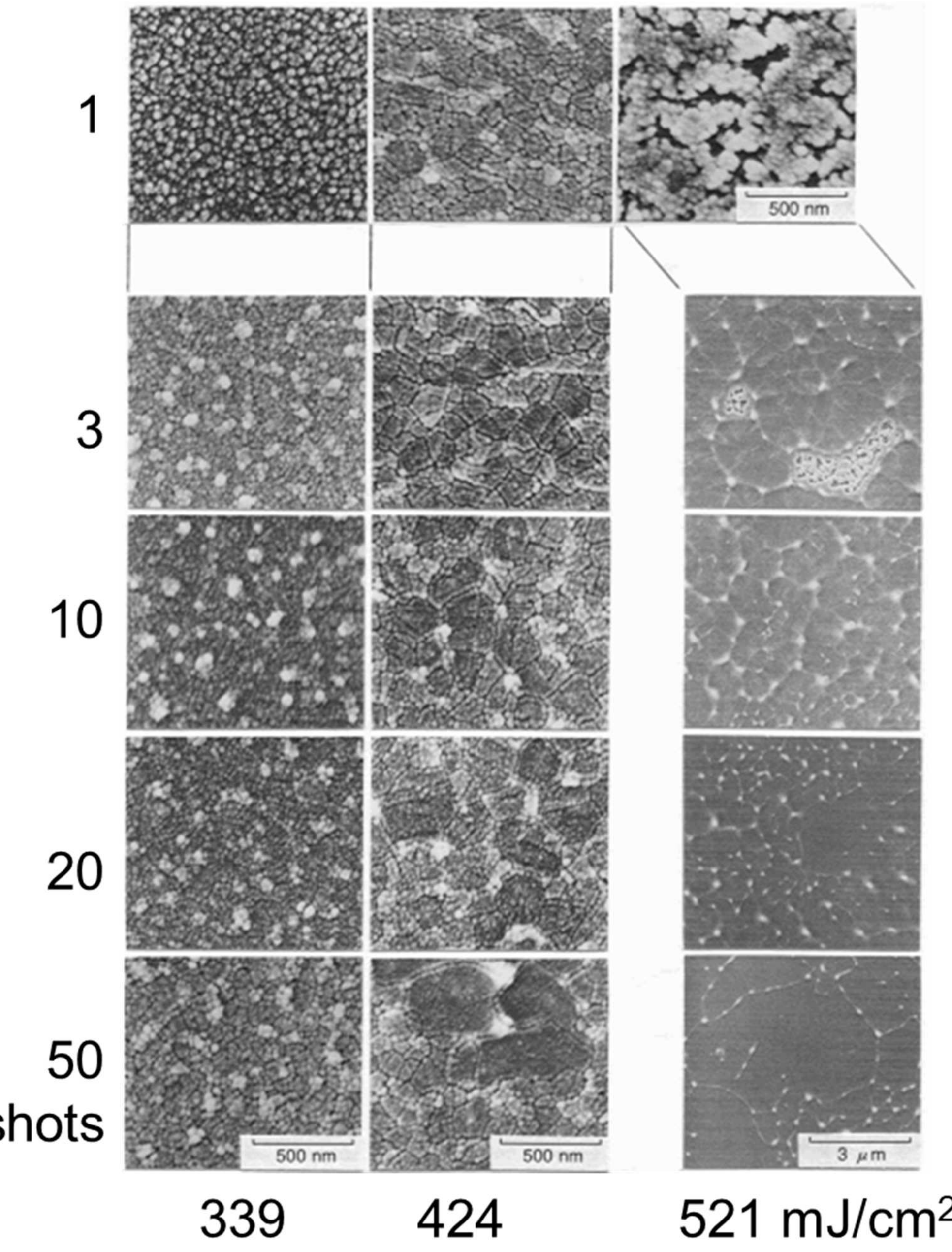


Figure 3.14 Microphotographs of obtained from SEM of Si films Secco-etched. Those films were prepared by the laser irradiation of 1, 3, 10, 20 and 50 shots at energy density of 339, 424, 521 mJ/cm^2, respectively [163)].

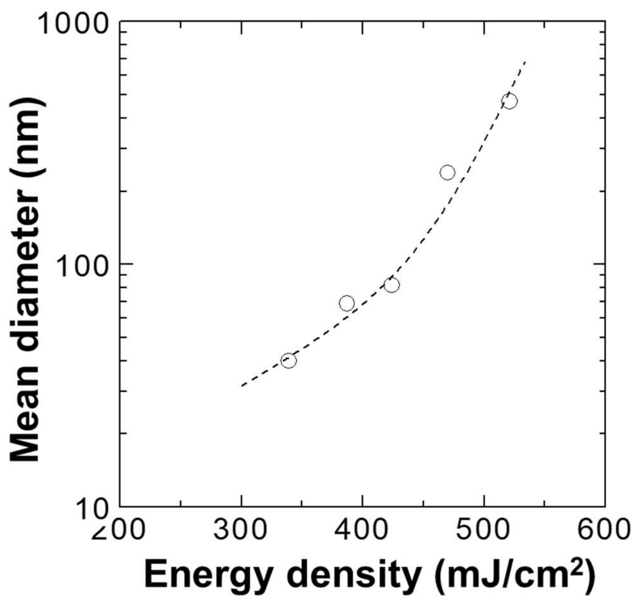


Figure 3.15 Grain size dependency on the irradiation energy density [158].

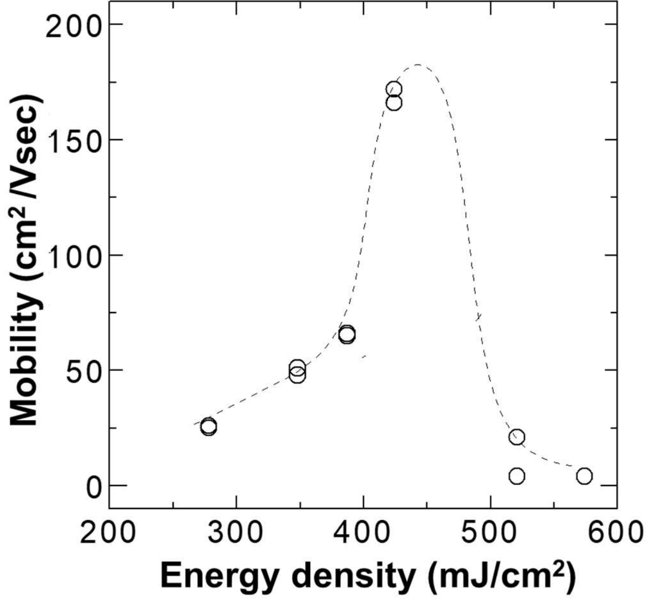


Figure 3.16 Variation in electron mobility with respect to energy density at which Si films were crystallized with 3 shots [166].

3.2.4 Thermal analysis

Numerical thermal analysis was performed by using a finite element analysis system COSMOS/M^{+}. The one-dimensional structure used for the analysis was Si (75

nm)/ substrate (SiO_2: 30 μm). The substrate was assumed to be SiO_2 in these simulations. The difference in thickness between simulation and experiment (1.1 mm) can be ignored because we confirmed that it has hardly any effect on the simulation results obtained. The parameters used in this simulation are shown in Table 3.3 [168)169)]. The author modified the values of specific heat that were around the temperatures for phase transformations to take account of latent heat in this analysis system. Also the waveforms shown in Figure 3.17 [166)] were used as the loading conditions. In addition to the waveform for XeCl excimer laser simplified of the pulse actually measured as shown in Figure 3.12 (b), the one for KrF excimer laser manufactured by Cymer was also illustrated in order to compare with each other.

[+]COSMOS/M is a registered trademark of Structural Research and Analysis Corporation.

Table 3.3 Parameters used in this simulation [168)169)].

a-Si

Temp., (K)	Thermal conductivity (μW/μm/K)
300,	26
1423,	67

Temp., (K)	Specific heat (μW μsec/μg/K)
100,	0.2593E6
300,	0.7150E6
700,	0.884E6
1100,	0.957E6
1422.9,	1.1E6
1423,	132E6
1433,	132E6
1433.1,	1.113E6
3539,	1.2E6
3540,	1620.7E6
3640,	1620.7E6

Temp., (K),	Density (μg/μm^3)
300,	2.33E-6
1423,	2.3E-6
1433,	2.62E-6
2000,	2.41E-6
3540,	1.85E-6

SiO_2

Temp., (K)	Thermal conductivity (μW/μm/K)
300,	1.38
500,	1.62
800,	2.17
1200,	4

Temp., (K)	Specific heat (μW μsec/μg/K)
300,	0.692E6
500,	0.906E6
800,	1.049E6
1200,	1.13E6
1600,	1.249E6

Temp., (K),	Density (μg/μm^3)
300,	2.2E-6
2208,	0.21E-6
2595,	0.19E-6

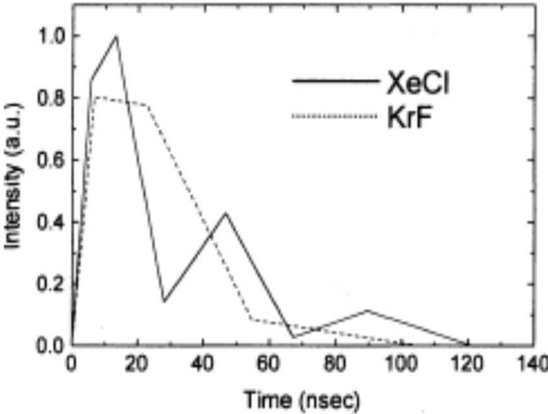


Figure 3.17 The waveforms of the pulses simplified to be used for the simulation [166].

Figure 3.18 shows a result of the numerical thermal analysis for the transient temperature during excimer laser induced melting and subsequent cooling of the Si film. This result starts with the beginning of the irradiating laser pulse. The four lines indicate the transient temperatures at the surface of the Si film, at the interface of the Si/substrate and at positions 100 nm and 1 μm below the interface. The irradiation energy was 350 mJ/cm^2. The surface of the Si film and the interface of the Si/substrate showed the same transient variation. The temperature of the Si film increased rapidly, and the maximum temperature was reached at about 60 nsec, which almost coincides with the end of the pulse, except for the tail portion shown in Figure 3.12 (b). The Si film then cooled to the melting point of crystalline Si. Temperatures inside the substrate were lower than that of the Si film. The temperatures at 1 μm below the interface were still rising when the cooling of the Si film started.

The variation in maximum temperature of the Si surface with respect to irradiation energy is shown in Figure 3.19. The maximum temperature reached the melting point of a-Si at about 200 mJ/cm^2. The temperature remained between 200 and 250 mJ/cm^2 because a-Si has some latent heat for melting [168]. Then it rose monotonically until it reached the boiling point of Si. The energy density of the melt corresponded to that of our experimental transient reflectivity study. In our other experiments the Si films remained after single pulse irradiation of more than 570 mJ/cm^2, but were ablated after multi-pulse irradiation of 570 mJ/cm^2. Therefore, we consider that the simulation gives us a valid estimation.

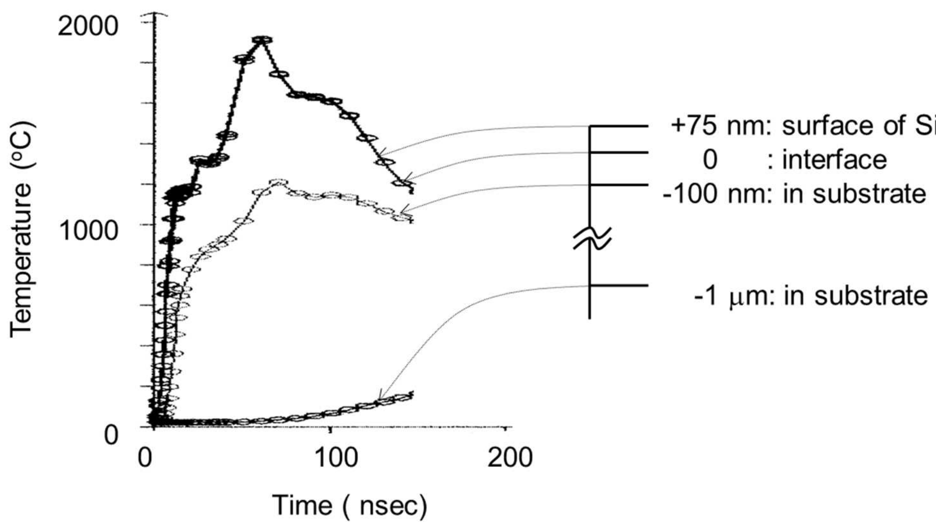


Figure 3.18 Transient temperature during excimer laser induced melting and subsequent cooling of a Si film estimated by COSMOS/M.

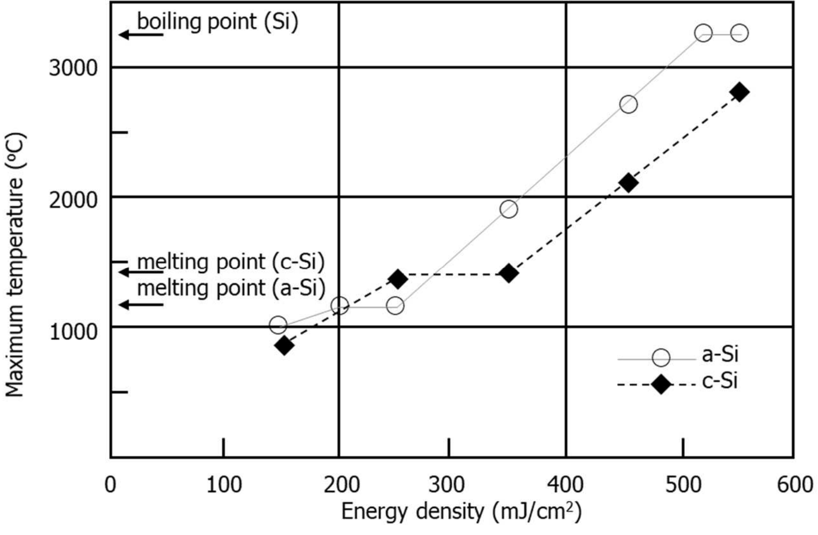


Figure 3.19 Variation in maximum temperature of the Si surface with respect to irradiation energy [166].

Normal nucleation of the crystalline phase occurs in the cooling process when a sample supercools so slowly that thermodynamic equilibrium is maintained (gradual cooling). In contrast, supercooling occurs so rapidly in amorphized samples that normal nucleation is suppressed (rapid quenching). In the case of excimer-laser-induced micro-

crystallization, which is an intermediate phenomenon between amorphization [159] and normal crystallization, it is considered that a spontaneous nucleation producing large amounts of nuclei follows a rapid quenching, and that numerous grains, smaller than those produced during normal crystallization, are produced. Since the transient temperature study described above assumes thermodynamic equilibrium, the cooling rate near the melting point of crystalline Si could be indicative of the supercooling phenomenon. Figure 3.20 shows the variation in cooling rate with respect to the energy density obtained from the transient temperature simulation. The cooling rate near the melting point of crystalline Si decreased with energy density. Reducing the cooling rate helps slow supercooling, i.e., it promotes crystal growth. However, the SEM study shows that micro-crystallization was observed in the films crystallized at higher irradiation energies (over 500 mJ/cm^2). This result suggests that molten Si is rapidly quenched, so as to cause rapid supercooling. The variation in maximum cooling rate in the transient temperature simulation supports the idea that the cooling rate increases with energy density. The maximum cooling rate appears immediately after the beginning of the temperature drop. When the cooling rate exceeds a critical value, the solidification process turns into a non-equilibrium condition, which results in rapid supercooling. In other words, the transient temperature doesn't trace the history obtained from simulation after exceeding the critical value. The border is about 1.6×10^{10} °C/sec at 500 mJ/cm^2 in Figure 3.20. This rate is an order of magnitude lower than the rate of amorphization for crystalline Si [170].

Figure 3.21 indicates a comparison of the maximum cooling rate of a-Si and that of the crystalline Si employed as the precursor of laser crystallization. It is found that the maximum cooling rate in the case of crystalline Si is less than that in the a-Si case. This result suggests that micro-crystallization of the (micro-) crystalline Si should occur at a higher energy density than that of the a-Si film. This difference is attributable to the larger latent heat and higher melting point of crystalline Si. The shift in energy density for micro-crystallization is supported by the SEM study results in Figure 3.14. Micro-crystallization was locally suppressed when the sample was irradiated by three shots at 521 mJ/cm^2. Therefore, in the overlapping irradiation method that uses a line-shaped beam, which is widely used for excimer laser crystallization, for instance, even if the micro-crystallization occurs after the first-shot irradiation at the critical energy density at which a-Si would be micro-crystallized, it can be re-crystallized normally through the subsequent irradiations.

The validity of the critical value for micro-crystallization was confirmed by investigating the relationship between film properties and crystallization conditions in a system that employed a KrF excimer laser. The cooling rate had to be kept below 1.6 ×

10^{10} °C/sec in order to obtain a highly reproducible excimer laser crystallization condition [173].

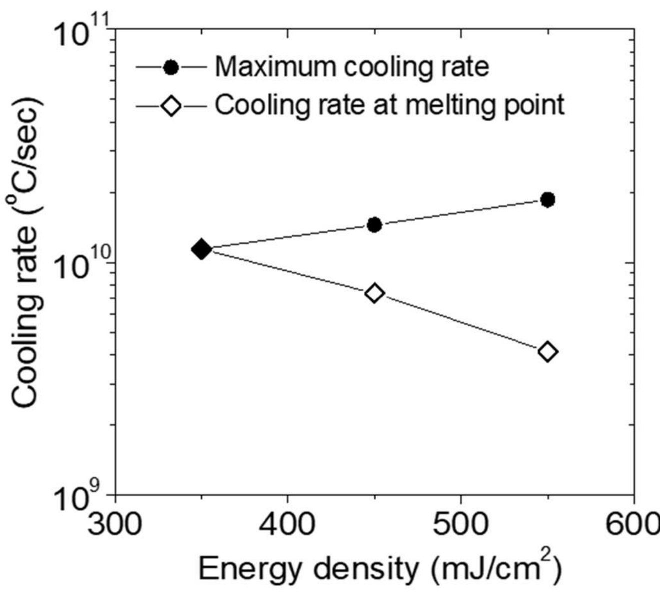


Figure 3.20 Variation in cooling rate with respect to the energy density [166].

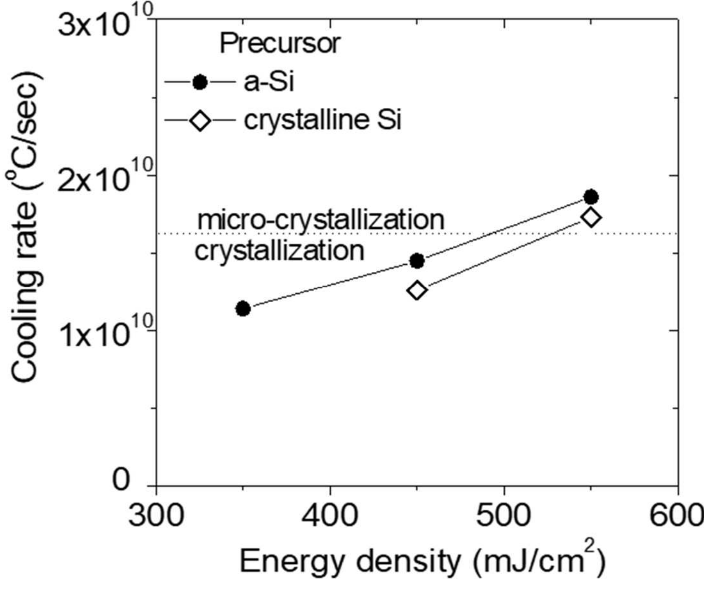


Figure 3.21 Comparison of the maximum cooling rate of a-Si and that of the crystalline Si employed as the precursor of laser crystallization [166].

3.2.5 Number of laser shots dependency [†3]

Dependency on the number of laser shots were investigated by electrical properties obtained from TFT characteristics first. Then, crystallographic properties were studied by using TEM observation and Raman spectroscopy. Figure 3.22 shows the drain current vs. gate voltage characteristics of the poly-Si TFTs fabricated with the number of laser shots ranging from 1 to 5. The SEM observations did not indicate remarkable variation in grain size as a function of the number of laser shots as shown in Figure 3.14. In contrast, the TFT characteristics varied dramatically between 1 and 2 shots, and slightly for each additional shot. This is due to the fact that the first shot produces an amorphous-crystalline transition, while successive shots produce crystalline-crystalline transformations [171)]. Figure 3.23 shows variation for mobility and threshold voltage in terms of the number of shots. Mobility increases monotonically with the number of shots, with maximum mobility being obtained at about 20 shots. These results indicate that film crystallinity varies with each individual irradiation step. In order better to understand the influences being exerted on TFT characteristics, the author estimated the density of carrier trap states at grain boundary of effective channel regions [65)]. Such density is known to be a major factor in determining these characteristics. The author conducted their estimations using a theory proposed by R. E. Proano, et al [66)]. Figure 3.24 shows a plot of density of carrier trap states at grain boundary in terms of the number of shots. Trap density decreases to approximately 1×10^{12} cm^{-2} at 20 shots, which is less than a third of that for film crystallized with only one shot. This resembles closely observed changes in mobility. The number of shots that minimizes trap density is the same as that which creates maximum mobility, i.e. mobility seems to be correlated with the grain boundary conditions.

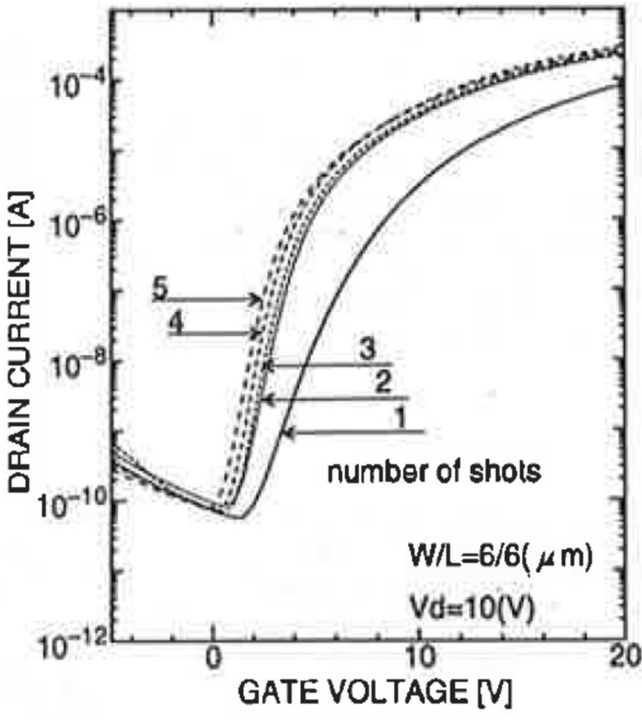


Figure 3.22 Drain current vs. gate voltage characteristics of the poly-Si TFTs fabricated, with the number of laser shots ranging from 1 to 5 [171].

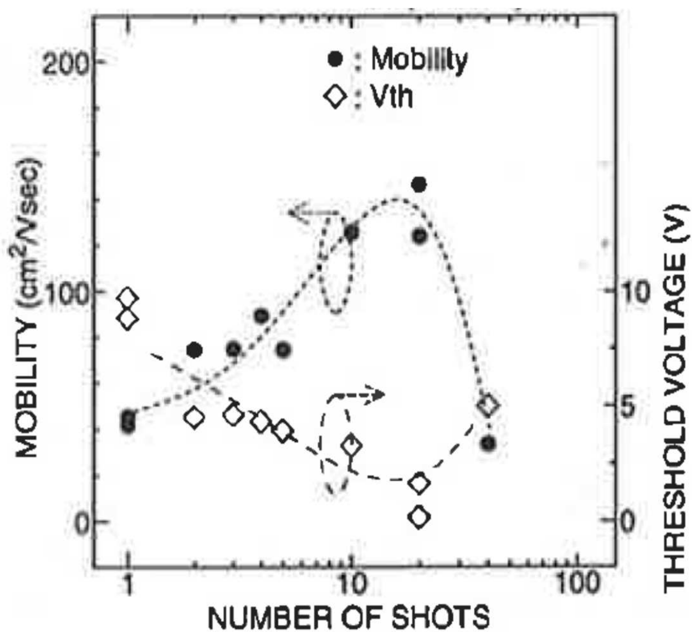


Figure 3.23 Electron mobility and threshold voltage in terms of the number of shots [171].

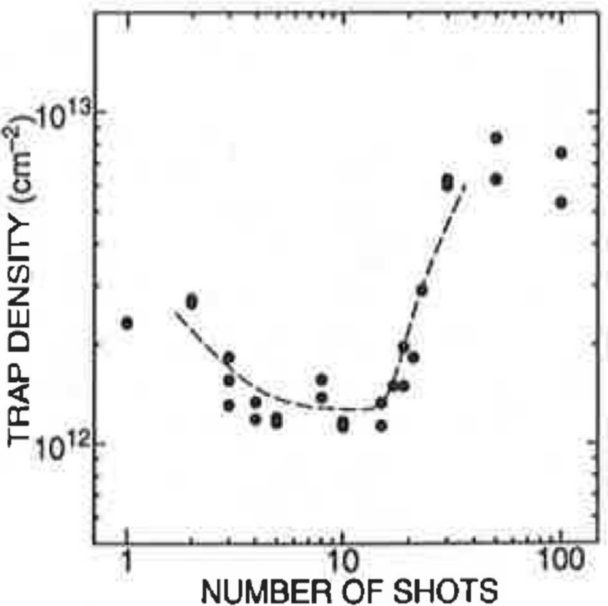


Figure 3.24 A plot of density of carrier trap states at grain boundary
in terms of the number of shots [171].

The microstructures of the films were also investigated by TEM and Raman spectroscopy as follows. It is known that the electrical properties of poly-Si films are determined by grain size and by conditions in disordered regions, such as defects in grains and grain boundaries. Figure 3.25 contains TEM microphotographs of films crystallized by 1, 2, 20 and 100 shots, respectively, at the same energy density of 380 mJ/cm^2. The TEM observation also corresponded to SEM results (339 and 424 mJ/cm^2) in Figure 3.14. Those show that for these films the number of shots has no effect on the grain size, which is about 150 nm diameter. This suggests that mobility depends on the defects in grains and on grain boundaries conditions, rather than on grain size. The behavior depending on the number of laser shots was different from another research results under substrate heated [174)175)]. It was considered to be the difference in effective energy range introduced. It was because enlargement for grains by multiple laser shots followed was observed under the micro-crystallization by the first pulse, i.e. under higher energy range, as shown in Figure 3.14 (521 mJ/cm^2).

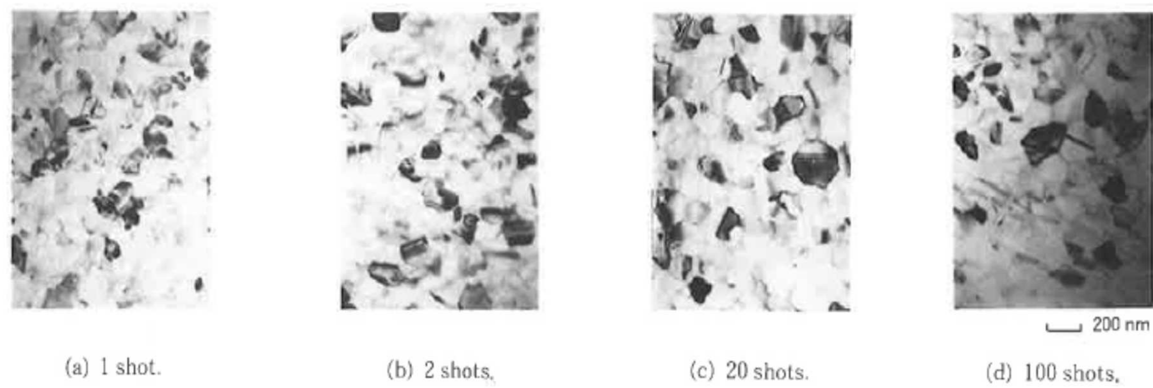


Figure 3.25 TEM microphotographs of films crystallized by 1, 2, 20 and 100 shots [171].

Raman scattering spectra shows a clear distinction between ordered and disordered states. And a sharp 520 cm^{-1} peak of crystalline silicon provides accurate indicator of crystallinity. Figure 3.26 shows the Raman spectra of both first irradiated (380 mJ/cm^2, 1 shot) and non-irradiated films. A broad band near 510 cm^{-1}, corresponding to an amorphous-like structure, is seen in the non-irradiated film. A sharp peak near 520 cm^{-1} is observed in the first-irradiated film. The symmetrical peak shape suggests the formation of a fine polycrystalline film, although the peak is wider than single crystalline silicon and its peak position shifts to a lower frequency. This indicates that the crystallization has already been completed in the one shot process. Previously noted TEM observations support these results. Figure 3.27 shows the Raman spectra of poly-Si films crystallized by 1, 2, 3, 5 and 10 shots, respectively, at an energy density of 380 mJ/cm^2. When the number of shots is few, we observe a small peak (arrows) at about 500 cm^{-1}. As Iqbal and Veprek have reported, such a peak suggests the existence of small grains, those of only a few nanometers in diameter [122]. This peak disappears as the number of shots increases. These results show that the number of shots has an effect on the microstructure in poly-Si films. This seems to contribute to the mobility behavior estimated by TFT characteristics. Figure 3.28 shows plots of both peak frequency and peak widths for the sharp 520 cm^{-1} peak in terms of number of shots. Peak frequency for laser crystallized silicon varies with the number of shots and is about 4 cm^{-1} lower than that of single crystalline. Shifts to lower peak frequency can be explained as being the results of residual strains inside the grains and of the smaller crystalline size. However, the results of TEM observations (Figure 3.25) let them rule out a size effect on Raman shift here, i.e. peak shift may be considered to be due simply to residual strains inside the grains. Such strains are caused by tensile stress: a molten silicon/quartz interface is fixed during the melting

process induced by the laser, and the expanded volume of molten silicon contracts during recrystallization. It is suggested that difference of peak positions arises from the fact that successive laser crystallization produces buffered layers at silicon/quartz interfaces, and that these buffered layers are formed either by a diffusion of oxygen atoms or by a transformation of dioxide surfaces. Oxygen diffusion was observed in a SIMS measurement of impurity doped silicon/quartz interface processed by multiple laser shots as shown in Figure 3.28. The mobility decrease observed after an excessive number of shots can also be explained by this oxygen diffusion. So they can consider that the individual laser re-crystallization is controlled by the conditions at silicon/quartz interface, and that there are some optimum conditions for the laser re-crystallization process. Peak width decreased with the number of shots; the minimum width has been shown to occur at about 7 shots as shown Figure 3.29. Decreasing peak width may either be due to an enlargement of grains, or to a decrease in such silicon disorder as grain boundaries or defects in grains. Since the TEM observations have shown no grain enlargement, decreasing peak width appears to have been caused by reduced disorder. This behavior may be correlated with the disappearance of small grains mentioned previously. However, the number of shots that provides maximum mobility is different from that which provides minimum Raman peak width. This inconsistency may be considered to originate in the difference between the channel region and the Raman measurement region. The TFT channel region that contributes to electron conduction is located in a part of the poly-Si film near the gate insulator/poly-Si interface, while the Raman measurement region involves the whole poly-Si film in the direction of incidence of the argon ion laser. The successive excimer laser irradiation seems both to reduce silicon disorders in the channel region near the gate insulator/poly-Si interface, and to produce a kind of disordered layer at poly-Si/quartz interface, which is formed by a diffusion of oxygen atoms.

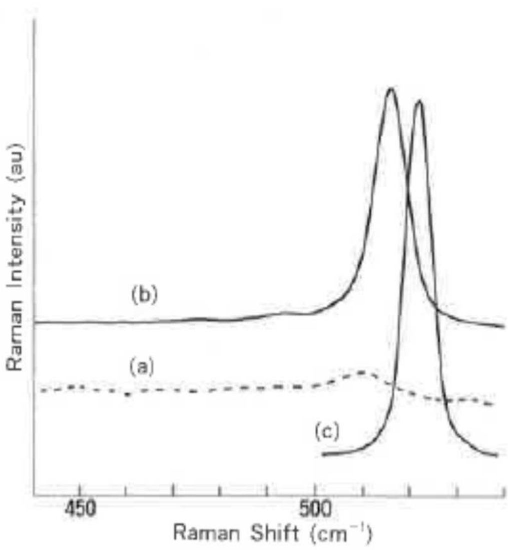


Figure 3.26 Raman scattering spectra of (a) starting (non-irradiated) film,
(b) poly-Si film crystallized by one laser shot (380 mJ/cm^2) and
(c) single crystalline silicon wafer, respectively [171].

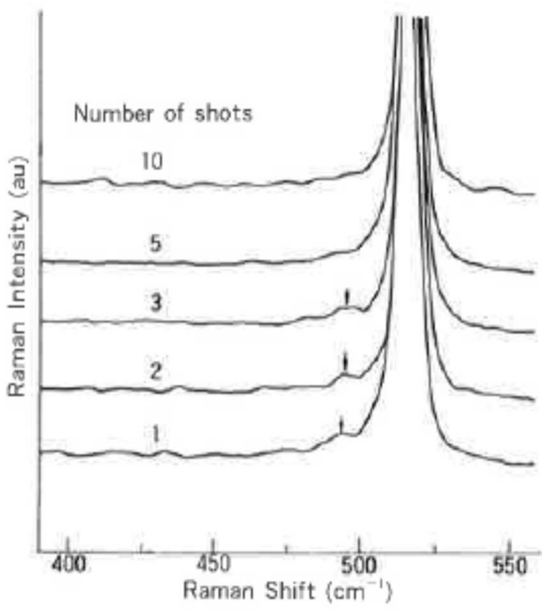


Figure 3.27 Raman spectra of poly-Si films crystallized by 1, 2, 3, 5 and 10 shots,
respectively, at an energy density of 380 mJ/cm^2 [172].

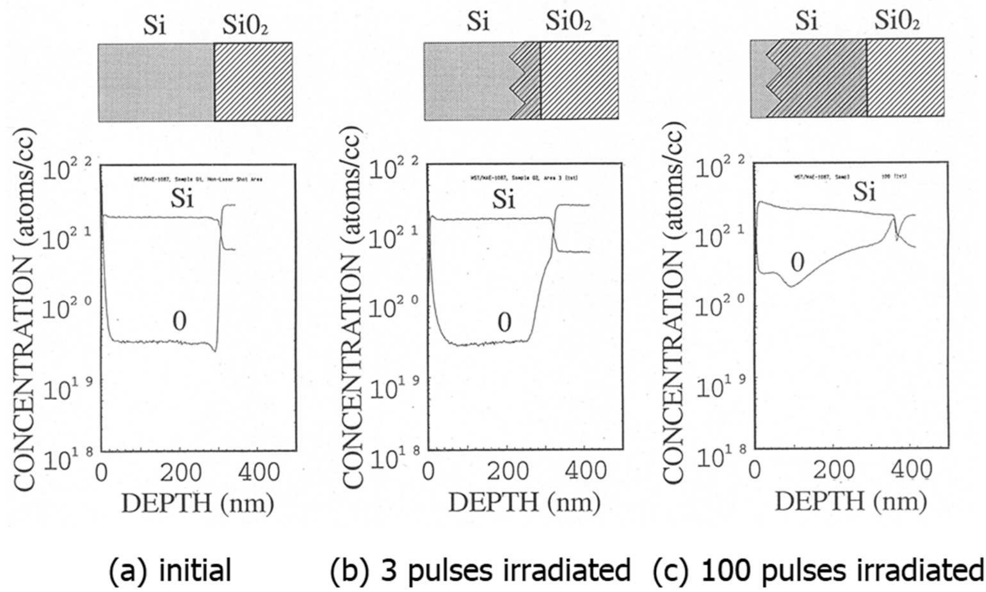


Figure 3.28 SIMS study for a-Si precursor film and poly-Si films crystallized by 3 and 10shots, respectively, at an energy density of 380 mJ/cm^2.

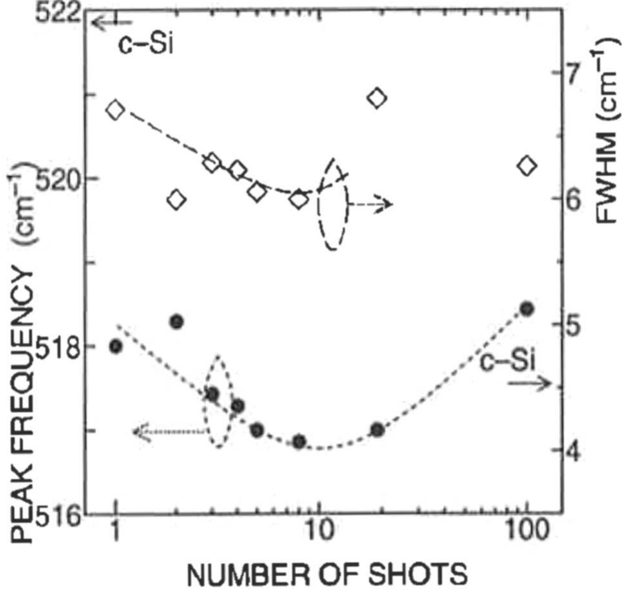


Figure 3.29 Plots of both peak frequency and peak widths for the sharp 520 cm^{-1} peak in terms of number of shots [171)].

3.2.6 Summary for the liquid phase crystallization

This section discussed that the properties of excimer laser crystallized poly-Si films are strongly dependent on both the irradiation energy and the number of laser shots.

Cooling rate during excimer laser crystallization of amorphous silicon was evaluated by using numerical transient-temperature simulation in order to investigate the fact that electron mobility sharply decreased at higher energy range, i.e. a transition to a non-equilibrium condition, which results in micro-crystallization. Since the results of cooling rate near the melting point of crystalline Si were not supported by the findings of the SEM observation, the maximum cooling rate during the crystallization was focused. The maximum cooling rate increased monotonically with irradiation energy. It was found that the micro-crystallization occurred at a quenching rate of 1.6×10^{10} °C /sec. Furthermore, the maximum cooling rate for the crystalline Si precursor was smaller than the rate for a-Si, i.e., the (micro-) crystalline Si should be micro-crystallized at a higher energy density than the a-Si. The shift in energy density for micro-crystallization was supported by the findings of the SEM study. Micro-crystallization can be suppressed by multiple-shot crystallization at the critical energy density at which a-Si would be micro-crystallized. Cooling rate below 1.6×10^{10} °C /sec must be maintained to ensure that the excimer laser crystallization process is reproducible.

Another effect of the number of laser shots on the film quality was also investigated. It was discovered that electron mobility, one of the most important of all TFT characteristics, increased monotonically with the number of irradiations, with maximum mobility being obtained at about 20 shots. The density of carrier trap states at grain boundary was reduced to 1×10^{12} cm^{-2}, which is less than a third of that for film crystallized with a single shot under the same conditions. TEM observations showed that, for these poly-Si films, the number of shots had no effect on grain size, which was about 150 nm diameter. Raman studies indicated that the disorder in those films, including small grains, grain boundaries and defects in grains lessened as a result of a number of successive shots, and then worsened again after further shots.

These results suggest that the conditions at silicon/quartz interface play an important role during the laser re-crystallization, and that there are some optimum conditions for the re-crystallization process. Controlling the number of shots is very important in poly-Si TFT fabrications.

3.3 Summary

In this chapter, the author proposed and successfully demonstrated the grain boundary filtration with Ge thin films under the selective-nucleation and solid-phase epitaxy, and clarified the issues when applying it to Si thin films. In the excimer laser crystallization, which is recrystallization via the liquid phase, he discovered that the number of laser shots contributed to reduction of defects in grains/grain boundaries,

differing from that the irradiation energy directly contributed to variations in grain-size. And also he found out that the maximum cooling rate must be maintained at less than 1.6 $\times 10^{10}$ °C/sec to avoid micro-crystallization.

The three growth methods discussed in chapters 2 and 3 are compared as follows. A technique employing thermally non-equilibrium plasma process as same as a-Si film deposition via vapor phase is very much attractive for obtaining a large grain polycrystalline film on a glass substrate. A lot of prior researches had tried to fabricate a large grain, i.e. high mobility, polycrystalline film on a glass substrate, but unfortunately they had not reached to success. (The values of carrier mobility for deposited films are still about 25 cm^2/Vsec on a small glass substrate [128] and 3 cm^2/Vsec on a large substrate acceptable in the industry [129] even in 2000's researches followed.) In contrast, two-dimensional epitaxial growth on single crystalline substrate were successfully demonstrated under vapor phase at low temperature as described in chapter 2. These results do not agree to the idea that the reason why a large grain polycrystalline film on a glass substrate cannot be formed is that crystalline growth does not occur at low temperature. One possible reason is that quite a lot of islands are seeded on the glass surface simultaneously at the initial stage of film deposition. Those behaviors limit the enlargement for the grain because the distance among islands could be very short and the crystalline orientation of those could be random. In order to extend this technique to the large-grained crystalline film formation on a glass substrate, therefore, another technique is necessary to control the nucleation process instead of crystalline substrates employed in this study. Thus, further approach is expected, either reducing the nucleation site, i.e. number of islands, or aligning the orientation of those island, in order to obtain the large-grained crystalline films on a glass substrate.

The approaches remained to obtain a large grain, i.e. high mobility, polycrystalline film on a glass substrate are techniques that Si thin film was prepared first and then (re)crystallize it via solid phase or liquid phase. The target was focused on how to form a large grain film because the crystalline growth had been already demonstrated in 1970's by utilizing thermal anneal via solid phase [97] and laser anneal via liquid phase [103][105], respectively. Solid phase crystallization technique featuring selective nucleation and grain-boundary filtration were discussed in the section 3.1. In the study of Ge, the experimental results demonstrated a maximum grain size of 20 μm radius can be achieved based on estimates of the product of the SPE rate and the incubation time for spontaneous nucleation. In another study of Si, more than several micrometers of grain growth were successfully demonstrated at around 600 °C, that is applicable conventional glass substrates. The performance might be enough for those films to be applied to devices

required high-speed driving such as a peripheral circuit for LCD although some issues remained. To apply to industrial products, however, an important concern was still remained that the technique required metals for the selective nucleation. For example, one of the other research groups employed Ni as catalyst to fabricate precursor films for laser annealing. That group reported additional gettering process to remove Ni from active area was effective to reduce off-current in TFT characteristics [144)]. This crystallization technique via solid phase was attractive but was put on hold as the residual Ni might influence reliability for TFT driving.

The candidate remained was the laser crystallization that is via liquid phase. Properties of excimer laser crystallized poly-Si films strongly depended on both the irradiation energy and the number of laser shots as described in section 3.2. One of the most important parameter is the cooling rate during the process of melt and solidification. In order to obtain a large grain film, an adequate energy should be chosen because the cooling rate depends on the irradiation energy, and because the higher energy actually caused formation for smaller grains. Another important parameter to obtain high quality polycrystalline film is the number of laser shots on the Si thin film. There is the appropriate range in the number of shots to fabricate better film as same as the irradiation energy. However, it is not because of the variation of grain size appeared in microphotographs. The experimental results suggested the multiple laser shots reduce the underlying disorders such as small grains, grain boundaries and defects in grains and that further number of shots rather produce those disorders. Laser annealing technique can simply provide high quality film whose electron mobility is higher than 100 cm^2/Vsec by controlling parameters as described in the section 3.2. This is the competitive advantage of laser anneal over other techniques, such as plasma CVD and solid phase crystallization, as summarized in Table 3.4. In contrast, there still is an important issue for the uniformity of the films. It is because the size of laser beam is quite smaller than the one of the substrate and also because the stability of the laser emission was not enough. The issue for the uniformity was also one of the reason why results of the prior researches for laser anneal in 1970's was not actually applied in industry in the fields of semiconductor. Improvement for uniformity of the excimer laser crystallized poly-Si TFTs is described in the next chapter.

Table 3. 4 Summary; comparison for three ways to fabricate crystalline Si thin- films

	Vapor phase	Solid phase	Liquid phase
crystalline-growth ability (with seed)	✔ seed	*Prior researches in 1970's ex) Sankur et al. (1973)*	*Prior researches in 1970's ex) Young et al. (1978)*
film formation on foreign substrate	*Researches followed even in 2000's as μc-Si ex) Takahashi et al. (2007)*	✔ seed	✔
TFT application			
electrical performance	poor (mobility 3~25 cm²/Vsec)	excellent (≒ single crystal) with concern of contamination via seed metal	excellent (mobility >100 cm²/Vsec)
uniformity	excellent	good	poor

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†3 *Reproduced from "H. Tanabe, K. Sera, K. Nakamura, K. Hirata, K. Yuda, and F. Okumura, "Excimer laser crystallization of amorphous silicon films for poly-Si TFT fabrication", Mat. Res. Soc. Symp. Proc., vol. 321, pp. 677-682, (1994)," with the copyright permission of Cambridge University Press.*

4. Application of poly-Si films to thin-film transistors and related devices

As discussed in the chapter 3, the excimer laser crystallization was chosen to fabricate poly-Si thin-films for TFTs. It enables to drive peripheral circuits of active-matrix displays because of its high-mobility characteristics, which is more than one hundred times of that of a-Si:H TFTs. There were additional challenges critically to be solved in order to obtain the poly-Si TFTs of product grade under low-temperature. In this chapter, studies i) to improve uniformity, ii) to reduce photo leakage current, iii) to enable high reliability, and iv) to enhance carrier mobility are described. The former three challenges are indispensable to bring poly-Si TFT technology to the stage of product, and the last one is to aim to bring it to the higher stage.

i) Uniformity is the most important issue resulted in by using excimer laser crystallization, as described in section 3.3. ii) Photo-leakage current must be reduced to the level that enables normal operation for liquid crystal. The reasons are as follows. The demand for a high luminance and a high contrast ratio in LCDs is continuing to grow. High luminance would increase photo leakage current in the poly-Si TFTs, which diminishes the voltage that are held across the pixel electrodes, which would cause contrast ratio to be low. iii) The gate insulator plays an important role to enable reliable operation of MOS transistors including TFTs. The thermal oxide grown on single crystalline silicon is indispensable for Si-LSI industry. The silicon nitride film deposited underneath of a-Si:H by plasma-CVD is also essential. There were many candidates for both materials and methods to obtain the gate insulators. A silicon oxide film deposited by remote-plasma CVD are studied in this chapter. iv) Increasing the carrier mobility further would help to expand applications using the poly-Si TFTs, not only for pixel and peripheral drivers but also for memory and microprocessor on glass.

4.1 Principal structures for poly-Si TFTs

Principal structures of thin-film transistors (TFTs), that were combined with excimer laser crystallization process, are illustrated in Figure 4.1. The inverted-staggered structure (a') is widely used in a-Si:H TFTs because its fabrication process is simple [11)12)178)] and as the result, the number of photo masks can be reduced less than other structures stating below. However, there are some challenges to apply it to excimer laser crystallization and its poly-Si TFTs. As relatively thick active layer is employed in a-Si:H TFTs, back-channel etching process can be applied [176)177) 178)]. In contrast, thinner active

layer is preferred in poly-Si TFTs because the very shallow penetration depth of excimer laser enables very thin film crystallization. As the result, called etching stop layer is necessary for the poly-Si TFTs as shown in Figure 4.1 (a) [179]. The other challenge is the precise control for crystallization of Si films on a patterned gate metal layer. Heat flow under Si films is varied with or without the metal layer. Thick gate insulator may neglect the metal layer, but the performance of TFTs should be decided by the MOS capacitance, i.e. thin gate insulator is preferred.

Primary structure of staggered type TFT is described in Figure 4.1 (b') [108]. The issue to apply excimer laser crystallization is that the higher melting point metal is necessary for wiring because it is exposed to molten Si, i.e. very high temperature, during crystallization. Impurity diffusion from the metal to channel region must be also prevented. As the result, additional wiring metal with low-resistivity is needed as shown in (b) because the conductivity for the metal with high melting-point is not so high [171].

Planer type structure (c) is widely used in the excimer laser crystallized poly-Si TFTs to prevent those difficulties stated above [91]. The planer structure has an advantage that source-drain region can be fabricated self-aligned with the gate patterns. It enables to be minimum for the parasitic capacitance that is caused by the overlap of the gate and the source-drain. The planer structure is used in this chapter unless otherwise noted.

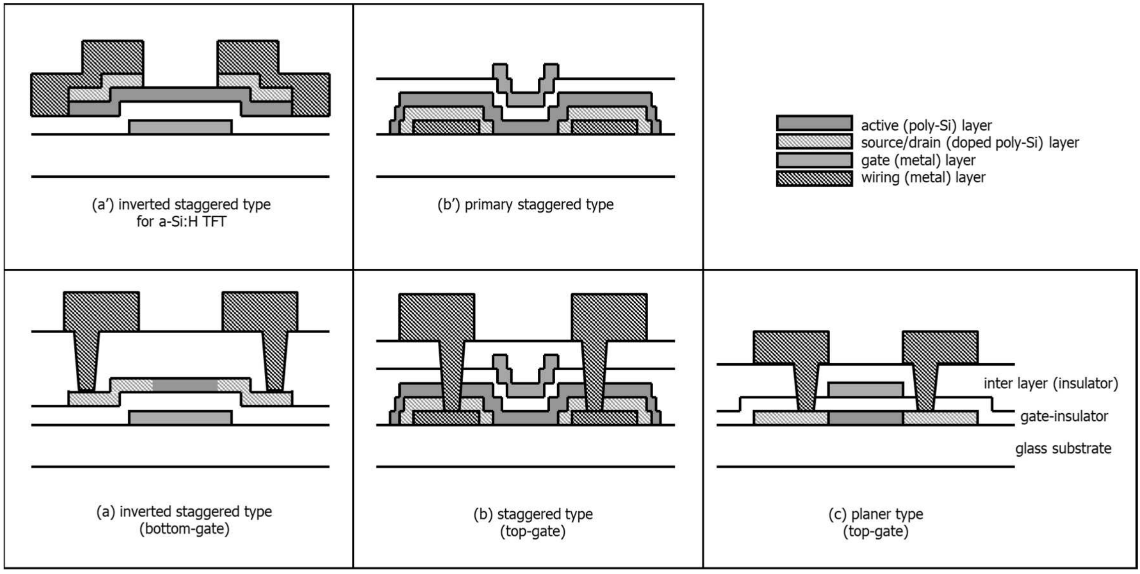


Figure 4.1 Principal structures of poly-Si TFTs.

Also, here must be described another aspect of poly-Si TFTs. The poly-Si TFTs has important characteristics in its leakage current under off-state. The carrier traps existed in the band-gap, originated by defects in grain boundary, effects on not only

driving current under on-state [68)75)] but also the leakage-current under off-state [180)181)]. The leakage current mechanism is explained by the presence of trap states originated in polycrystalline film as follows. Figure 4.2 illustrates relations of trap states in poly-Si and drain structure.

In the case of self-aligned single drain structure (a1), band diagram is illustrated in (a2). Under a medium strength of the electric fields, the leakage current is induced by two steps comprising of the thermal activation of an electron from the valence band to a trap state in the band gap, and electron tunneling through the reduced barrier to the conduction band. Furthermore, the tunneling of an electron is caused by field-enhanced emission under strong electric fields because the tunneling length decreases as the electric fields increases. These phenomena are not observed in single crystalline Si FETs. Also because this characteristic must affect the image quality of LCD, that was main target application of poly-Si TFTs, much efforts had been paid to reduce the leakage current by the ways in both structure [181)182)184)] and process [162)180)185)]. One of the effective way to reduce the leakage current is to put an offset region between the edge of gate, i.e. channel, and drain as shown in (b1) [183)]. The presence of offset region between the channel and the drain helps to alleviate the electric field, as shown in (b2), and results in reducing the leakage current. As a simple offset structure without doping also dramatically reduce the on-current, the offset region is normally employed with lightly doped condition, which is called lightly-doped drain (LDD) structure [181)186)].

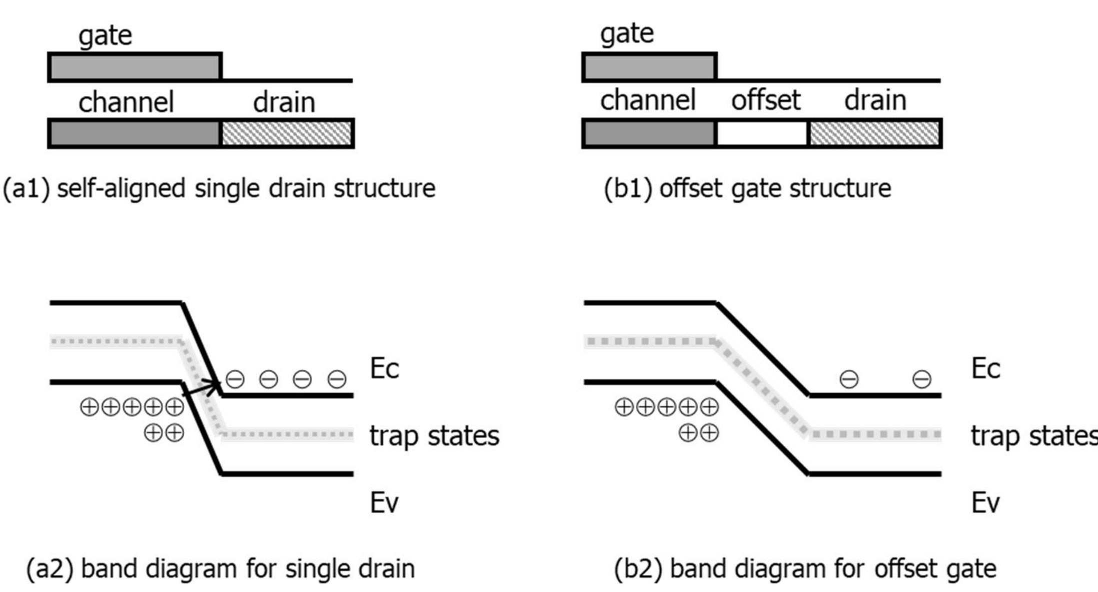


Figure 4.2 Drain engineering for trap states in poly-Si TFTs.

4.2 Uniformity

The poly-Si TFTs had been expected to apply in the fabrication of high-speed driver circuits on glass substrates [57)187)]. And the crystallization technique was one of the most important procedure in the throughout process to fabricate the poly-Si TFTs at low substrate temperature. However, it was very difficult to obtain uniform films with the excimer laser crystallization method even though high-mobility TFTs with more than 100 cm^2/Vsec had been reported [91)108)] because mainly of the variation for irradiation energy and the limited size of the laser beam [188)189)]. Irradiation energy variation was caused by a lack of pulse-to-pulse stability in the emission of excimer laser and spatial energy differences in the laser beam. The other problem was that overlapping of the laser beams was necessary on a substrate because the beam was generally much smaller than the substrate [190)]. The poor quality poly-Si films in the overlapped region between beams degrades the performance, when the beam is scanned [191)192)]. These difficulties apparently strongly depend on manufacturing equipment. Thus, the many development efforts had been done in both sides of the process and the equipment as summarized in Table 4.1. Several approaches in the process are discussed in this section. First, pre-crystallized films under solid phase was used as the precursor for excimer laser crystallization [183)]. The author expected the pre-existing large-grain crystalline grown by solid phase might affect the melt-solidification and resulted in uniformity to be better. Next, capping layer was used during excimer laser crystallization [157)158)]. In prior studies, capping layers had been used in laser-induced melt-solidification processes [193-195)], however there were no attempts to produce fine grains that contribute uniformity in device performance. As the results, these approaches alleviated variation of TFT characteristics against the variation of irradiation energy.

Then, a special circuit design on the glass substrate was employed to use only uniform region and to avoid the use of the edge region of the beam [196-198)]. It was somewhat tricky but quite realistic in those days to use only areas with uniform performance by avoiding peripheral region of laser beam. Finally, one dimensional scan method was proposed to expand the crystallization area [199)]. As many researchers still aspired the highest mobility value or the world first achievement at that time, these kinds of studies focusing uniformity improvement was minor but important to develop practical devices.

Table 4.1 Uniformity problems and improvement approaches for TFT characteristics

Issues	Improvement approaches in process	Improvement approaches in equipment
Laser energy deviation -Pulse-to-pulse instability -Spatial differences in a beam	less dependent on the energy **- crystalline precursors** **- capping layer**	- emission stability - optics design
Small beam size -Overlapping	less influence by the seam - substrate heating - 2-step annealing **- isolated circuit design** **- one dimensional scan**	- high power laser - line beam

4.2.1 Film selection for precursor

This subsection describes the effect of pre-crystallized precursor films in the excimer laser crystallization process and the uniform-quality poly-Si TFTs obtained through the use of the process. Device fabrication process was as follows. A-Si films of 80 nm and 120 nm in thickness were deposited at 500 °C on the quartz substrates, and were thermally crystallized at 600 °C in N_2 for 20 hours. Then XeCl excimer laser was irradiated to the solid phase crystallized poly-Si films. The range of energy density was from 190 to 450 mJ/cm^2. The number of shots was varied up to 50 shots without scanning. After the definition of the active areas, 100 nm thick gate-oxide was deposited by LPCVD, and the conventional MOSFET process were followed with maximum process temperature of about 900 °C. For the p-channel and n-channel source-drain formation, B^+ ions and P^+ ions were implanted at a dose of 1 × 15 cm^{-2} each. The offset gate structure was used to reduce the leakage current. The process conditions are summarized in Table 4.2.

Figure 4.3 shows the typical Id-Vg characteristics of n-ch. offset-gate TFT with the different energy densities. Increasing the irradiation energy made the threshold voltage to decrease and the leakage current to reduce. Figure 4.4 shows the dependency of the field effect mobility, that was calculated from the maximum of gm in the linear region of the self-aligned TFT, on the energy density. The thickness of poly-Si film was (a) 80 nm and (b) 120 nm. The mobility was constant below 190 mJ/cm^2, increased at 210 mJ/cm^2, then fairly constant at the range from 230 to 307 mJ/cm^2 for the (a) 80nm thick poly-Si. In the range over 307 mJ/cm^2, the mobility slightly increased and then decreased sharply. The similar behaviors were also shown in the case of the p-ch. TFTs, and also in the cases of (b) 120 nm thick poly-Si. It was already discussed in subsection 3.2.3 that

the mobility was strictly depended on energy density as shown in Figure 3.16. However, these results shown in Figure 4.4 were quite different from the above in that the mobility was almost constant at the specific range. These behaviors are explained by the discussion also in section 2.3. As shown in Figure 3.18, the maximum temperature of Si films during excimer laser irradiated melt-recrystallization reached the melting point of c-Si, that is slightly higher than that of a-Si. The temperature remained constant between 250 and 300 mJ/cm^2 because c-Si has some latent heat for melting [168]. Then it rose monotonically until it reached the boiling point of Si. The region that the mobility was constant at the range from 230 to 307 mJ/cm^2 almost corresponds to the region that the maximum temperature remained constant. In this subsection, solid phase crystallized poly-Si film was employed as the precursor for excimer laser crystallization. The precursor films had fairly good property of more than 50 cm^2/Vsec in mobility without laser irradiation as shown in Figure 4.4. The constant region of the maximum temperature originated in its latent heat was larger than that of a-Si as the precursor. These conditions made it possible to obtain wide constant range in mobility, i.e., uniform performance of TFTs in spite of large irradiation energy variation. This range of energy density was also found to be effective on the number of shots dependency. Figure 4.5 shows the number of shots dependency on (a) the mobility for both n-channel and p-channel and (b) the leakage current with the irradiation energy of 245 and 307 mJ/cm^2. The mobility showed constant from 1 shot to 50 shots. The leakage current increased with the number of shots over 20 shots in the case of 245 mJ/cm^2, however it remained constant in the case of 307 mJ/cm^2. It was also discussed in 2.3.5 that the mobility was depended on the number of laser shots as shown in Figure 2.32. Those results indicated that film crystallinity varies with each individual irradiation step. However, these results shown in Figure 4.5 were quite different from the above in that the mobility was almost constant at the whole range. It is considered because the precursor film already revealed better quality and because the high temperature process played a role to decrease the defects in grains and on grain boundaries throughout the all range for the number of shots. As discussed above, this method to employ the solid-phase-crystallized films as the precursor indicated a remarkable advantage against the conventional method to use a-Si films as the precursor, that must precisely control the irradiation energy to obtain uniform performance

Table 4.2 Experimental conditions for excimer laser crystallization of solid phase crystallized films

Precursor	a-Si; 80, 120 nm / LPCVD 500 ℃
SPC	600 ℃, N_2, 20 hours
Substrate	Quartz
Excimer laser	XeCl (λ = 308 nm)
- Beam size	4 x 4 mm
N-channel and P-channel TFT fabrication	
- Structure	Planar
- Maximum temperature	900 ℃
- Gate insulator	SiO_2 / LPCVD

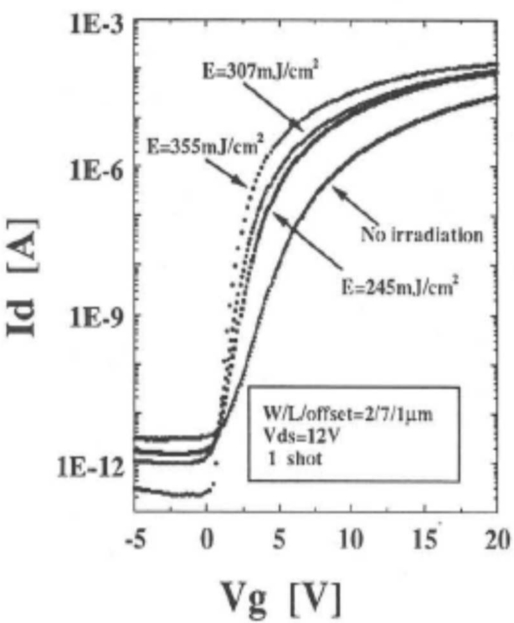


Figure 4.3 Id-Vg characteristics of the TFTs irradiated at the different energy densities.

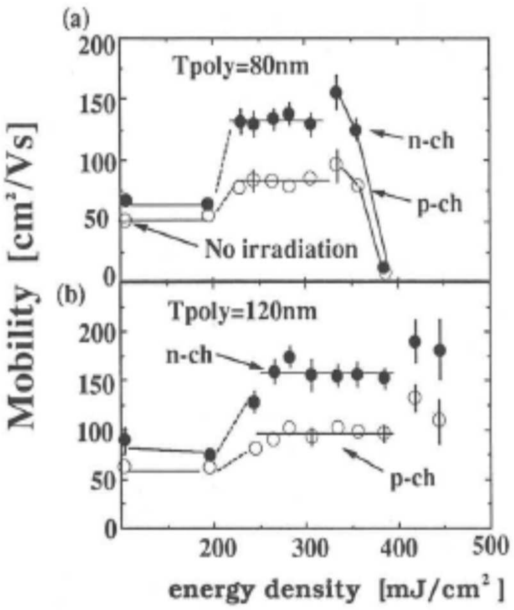


Figure 4.4 The mobility as a function of the energy density of the XeCl excimer laser. The thickness of the poly-Si film (Tpoly) is (a) 80nm and (b) l20nm.

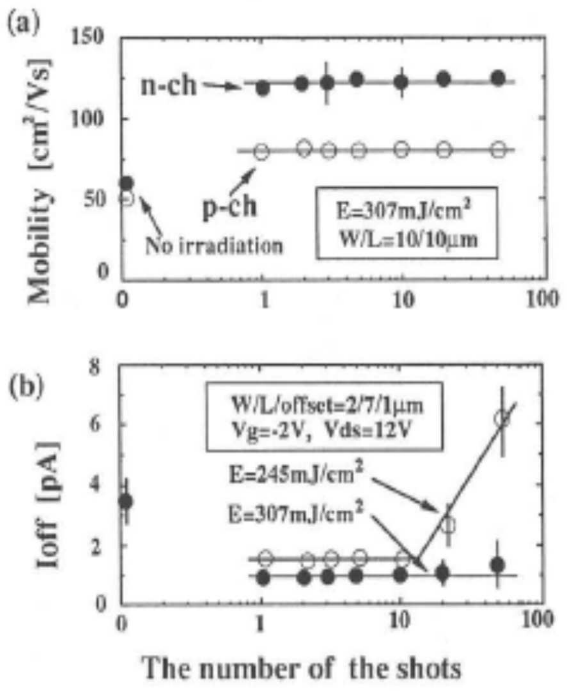


Figure 4.5 The mobility (a) and the leakage current (b) as a function of the number of the shots.

4.2.2 Process control during re-solidification

This subsection describes the role of capping layer in the excimer laser crystallization process and the uniform-quality poly-Si TFTs obtained through the use of the process. In prior studies, capping layers were used in laser-induced melt-solidification processes for achieving the graphoepitaxy [193)], reducing surface roughness [194)] or controlling optical reflectance [195)]. Figure 4.6 illustrates schematic views in the excimer laser crystallization for both with and without capping layer. In the experiments, a 75 nm-thick amorphous-silicon precursor was deposited on a quartz substrate by LP-CVD. A 100 nm-thick silicon dioxide, also fabricated by LP-CVD, was used as the capping layer. XeCl excimer laser was used for crystallization. Uniformity of the laser beam intensity was ± 5% within a 4 mm × 4 mm areas. The thickness for the capping layer was determined by the reflectance both obtained experimentally and estimated numerically, as follows. Figure 4.7 indicated the reflectance at a wavelength of 308 nm with the thickness of the SiO_2 capping layer. The reflectance changed dramatically as the capping layer thickness increases. The 100 nm-thick capping layer was chosen in this experiment because it has the same reflectance as a silicon surface, i.e. without capping layer. Therefore, no consideration is required for the difference in effective laser irradiation energy. To evaluate the performance of poly-Si film, n-channel TFTs with a staggered structure were fabricated. The process temperature was maintained at 600 °C or less as described in section 3.2.

Table 4.3 Experimental conditions for excimer laser crystallization with capping layer.

Precursor	a-Si; 75 nm / LPCVD 560 °C
Cap layer	SiO_2; 100 nm / LPCVD 400 °C
Substrate	Quartz
Excimer laser	XeCl (λ = 308 nm)
- Beam size	4 x 4 mm
N-channel TFT fabrication	
- Structure	Staggered
- Maximum temperature	600 °C
- Gate insulator	SiO_2 / LPCVD
- Typical size (W/L)	6/6 µm

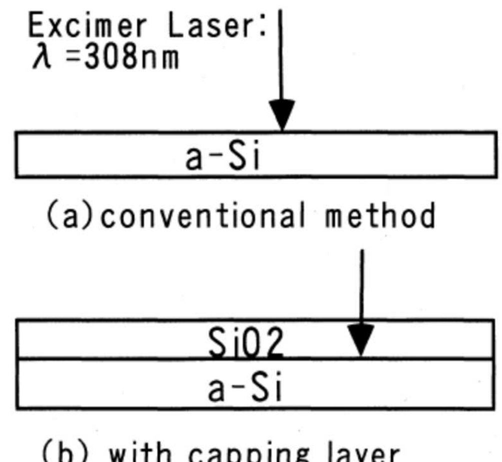


Figure 4.6 Grain size variation with laser energy density.

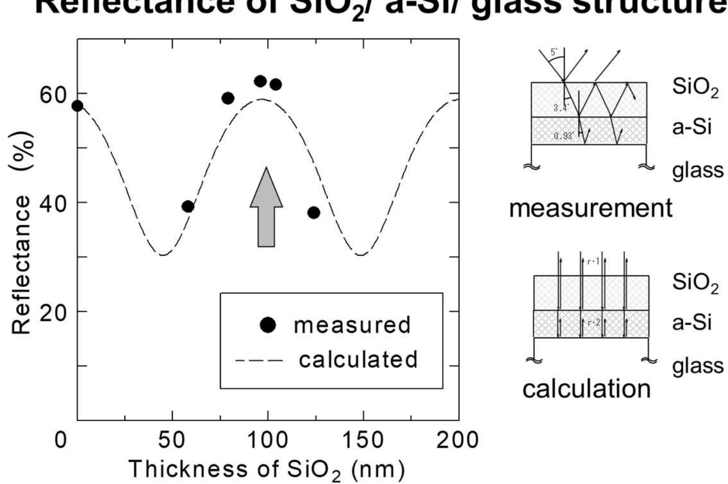


Figure 4.7 Surface reflectance of 308 nm wavelength light

Figure 4.8 shows mean grain diameters of film fabricated at various levels of energy density. In conventional crystallization, the grain size sharply increases with energy density. It also increases in the films crystallized with the capping layer, but very little compared with in the films crystallized conventionally. Figure 4.9 indicates surface morphology for those films obtained with two processes, observed by AFM (atomic force microscope). There was a big difference in the roughness. A much smoother surface was observed on the film crystallized with capping layer. Figure 4.10 shows plots of Raman peak width against the various irradiation energy density levels. For the films fabricated with the conventional method, the peak width decreased as energy increased and the minimum width was obtained at about 450 cm^{-1}. This suggested that the film quality

degraded in the high energy range more than 450 mJ/cm^2. For the films crystallized with capping layer, however, the Raman width decreased monotonically in this energy range and the values are larger than those width of conventionally fabricated films. The films crystallized with the capping layer are lower in quality than those made conventionally. One of the reason for the difference in quality was the difference in the heat capacities in the melting process. The conventional process put the energy into the silicon film more effectively because the capping layer is also heated in this process. These differences in grain size, surface roughness and crystalline quality discussed above could be explained by the results followed. Cross sectional TEM photograph for those films are shown in Figure 4.11. The conventional crystallization produced the poly-Si film with a columnar structure. In this case, most nucleation sites were located on the Si-substrate interface when the molten Si cooled and started to solidify. The crystal growth started at the interface and proceeds toward the front surface. With the use of the capping layer, in contrast, a two-layer structure in the Si film was formed. There can be seen very small grains and a lot of defects. This suggests that the interface of the capping layer and the Si also provides nucleation sites. The crystal growth started at both the upper and lower interfaces. The laser crystallization employing the capping layer effectively formed fairly good quality of poly-Si films, whose grain size varied very little with increased crystallization energy and whose surface was much smother.

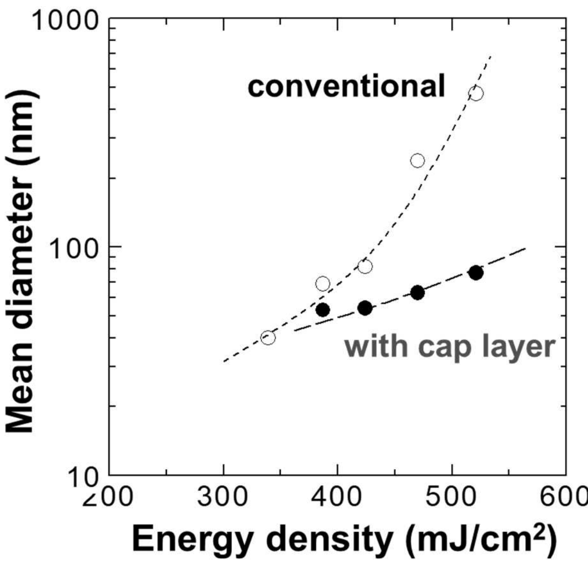


Figure 4.8 Grain size variation with laser energy density.

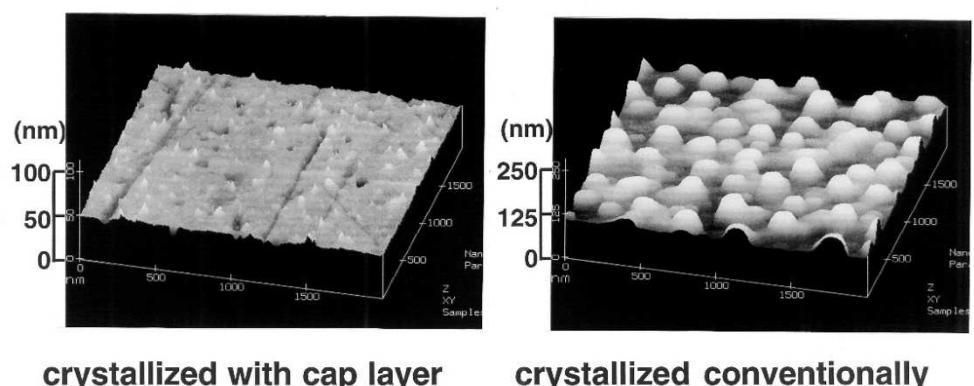


Figure 4.9 Surface roughness for the films
obtained by AFM (atomic force microscope).

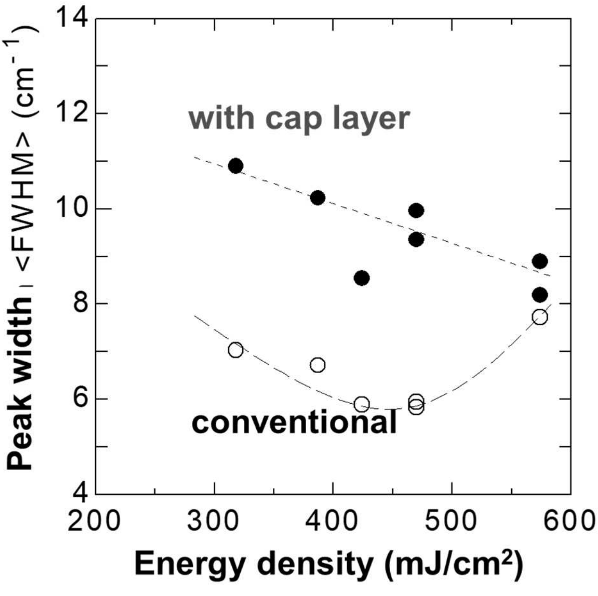


Figure 4.10 Peak width (FWHM) obtained by Raman spectroscopy.

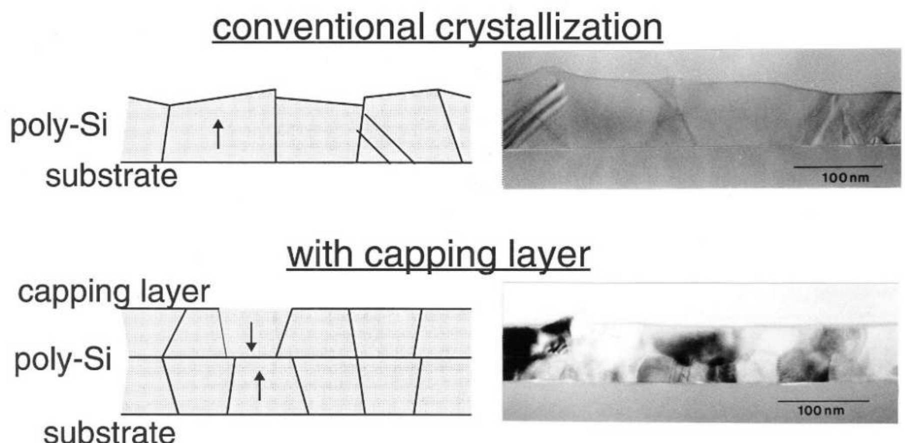


Figure 4.11 Cross sectional TEM photograph for the films fabricated by (a) conventionally and (b) with capping layer.

These characteristics in the films crystallized with capping layer suggested that grain size would hardly change at all with irradiation energy deviation, and that highly uniform characteristics of TFTs would be obtained. Figure 4.12 shows field effect mobility obtained from n-ch. TFTs as a function of the irradiation energy. In the conventionally fabricated TFTs, electron mobility variation was highly sensitive to the energy density as discussed in the section 2.3. The mobility increased with energy density. The peak value was obtained at about 450 mJ/cm^2 and then the mobility sharply decreased. When a capping layer was used, in contrast, the mobility increased gradually with energy density. In an energy range at around 400 mJ/cm^2, the mobility was remained fairly constant with respect to energy density. Applied this condition to the process for a large glass substrate of 350 × 300 mm^2, excellent uniformity of TFT characteristics was revealed as shown in Figure 4.13. Thus, it was confirmed that the capping layer was very useful for fabricating uniform performance TFTs.

In this method, grain size increases from 40 to 60 nm with the energy density, between 350 and 500 mJ/cm^2, and a two-layer structure is obtained, as compared with 40-400 nm range and a columnar structure with the conventional method. In the conventional laser melt-recrystallization, the nucleation site is on the interface of silicon/substrate, which causes free solidification of molten silicon in the direction of the top surface, and which results in crystallization dependent on energy density. In the newly developed technique, however, it can be assumed that the interface of silicon /capping layer plays the role of another nucleation site, and that the resultant two-way solidification controls grain size variability with respect to the irradiation energy. Excellent uniformity was attained in the poly-Si TFTs fabricated with the use of capping layer, i.e. mobility

was 50 cm^2/Vsec with 10 % deviation in the irradiation energy range from 380 to 470 mJ/cm^2. The wide process window for irradiation energy meant that peripheral driving circuits could be integrated by using those TFTs with 50 cm^2/Vsec in mobility even though total deviation of irradiation energy reached to be ± 10 %. This method could compensate variation of laser equipment more effectively than conventional one in both pulse-pulse instability and spatial deviation in a beam. The influence of spatial energy deviation on TFT characteristics is discussed in the next subsection 4.2.3.

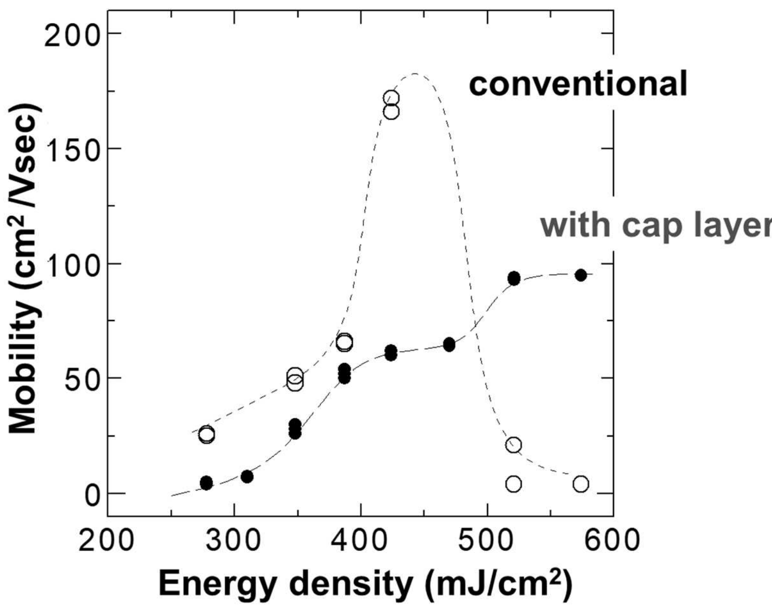


Figure 4.12 Electron mobility variation in n-ch. TFTs with laser irradiation energy.

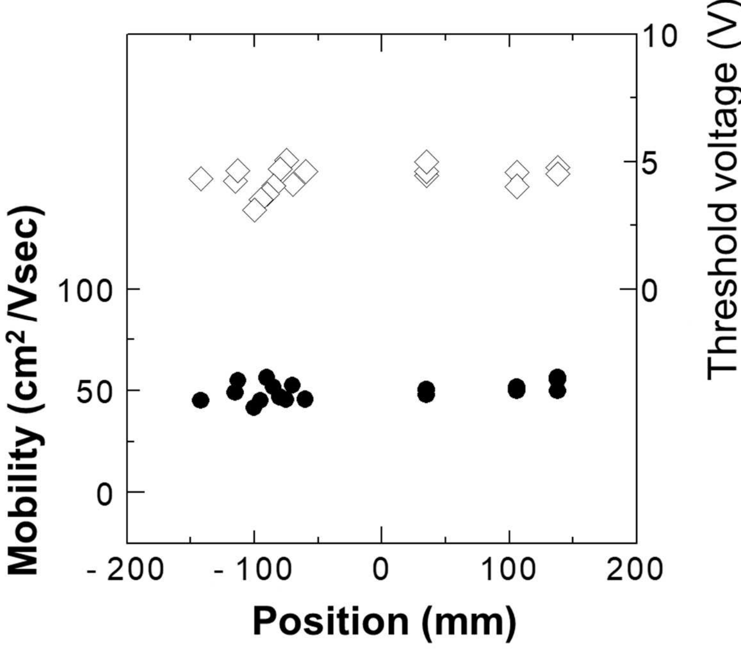


Figure 4.13 Mobility and threshold voltage distribution over a large substrate.

4.2.3 Divided design into adequate unit size

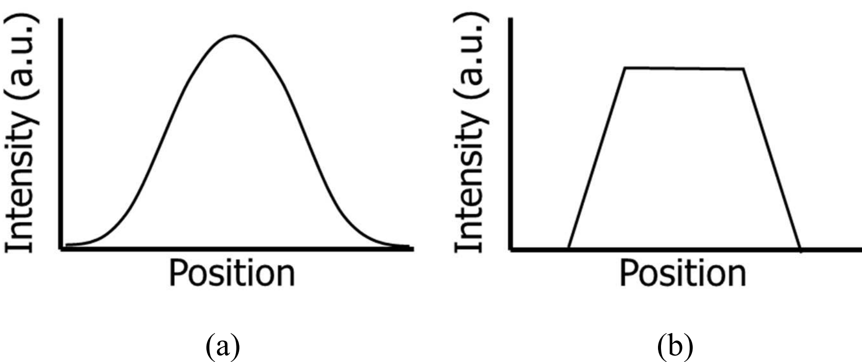
In this subsection, the beam profile of excimer laser is reviewed first, and next the issue for scanning the beam in order to obtain uniform performance for TFTs is discussed. Then a step and exposure method was demonstrated by using a beam whose uniformity was improved. Finally, a single scanning method is proposed.

The original output of an excimer laser is a quasi-rectangular beam with a near-Gaussian profile in the short axis as shown in Figure 4.14 (a), and a near-mesa profile in the long axis [188)]. The beam is generally reshaped to be ideal mesa profile as shown in Figure 4.14 (b) by the optics composed of typically a beam expander and intensity homogenizer. Because the size of reshaped beam of 5 × 5 mm in this study was much smaller than the one of a typical glass substrate, the beam was scanned to crystallize the area required. In this case, "scan" means the successive laser pulse irradiations overlapped with a constant frequency under the stage movement with a constant speed as shown in Figure 4.21 (a) [189)192)]. However, the TFT characteristics obtained by that method varied and lacked for reproducibility. The reason can be explained as follows. Region i), ii) and iii) in Figure 4.15 were assumed as a simple scanning model. The i) region was crystallized with an edge portion of the beam first (n-1) and recrystallized with a plateau portion next (n). The ii) region was crystallized twice with the plateau portion. So uniform

performance can be expected at this region. The iii) region, the order was reversed with the i) region, was crystallized with a plateau portion first (n-1) and another edge portion next (n).

Accordingly, a series of experiment for region i), ii) and iii) as described Table 4.4 (1), (2) and (3) was done and obtained the mobility variation as shown Figure 4.16. In the condition (1) that the energy for the first shot was lower than that of the second one, the peak of the mobility was revealed at about 340 mJ/cm^2. In contrast, mobility values in the whole range were almost same although there seemed slight variation in the condition (3) that the energy for the first shot was higher than that of the second one. The mobility value of condition (2) that the energies for the first and second shot were same was in the range obtained from the condition (3). These results suggested that second crystallization was more severely affected by lower energy than by higher one of first crystallization. In other words, it may conclude that crystallization history, especially lower energy crystallization in the prior shot, should be strictly controlled or that the region with lower energy in the peripheral of the beam should be avoided to fabricate a device. Therefore, a crystallization method to use only the plateau region was attempted.

Uniformity for the mesa shaped beam was not perfect actually, especially in the plateau region, even though it was produced through homogenizer. Figure 4.14 (b) described an ideal mesa shaped beam profile. However, the quality of homogenized beam depended on its design and optics used as shown in Figure 4.17. Uniformity for the beam A and B was ± 6.7% and ± 3%, respectively. Figure 4.18 shows the variations in the mobility and the threshold voltage from the TFT (W/L =6/6 μm) fabricated by using the beam A and B. Figure 4.18 (a) indicates twin peaks in mobility corresponding to each side edge of the beam A. In contrast, the uniformity in mobility was improved to be ± 4.2% by using the beam B as shown in Figure 4.18 (b).



(a) (b)

Figure 4.14 Intensity profiles illustrated for (a) the original beam of excimer laser and (b) homogenized beam at substrate surface.

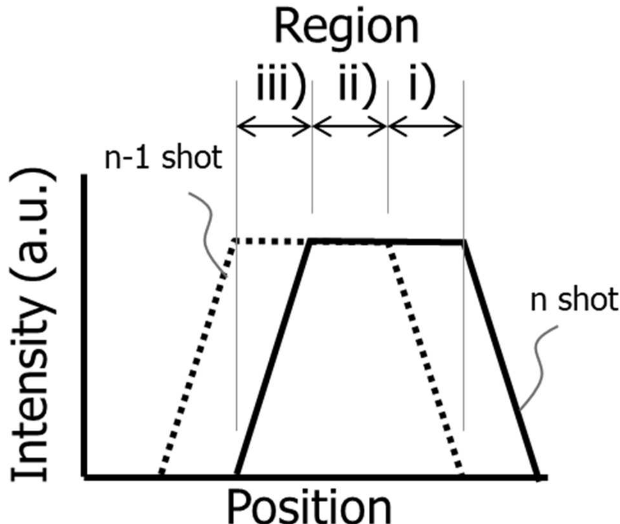


Figure 4.15 A simple model for scanning the beam. Histories; region i) front edge and homogenized region ii) 2 × homogenized region iii) homogenized and rear edge.

Table 4.4 Experimental irradiation condition

	1st shot	2nd shot	(mJ/cm^2)
(1)	263	263 – 360	
(2)	406	406	
(3)	406	263 – 406	

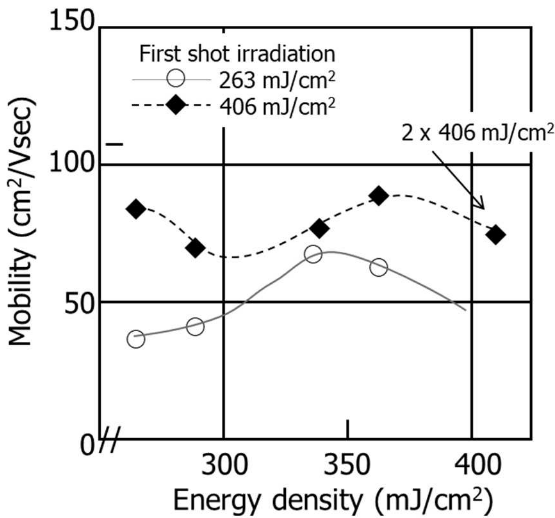


Figure 4.16 Mobility variation dependency on the second irradiation energy in the films crystallized with the first irradiation of 263 and 406 mJ/cm^2, respectively.

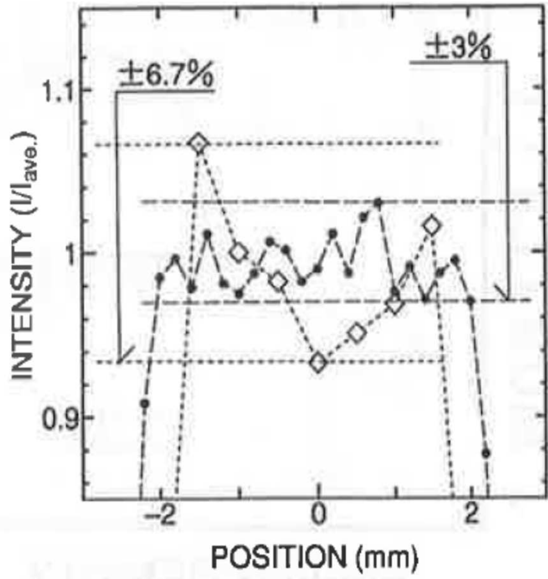


Figure 4.17 Intensity profiles for beam A and B,
whose uniformity was ± 6.7% and ± 3%, respectively.

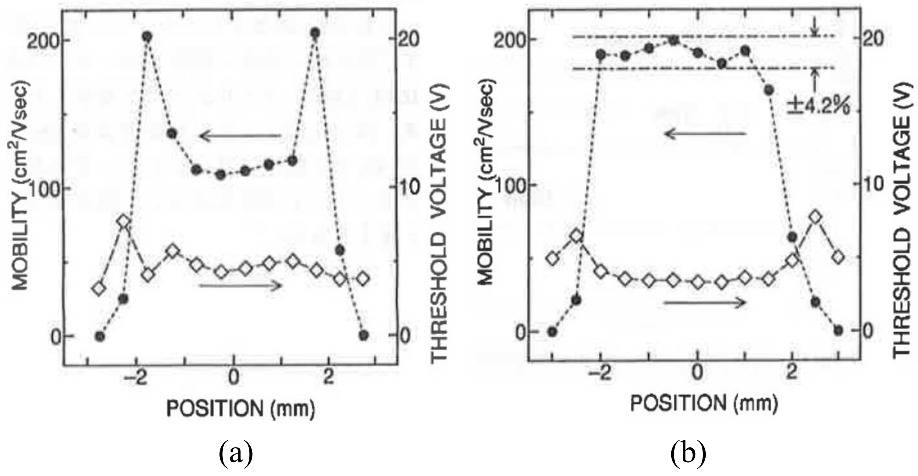
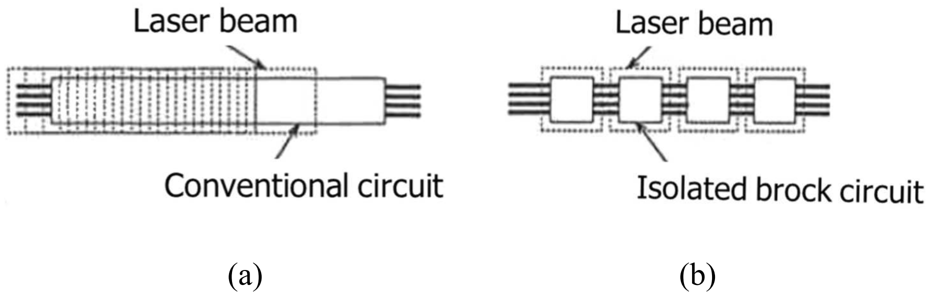


Figure 4.18 Mobility and threshold voltage profiles
fabricated by using (a) beam A and (b) beam B.

The beam B was applied to fabricate a scanning driver integrated in a linear image sensor. Figure 4.19 (b) illustrates the concept for isolated brock circuit with step and exposure method, comparing with continuous circuit with conventional scanning exposure in Figure 4.19 (a) [197)198)]. The poly-Si TFT driver was divided into several isolated block circuits. The size of each block was designed to be smaller than that of uniform area in the beam B. Because there was no TFTs between the blocks, the scanning

driver could be composed by poly-Si TFTs with highly uniform performance. The assembly for the image sensor is illustrated in Figure 4.20. By using those circuit design and process method, the poly-Si TFT CMOS driver integrated linear image sensor for A6 size with 720 bits at 8 line/mm was successfully demonstrated. The driver circuit with the CMOS shift register functioned at 1MHz clock under a 12 V supply voltage. This indicated that the driver has the capability of driving the image sensor at a scanning speed of 5 msec/line for an A4 size. The minimum readout time was measured at less than 2 μs/bit with 28 dB of S/N (signal/noise ratio), that was adequate for use in G3 mode facsimile.



(a) (b)

Figure 4.19 A concept for the step and exposure method and the isolated brock circuit. (a) conventional circuit and (b) isolated brock circuit.

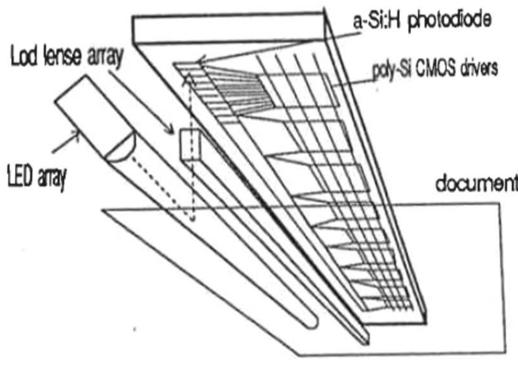


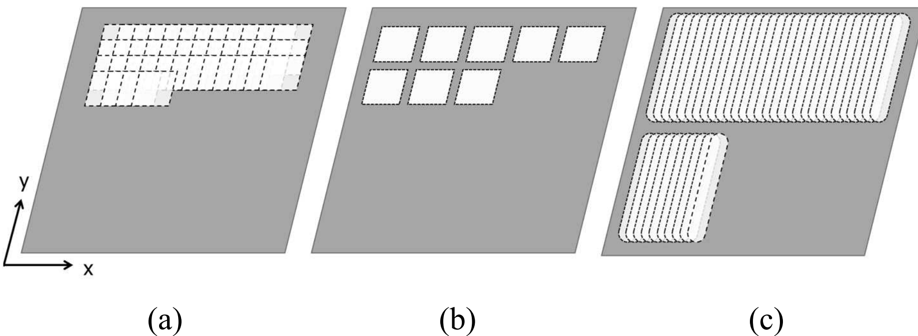
Figure 4.20 Illustration for the image sensor assembly [197].

4.2.4 Proposal for practical use

As discussed in this section, several ways were demonstrated to achieve uniform performance TFTs. Excellent uniformity was attained in the poly-Si TFTs fabricated with the use of capping layer. The deviation within 10% with mobility of about 50 cm^2/Vsec

was demonstrated on a large glass substrate. Also, by employing the isolated block circuit design, uniform and high performance TFTs were able to be applied to real devices. These results in this study were one of advantage against prior studies that aspired highest numerical values, in the view of practical development.

As for the set of isolated block circuit design and step/exposure method was able to apply to one-dimensional devices, such as a linear image sensor described above and peripheral driving circuits in displays. Because they could be divided into suitable size in each. However, it might be required extremely high power laser in order to apply it to two-dimensional active area in a display. In early 1990's a French manufacturer developed a high power laser that could output 15 J/pulse [189]. The area can be irradiated with an energy density of 300 mJ/cm^2 is only 50 cm^2 even using that laser without any optical loss. In the case of a display, the size must be limited to be about 4-inch diagonal. Therefore, the author proposed one-dimensional scanning method as below. Compared with the conventional method illustrated in Figure 4.21 (a), the proposed one (c) had features that avoid the line-shape overlapping for peripheral part "edge" of beams in x-direction and that has no overlapping area in y-direction [199]. And compared with the step and exposure method (b) demonstrated above, the method (c) could be applied to a device with larger size than that of beam because it had a potential to be enlarged the beam in y-direction. The overlapped laser pulse irradiations in x-direction as illustrated in Figure 4.15 was inevitable. However, the variation was expected to be homogenized statistically, not essentially, as a result of extremely small pitch irradiation. Following these studies, afterwards, a German manufacturer developed a line-shaped beam with a very high aspect ratio, for example 0.4 mm in x-direction and 150 mm in y-direction [200]. The technology has been improved much and scale-upped to be used widely in the industry.



(a) (b) (c)

Figure 4.21 Illustrations for three kinds of the beam scanning; (a) conventional scanning in x-y directions, (b) step and exposure method demonstrated, and (c) one directional scanning proposed.

4.3 Photo-leakage current

4.3.1 LCD with high luminance and high contrast ratio

The demand for a high luminance and high contrast ratio in applications of LCDs, such as projection light-valves [72)75)201)202)], mobile phones and PC monitors, has been growing with spreading wider into those applications. The luminance for LCDs, simply speaking, are decided by multiply of aperture ratio for TFT arrays and the luminance of backlight unit. The contrast ratio, on the other hand, is affected by the voltage to be hold for each pixel. The TFT driving a pixel has roles to write a data voltage under on-state as well as to hold it until the time wrote a next data voltage under off-state. Under the off state, the leakage current should be low enough to hold the data voltage. However, high luminance would increase photo-leakage current in the TFTs, that diminishes the data voltage, in turn, that would make the contrast ratio low. Consequently, it is important to suppress the photo-leakage current to obtain high-luminance and high-contrast LCDs. There are three ways to obtain those high-contrast LCDs. The one is to increase the storage capacitance of each pixel much enough to tolerate the leakage current electrically [203)]. The second one is to employ light-shield layer so that the light reach to the active poly-Si layer of the TFTs are physically reduced [204)]. The third one is to reduce the photo-leakage current itself in TFTs electronically.

4.3.2 Experimental procedures

In this section, the poly-Si TFTs with lightly-doped drain (LDD) structure that is a kind of offset-gate structures stated in section 4.1 were employed to investigate how the phot-leakage current being suppressed electronically by reducing the volume of active poly-Si layers. The structural parameters, such as thickness (t) of the active layer, width (W), channel length (L) and LDD length (L-LDD) of TFTs. A blue light, about 21 mW/cm^2, was used to illuminate on active layers without intentional light-shield from reverse surface of glass substrates. Then Id-Vg characteristics were measured with variety of structural parameters.

4.3.3 Results and discussion

Figure 4.22 shows the thickness (t) dependency on the photo-leakage current. As the thickness of the active layer was reduced from 60 nm to 30 nm, the photo-leakage current became half proportionally to the thickness without sacrificing on-currents of the TFTs, provided that sheet resistances of whole parts in the TFTs were kept constant. It

was suggested that the active layers should be made as thin as possible, as long as fabrication processes permitted. Figure 4.23 (a) shows the channel width (W) dependency on the photo-leakage current. As the channel width was reduced, the photo-leakage current was decreased proportionally. The L and the L-LDD dependency are revealed in Figure 4.23 (b) and (c), respectively. The photo-leakage current remained almost constant in the L range from 1 um to 4 μm with some fluctuations. In contrast, as the L-LDD decreased, the photo-leakage current was decreased linearly.

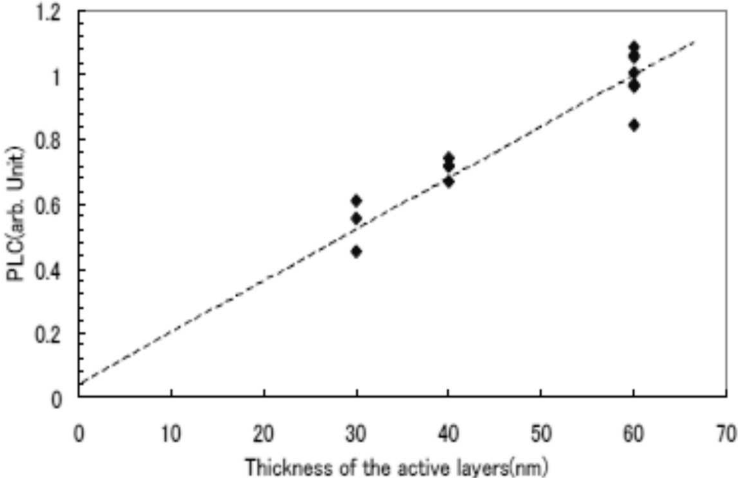


Figure 4.22 Thickness (t) of active layer dependency on photo-leakage current.

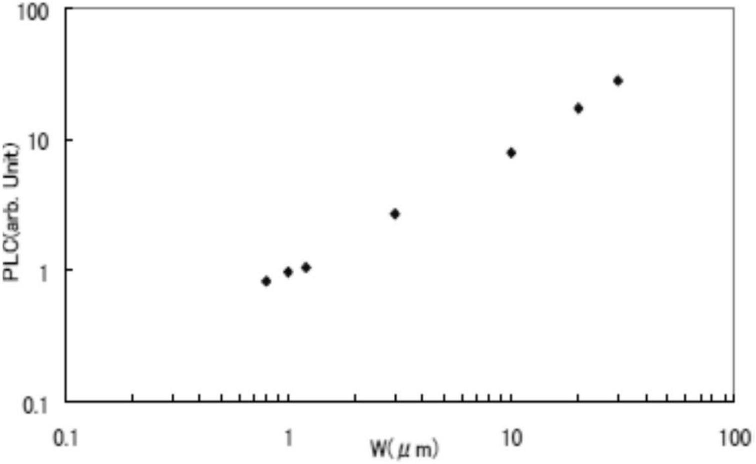


Figure 4.23 (a) Channel width (W) of TFTs dependency
on photo-leakage current. (L = 4 μm)

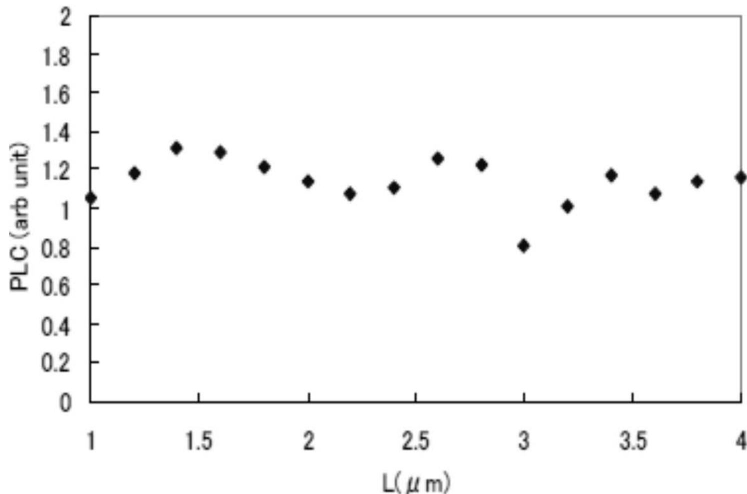


Figure 4.23 (b) Channel length (L) of TFTs dependency on photo-leakage current. (W = 4 μm)

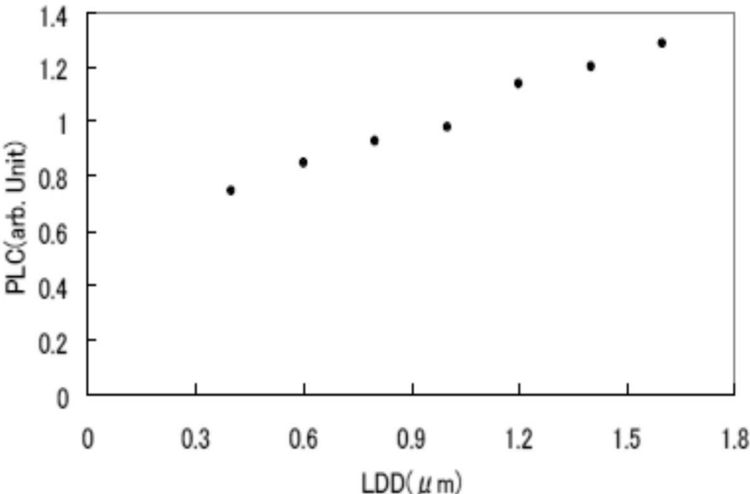


Figure 4.23 (c) LDD length of TFTs dependency on photo-leakage current. (W/L = 4/4 μm)

The mechanism for the photo-leakage current was considered as follows. As illustrated in Figure 4.24, electron-hole pairs would be excited when photon reaches the poly-Si layer. Although some of the excited pairs could disappear due to recombination of them before the pairs reach the drain region, some of them reach the drain region due to the potential difference across the LDD regions. If the number of carriers that reach the drain regions exceeded the number of them that recombine, the photo-leakage current can be observed to a certain extent.

The fact that the L did not effect on the photo-leakage current suggested that the lifetime for photo-generated carriers was not long enough to reach the drain region. Then, the series of experimental results showed that the photo-leakage currents were determined by the volume for LDD region, i.e. W × L-LDD × t. The thickness (t) of the poly-Si active layers had the most significant effect on the photo-leakage current reduction. Also it had the advantage that the reduction of the thickness (t) was possible without decreasing the on-current because sheet resistances of whole parts in the TFTs were kept constant by adjusting impurity conditions according to the change of the thickness. In contrast, as far as the channel width (W) and the LDD length (L-LDD) were concerned, there were some trade-offs. Decreasing the W also would reduce on-current. And decreasing L-LDD would increase the field emission current caused by the strong electric fields. Also the limitations for reducing the thickness was considered as follows. Quantitatively, transmittance of irradiated beam was estimated to be about 1% at thickness of 30 nm. Increase of the transmitted light directly changes the melt process itself and requires additional treatment to avoid unfavorable scattering. And qualitatively, the reduction of film thickness results in decreasing heat capacity, and requires precise control of irradiation energy more. Therefore, the adequate thickness was considered to be about 30 nm in practice. As discussed above, it was found that thinning the poly-Si active layer was the most effective way to suppress the photo-leakage current without any additional structure [205]. This technology has been widely used in actual products in high-luminance LCDs [206)209)].

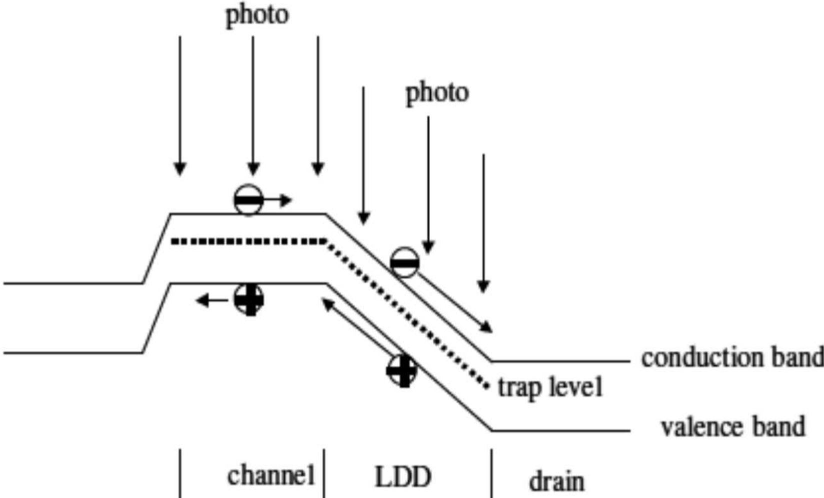


Figure 4.24 Schematic drawing the band diagram around the drain in TFTs under off-state.

4.4 Reliability

In the fabrication process for top-gate structure poly-Si TFTs, depositing silicon dioxide (SiO_2) film on mesa poly-Si islands is widely used. Prior to the SiO_2 deposition, however, the surface of the poly-Si islands is exposed to air and covered with a photo-resist. Even though a cleaning process is performed before the deposition, anxiety about the interface quality is inevitable. In the case of LSI process, a Si/SiO_2 interface must be formed in bulk Si through thermal oxidation. Even in the case of a-Si:H TFTs, an a-SiNx/a-Si:H interface is conventionally formed without exposure to air. In the poly-Si TFT fabrication process, therefore, a means of maintaining a clean surface during the interval between active layer formation and the gate oxide deposition should be developed and its advantages evaluated. In previous studies, a consecutive gate oxide deposition following active layer formation has been demonstrated and has been shown to be an effective way to obtain higher carrier mobility [208)209)]. This section discusses the attempt to form a clean poly-Si/SiO_2 interface through consecutive remote-plasma chemical vapor deposition (RP-CVD) [210)] of SiO_2 following excimer laser crystallization of the poly-Si layer. And then it is confirmed that threshold voltage (Vth) shift under dc stress can be reduced through this method.

4.4.1 Design and development for apparatus

Figure 4.25 illustrates the cluster-tool type apparatus we used in our experiments [213)]. It comprises a loading/unloading chamber, a heat-up chamber, two process chambers for the excimer laser crystallization (KrF: $\lambda = 248$ nm) and for the RP-CVD [212-214)], and a transfer chamber connected to the other four chambers such that exposure to air is avoided. Figure 4.34 illustrates cross sectional view of the RP-CVD chamber. A grounded mesh electrode has a role to confine the plasma between the upper electrode and the mesh electrode. The design that the substrate is located outside region of plasma are expected to avoid the plasma damages and to prevent excessive reaction in gas phase between oxygen and SiH_4. The RP-CVD process consists of five steps: 1) plasma-excitation of O2 and He gases; 2) transport of plasma-activated species, such as oxygen radicals (O*) and helium radicals, towards the substrates; 3) injection of SiH_4 near the substrate; 4) gas-phase reaction of the SiH_4 with the plasma-activated species; and 5) SiO_2 thin film deposition on the substrate surface.

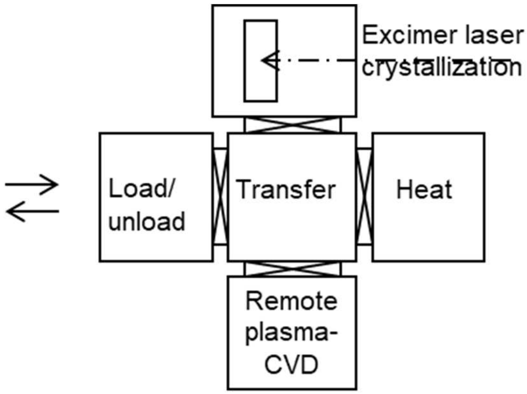


Figure 4.25 Plane view of the apparatus for
laser crystallization of Si film and SiO_2 film deposition

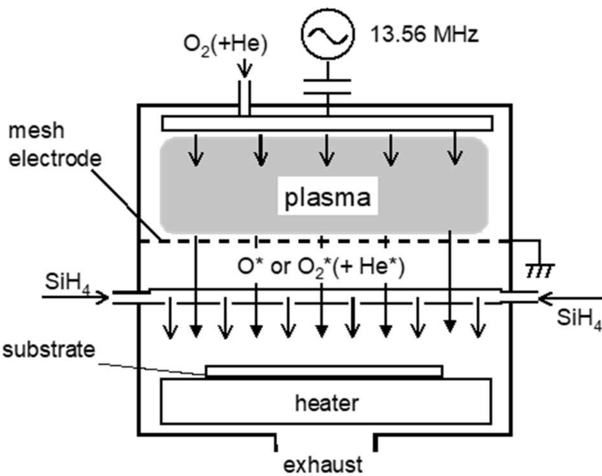


Figure 4.26 Cross sectional view of the RP-CVD chamber.

4.4.2 TFT fabrication

In the fabrication process for the poly-Si/SiO_2 interface, a substrate covered with a 75 nm thick a-Si film was loaded into the crystallization chamber. Then the film was crystallized and the substrate was transferred to the RP-CVD chamber by a robot hand within the apparatus. Then a 10-nm thick SiO_2 film was deposited. The deposition temperature, the pressure and the O_2/SiH_4 flow rate were 350 °C, 0.1 Torr and 40, respectively. After the isolation of mesa SiO_2/poly-Si islands, LP-CVD was used to cover them with a 30-nm thick SiO_2 layer.

The TFT fabrication flow is illustrated in Figure 4.27. A 1 μm thick SiO_2 passivation layer was deposited on the clean glass substrate through the low-pressure chemical-vapor-deposition (LP-CVD) technique. An a-Si film was then deposited on the substrate, and the series processes are performed in the cluster-type apparatus described above. After the isolation, LP-CVD was used to cover each SiO_2/poly-Si island with a 30-nm thick SiO_2 layer. For comparison, the author also employed a conventional process to form another poly-Si/SiO_2 interface, which includes the steps of laser crystallization, mesa island isolation in the air and 40-nm thick gate-oxide formation through LP-CVD. In both types of TFTs, an n^+-Si/WSi layer was then formed for the gate electrode. Self-aligned source-drain regions for the p-channel TFTs were then formed through the boron-ion doping method. Following this, the dopant activation at 550 °C and the plasma hydrogenation were performed. Finally, the TFT fabrication was completed by interlayer SiNx deposition, contact-hole formation and Al metallization. Experiments for measuring Vth shift under dc stress were performed in N_2 ambient at room temperature after 300 °C annealing to eliminate any possible influence of humidity [215].

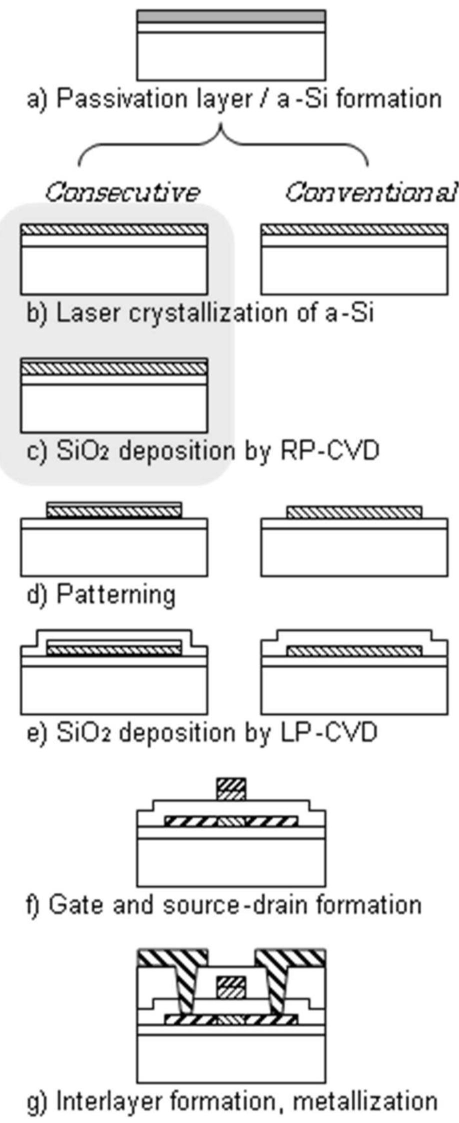


Figure 4.27 TFT fabrication flow.

4.4.3 Vth shift comparison

Figures 3.28 and 3.29 show negative Vth shift under dc stress in p-channel TFTs fabricated by using the above procedures. In the evaluation time period, the value of Vth shift in the consecutively processed TFTs was about one order of magnitude lower than that in the conventionally processed TFTs. In contrast, it was found that the degradation rate of the former was slightly higher than that of the latter. This has hardly any effect on the device operation, however, because extrapolation reveals that the time that the value of Vth shift under dc stress in consecutively processed TFTs exceeds that in conventionally processed ones is more than 10^8 seconds (about 3 years). We also confirmed that the dc stress for 10^5 seconds is equivalent to a pulse stress for 10^8 seconds

in conventionally processed TFTs. The shifts at 10^5 seconds were 0.15 V (conventional) and 0.03 V (consecutive), respectively.

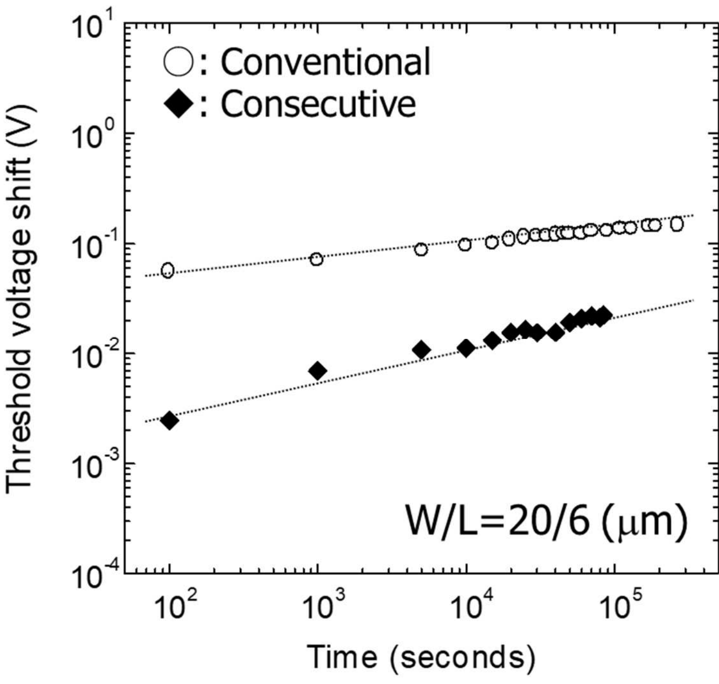


Figure 4.28 Negative Vth shift in p-ch. TFT under dc stress (Vg=-5V, Vd=0V).

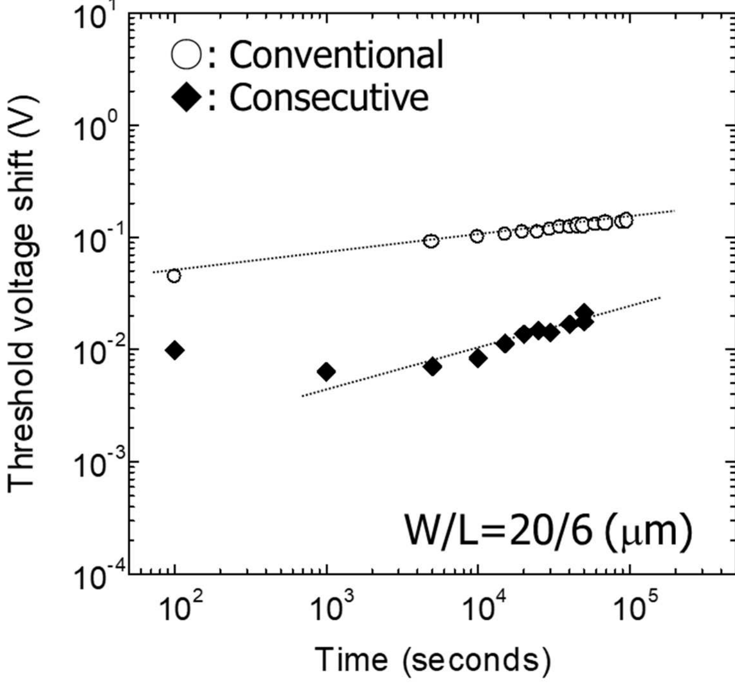


Figure 4.29 Negative Vth shift in p-ch. TFT under dc stress (Vg=-5V, Vd=-5V).

Table 4.5 Fixed oxide charge density (cm^{-2})

LP-CVD SiO_2	RP-CVD SiO_2
4.1×10^{11}	6.8×10^{11}

What is the reason for the reduction in the Vth shift? It had previously been reported that the positive charge created by a chemical reaction of hydroxyl group materials (absorbed water or Si-OH bonds) in gate oxide is the origin of the negative Vth shift in p-channel TFTs [215]. In this experiment, however, the amount of absorbed water was insignificant because the samples had been annealed at 300 °C as described above. It has also been reported that there is a correlation between the amount of Si-OH bonds and SiO_2 fixed oxide charge density (Df) [217]. However, the reduction in Vth shift cannot be explained by Df reduction either, because the Df in RP-CVD oxide is larger than that in LP-CVD oxide as shown in Table 4.5. Therefore, it is considered that the consecutive process itself, which can prevent native oxide formation, is the reason for the reduction of Vth shift. In conclusion, a clean poly-Si/SiO_2 interface formation, through consecutive remote-plasma chemical vapor deposition (RP-CVD) of SiO_2 following excimer laser crystallization of the poly-Si layer, effectively improved poly-Si TFT reliability. This is shown by the fact that Vth shift in TFTs fabricated with this process was 0.03 V at 10^5 seconds as compared with 0.15V in conventional TFTs. This reduction of Vth shift achieved with the clean interface formation has the potential to play an important role in attaining lower-voltage operation of poly-Si TFT devices.

4.5 Ultra high-mobility for integrating further functions

One of the goals for TFTs is to catch up with Si-LSI in their performance, such as mobility, enabling to integrate such fast logic circuits [217][218] and high density memories [219][220] as fabricated by current LSI technologies into a display substrate. Figure 4.30 shows a shift in research trend from AM-LCD on glass to System-on-glass (SOG) in early 2000's [221]. The integration for those functions, such as memory and MPU [222], on a glass requires higher mobility active layer to enable short-channel and low-voltage driving. Therefore, the active layer in TFT should be transformed from poly-crystalline to single-crystalline because the limitation for the mobility is mainly caused by their grain boundaries as illustrated in Figure 4.31. An approach based on the idea that active layer, at least channel region, should be a single crystalline was attempt to avoid the never-ending expansion for the size for single crystalline Si substrate. That approach required two technologies, the one was to make large grains with micrometer size [223-227] and the

other was to control the place for the grains [228)229)], that was almost same as the idea for selective nucleation and solid phase epitaxy [100)134)] discussed in section 3.1. This section describes the results attempted to fabricate Si grains at the location intentionally controlled and with the size of micrometer-order. First, the laser crystallization apparatus was developed to enable the size of grain enlarged and the grain location intentionally controlled, that was able to operate large glass substrates equivalent with the size for mass-manufacture. Then, the film properties fabricated by using the equipment were studied.

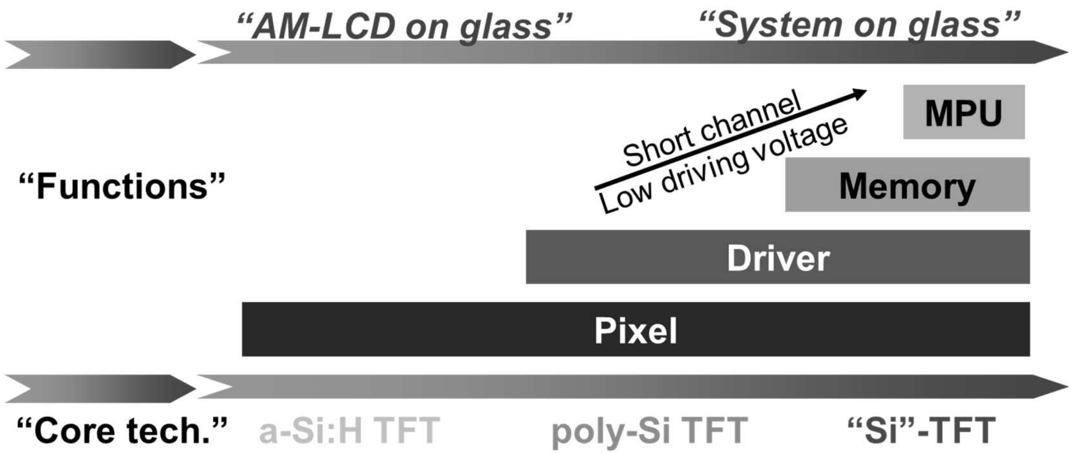
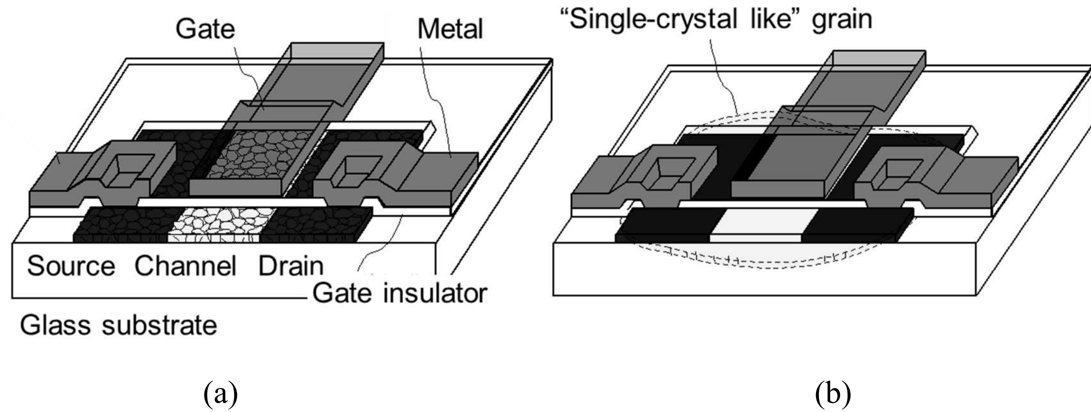


Figure 4.30 A trend in research toward System-on-glass (SOG) in 2000's.



(a) (b)

Figure 4.31 Illustrations for (a) conventional poly-Si TFT and (b) Single-grain Si TFT.

4.5.1 Novel apparatus for fabricating large grain Si films at desired position

Figure 4.32 schematically shows the newly developed excimer laser crystallization equipment [230)231)]. A beam generated by XeCl excimer laser that

wavelength was 308 nm and pulse width was 50 nsec at FWHM was focused on the mask through homogenizer, and then the beams shaped by the mask were projected on a substrate through a 1/3-reduction imaging lens. The mask stage was composed of an xy-stage, air bearings and linear motors. As the position for the mask was aligned to a mark on the substrate, the shaped beam could be irradiated on the desired position on the substrate. The shaped beam was also enabled to scan by the translation for the mask, and was controlled to be precise stepwise translation by the xy-stage. The maximum field size for the shaped beams was 6 × 10 mm. The beams could be created with variety of shapes by designing the mask apertures. An imaging lens whose numerical aperture was greater than that of lenses used in conventional excimer laser crystallization equipment was installed to enable the beam edge profile to be highly steep. The maximum size of the substrate was 300 × 350 mm and the substrate could be transferred up to be 100 mm/sec by an XY stage employing linear motors. The substrate stage was mounted on the three air cylinders that were placed on the XY stage. The XY stage was used to select individual field areas across the substrate. That is, as shown in Figure 4.33, the role of substrate (XY) stage was to select field area globally. In contrast, the role of mask (xy) stage was to translate precisely including alignment to the marks. Therefore, this technology can easily cope with expansion for the size of glass substrates. It had the function to focus the projected beam automatically on the substrate as summarized in Figure 4.34. Thickness tolerance of conventional glass substrates were less than 50 μm over 400 mm for so-called Generation II size (360 × 470 mm). A laser sensor measured the precise distance and the inclination of the substrate surface for a given field area. The air cylinders controlled attitude of to be within 3.8 μm of the depth of focus for the projection system at every field area. It had the roles of compensation both height and tilt. The substrate stage was installed in the chamber to enable the crystallization process could be conducted in N_2 atmosphere. Figure 4.35 illustrates a typical beam profile used in the series of this experiment. The projected beams on the substrate was shaped to be 1.3 - 10 μm (w) × 100 μm (l) with steepness of 1 μm (ds) at the edge[232].

By utilizing this apparatus, a 60 nm-thick a-Si film was prepared on a glass substrate for following crystallization experiments. Planar-type TFTs were also fabricated to characterize those crystallized films. A gate SiO_2 film was deposited at 330 °C by remote-plasma CVD [213][214]. The thickness of the SiO_2 film was 40 nm. Dopant activation was performed at 550 °C for source-drain formation. The dimensions for the TFTs were 10 μm of channel width and 2 μm of channel length. The position for the source-drain was arranged in the direction of w shown in Figure 4.35.

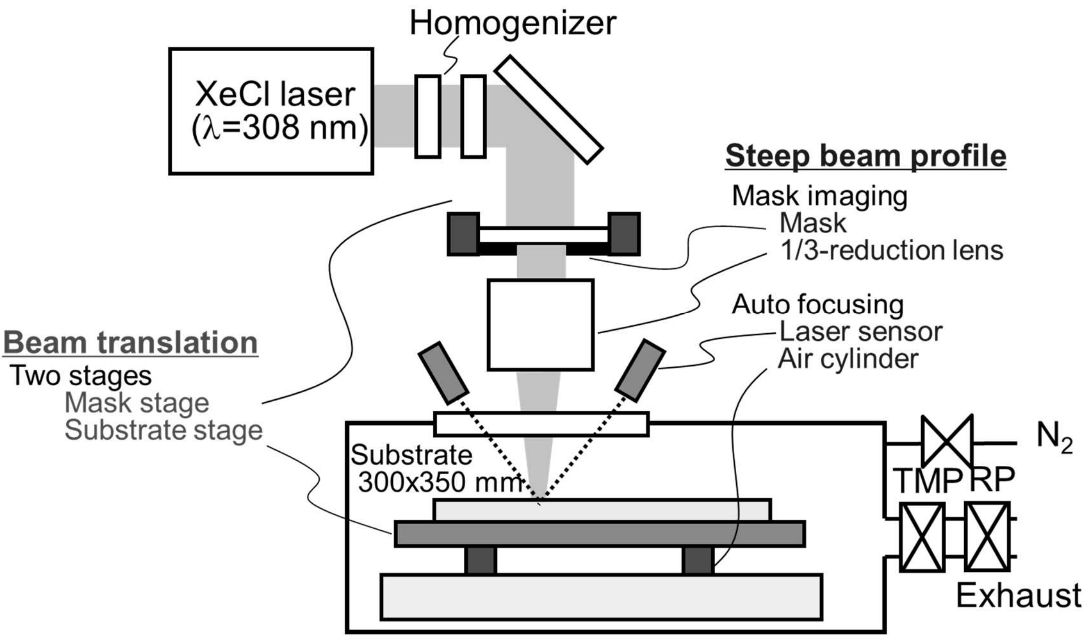


Figure 4.32 Schematic drawing the excimer laser crystallization equipment.

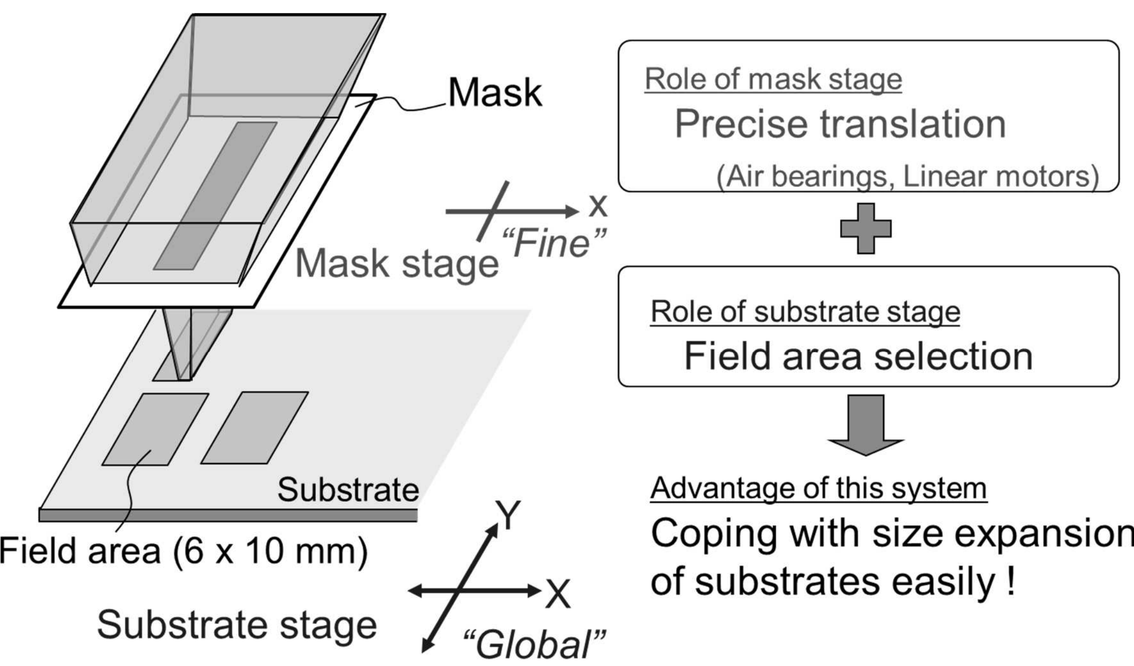


Figure 4.33 Functions of mask stage and substrate stage.

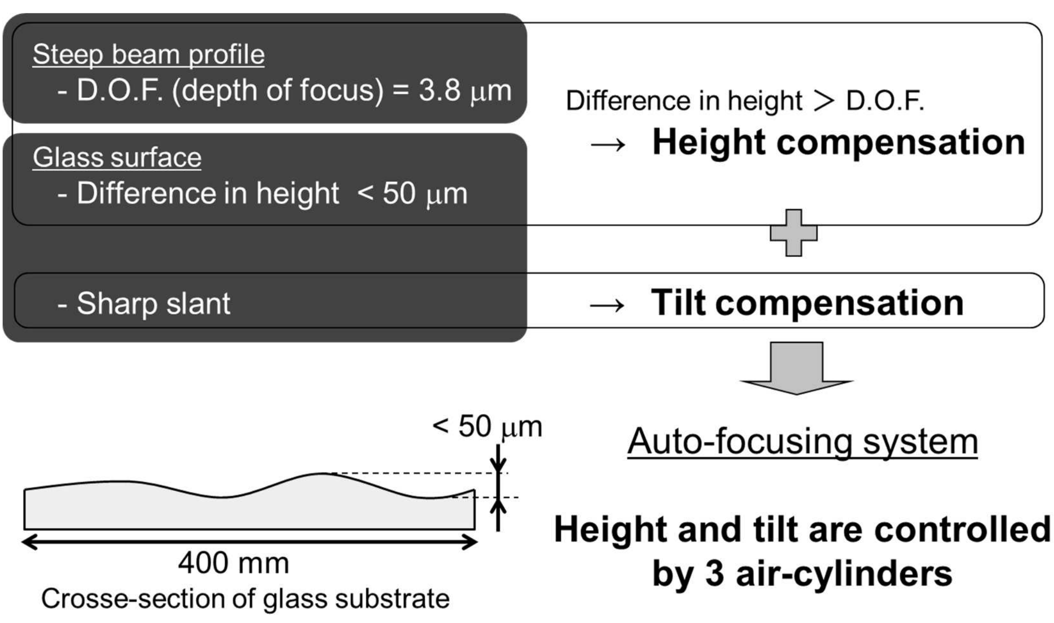


Figure 4.34 Necessity for auto-focusing system and role of air-cylinders.

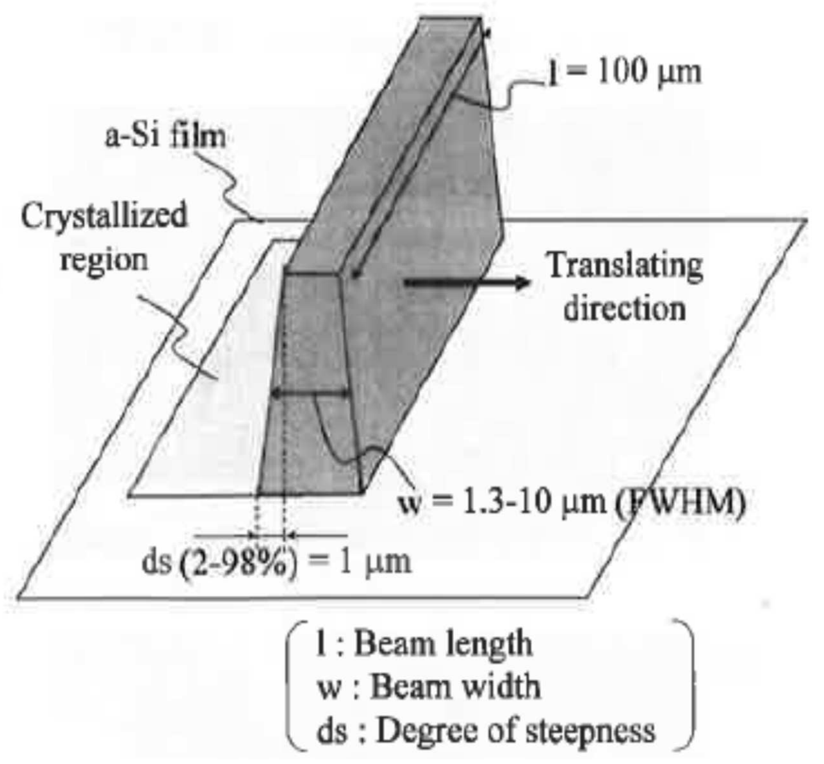
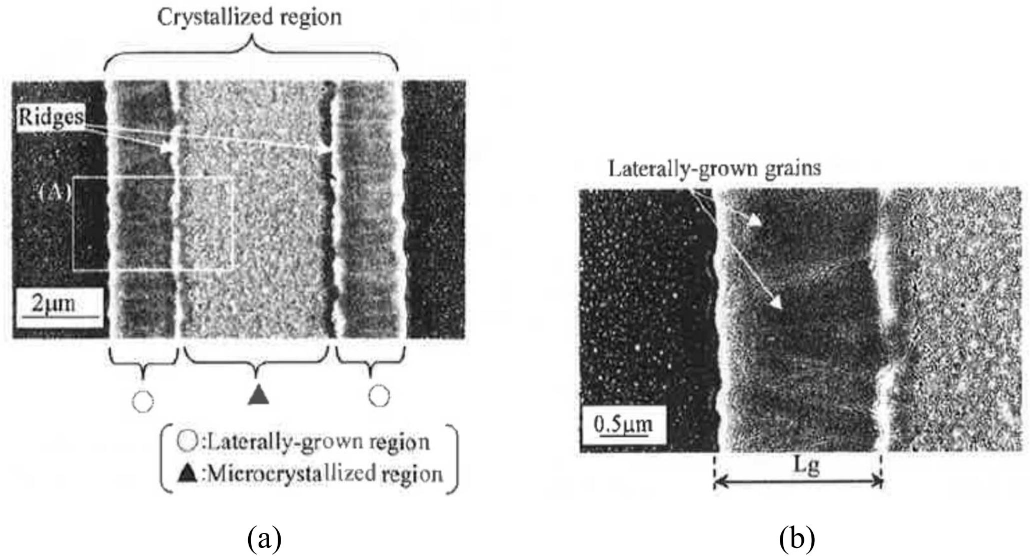


Figure 4.35 Schematic drawing the beam profile and beam translation[232].

4.5.2 Formation of large grain poly-Si films

Figure 4.36 show (a) the SEM image of a Secco-etched [165] Si film crystallized by a single pulse at a laser energy density of 600 mJ/cm^2 and with a beam width of 7 µm, and (b) the high magnification image (A) [232]. Secco-etching was conducted to highlight the grain boundary. There observed two sets of laterally-grown region and ridge at both sides of micro-crystallized region. The high magnification image (b) suggested that grains with individual size of approximately 0.3 µm were observed at directly to the right side of the ridge. The ridge appeared to have been formed by collisions between grain growths proceeding from opposite directions, left and right. In other words, the growth of the long grains originated at the beam edge and proceeded toward the inner region until colliding with grain growth proceeding from the microcrystalline region. On the basis of the SEM image, the lateral growth length of the long grains was estimated to be 1.8 µm. The difference in the lengths between the left and right sides of the ridge might be explained by the time lag for the nucleation between at the beam edge and at peripheral of microcrystalline region. As discussed in the section 3.2, the maximum temperature of the Si film was depended on the irradiation energy. It also meant that the time to reach the solidification point depended on the irradiation energy. That is to say, the nucleation started at the edge of the beam earlier than that started at the peripheral of the microcrystalline region, i.e. near center of the beam. It suggested that the increasing the time lag to start nucleation was effective to enlarge the lateral growth length.

Figure 4.37 shows the lateral growth length depending on the irradiation energy for a constant beam width of 7 µm. The lateral growth was observed above 400 mJ/cm^2, and the length increased with the irradiation energy [232]. The length reached 2.8 µm at an irradiation energy of 900 mJ/cm^2. Higher irradiation energy made the nucleation delay in the microcrystalline region. Assuming the energy value was constant to nucleate at the edge of beam, the delay gave the time for grains to extend further toward the inner region. Further significant increase in the irradiation energy, however, would be expected to results in decreasing the growth length because microcrystalline region would be enlarged or Si film would be ablated. Those results suggested that a quasi-single crystalline Si TFT with channel length of about 2 µm could be arranged at the position grains were laterally grown.



(a) (b)

Figure 4.36 (a) SEM image of single-pulse-crystallized Si film
and (b) High magnification image of region (A) [232] .

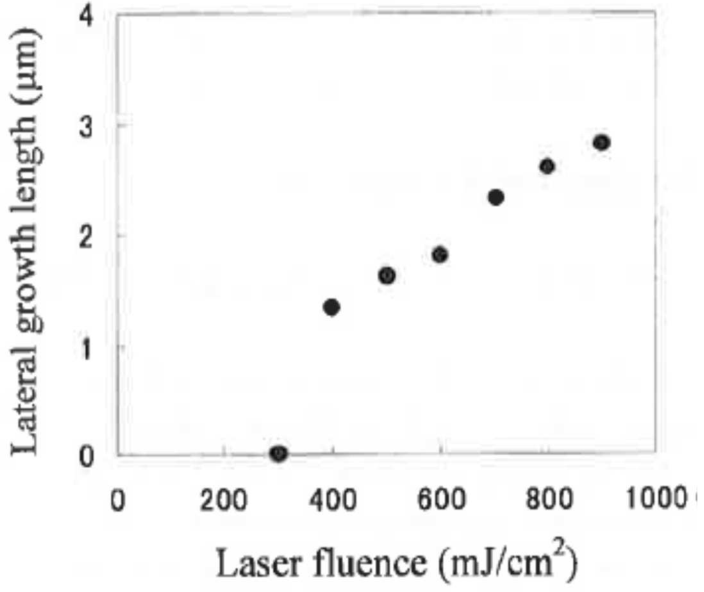


Figure 4.37 Lateral growth length depending
on irradiation energy w=7 μm [232].

In the case that larger grains were necessary, a process to repeat irradiation and translation was effective as described below. Figure 4.38 shows SEM image of Si film crystallized by repeating a set of single-shot irradiation of 600 mJ/cm^2 and translation of 1 μm with beam width of 3.7 μm[232]. Figure 4.39 shows a classification of the Si film

structures depending on the conditions both irradiation energy and beam width. The structures were mainly depending on the irradiation energy [232]. Fine grain structures were observed under the conditions of lower energy range. In contrast, there observed Si films ablated under the conditions of higher energy range and relatively longer beam width. The range of irradiation energy that grains were extended was significantly wide, more than ± 10 % from a mid-value of 600 mJ/cm^2 for the beam width of 3 µm. A series of these study indicated that selection for higher energy range and narrower beam width made it possible to enlarge the conditions to obtain extended grains.

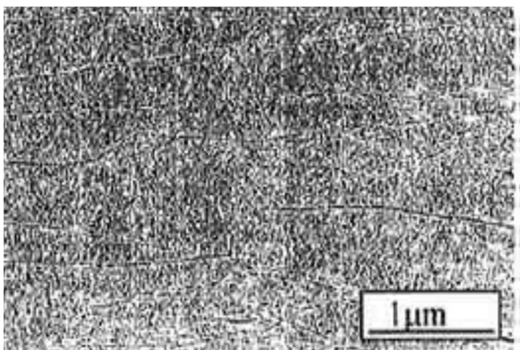


Figure 4.38 SEM image of Si film crystallized by repeating irradiation and translation[232].

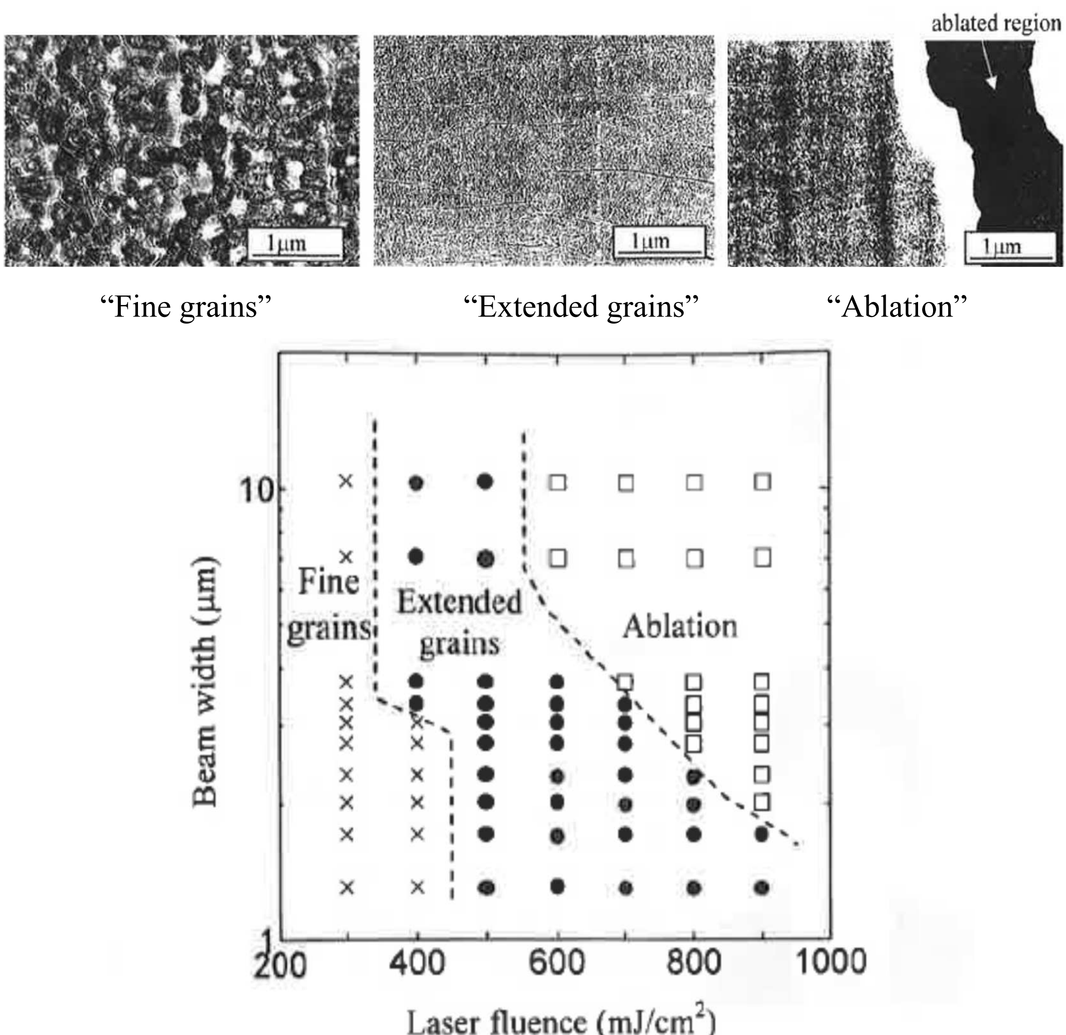


Figure 4.39 Classification for the structure of Si films [232].

4.5.3 High performance TFTs by employing the large grain poly-Si films

Then TFTs were fabricated by employing the Si films crystallized with irradiation energy range of 300-600 mJ/cm^2, a beam width of 3.7 μm and pulse-pulse translation distance of 0.5 μm. Figure 4.40 shows typical Id -Vg (drain current - gate voltage) characteristics for both an n-channel and a p-channel TFTs. And, Figure 4.41 plots mobility as a function of irradiation energy. The mobility in n-ch. TFTs increased sharply from 150 to near 300 cm^2/Vsec with increasing the irradiation energy from 300 to 400 mJ/cm^2, and remained almost constant around 270 cm^2/Vsec. The mobility in p-ch. TFTs followed similar trend with being the constant mobility of 230 cm^2/Vsec. The range the mobility kept constant coincided with the range that extended grain was obtained. In n-ch. TFTs, mobility values more than 250 cm^2/Vsec can be achieved by

using other excimer laser crystallization methods[209], such as one directional scanning discussed in the section 4.2. In such case, however, the fluctuation of irradiation energy needed to be strictly controlled within ±5 %. It was found that this study gave wide process margin in this respect. It was also found that the mobility in p-ch. TFTs in this study revealed higher value than those in prior reports. As described above, a new excimer laser crystallization system to produce quasi-single crystalline Si films stably on a large glass substrate of 300 × 350 mm was developed. As the results, it made possible to fabricate high mobility, 270 $cm^2/Vsec$ in n-ch. and 230 $cm^2/Vsec$ in p-ch., TFTs at predetermined positions as shown in Figure 4.42 [233][234].

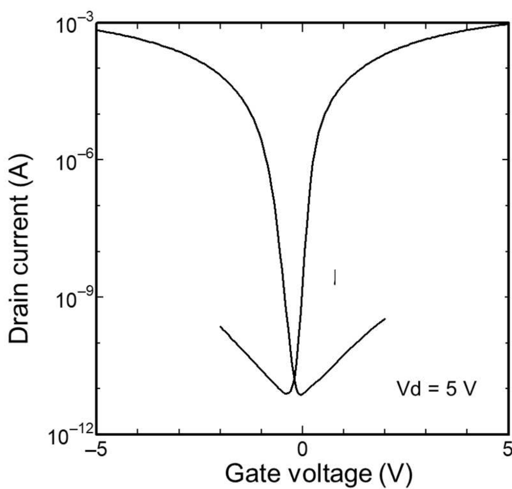


Figure 4.40 Id-Vg characteristics (|Vd| = 5V, W/L = 10/2 μm) employing a film crystallized with irradiation energy of 400 mJ/cm^2.

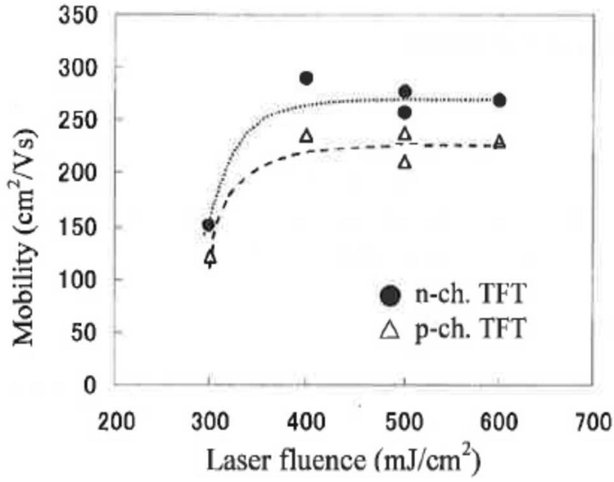


Figure 4.41 Mobility dependence on irradiation energy[232].

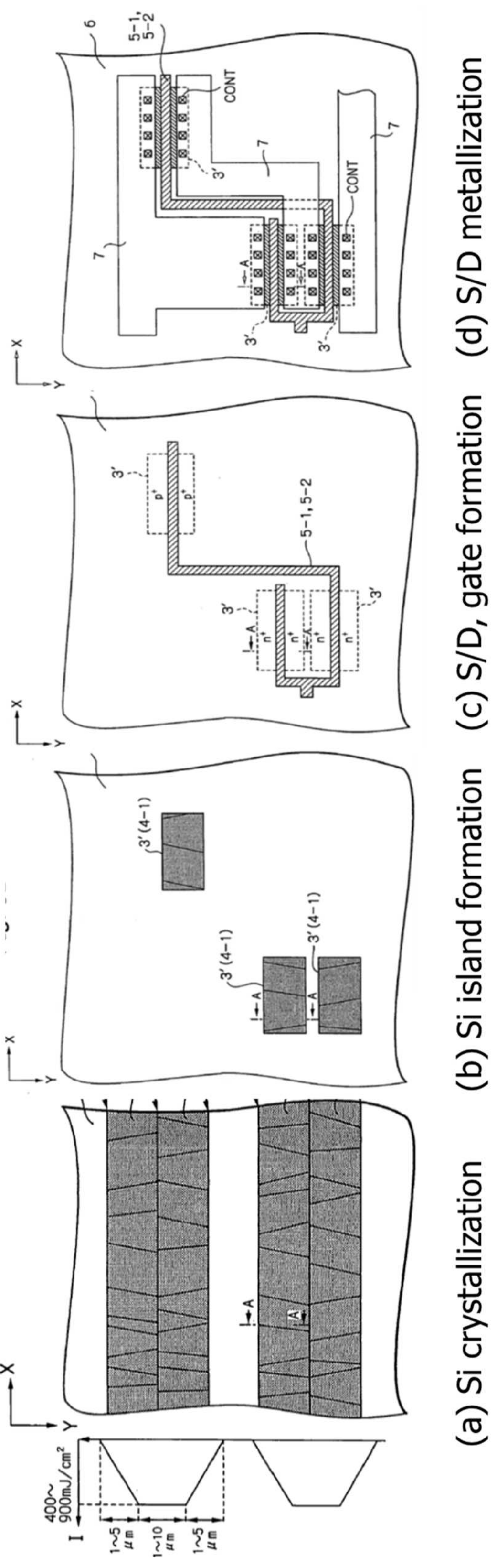


Figure 4.42 TFTs designed at predetermined positions.

4.6 Summary

In this chapter, the author proposed and demonstrated the ways to improve poly-Si TFT characteristics in i) uniformity, ii) photo-leakage current and iii) reliability. In addition to those, he also developed iv) a novel apparatus for fabricating quasi-single grain Si thin-films and demonstrated high-mobility TFTs by employing those films.

i) In the uniformity issue, quite uniform TFTs were obtained by the approaches in process, employing pre-crystallized film as the precursor or using capping layer during crystallization. Quite uniform mobility characteristics within 10% was obtained with wide range of irradiation energy more than 90 mJ/cm^2 in both of those. Also it was demonstrated that a new design with plural isolated circuit blocks was effective to operate one-dimensional driver circuit which was longer than the exposure area of individual laser shot by applying to a driver-integrated linear image sensor. These results in this study were one of advantage against prior studies that aspired highest numerical values, in the view of practical development. Then a scanning method in one direction (x) was proposed, that was avoid to produce the overlapping region in another direction (y). ii) In order to suppress the photo-leakage current, it was found that thinning the poly-Si active layer, especially in LDD region, was the most effective without any additional structure. It can be reduced proportional to the thickness. Limitation of the thickness estimated to be about 30 nm due to other restrictions in process. This technology has been widely used in actual products in high-luminance LCDs. iii) For stable operation, a clean poly-Si/SiO_2 interface formation, through consecutive deposition of SiO_2 following excimer laser crystallization of the poly-Si layer, effectively improved the reliability. This was shown by the fact that Vth shift in TFTs fabricated with this process was 0.03 V at 10^5 seconds as compared with 0.15V in conventional TFTs. Finally, iv) to fabricate large-grain crystalline Si films and those TFTs practically, a novel apparatus was developed. It was equipped functions of a substrate-stage able to compensate attitude (tilt as well as height) in a vacuum chamber, a mask-stage able to translate precisely and a mask-projection optical system with one-third reduction lens. By using the apparatus, lateral grain growth reached to be 2.8 μm in a single laser shot and the mobility in both n- and p-channel indicated more than 200 cm^2/Vsec.

5. Conclusion

The main purpose for this series of study is to make it possible for large-area microelectronics devices based on poly-Si TFTs to be used practically. In this thesis, low-temperature growth techniques for crystalline silicon were studied first in three different ways under gas, solid and liquid phase. As they were at different time periods, those investigating objectives were adopted along each technical stage when they were studied. Then, the excimer laser crystallization was selected to study how fabricate poly-Si TFTs for practical use. As there were still many challenges in order to apply it practically, this work focused on practical development, such uniformity and reliability. Thus, some of individual study were accompanied by the developments of novel apparatus to fabricate the poly-Si films and their TFTs.

5.1 Low-temperature crystalline growth technologies for silicon thin-films

5.1.1 Gas phase direct deposition by using HR-CVD

This series of study was aimed to understand behaviors for crystalline growth at low temperature employing the HR-CVD. First, by utilizing a conventional coaxial microwave plasma reactor, epitaxial growth was observed on the Si (110) and (100). The growth rate reached to be 1.5 nm/sec, that was almost equivalent to that of μc-Si films on a glass substrate. Impurity doping was also achieved by mixture of source gases. However, the crystalline structure was deteriorated as increasing thickness or impurity concentration. There was an optimum temperature range of about 300-350 °C in the epitaxial growth.

Because it was considered that not only the kinetic energy supplied from the substrate temperature but also the balances of chemical reactions originated by atomic hydrogen played an important role in this growth process, an additional microwave plasma reactor was introduced to supply atomic hydrogen into growth surface. As the results, the supply of additional hydrogen effectively promoted the epitaxial growth increasing both thickness and doping concentration. The highest temperature for epitaxial growth was extended to be 400 °C and also the optimum temperature decreased to be 300 °C. Atomic hydrogen surely played an important role to promote reactions in making Si-network, and enabled to obtain higher concentration of impurity doping and thicker growth of epitaxial films. The highest electron Hall mobility was obtained to be 115 $cm^2/Vsec$ with the carrier concentration of 2×10^{16} cm^{-3} in the epitaxially grown P-doped silicon film. However, there still remained two major approaches, microscopically to

control the nucleation process and macroscopically to deposit those films on a large substrate, in order to extend this technique to the large-area microelectronics.

5.1.2 Solid phase crystallization employing grain-boundary filtration with SNSPE

A grain boundary filtration technique was proposed and demonstrated for fabricating single large grain semiconductor thin films on amorphous substrates by using selective nucleation (SN) and lateral solid-phase-epitaxy (SPE). In the study of Ge, the lateral SPE started at the edge of the SN site and the grain selection process produced only one grain orientation at the entrance to the main rectangular island. A single planar grain which is larger than 100 μm^2 was successfully crystallized at 400 °C in approximately 1300 min. without any occurrence of spontaneous nucleation.

In another study of Si, more than several micrometers of grain growth were successfully demonstrated at around 600 °C by introducing Ni into SN sites. However, grain boundary filtration through the planer constrictions was not enough. There were two possible reasons. The one is that the concentration of Ni in the seed selection region was not enough to promote the silicide mediated crystallization further because the growth front was expanding wider after the lateral grain growth reached to main island. The other was corresponding to the needle-like growth mechanism unique to Ni mediated crystallization. When two crystallized needles collide each other, the growth was stopped and resulted in leaving amorphous regions around the needle-like crystalline grains.

5.1.3 Liquid phase crystallization by utilizing excimer laser

This subsection revealed that the properties of excimer laser crystallized poly-Si films are strongly dependent on both the irradiation energy and the number of laser shots. As for the irradiation energy dependency, cooling rate was evaluated by using numerical transient-temperature simulation in order to investigate the fact that electron mobility sharply decreased at higher energy range which results in micro-crystallization. Since the results of cooling rate near the melting point of crystalline Si were not supported by the findings of the SEM observation, the maximum cooling rate during the crystallization was focused. The maximum cooling rate increased monotonically with irradiation energy. It was found that the micro-crystallization occurred at a quenching rate of 1.6×10^{10} °C /sec. Furthermore, the maximum cooling rate for the crystalline Si precursor was smaller than the rate for a-Si, i.e., the (micro-) crystalline Si should be micro-crystallized at a higher energy density than the a-Si. It suggested that the micro-crystallization can be suppressed by multiple-shot crystallization at the critical energy density at which a-Si would be micro-crystallized.

As for the number of laser shots dependency, electron mobility increased monotonically with the number of irradiations, with maximum mobility being obtained at about 20 shots. TEM observations showed that, for these poly-Si films, the number of shots had no effect on grain size, which was about 150 nm diameter. In contrast, Raman studies indicated that the disorder in those films, including small grains, grain boundaries and defects in grains lessened as a result of a number of successive shots, and then worsened again after further shots. These results suggested that the conditions at silicon/quartz interface play an important role during the laser re-crystallization, and that there are some optimum conditions for the re-crystallization process.

5.2 Excimer laser crystallized poly-Si TFT Technology

5.2.1 Fabrication for uniform performance TFTs

It had been very difficult to obtain uniform films with the excimer laser crystallization method because of the variation for irradiation energy and of the limited size of the laser beam. Irradiation energy variation was caused by a lack of pulse-to-pulse stability in the emission of excimer laser and spatial energy differences in the laser beam. The laser irradiation was forced to be overlapped because of the limited size of single laser beam. To overcome the former issue, two of new method were confirmed to be effective. The pre-crystallized films under solid phase as the precursor were showed wide window in irradiation energy. Capping layer was also effective to suppress the variety of grain size against the irradiation energy. Quite uniform mobility characteristics within 10% was obtained with wide range of irradiation energy more than 90 mJ/cm^2 in both of those. These approaches alleviated variation of TFT characteristics against the variation of irradiation energy. To avoid the latter issue, a special circuit design on the glass substrate was employed to use only uniform region and to avoid the use of the edge region of the beam. This method was successfully demonstrated by applying to a one-dimensional image sensor. In the view of practical development, these results obtaining uniform performance showed remarkable progress against prior studies that aspired highest numerical values.

5.2.2 Reduction for photo-leakage current

The series of experimental results showed that the photo-leakage currents were determined by the volume for LDD (Lightly Doped Drain) region, i.e. "channel width" × "LDD length" × "thickness". The thickness of the poly-Si active layers had the most significant effect on the photo-leakage current reduction. Also it had the advantage that

the reduction of the thickness was possible without decreasing the on-current because series resistances of whole parts in the TFTs were kept constant by adjusting impurity conditions according to the change of the thickness. In contrast, as far as the channel width and the LDD length were concerned, there were some trade-offs. Decreasing the channel width also would reduce on-current. And decreasing LDD length would increase the field emission current caused by the strong electric fields. As stated above, thinning the poly-Si active layer was the most effective way to suppress the photo-leakage current without any additional structure. It can be reduced proportional to the thickness. Limitation of the thickness estimated to be about 30 nm due to other restrictions in process. This technology has been widely used in actual products in high-luminance LCDs.

5.2.3 Improvement for reliability for the TFTs

A clean poly-Si/SiO_2 interface formation, through consecutive remote-plasma chemical vapor deposition of SiO_2 following excimer laser crystallization of the poly-Si layer, effectively improved poly-Si TFT reliability. This is shown by the fact that Vth shift in TFTs fabricated with this process was 0.03 V at 10^5 seconds as compared with 0.15V in conventional TFTs. This reduction of Vth shift achieved with the clean interface formation has the potential to play an important role in attaining lower-voltage operation of poly-Si TFT devices.

5.2.4 Development for high-mobility TFTs and the apparatus for manufacture

In order to obtain higher performance TFTs, an apparatus was developed to obtain location controlled large-grain Si films. It featured optical projection systems with maximum field size of 6 × 10 mm, two independent stages for precise translation of mask and for field area selection on substrate, and attitude control system to compensate both height and tilt on the surface of conventional glass substrate. This technology could easily cope with each generation in production even the size of glass substrates was expanded. By using apparatus, lateral growth length up to 2.8 μm with single laser shot were demonstrated. Precise translation of mask also enabled to extend the growth length in laterally. The field effect mobility of 270 cm^2/Vsec for n-channel TFT and 230 cm^2/Vsec for p-channel TFT were demonstrated at predetermined positions by employing those films.

5.3 Current status

Today, the excimer laser crystallization is the dominant technology, as one of the key processes in the LTPS, to produce high-resolution displays indispensable for

smartphone products[235]. Table 5.1 shows the current status for the LTPS compared with a-Si TFTs and HTPS. It has already reached enough level to manufacture LCDs and OLEDs in small size less than roughly 10-inch diagonal. In recent years, manufacturers are challenging to extend its applications. One approach is to enlarge their size. For example, the demand for high-resolution displays more than 10-inch diagonal have been gradually increased to show more information in vehicles[236]. Because those automotive displays require high-luminance[237], typically more than 800 cd/m^2, the technology to reduce photo-leakage current, such discussed in section 4.3, is indispensable for LCDs. As for OLED, because higher driving current is necessary to drive each OLED pixel with higher luminance than smartphone, improvement for the reliability, such discussed in section 4.4, is important more and more. Also, the LTPS technology has been applied to an OLED product that size is more than 20-inch diagonal [238]. The other approach is to make displays flexible. Curved displays have been practically installed in smartphone products. Some of smartphone products have released with featuring folding displays [239]. Much attention is paid in reliability because the process temperature is decreased to employ flexible substrate, such polyimide.

Table 4.1 Current applications in market by growth method

	Gas phase	Solid phase	Liquid phase
Film property (typical)	amorphous (a-Si:H)	crystalline (poly-Si)	crystalline (poly-Si)
Typical process temperature	300 °C	1000 °C	500 °C
Substrate	Glass	Quartz	Glass
Main application	AM-LCD	LC light-valve (for projector)	AM-LCD AM-OLED
Typical size	Medium- Large (>10")	Very small (<2 ")	Small (4-6")
Display resolution	< 200 ppi	> 800 ppi	300 ~ 500 ppi
Named in industry	TFT	HTPS	LTPS

5.4 Future prospects

The poly-Si TFT technology has been widely used in practical product and established a solid position in display industry as described above. However, there still remains some technical issues to be challenged because OLED (driven by current) requires uniformity and stability in TFT characteristics more than LCD (driven by voltage). The first one is uniformity in TFT characteristics. The issue is originated by fabrication method that the laser beam is scanned to cover the whole substrate. Compensation circuits are employed to alleviate the image mura caused by the variation in driving current originated in the beam scanning[79)237)]. The compensation circuits need typically 6-7 TFTs for each pixel, and it is one of the reasons that the resolution for OLEDs is less than that of LCDs that is driven by single TFT for each pixel [178)]. The second one is transient stability in dynamic characteristics. That is a retention phenomenon observed at the time to change image data [240)]. The phenomenon called "image retention" is observed, for example, when displayed image was changed to be fully gray just after white/black image like a chess board. The third one is the leakage current in the dark state. There is an attempt to reduce the power consumed for rewriting by reducing the frame frequency from 60 Hz to about 15 Hz, and to 1 Hz desirably [241)]. At this time, the driving TFT connected to the light emitting element is required to constantly supply a current. As shown in Figure 1.4 (c), the driving TFT is controlled by the switch TFT and the voltage applied to the driving TFT is held by storage capacitor (Cs). By reducing frame frequency, the brightness fluctuates and is visually recognized as a flicker as the current decreases due to the variation of the gate voltage applied to the drive transistor originated in the leakage-current in the switch transistor. Therefore, the reduction for leakage-current is now expected for poly-Si TFTs.

Origin of the first challenge is the size of laser beam is still smaller than that of glass substrate as described in section 4.2. The beam size has been increased, but the substrate size has also been expanded. This series of study can suggest some ways to overcome this challenge. Practically, the cap layer is effective to suppress reflection of Si surface to be roughly one half as discussed in section 4.2. It means that efficiency of irradiation energy to contribute melt-recrystallization could be increased. Combining with a high-power laser, such 15 J/pulse[189)], the single shot crystallization that is described as the step and exposure method in section 4.2 makes it possible to enlarge the area crystallized without scanning. At that time when the step and exposure method was studied, the size of target products was unknown. Now, however, the target size is apparent. Area of the single-shot crystallization could be enlarged to 100 cm^2 that is

equivalent to 6-inch diagonal, typical size of current smartphone displays. Or desirably, further development for the direct deposition technique as discussed in chapter 2 is expected to overcome this issue. In this case, two major developments, microscopically to control the nucleation process and macroscopically to deposit on large substrate, are expected as already discussed.

Regarding the second and third challenges, the origins are common and they are caused by the existence of defects, such grain boundary. As for the second one, the reason is considered that driving current requires some period to reach targeted data value when the current dynamically changed because there is some finite time for carriers to be trapped or released at defects in poly-Si film. When displayed image was changed to be fully gray just after white/black image like a chessboard, a border between areas previously white and black is visible because there remains a difference in between target and transient currents. The polarity in transient currents after white and after black is opposite from each other. As for the third one, the leakage-current is caused through trap states in the band-gap that is inevitable for polycrystalline films as described in section 4.1. Thus, it is effective to avoid grain-boundary in poly-Si films for both the second and third challenges. The attempts for grain-boundary filtration discussed in section 3.1 and for quasi-single grain TFTs demonstrated in section 4.5 are promising to overcome those challenges.

Besides for applying to those advanced OLED displays discussed above, the poly-Si TFTs have been expected to use for micro-LED displays recently. The micro-LED as an emission device have two major characteristics paid attention to. The one is that the current density that gives peak of quantum efficiency is typically much higher than that of OLED [242)243)]. The other is that wavelength of emission light varies depending on the driving current [244)]. It is a fatal issue to be applied to displays because the color changes within the range of grayscales. It means that analog modulation method conventionally used in LCDs and OLEDs is not suitable for the micro-LED displays. The simple ways to avoid it is to employ pulse width modulation [245)]. The driving current is kept constant and the grayscale is controlled by the pulse width. In order to achieve it, the TFT technologies are required much higher operation current, i.e. higher carrier mobility, than that provided by current poly-Si TFTs. One of the most promising solution would be the grain-boundary free crystalline films and quasi-single grain TFTs discussed in section 3.1 and 4.5, respectively. The results obtained in this study would play an important role to develop future displays, such advanced OLEDs and micro-LEDs, and also the large-area microelectronics devices in the future.

Supplement I: Historic position for this series of study

Table S-1. Typical topics for TFTs

1960 | 1970 | 1980 | 1990 | 2000

Section	Year	Reference	Topic
Thin-film transistors	1962	Weimer 53)	CdS TFT
Thin-film transistors	1973	Brody 7)	AM-LCD (CdS)
Thin-film transistors	1979	LeComber 31)	a-Si:H TFT
gas phase	1982	Matsui 10)	MBD
gas phase	1983	Malhi 161)	LPCVD
gas phase	1992	Nagahara 127)	SiH4/SiF4
gas phase	2003	Hanna 128)	Si2H6/GeF4
solid phase	1986	Noguchi 95)	Si+I/I
solid phase	1989	Panwar 88)	SPC
solid phase	1993	Liu 133)	Pd induced
liquid phase	1966	Fa 58)	poly-Si FET
liquid phase	1974	Laff 55)	Ar laser TFT
liquid phase	1979	Lee 59)	Ar laser FET
liquid phase	1982	Morin 57)	Q Ruby p-Si TFT
liquid phase	1986	Sameshima 91)	LTPS (ELA)
liquid phase		Chapter 4	
Topics for display products	1984	Suwa Seikosya 8)	2" HTPS product
Topics for display products	1988	Sharp 12)	14" a-Si TFT product
Topics for display products	1996	Sanyo/Sony 33)	2.5" LTPS-LCD
Topics for display products	2003	Sanyo/Kodak 40)	2.61" LTPS-OLED
Topics for Si-MOSFETs	1960	Kahng 2)	MOS tr.
Topics for Si-MOSFETs	1965	Moore 5)	Moore's law
Topics for Si-MOSFETs	1970	Intel 51)	1k DRAM
Topics for Si-MOSFETs	1985	Toshiba 52)	1M DRAM

Table S-2. Typical topics for thin-film crystalline growth techniques

1970 | 1980 | 1990 | 2000

Crystalline growth technologies

Phase	Year	Reference	Topic
gas phase	1975	Nagashima 84)	APCVD
gas phase	1978	Kamins 85)	LPCVD
gas phase	1982	Matsui 10)	MBD
gas phase	1984	Hayashi 247)	LPCVD
gas phase	1986	Morozumi 33)	LPCVD
gas phase	1975	Spear 42)	a-Si:H
gas phase	1979	Morin 70)	PECVD
gas phase	1982	Kamins 86)	PECVD
gas phase	1987	Beart 113)	PCVD epi
gas phase		Chapter 2	
gas phase	1992	Nagahara 127)	poly-Si TFT
gas phase	2003	Hanna 128)	poly-Si TFT
solid phase	1976	Csepregi 92)	I/I disorder
solid phase	1977	Roth 93)	a-Si SPE
solid phase	1982	Ohmura 94)	L-SPE a-Si
solid phase	1983	Ishiwara 246)	L-SPE
solid phase	1986	Noguchi 95)	Si+I/I
solid phase	1988	Hatalis 87)	SPC a-Si
solid phase		Section 3.1	
solid phase	1972	Caywood 96)	SPE w metal(Ge)
solid phase	1973	Sankur 97)	SPE w metal(Si)
solid phase	1995	Lee 98)	Pd
solid phase	1996	Lee 99)	Ni
solid phase	1996	Yang 100)	SNSPE(Ge)
liquid phase	1978	Gat 104)	Cw-laser
liquid phase	1979	Geis 90)	graphoepitaxy
liquid phase	1982	Atwater 107)	Orientation selection
liquid phase	1974	Laff 55)	Ar
liquid phase	1975	Fan 103)	YAG
liquid phase	1978	Young 105)	Q Ruby
liquid phase	1982	Morin 57)	Q Ruby p-Si TFT
liquid phase		Section 3.2	
liquid phase	1982	Young 106)	Excimer
liquid phase	1986	Sameshima 91)	LTPS (ELA)
liquid phase	1989	Sera 108)	LTPS (ELA)

Supplement II: Growth history for flat-panel displays industry

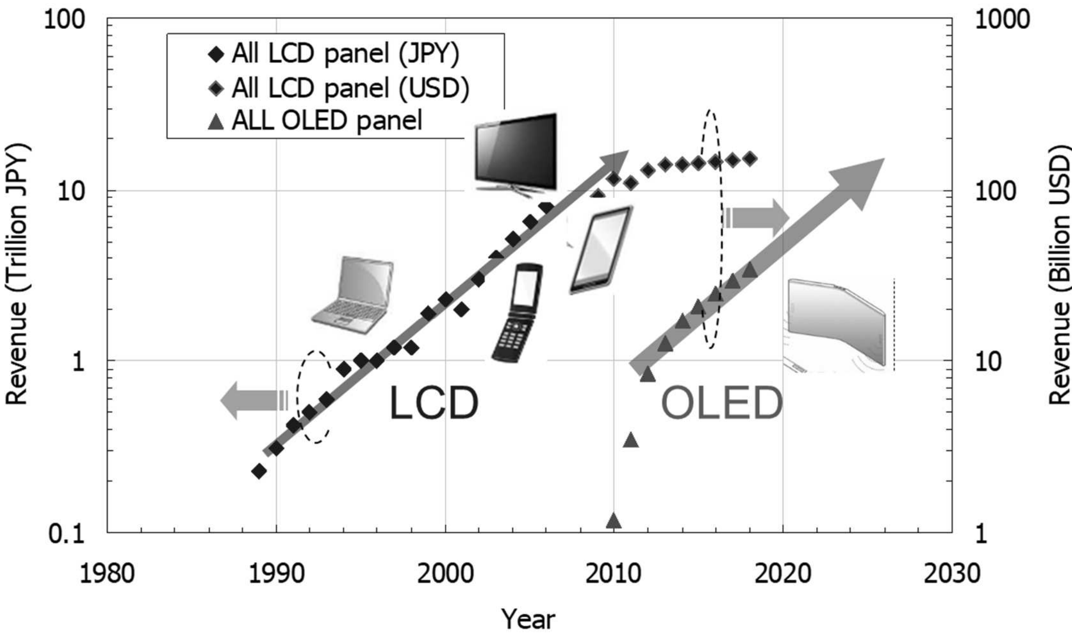


Figure S-3 Trends for revenues of LCD and OLED
The author created the figure based on a literature[248)] and some statistical data.

Supplement III: Position of poly-Si TFTs in the display industry

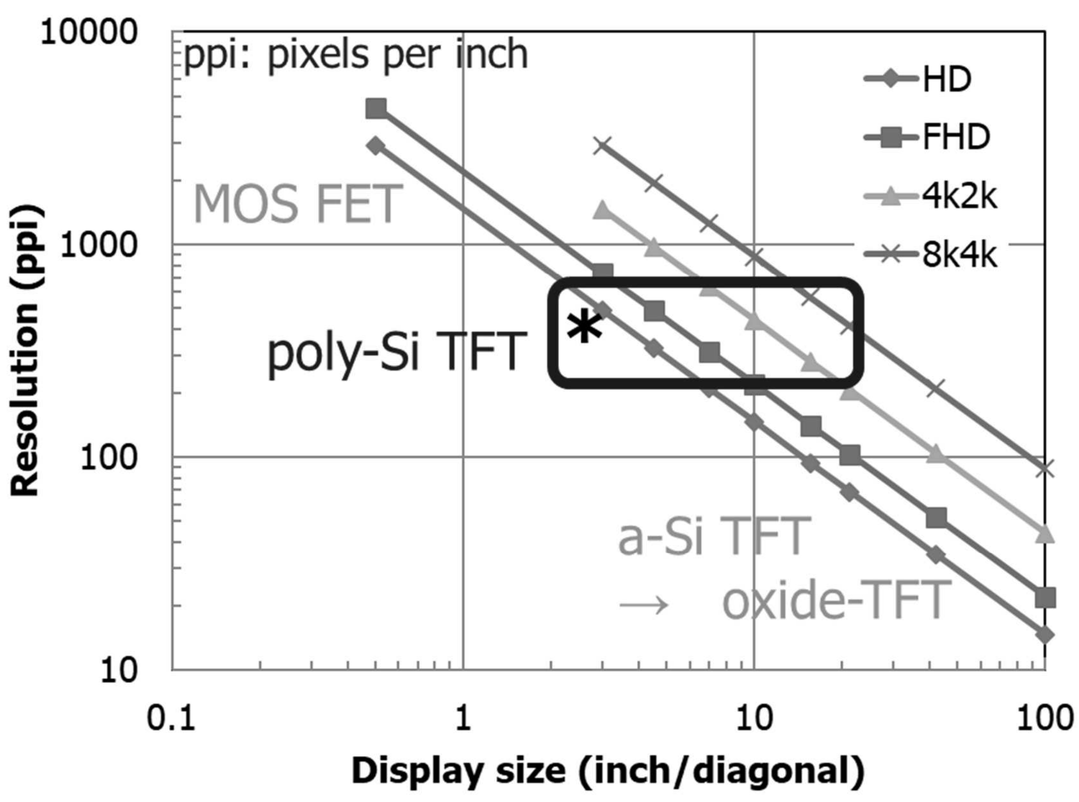


Figure S-4 Area in resolution and size that poly-Si TFT excels
*: 413 ppi/2.7 inch

NEC LCD Technologies Announces New 2.7-inch LCD Module Boasting an Exceptionally High Pixel Density

For immediate use April 21, 2008
NEC LCD Technologies, Ltd.

TOKYO, SANTA CLARA, Calif., U.S.A., DUESSELDORF, Germany, April 21, 2008 --- NEC LCD Technologies, together with its sales and marketing channels in the Americas and Europe, NEC Electronics America Inc., and NEC Electronics (Europe) GmbH, today announced that it will begin shipping samples of its new low-temperature polysilicon (LTPS) thin-film-transistor (TFT) liquid crystal display (LCD) module, part number NL9654HL06-01J, at the end of July 2008. The new LCD module boasts an exceptionally high pixel density of 413 pixels per inch in a small-size direct view LCD.

The new module supports quarter high-definition (QHD) resolution of 960 x 540 pixels, which is compatible with full high-definition (HD) resolution, has a compact size of 2.7 inches (6.8 centimeters diagonal), and achieves both a wide color gamut of 70 percent (NTSC ratio) and high luminance of 300 candelas per square meter (cd/m2). When incorporated in the viewfinder of a video camcorder for professional broadcast use, the new module enables highly accurate adjustment of focus. In addition, the module can be used to check colors through the viewfinder, without the need for external monitors.

2.7-inch TFT LCD Module
[NL9654HL06-01J]

Figure S-5 An example for product.[204)]

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References

1) J. Bardeen and W. H. Brattain, "The Transistor, A Semi-Conductor Triode," Phys. Rev. 74, p. 230, (1948), DOI: https://doi.org/10.1103/PhysRev.74.230
2) D. Kahng, "A historical perspective on the development of MOS transistors and related devices," in IEEE Transactions on Electron Devices, vol. 23, no. 7, pp. 655-657, (1976), DOI: 10.1109/T-ED.1976.18468.
3) R. N. Noyce, "Semiconductor device-and-lead structure," US Patent, No. 2981877, (1961)
4) J. S. Kilby, "Miniaturized electronic circuits," US Patent, No. 3138743, (1964)
5) G. E. Moore, "Cramming more components onto integrated circuits," Electronics, volume 38, number 8, p.114, (1965)
6) Scott E. Thompson and Srivatsan Parthasarathy, "Moore's law: the future of Si microelectronics," Materials Today, Volume 9, Issue 6, p.20-25, (2006), DOI: https://doi.org/10.1016/S1369-7021(06)71539-5
7) T. P. Brody, J. A. Asars and G. D. Dixon, "A 6 × 6 inch 20 lines-per-inch liquid-crystal display panel," IEEE Transactions on Electron Devices, vol. 20, no. 11, pp. 995-1001, (1973), doi: 10.1109/T-ED.1973.17780.
8) S. Morozumi, K. Oguchi, S. Yazawa, T. Kodaira, H.Ohshima and T. Mano : "B/W and Color LC Video Displays Addressed by Poly-Si TFTs", SID Digest, pp. 156-157 (1983)
9) T. Nishimura, Y. Akasaka, H. Nakata, "Characteristics of TFT fabricated in laser-recrystallizedpoly-Silicon for active LC display," Digest of Society for Information Display International Symposium, pp. 36-37, (1982)
10) M. Matsui, J. Owada, Y. Shiraki, E. Maruyama, H. Kawakami, "A 10X10 Polycrystalline-Silicon Thin-Film Transistor Matrix for Liquid-Crystal Display," Conference on Solid State Devices, pp. 141-142, (1982), DOI: https://doi.org/10.7567/SSDM.1982.C-4-4
11) S. Hotta, S. Nagata, Y. Miyata, K. Yokoyama, K. Adachi, T. Chikamura, M. Yoshiyama, A. Nishkawa, and K. Kawasaki, "Full-Color Multi-Gap LC-TV Display Panel Addressed by a-Si TFTs," SID Digest, pp. 296–297, (1986)
12) T. Nagayasu, T. Oketani, T. Hirobe, H. Kato, S. Mizushima, H. Take, K. Yano, M. Hijikigawa, and I. Washizuka, "A 14-in.-diagonal full-color a-Si TFT LCD," the 1988 International Display Research Conference, pp. 56-58, (1988), doi: 10.1109/DISPL.1988.11274.
13) F. Okumura, K. Sera, H. Asada, S. Kaneko, H. Ichinose, S. Naemura, K. Tanaka, T.

Yokoi, C. Tani, "Ferroelectric liquid-crystal shutter array with poly-Si TFT driver," the 1988 International Display Research Conference, pp. 174-177, (1988), doi: 10.1109/DISPL.1988.11304.

14) P. Weimer, G. Sadasiv, H. Borkan, L. Meray-Horvath, J. Meyer and F. Shallcross, "A thin-film solid-state image sensor," 1966 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, pp. 122-123, (1966), DOI: 10.1109/ISSCC.1966.1157701.
15) Hiroshi Hayama, Yasuo Nara, Kohichiro Ishibashi, Masakiyo Matsumura, "A Proposed Novel Amorphous-Silicon Image Sensor," Conference on Solid State Devices, pp. 99-100, (1980), DOI: https://doi.org/10.7567/SSDM.1980.B-4-8
16) Y. Kanoh, S. Usui, A. Sawada and M. Kikuchi, "A contact-type linear sensor with a GD a-Si:H photodetector array," 1981 International Electron Devices Meeting, pp. 313-316, (1981), DOI: 10.1109/IEDM.1981.190074.
17) T. Hamano, H. Ito, T. Nakamura, T. Ozawa, M. Fuse, M. Takenouchi , "An Amorphous Si High Speed Linear Image Sensor," Conference on Solid State Devices, pp. 41-42, (1981), DOI: https://doi.org/10.7567/SSDM.1981.B-2-1
18) S. Kaneko, M. Sakamoto, F. Okumura, T. Itano, H. Kataniwa, Y. Kajiwara, M. Kanamori, M. Yasumoto, T. Saito, T. Ohkubo, "Amorphous Si:H contact linear image sensor with Si3N4blocking layer," 1982 International Electron Devices Meeting, pp. 328-331, (1982), DOI: 10.1109/IEDM.1982.190286
19) Toshiaki Kagawa, Nobuo Matsumoto and Kenji Kumabe, "Amorphous Silicon Photoconductive Sensor," Jpn. J. Appl. Phys., Vol. 21, Supplement 21-1, pp. 251-256, (1982)
20) K. Ozawa, N. Takagi, K. Hiranaka, S. Yanagisawa, K. Asama, "Contact-Type Linear Sensor Using Amorphous Si Diode Array," Conference on Solid State Devices, pp. 125-126, (1982), DOI: https://doi.org/10.7567/SSDM.1982.C-3-2
21) H. Yamamoto, T. Baji, H. Matsumaru, Y. Tanaka, K. Seki, T. Tanaka, A. Sasano, T. Tsukada, "High Speed Contact Type Linear Sensor Array Using a-Si pin Diodes," Extended abstracts of the 15th Conference on Solid State Devices and Materials, pp. 205-208, (1983), DOI: https://doi.org/10.7567/SSDM.1983.B-4-7
22) A. Sasano, H. Yamamoto, K. Seki, Y. Tanaka, T. Baji, T. Tanaka, H. Matsumaru, T. Tsukada, "Semitransparent Metal-Si Electrodes for a-Si:H Photodiodes and Their Application to a Contact-Type Linear Sensor Array," Extended abstracts of the 16th International Conference on Solid State Devices and Materials, pp. 555-558, (1984), DOI: https://doi.org/10.7567/SSDM.1984.B-12-3
23) M. Sakamoto, F. Okumura, Y. Kajiwara, H. Uchida and S. Kaneko, "High Speed

and High Resolution ISO A4 Size Amorphous Si:H Contact Linear Image Sensor," in IEEE Transactions on Components, Hybrids, and Manufacturing Technology, vol. 7, no. 4, pp. 429-433, (1984), DOI: 10.1109/TCHMT.1984.1136372.

24) S. Morozumi, H. Kurihara, T. Takeshita, H. Oka and K. Hasegawa, "Completely integrated contact-type linear image sensor," in IEEE Transactions on Electron Devices, vol. 32, no. 8, pp. 1546-1550, (1985), DOI: 10.1109/T-ED.1985.22162.
25) Josef C. Lapp, "AMLCD Substrates Trends in Technology," Corning Technical Information Paper, TIP 102, (2004)
26) Karl Ferdinand Braun "Electrical Oscillations and Wireless Telegraphy" – Nobel Lecture, (1909), https://www.nobelprize.org/prizes/physics/1909/braun/lecture/
27) Friedrich Reinitzer, "Beiträge zur Kenntniss des Cholesterins," Monatshefte für Chemie 9, pp. 421–441, (1888), DOI: https://doi.org/10.1007/BF01516710
28) G. H. Heilmeier, L. A. Zanoni and L. A. Barton, "Dynamic scattering: A new electrooptic effect in certain classes of nematic liquid crystals," in Proceedings of the IEEE, vol. 56, no. 7, pp. 1162-1171, (1968), DOI: 10.1109/PROC.1968.6513.
29) M. Schadt and W. Helfrich, "Voltage-dependent optical activity of a twisted nematic liquid crystal," Appl. Phys. Lett. 18, p. 127 (1971), DOI: https://doi.org/10.1063/1.1653593
30) P. G. Le Comber, W. E. Spear and A. Ghaith, "Amorphous-silicon field-effect device and possible application," in Electronics Letters, vol. 15, pp. 179-181, (1979), DOI: 10.1049/el:19790126.
31) R. Kiefer, B. Weber, F. Windscheid, G. Baur, "In-plane switching of nematic liquid crystals," Proceedings of the 12th International Display Research Conference (Japan Display'92), pp. 547-550, (1992)
32) S. Morozumi, R. Araki, H. Ohshima, M. Matsuo, T. Nakazawa, and T. Satoh, "Low-temperature processed poly-Si TFT and its application to large area LCD," Proceedings of the 6th International Display Research Conference (Japan Display '86), pp. 196-199, (1986)
33) Kiyoshi Yoneda, "Recent Progress of Low Temperature Poly Si TFT Technology," Mat. Res. Soc. Symp. Proc., vol. 508, pp. 47-52, (1998)
34) André Bernanose, Marcel Comte et Paul Vouaux, "Sur un nouveau mode d'émission lumineuse chez certains composés organiques," J. Chim. Phys., Vol. 50, pp. 64–68, (1953)
35) M. Pope, H. P. Kallmann, and P. Magnante, "Electroluminescence in Organic Crystals," J. Chem. Phys. 38, pp. 2042 (1963), DOI: https://doi.org/10.1063/1.1733929

36) C. W. Tang and S. A. VanSlyke, “Organic electroluminescent diodes,” Appl. Phys. Lett. 51, pp. 913-915, (1987), DOI: https://doi.org/10.1063/1.98799
37) Takahiro Nakayama, Yuzo Itoh, and Atsushi Kakuta, “Organic photo - and electroluminescent devices with double mirrors,” Appl. Phys. Lett. 63, pp. 594-595, (1993), DOI: https://doi.org/10.1063/1.109959
38) J. C. Scott, S. Karg, S. A. Carter, “Bipolar charge and current distributions in organic light-emitting diodes,” Journal of Applied Physics Vol. 82, pp. 1454 (1997); https://doi.org/10.1063/1.365923
39) M. A. Baldo, D. F. O'Brien, Y. You, A. Shoustikov, S. Sibley, M. E. Thompson, S. R. Forrest, “Highly efficient phosphorescent emission from organic electroluminescent devices,” Nature 395, pp. 151–154, (1998), DOI: https://doi.org/10.1038/25954
40) P. Destruel, J. Farenc, P. Jolinat, I. Seguy, S. Archambeau, M. Mabiala, G. Ablart, “OLEDs a new technology for lighting and displays,” Proceedings of the 10th International Symposium on the Science and Technology of Light Sources (Light Source 2004), pp. 135 – 141, (2004)
41) R. C. Chittick, J. H. Alexander and H. F. Sterling, “The Preparation and Properties of Amorphous Silicon,” Journal of The Electrochemical Society, vol. 116, pp. 77 (1969), DOI: https://doi.org/10.1149/1.2411779
42) W. E. Spear, P. G. LeComber, “Substitutional doping of amorphous silicon,” Solid State Communications, vol. 17, pp. 1193 - 1196, (1975), DOI: https://doi.org/10.1016/0038-1098(75)90284-7
43) W. E. Spear, P. G. Le Comber, S. Kinmond, and M. H. Brodsky, “Amorphous silicon p -n junction,” Appl. Phys. Lett. vol. 28, pp. 105 - 107 (1976); DOI: https://doi.org/10.1063/1.88658
44) D. E. Carlson, and C. R. Wronski, “Amorphous silicon solar cell,” Appl. Phys. Lett. vol. 28, pp. 671 – 673, (1976), DOI: https://doi.org/10.1063/1.88617
45) R. A. Street, S. Nelson, L. Antonuk, V. Perez Mendez, “Amorphous Silicon Sensor Arrays for Radiation Imaging,” MRS Proceedings, vol. 192, pp. 441, (1990), DOI:10.1557/PROC-192-441
46) X. D. Wu, R. A. Street, R. Weisfield, S. Ready and S. Nelson, "Page sized a-Si:H 2-dimensional array as imaging devices," Proceedings of 4th International Conference on Solid-State and IC Technology, pp. 724-726, (1995), DOI: 10.1109/ICSICT.1995.503540.
47) L. E. Antonuk, J. Yorkston, W. Huang, J. H. Siewerdsen, J. M. Boudry, Y. el-Mohri, and M. V. Marx, “A real-time, flat-panel, amorphous silicon, digital x-ray imager,”

RadioGraphics, pp. 993-1000, (1995), DOI: https://doi.org/10.1148/radiographics.15.4.7569143
48) Nader Safavian, M. Yazdandoost, D. Wu, A. Sultana, M. H. Izadi, K. S. Karim, A. Nathan, J. A. Rowlands, "Characterization of current programmed amorphous silicon active pixel sensor readout circuit for dual mode diagnostic digital x-ray imaging," Proc. SPIE 7258, Medical Imaging 2009: Physics of Medical Imaging, 725815 (2009), DOI: https://doi.org/10.1117/12.813886
49) M. J. Grimes, A. C. Grimm and J. F. Wilhelm, "Improvements in the RCA Three-Beam Shadow-Mask Color Kinescope," in Proceedings of the IRE, vol. 42, pp. 315-326, (1954), DOI: 10.1109/JRPROC.1954.274643.
50) A. Rose, P. K. Weimer and H. B. Law, "The Image Orthicon-A Sensitive Television Pickup Tube," in Proceedings of the IRE, vol. 34, pp. 424-432, (1946), DOI: 10.1109/JRPROC.1946.225966.
51) WWW article by Intel Museum, https://www.intel.co.jp/content/www/jp/ja/company-overview/intel-museum.html
52) WWW article (in Japanese) by Toshiba Science Museum, https://toshiba-mirai-kagakukan.jp/learn/history/ichigoki/1985dram/index_j.htm
53) P. K. Weimer, "The TFT A New Thin-Film Transistor," in Proceedings of the IRE, vol. 50, pp. 1462-1469, (1962), DOI: 10.1109/JRPROC.1962.288190.
54) D. E. Carlson and C. R. Wronski, “Amorphous silicon solar cell,” Appl. Phys. Lett., vol. 28, pp. 671-673, (1976), DOI: https://doi.org/10.1063/1.88617
55) R. A. Laff and G. L. Hutchins, "V-1 laser fabrication of large-area arrays: Thin-film silicon isolated devices on fused Silica substrates," in IEEE Transactions on Electron Devices, vol. 21, pp. 743-743, (1974), DOI: 10.1109/T-ED.1974.18037.
56) M. Matsui, Y. Shiraki, Y. Katayama, K. L. I. Kobayashi, A. Shintani, and E. Maruyama, “Polycrystalline-silicon thin-film transistors on glass,” Appl. Phys. Lett. vol. 37, pp. 936-937, (1980), DOI: https://doi.org/10.1063/1.91766
57) F. Morin, P. Coissard, M. Morel, E. Ligeon and A. Bontemps, “Polysilicon transistors on glass by pulsed-laser annealing,” J. of Appl. Phys., vol. 53, 3897-3899, (1982), DOI: https://doi.org/10.1063/1.331094
58) C. H. Fa and T. T. Jew, "The poly-Silicon insulated-gate field-effect transistor," in IEEE Transactions on Electron Devices, vol. ED-13, pp. 290-291, (1966), DOI: 10.1109/T-ED.1966.15682.
59) K. F. Lee, J. F. Gibbons, K. C. Saraswat, T. I. Kamins, “Thin film MOSFET’s fabricated in laser-annealed polycrystalline silicon,” Appl. Phys. Lett. 35, pp. 173-174, (1979), DOI: https://doi.org/10.1063/1.91025

60) M. E. Roulet and P. Schwob, K. Affolter, W. Lüthy, M. von Allmen, M. Fallavier, J. M. Mackowski, M. A. Nicolet, and J. P. Thomas, “Laser annealing of silicon on sapphire,” Journal of Applied Physics vol. 50, pp. 5536-5538, (1979), DOI: https://doi.org/10.1063/1.326616
61) T. I. Kamins and P. A. Pianetta, "MOSFETs in laser-recrystallized poly-Silicon on quartz," in IEEE Electron Device Letters, vol. 1, pp. 214-216, (1980) DOI: 10.1109/EDL.1980.25293.
62) Hiroshi Ishiwara, Hiroshi Yamamoto, Seijiro Furukawa, Masao Tamura and Takashi Tokuyama, “Lateral solid phase epitaxy of amorphous Si films on Si substrates with SiO_2 patterns,” Appl. Phys. Lett. vol. 43, pp. 1028-1030, (1983), DOI: https://doi.org/10.1063/1.94217
63) C. -. Chen, H. W. Lam, S. D. S. Malhi and R. F. Pinizzotto, "Stacked CMOS SRAM cell," in IEEE Electron Device Letters, vol. 4, pp. 272-274, (1983), DOI: 10.1109/EDL.1983.25730.
64) John Y. W. Seto, “The electrical properties of polycrystalline silicon films,” Journal of Applied Physics, vol. 46, pp. 5247-5254, (1975), DOI: https://doi.org/10.1063/1.321593
65) J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, and M. Rider, “Conductivity behavior in polycrystalline semiconductor thin film transistors,” Journal of Applied Physics, vol. 53, pp. 1193-1202, (1982), DOI: https://doi.org/10.1063/1.330583
66) R. E. Proano, R. S. Misage and D. G. Ast, "Development and electrical properties of undoped polycrystalline silicon thin-film transistors," in IEEE Transactions on Electron Devices, vol. 36, pp. 1915-1922, (1989), DOI: 10.1109/16.34270.
67) D. R. Campbell, “Enhanced conductivity in plasma hydrogenated polysilicon films,” Appl. Phys. Lett. vol. 36, 604-606, (1980), DOI: https://doi.org/10.1063/1.91563
68) S. D. S. Malhi, R.R. Shah, H. Shichijo, R.F. Pinizzotto, C.E. Chen, P.K. Chatterjee, H.W. Lam, "Effects of grain boundary passivation on the characteristics of p-channel MOSFETs in LPCVD poly-Silicon," in Electronics Letters, vol. 19, pp. 993-994, (1983), DOI: 10.1049/el:19830674.
69) G. P. Pollack, W.F. Richardson, S.D.S. Malhi, T. Bonifield, H. Shichijo, S. Banerjee, M. Elahy, A.H. Shah, R. Womack, P. K. Chatterjee, "Hydrogen passivation of poly-Silicon MOSFET's from a plasma Nitride source," in IEEE Electron Device Letters, vol. 5, pp. 468-470, (1984), DOI: 10.1109/EDL.1984.25991.

70) F. Morin, and M. Morel, “Polycrystalline silicon by glow discharge technique,” Appl. Phys. Lett., vol. 35, 686-688, (1979), DOI:https://doi.org/10.1063/1.91254
71) Akihisa Matsuda, Satoshi Yamasaki, Katsumi Nakagawa, Hideyo Okushi, Kazunobu Tanaka, Sigeru Iizima, Mitsuo Matsumura1 and Hideo Yamamoto, “Electrical and Structural Properties of Phosphorous-Doped Glow-Discharge Si:F:H and Si:H Films,” Jpn. J. Appl. Phys., vol. 19, pp. L305-L308, (1980), DOI: https://doi.org/10.1143/JJAP.19.L305
72) John W. Bowron, Terry C. Schmidt, "New high-resolution reflective liquid crystal light valve projector: Electrohome DLV 1280," Proc. SPIE 3296, Projection Displays IV, (17 April 1998); https://doi.org/10.1117/12.305519
73) E. G. Colgan, F. Doany, M. Lu, A. Rosenbluth, K.-H. Yang, M. Uda, M. Shinohara, T. Tomooka, T. Tsukamoto, “Optimization of light-valve mirrors,” Journal of the Society for Information Display, Vol. 6, pp. 247-251, (1998)
74) G. W. Jones, “Active Matrix OLED Microdisplay,” Society for Information Display 2001, Digest of Technical Papers, vol. 32, pp.134-137, (2001), DOI: https://doi.org/10.1889/1.1831812
75) N. Okamoto, Y. Itoh, J. Ito, “High Brightness and High Resolution Technology of p-Si TFT-LCD Front Projectors, Proceedings of the 4th International Display Workshop (IDW), pp. 813-816, (1997)
76) Katsuhide Uchino, Tomohiro Kashima, Fumiaki Abe, Masumi Hirano, Masahiko Satoh, Toshikazu Maekawa, “Ultra-High Brightness 1.8-in. XGA poly-Si TFT LCD,” Society for Information Display 1998 International Symposium, Digest of Technical Papers, vol. 29, pp.1067-1068, (1998), DOI: https://doi.org/10.1889/1.1833670
77) M. Hosokawa, K. Oguchi, M. Ikeda, S. Yazawa, K. Endo, “Dichroic Guest-Host Active Matrix Video Display,” Society for Information Display 1981 International Symposium, Digest of Technical Papers, vo. 12, pp. 114-115, (1981)
78) F. C. Luo, J. Patterson, T. Braunstein, and D. Leksell, “A 640×480 CdSe TFT-LC Display Panel,” Society for Information Display 1985 International Symposium, Digest of Technical Papers, vol.16, p. 286-288, (1985)
79) R. M. A. Dawson, Z. Shen, D. A. Furst, S. Connor, J. Hsu, M. G. Kane, R. G. Stewart, A. Ipri, C. N. King, P. J. Green, R. T. Flegal, S. Pearson, W. A. Barrow, E. Dickey, K. Ping, C. W. Tang, S. Van Slyke, F. Chen, J. Shi, J. C. Sturm and M. H. Lu: “Design of an Improved Pixel for a Polysilicon Active-Matrix Organic LED Display”, Society for Information Display 1998 International Symposium, Digest of Technical Papers, vol.29, pp. 11-14, (1998)

80) Y. Oana : “A 240×360 Element Active Matrix LCD with Integrated Gate-Bus Drivers Using Poly-Si TFTs”, Society for Information Display 1984 International Symposium, Digest of Technical Papers, vol.15, pp. 312-315, (1984)
81) https://www.ave.nikon.co.jp/fpd/lineup/index.htm; the drawing based on the information of Nikon in the WWW, (2020).
82) Koichi Miyachi, Kazuki Kobayashi, Yuichiro Yamada, Shigeaki Mizushima, “The World's First Photo Alignment LCD Technology Applied to Generation Ten Factory,” Society for Information Display 2010 International Symposium, Digest of Technical Papers, vol. 41, pp.579-582, (2010), DOI: https://doi.org/10.1889/1.3500533
83) H. Ohshima, “Past, Present and Future of Mobile Displays,” The proceedings of the 20th International Workshop on Flatpanel Displays and Devices, pp. 13-16, (2013) .
84) Naoyuki Nagasima and Nagiko Kubota, “Structures of Si Films Chemically Vapor-Deposited on Amorphous SiO_2 Substrates,” Jpn. J. Appl. Phys., vol. 14, pp. 1105-1112, (1975), DOI: https://doi.org/10.1143/JJAP.14.1105
85) T. I. Kamins, M. M. Mandurah and K. C. Saraswat, “Structure and Stability of Low Pressure Chemically Vapor-Deposited Silicon Films,” J. Electrochem. Soc., vol. 125, pp. 927, (1978), DOI: https://doi.org/10.1149/1.2131593
86) T. I. Kamins and K. L. Chiang, “Properties of Plasma-Enhanced CVD Silicon Films: I : Undoped Films Deposited from 525 to 725 C,” J. Electrochem. Soc. vo. 129, pp. 2326- (1982), DOI: https://doi.org/10.1149/1.2123504
87) Miltiadis K. Hatalis and David W. Greve, “Large grain polycrystalline silicon by low-temperature annealing of low-pressure chemical vapor deposited amorphous silicon films,” Journal of Applied Physics, vol. 63, pp. 2260-2266, (1988), DOI: https://doi.org/10.1063/1.341065
88) O.S. Panwar, R.A. Moore, N.S.J. Mitchell, H.S. Gamble, B.M. Armstrong, “Low-temperature crystallisation of amorphous-silicon films for the fabrication of thin-film transistors,” Applied Surface Science, vol. 36, pp. 247-256, (1989), DOI: https://doi.org/10.1016/0169-4332(89)90920-3
89) T. Aoyama, G. Kawachi, N. Konishi, T. Suzuki, Y. Okajima and K. Miyata, “Crystallization of LPCVD Silicon Films by Low Temperature Annealing,” J. Electrochem. Soc., vol. 136, pp. 1169-,(1989), DOI: https://doi.org/10.1149/1.2096829
90) M. W. Geis, D. C. Flanders, and Henry I. Smith, “Crystallographic orientation of silicon on an amorphous substrate using an artificial surface-relief grating and laser crystallization,” Applied Physics Letters, vol. 35, pp. 71-74, (1979), DOI:

https://doi.org/10.1063/1.90936

91) T. Sameshima, S. Usui and M. Sekiya, "XeCl Excimer laser annealing used in the fabrication of poly-Si TFT's," in IEEE Electron Device Letters, vol. 7, pp. 276-278, (1986), DOI: 10.1109/EDL.1986.26372.
92) L. Csepregi, E. F. Kennedy, S. S. Lau, J. W. Mayer, and T. W. Sigmon, “Disorder produced by high-dose implantation in Si,” Applied Physics Letters, vol. 29, pp. 645-648, (1976), DOI: https://doi.org/10.1063/1.88886
93) John A. Roth and C. Lawrence Anderson, “Silicon epitaxy by solid-phase crystallization of deposited amorphous films,” Applied Physics Letters, vol. 31, pp. 689-691, (1977), DOI: https://doi.org/10.1063/1.89506
94) Yamichi Ohmura, Yoshiaki Matsushita and Masahiro Kashiwagi, “Solid-Phase Lateral Epitaxial Growth onto Adjacent SiO_2 Film from Amorphous Silicon Deposited on Single-Crystal Silicon Substrate,” Jpn. J. Appl. Phys. , vol. 21, pp. L152-154, (1982), DOI: https://doi.org/10.1143/JJAP.21.L152
95) Takashi Noguchi, Hisao Hayashi and Takefumi Ohshima, “Low Temperature Polysilicon Super-Thin-Film Transistor (LSFT),” Jpn. J. Appl. Phys., vol. 25, pp. L121-122, (1986), DOI: https://doi.org/10.1143/JJAP.25.L121, An erratum, Jpn. J. Appl. Phys., vol. 26, pp. L153, (1987), DOI: https://doi.org/10.1143/JJAP.26.L153
96) J. M. Caywood, A. M. Fern, J. O. McCaldin, and G. Ottaviani, ”Solid-Phase Growth of Ge from Evaporated Al Layer,” Applied Physics Letters, vol. 20, pp. 326-327, (1972), DOI: https://doi.org/10.1063/1.1654170
97) H. Sankur, J.O. McCaldin and John Devaney, ”Solid-phase epitaxial growth of Si mesas from Al metallization,” Applied Physics Letters vol. 22, pp. 64-66, (1973), DOI: https://doi.org/10.1063/1.1654558
98) Seok-Woon Lee, Yoo-Chan Jeon, and Seung-Ki Joo, “Pd induced lateral crystallization of amorphous Si thin films,” Applied Physics Letters, vol. 66, pp. 1671-1673, (1995),DOI: https://doi.org/10.1063/1.113888
99) Seok-Woon Lee and Seung-Ki Joo, "Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization," in IEEE Electron Device Letters, vol. 17, pp. 160-162, (1996), DOI: 10.1109/55.485160.
100) C. M. Yang and Harry A. Atwater, “Selective solid phase crystallization for control of grain size and location in Ge thin films on silicon dioxide,” Appl. Phys. Lett., vol. 68, pp. 3392-3394, (1996), DOI: https://doi.org/10.1063/1.116514
101) Sorab K. Ghandhi, “Chapter 3, Crystal growth and doping,” *VLSI Fabrication Principles (2nd edition)*, pp. 102-149, (1994), John Wiley & Sons, Inc.
102) H. Fischer and W. Pschunder, "Low-cost solar cells based on large-area

unconventional silicon," in IEEE Transactions on Electron Devices, vol. 24, pp. 438-442, (1977), DOI: 10.1109/T-ED.1977.18753.
103) John C. C. Fan and H. J. Zeiger, "Crystallization of amorphous silicon films by Nd:YAG laser heating," Applied Physics Letters, vol. 27, pp. 224-226, (1975), DOI: https://doi.org/10.1063/1.88437
104) A. Gat, L. Gerzberg, J. F. Gibbons, T. J. Magee, J. Peng, and J. D. Hong, "cw laser anneal of polycrystalline silicon: Crystalline structure, electrical properties," Applied Physics Letters, vol. 33, pp. 775-778, (1978), DOI: https://doi.org/10.1063/1.90501
105) R. T. Young, C. W. White, G. J. Clark, J. Narayan, W. H. Christie, M. Murakami, P. W. King, and S. D. Kramer, "Laser annealing of boron-implanted silicon," Applied Physics Letters vol. 32, pp. 139-141, (1978), DOI: https://doi.org/10.1063/1.89959
106) R. T. Young, G.A. van der Leeden, J. Narayan, W.H. Christie, R.F. Wood, D.E. Rothe, and J.I. Levatteret, "Characterization of excimer laser annealing of ion implanted Si," in IEEE Electron Device Letters, vol. 3, pp. 280-283, (1982), DOI: 10.1109/EDL.1982.25569.
107) H. A. Atwater, Henry I. Smith and M. W. Geis, "Orientation selection by zone-melting silicon films through planar constrictions," Applied Physics Letters, vol. 41, pp. 747-749, (1982); https://doi.org/10.1063/1.93664
108) K. Sera, F. Okumura, H. Uchida, S. Itoh, S. Kaneko and K. Hotta, "High-performance TFTs fabricated by XeCl excimer laser annealing of hydrogenated amorphous-silicon film," in IEEE Transactions on Electron Devices, vol. 36, pp. 2868-2872, (1989), DOI: 10.1109/16.40970
109) Shoji Nishida, Tsunenori Shiimoto, Akira Yamada, Shiro Karasawa, Makoto Konagai, and Kiyoshi Takahashi, "Epitaxial growth of silicon by photochemical vapor deposition at a very low temperature of 200 °C," Applied Physics Letters, vol. 49, pp. 79-81, (1986), DOI: https://doi.org/10.1063/1.97626
110) Naoki Shibata, Kaichi Fukuda, Hirokazu Ohtoshi, Jun-ichi Hanna, Shunri Oda and Isamu Shimizu, "Preparation of Polycrystalline Silicon by Hydrogen-Radical-Enhanced Chemical Vapor Deposition," Jpn. J. Appl. Phys., vol. 26, pp. L10-13, (1987), DOI: https://doi.org/10.1143/JJAP.26.L10
111) Tsuyoshi Uematsu, Sunao Matsubara, Masao Kondo, Masao Tamura and Tadashi Saitoh,"Very-Low-Temperature Silicon Epitaxy by Plasma-CVD Using SiH_4-PH_3-H_2 Reactants for Bipolar Devices, " Jpn. J. Appl. Phys., vol. 27, pp. L493-495, (1988), DOI: https://doi.org/10.1143/JJAP.27.L493
112) Tadahiro Ohmi, Kiyohiko Matsudo, Tadashi Shibata, Takeshi Ichikawa and

Hiroshi Iwabuchi, "Very-Low-Temperature Epitaxial Silicon Growth By Low-Kinetic-Energy Particle Bombardment," Jpn. J. Appl. Phys. 27 L2146-2148, (1988), DOI: https://doi.org/10.1143/JJAP.27.L2146

113) K. Baert, J. Symons, W. Vandervorst, J. Vanhellemont, M. Caymax, J. Poortmans, J. Nijs, and R. Mertens, "Very low temperature (250 ℃) epitaxial growth of silicon by glow discharge of silane," Applied Physics Letters, vol. 51, pp. 1922-1924, (1987), DOI: https://doi.org/10.1063/1.98301

114) Shunri Oda, Shun'ichi Ishihara, Naoki Shibata, Hajime Shirai, Akihiro Miyauchi, Kaichi Fukuda, Akihito Tanabe, Hirokazu Ohtoshi, Jun'ichi Hanna and Isamu Shimizu, "The Role of Hydrogen Radicals in the Growth of a-Si and Related Alloys," Jpn. J. Appl. Phys., vol. 25, pp. L188-190, (1986), DOI: https://doi.org/10.1143/JJAP.25.L188

115) Naoki Shibata, Akihiro Miyauchi, Akihito Tanabe, Jun-ichi Hanna, Shunri Oda and Isamu Shimizu, "Hole Transport in a-Si:H(F) Prepared by Hydrogen-Radical-Assisted Chemical Vapor Deposition," Jpn. J. Appl. Phys., vol. 25, pp. 1783-1787, (1986), DOI: https://doi.org/10.1143/JJAP.25.1783

116) Naoki Shibata, Akihito Tanabe, Jun-ichi Hanna, Shunri Oda and Isamu Shimizu, "Preparation of Highly Photoconductive a-SiGex from Fluorides by Controlling Reactions with Atomic Hydrogen," Jpn. J. Appl. Phys., vol. 25, pp. L540-543, (1986), DOI: https://doi.org/10.1143/JJAP.25.L540

117) Hiroshi Tanabe, *Growth of Crystalline Si Thin Film at Low Substrate Temperature,* (in Japanese) Unpublished Master's Thesis, Department of Electronic Chemistry, Tokyo Institute of Technology, (1989)

118) W. Kern and D. A. Puotinen, "Cleaning solutions based on hydrogen peroxide for use in silicon semiconductor technology," RCA Rev. vol. 31, pp. 187-206, (1970)

119) P. J. Zanzucchi, "Chapter 4 The Vibrational Spectra of a-Si: H," *Semiconductors and Semimetals, vol. 21, Hydrogenated Amorphous Silicon, (ed. by Jacques I. Pankove) Part B*, Academic Press, pp. 113-140, (1984),

120) L. J. van der Pauw, "A method of measuring specific resistivity and Hall effect of discs of arbitrary shape," Philips Res. Rep., vol. 13, pp.1-9, (1958)

121) Dionisio Bermejo, Manuel Cardona, "Raman scattering in pure and hydrogenated amorphous germanium and silicon," Journal of Non-Crystalline Solids, vol. 32, pp. 405-419, (1979), DOI: https://doi.org/10.1016/0022-3093(79)90085-1.

122) Z. Iqbal and S. Veprek, "Raman scattering from hydrogenated microcrystalline and amorphous silicon," J. Phys. C: Solid State Phys., vol. 15, pp. 377-392, (1982), DOI: https://doi.org/10.1088/0022-3719/15/2/019

123) Robert C. Wheast, *Handbook of Chemistry and Physics 63rd Edition 1982-1983*, CRC Press, (1982)
124) Seishi Kikuchi, “Diffraction of Cathode Rays by Mica,” Proceedings of the Imperial Academy, vol. 4, pp. 271-274, (1928)
125) N. Shibata, K. Fukuda, H. Ohtoshi, J. Hanna, S. Oda, and I. Shimizu,”Growth of Amorphous and Crystalline Silicon by HR-CVD (Hydrogen Radical Enhanced CVD),” MRS Proceedings, vo. 95, pp. 225-230, (1987), DOI: 10.1557/PROC-95-225
126) H. Tanabe, M. Azuma, T. Uematsu, H. Shirai, J. Hanna, and I. Shimizu, “Growth of Crystalline Silicon, Microcrystalline and Epitaxial at Low Substrate Temperature,” MRS Proceedings, vol. 149, pp. 17-22, (1989), DOI: 10.1557/PROC-149-17
127) Tatsuro Nagahara, Kenji Fujimoto, Naoki Kohno, Yusaku Kashiwagi and Hisashi Kakinoki, “In-Situ Chemically Cleaning Poly-Si Growth at Low Temperature,” Jpn. J. Appl. Phys. vol. 31, pp. 4555-4558, (1992), DOI: https://doi.org/10.1143/JJAP.31.4555
128) Jun-ichi Hanna, JuanJin Zhang, Jeong-Woo Lee, Kousaku Shimizu, “Deposition of Poly-Si and SiGe Thin Films at 450 °C by Reactive Thermal CVD and their TFT Application,” Tech. Digest AM-LCD ’03, pp. 83-86, (2003),
129) Eiji Takahashi, Yasuaki Nishigami, Atsushi Tomyo, Masaki Fujiwara, Hirokazu Kaki, Kiyoshi Kubota, Tsukasa Hayashi, Kiyoshi Ogata, Akinori Ebe and Yuichi Setsuhara, “Large-Area and High-Speed Deposition of Microcrystalline Silicon Film by Inductive Coupled Plasma using Internal Low-Inductance Antenna,” Jpn. J. Appl. Phys., vol. 46, pp. 1280-1285, (2007), DOI: https://doi.org/10.1143/JJAP.46.1280
130) W. E. Jones, S. D. Macknight and L. Teng, “Kinetics of atomic hydrogen reactions in the gas phase,” Chemical Reviews, vo. 73, pp. 407-440, (1973)
131) S. S. Lau, W. F. van der Weg, “Solid phase epitaxy,” in *Thin films - interdiffusion and reactions*, edited by J. M. Poate, K. N. Tu, and J. W. Mayer, Wiley-Interscience, New York, chapter 12, pp. 433-480, (1978)
132) Gang Liu and S. J. Fonash, “Selective area crystallization of amorphous silicon films by low - temperature rapid thermal annealing,” Appl. Phys. Lett., vol. 55, pp. 660-662, (1989), DOI: https://doi.org/10.1063/1.101814
133) Gang Liu and Stephen J. Fonash, “Polycrystalline silicon thin film transistors on Corning 7059 glass substrates using short time, low-temperature processing,” Appl. Phys. Lett., vol. 62, pp. 2554-2556, (1993), DOI: https://doi.org/10.1063/1.109294

134) C. Chen, and H. Atwater, "Polycrystalline Si Films Fabricated by Low Temperature Selective Nucleation and Solid Phase Epitaxy Process," MRS Proceedings, vol. 485, pp. 67-72, (1997), DOI: 10.1557/PROC-485-67

135) R. C. Cammarata and C. V. Thompson, K. N. Tu, "NiSi2 precipitation in nickel-implanted silicon films," Appl. Phys. Lett., vol. 51, pp. 1106-1108, (1987), DOI: https://doi.org/10.1063/1.99003

136) C. Hayzelden, J. L. Batstone, R. C. Cammarata, "In situ transmission electron microscopy studies of silicide-mediated crystallization of amorphous silicon," Appl. Phys. Lett., vol. 60, pp. 225-227, (1992), DOI: https://doi.org/10.1063/1.106971

137) C. Hayzelden, J. L. Batstone, "Silicide formation and silicide-mediated crystallization of nickel-implanted amorphous silicon thin films," Journal of Applied Physics, vol. 73, pp. 8279, (1993), DOI: https://doi.org/10.1063/1.353446

138) Victor E. Borisenko, Peter J. Hesketh, "Diffusion Synthesis of Silicides in Thin-Film Metal-Silicon Structures," in *Rapid Thermal Processing of Semiconductors*, Springer Science+Business Media, New York, chapter 5, pp.149-191, (1997)

139) H. Jin Song and James S. Im, "Single-crystal Si islands on SiO_2 obtained via excimer-laser irradiation of a patterned Si film," Appl. Phys. Lett., vol. 68, pp. 3165-3167, (1996), DOI: https://doi.org/10.1063/1.115812

140) J. F. Ziegler, J. P. Biersack, and U. Littmark, *The Stopping and Range of Ions in Matter*, Pergamon, New York, (1985)

141) R. Puglisi, H. Tanabe, C. Chen, H. A. Atwater, E. Rimini, "Ni-Induced Selective Nucleation and Solid Phase Epitaxy of Large-Grained Poly-Si on Glass," MRS Proceedings, vol. 587, O8.1, (1999), DOI: 10.1557/PROC-587-O8.1

142) R. A. Puglisi, H. Tanabe, C. M. Chen, Harry A. Atwater, "Large-grained polycrystalline Si films obtained by selective nucleation and solid phase epitaxy," Materials Science and Engineering: B, vol. 73, pp. 212-217, (2000), DOI: https://doi.org/10.1016/S0921-5107(99)00466-3.

143) Yoshiharu Hirakata, Masayuki Sakakura, Shingo Eguchi, Yutaka Shionoiri, Shumpei Yamazaki, Hajime Washio, Yasushi Kubota, Naoki Makita, Masaya Hijikigawa, "4-in. VGA Reflection-Type Poly-Si TFT LCD with Integrated Digital Driver Using Seven-Mask CG Silicon CMOS Process," SID digest, pp. 1014-1017, (2000)

144) Hiromi Sakamoto, Naoki Makita, and Masaya Hijikigawa, Mitsuaki Osame, Yoshifumi Tanada, and Shumpei Yamazaki, "2.6 inch HDTV Panel Using CG Silicon," SID digest, pp. 1190-1193, (2000)

145) A. Ourmazd and W. Schröter, “Phosphorus gettering and intrinsic gettering of nickel in silicon,” Appl. Phys. Lett., vol. 45, pp. 781-783, (1984), DOI: https://doi.org/10.1063/1.95364
146) Toru Takayama, Hishashi Ohtani, Akiharu Miyanaga, Toru Mitsuki, Hideto Ohnuma, Setsuo Nakajima and Ssumpei Yamazaki, “Continuous Grain Silicon Technology and Its Applications for Active Matrix Display”, Tech. Digest. AM-LCD 2000, pp. 25-18, (2000)
147) J. Narayan, C. W. White, M. J. Aziz, B. Stritzker, and A. Walthuis, “Pulsed excimer (KrF) laser melting of amorphous and crystalline silicon layers,” J. Appl. Phys., vol. 57, pp. 564-567, (1985), DOI https://doi.org/10.1063/1.334738
148) Yasushi Morita and Takashi Noguchi, “UV Pulsed Laser Annealing of Si+ Implanted Silicon Film and Low-Temperature Super-Thin Film Transistors,” Jpn. J. Appl. Phys., vol. 28, pp. L309-311, (1989), DOI: https://doi.org/10.1143/JJAP.28.L309
149) F. Foulon, E. Fogarassy, A. Slaoui, C. Fuchs, S. Unamuno & P. Siffert, “Melting threshold of crystalline and amorphized Si irradiated with a pulsed ArF (193 nm) excimer laser,” Appl. Phys. A, vol. 45, pp. 361–364, (1988), DOI: https://doi.org/10.1007/BF00617943
150) T. Serikawa, S. Shirai, A. Okamoto and S. Suyama, "Low-temperature fabrication of high-mobility poly-Si TFTs for large-area LCDs,"IEEE Transactions on Electron Devices, vol. 36, pp. 1929-1933, (1989), DOI: 10.1109/16.34272.
151) Toshiyuki Sameshima, Masaki Hara and Setsuo Usui, “Measuring the Temperature of a Quartz Substrate during and after the Pulsed Laser-Induced Crystallization of a-Si:H,” Jpn. J. Appl. Phys., vol. 28, pp. L2131-2133, (1989), DOI: https://doi.org/10.1143/JJAP.28.L2131
152) Toshiyuki Sameshima, Masaki Hara and Setsuo Usui, “XeCl Excimer Laser Annealing Used to Fabricate Poly-Si TFT's,” Jpn. J. Appl. Phys., vol. 28, pp. 1789-1793, (1989), DOI: https://doi.org/10.1143/JJAP.28.1789
153) G. J. Galvin, M. O. Thompson, J. W. Mayer, R. B. Hammond, N. Paulter, and P. S. Peercy, “Measurement of the Velocity of the Crystal-Liquid Interface in Pulsed Laser Annealing of Si, “Phys. Rev. Lett., vol. 48, pp. 33-36, (1982), DOI: https://doi.org/10.1103/PhysRevLett.48.33
154) D. H. Lowndes, R. F. Wood, and J. Narayan, “Pulsed-Laser Melting of Amorphous Silicon: Time-Resolved Measurements and Model Calculations,” Phys. Rev. Lett. , vol. 52, pp. 561-564, (1984), DOI:https://doi.org/10.1103/PhysRevLett.52.561
155) G. E. Jellison, Jr., D. H. Lowndes, D. N. Mashburn, and R. F. Wood, “Time-resolved reflectivity measurements on silicon and germanium using a pulsed

excimer KrF laser heating beam," Phys. Rev. B, vol. 34, pp. 2407-2415, (1986), DOI: https://doi.org/10.1103/PhysRevB.34.2407

156) K. Winer, G. B. Anderson, S. E. Ready, R. Z. Bachrach, R. I. Johnson, F. A. Ponce, and J. B. Boyce, "Excimer-laser-induced crystallization of hydrogenated amorphous silicon," Appl. Phys. Lett., vol. 57, pp. 2222-2224, (1990), DOI: https://doi.org/10.1063/1.103897

157) Hiroshi Tanabe, Hiroshi Okumura, Katsuhisa Yuda, Kenji Sera and Fujio Okumura, "CAPPING LAYER EFFECT ON UNIFORMITY OF EXCIMER LASER CRYSTALLIZED Poly-Si THIN FILM TRANSISTORS," 1996 MRS Spring Meeting, Symposium G: Semiconductors on Insulators—Fundamentals and Technology, G3.5, (1996)

158) K. Sera, H. Tanabe, H. Okumura, K. Yuda, and F. Okumura, "Uniformity improvement of excimer laser crystallized poly-Si thin film transistors", International Workshop on Active-Matrix Liquid-Crystal Displays '96, Digest of Technical Papers, pp. 85-88, (1996)

159) T. Sameshima, M. Hara, N. Sano, S. Usui, "XeCl Excimer Laser-Induced Amorphization and Crystllization of Silicon Films," 1990 International Conference on Solid State Devices and Materials, pp.967-970, (1990), DOI: https://doi.org/10.7567/SSDM.1990.S-E-8

160) T. I. Kamins and P. J. Marcoux, "Hydrogenation of transistors fabricated in polycrystalline-silicon films," IEEE Electron Device Letters, vol. 1, pp. 159-161, (1980), DOI: 10.1109/EDL.1980.25272.

161) S. D. S. Malhi, R.R. Shah, H. Shichijo, R.F. Pinizzotto, C.E. Chen, P.K. Chatterjee, H.W. Lamet, "Effects of grain boundary passivation on the characteristics of p-channel MOSFETs in LPCVD polysilicon," Electronics Letters, vol. 19, pp. 993-994, (1983), DOI: 10.1049/el:19830674.

162) T. Aoyama, Y. Koike, Y. Okajima, N. Konishi, T. Suzuki and K. Miyata, "Effect of hydrogenation of the leakage currents of laser-annealed polysilicon TFTs," IEEE Transactions on Electron Devices, vol. 38, pp. 2058-2061, (1991) DOI: 10.1109/16.83729.

163) Hiroshi Okumura, Hiroshi Tanabe, Fujio Okumura, "TFT Characteristics with Microstructure for Excimer Laser Annealed Poly-Si Films", International Workshop on Active-Matrix Liquid-Crystal Displays 1995, Digest of Technical Papers, pp. 19-22, (1995)

164) Hiroshi Okumura, Hiroshi Tanabe, Fujio Okumura, "Effect of the Grain Growth Process on the Characteristics for the Excimer Laser Crystallized Poly-Si Thin Film

Transistors," MRS Proceedings, vol. 403, pp. 315-320, (1995), DOI: 10.1557/PROC-403-315

165) F. Secco d' Aragona, "Dislocation Etch for (100) Planes in Silicon," J. Electrochem. Soc., vol. 119, pp. 948-951, (1972), DOI: https://doi.org/10.1149/1.2404374

166) Hiroshi Tanabe, "Cooling Rate Simulations and Film Properties in Excimer Laser Crystallization of Silicon Thin Films", International Workshop on Active-Matrix Liquid-Crystal Displays (AM-LCD) 2000, Digest of Technical Papers, pp. 269-272, (2000)

167) Hiroshi Tanabe, "Effect of cooling late on excimer laser crystallization of silicon thin films", NEC Research and Development, Vol. 41, No. 2, pp. 202-206, (2000)

168) R.F. Wood, G.E. Jellison, *Semiconductors and Semimetals,* vol. 23, Edited by R.F. Wood, C.W. White, R.T. Young, Academic Press, Orlando, pp.189-193, (1984)

169) *Thermophysical Properties Handbook*, Yonendo, Tokyo, (1990), (in Japanese)

170) R. Tsu, R.T. Hodgson, T.Y. Tan, J.E. Baglin, "LASER-INDUCED ORDER-DISORDER TRANSITIONS IN SILICON BY PULSED UV LASER," in *Laser and Electron Beam Processing of Materials*, Edited by C.W. WHITE, P.S. PEERCY, Academic Press, pp. 149-155, (1980)

171) Hiroshi Tanabe, Kenji Sera, Ken-Ichi Nakamura, Kazumi Hirata, Katsuhisa Yuda, Fujio Okumura, "Excimer Laser Crystallization of Amorphous Silicon Films for Poly-Si TFT Fabrication," MRS Proceedings, vol. 321 (Symposium E – Crystallization and Related Phenomena in Amorphous Materials—Ceramics, Metals, Polymers, and Semiconductors), pp. 677-682, (1993), DOI: 10.1557/PROC-321-677

172) Hiroshi Tanabe, Kenji Sera, Ken-ichi Nakamura, Kazumi Hirata, Katsuhisa Yuda, and Fujio Okumura, "Excimer laser crystallization of amorphous silicon films", NEC Research and Development, Vol. 35, No. 3, pp. 254-260, (1994)

173) Hiroshi Tanabe, Japanese Patent, 3289681, (2000)

174) Hiroyuki Kuriyama, Seiichi Kiyama, Shigeru Noguchi, Takashi Kuwahara, Satoshi Ishida, Tomoyuki Nohda, Keiichi Sano, Hiroshi Iwata, Hiroshi Kawata, Masato Osumi, Shinya Tsuda, Shoichi Nakano and Yukinori Kuwano, "Enlargement of Poly-Si Film Grain Size by Excimer Laser Annealing and Its Application to High-Performance Poly-Si Thin Film Transistor," Jpn. J. Appl. Phys., vo. 30, pp. 3700-3703, (1991), DOI: https://doi.org/10.1143/JJAP.30.3700

175) Hiroyuki Kuriyama, Tomoyuki Nohda, Satoshi Ishida, Takashi Kuwahara, Shigeru Noguchi, Seiichi Kiyama, Shinya Tsuda and Shoichi Nakano, "Lateral Grain

Growth of Poly-Si Films with a Specific Orientation by an Excimer Laser Annealing Method," Jpn. J. Appl. Phys., vo. 32, pp. 6190-6195, (1993), DOI: https://doi.org/10.1143/JJAP.32.6190
176) M. Ando, K. Ogawa, H. Asuma, Y. Maeda, F. Leblanc and T. Minemura, "Effect of a-Si:H Film Quality on the Space Charge Limited Current in a-Si:H Thin-Film Transistors," International Workshop on Active-Matrix Liquid-Crystal Displays (AM-LCD) 1998, Digest of Technical Papers, pp. 156-159, (1998)
177) Masahiko Ando, Masatoshi Wakagi and Tetsuroh Minemura, "Effects of Back-Channel Etching on the Performance of a-Si:H Thin-Film Transistors," Jpn. J. Appl. Phys., vol. 37, pp. 3904-3909, (1998), DOI: https://doi.org/10.1143/JJAP.37.3904
178) T. Tsukada, "Amorphous silicon thin-film transistors," Journal of Non-Crystalline Solids, vol. 164–166, Part 2, pp. 721-726, (1993)
179) H. Hayashi; M. Kunii; N. Suzuki; Y. Kanaya; M. Kuki; M. Minegishi; T. Urazono; M. Fujino; T. Noguchi; M. Yamazaki, "Fabrication of low-temperature bottom-gate poly-Si TFTs on large-area substrate by linear-beam excimer laser crystallization and ion doping method," Proceedings of International Electron Devices Meeting, pp. 829-832, (1995), DOI: 10.1109/IEDM.1995.499345.
180) I. -W. Wu, T. -Y. Huang, W. B. Jackson, A. G. Lewis and A. Chiang, "Passivation kinetics of two types of defects inpoly-Silicon TFT by plasma hydrogenation," IEEE Electron Device Letters, vol. 12, pp. 181-183, (1991), DOI: 10.1109/55.75757.
181) Masatoshi Yazakis, Satoshi Takenaka and Hiroyuki Ohshima, "Conduction Mechanism of Leakage Current Observed in Metal-Oxide-Semiconductor Transistors and Poly-Si Thin-Film Transistors," Jpn. J. Appl. Phys., vol. 31, pp. 206-209, (1992), DOI: https://doi.org/10.1143/JJAP.31.206
182) K. Sera, H. Asada, F. Okumura, H. Tanabe, K. Nakamura, A. Tada, S. Kaneko, "Excimer Laser Annealed poly-Si TFTs for CMOS Circuits," Extended Abstracts of 1991 International Conference on Solid State Devices and Materials, pp.590-592, (1991), DOI: https://doi.org/10.7567/SSDM.1991.S-A-5
183) N. Kodama, H. Tanabe, K. Sera, K. Hamada, S. Saitoh, F. Okumura, K. Ikeda, "Uniform Performance TFT with Excimer Laser Annealing of Solid Phase Crystallized Poly-Si," Extended Abstracts of 1993 International Conference on Solid State Devices and Materials, pp. 431-433, (1993), DOI: https://doi.org/10.7567/SSDM.1993.PB-2-3
184) M. Bonnel, N. Duhamel, M. Kanouci, B. Loisei, Y. Pelous, "Si poly TFT's with low off-current for flat panel displays," Proceedings of the 13th International

Display Research Conference (Euro Display '93), pp. 199-202, (1993)
185) S. Maegawa, S. Maegawa, T. Ipposhi, S. Maeda, H. Nishimura, T. Ichiki, M. Ashida, O. Tanina, Y. Inoue, T. Nishimura, N. Tsubouchi, "Performance and reliability improvement in poly-Si TFTs by fluorine implantation," Proceedings of IEEE International Electron Devices Meeting, pp. 41-44, (1993), doi: 10.1109/IEDM.1993.347403.
186) I-W. Wu, A. Lewis, A. Chiang, "Effects of Solid Phase Crystallization and LDD Doping on Leakage Current Distributions in Poly-Si TFTs with Multiple Gate Structures," Proceedings of the 12th International Display Research Conference (Japan Display '92), pp.455-458, (1992)
187) Yasuhisa Oana,"180-Bit Static Shift Register and Driver Using Poly-Silicon MOSFFTs," Extended Abstracts of the 15th Conference on Solid State Devices and Materials, pp. 281-284, (1983), DOI: https://doi.org/10.7567/SSDM.1983.A-7-9
188) S. Chen, J. B. Boyce, I-W. Wu, A. Chiang, R. I. Johnson, G. b. Anderson, S. E. Ready, "A low shot density high throughput excimer laser annealing process and system for poly-Si-TFT AMLCD manufacturing," Proceedings of the 13th International Display Research Conference (Euro Display '93), pp. 195-198, (1993)
189) Marc Stehle, Bruno Godard, "Single shot excimer laser annealing," SID Digest, pp. 73-74, (1995)
190) Sheau Chen, Yale H. Sun, "High throughput excimer laser annealing system for low temperature for poly-Si-TFT AMLCD manufacturing," SID Digest, pp. 71-72, (1995)
191) H. Tanabe, K. Sera, K. Nakamura, H. Asada, F. Okumura, "High Performance Poly-Si TFTs Fabricated by Excimer Laser Annealing," The Institute of Electronics, Information and Communication Engineers (IEICE), ED92-42, SDM92-23 (in Japanese), pp. 23-28, (1992)
192) Ichirou Asai, Noriji Kato, Mario Fuse, Toshihisa Hamano, "Poly-Silicon Thin-Film Transistors with Uniform Performance Fabricated by Excimer Laser Annealing," Jpn. J. Appl. Phys., vol. 32, pp. 474-481, (1993), DOI: https://doi.org/10.1143/JJAP.32.474
193) M. W. Geis, D. A. Antoniadis, D. J. Silversmith, R. W. Mountain, and Henry I. Smith, "Silicon graphoepitaxy using a strip-heater oven," Applied Physics Letters, vol. 37, pp. 454-456, (1980), DOI: https://doi.org/10.1063/1.91962
194) D. K. Biegelsen, N. M. Johnson, D. J. Bartelink, and M. D. Moyer, "Laser-induced crystallization of silicon islands on amorphous substrates: Multilayer structures," Applied Physics Letters, vol. 38, pp. 150-152, (1981), DOI:

https://doi.org/10.1063/1.92282
195) J. P. Colinge, E. Demoulin, D. Bensahel, and G. Auvert, “Use of selective annealing for growing very large grain silicon on insulator films,” Applied Physics Letters, vol. 41, pp. 346-347, (1982), DOI: https://doi.org/10.1063/1.93507
196) Hiroshi Tanabe, Hideki Asada, Japanese Patent, 3163693, (1993)
197) K. Sera, H. Asada, F. Okumura, H. Tanabe, K. Nakamura, H. Sekine, I. Fujieda, S. Tsujimura, S. Kaneko, “Integrated Contact-Type Linear Image Sensor with Excimer –Laser-Annealed Poly-Si-TFT Driver,” SID Digest, pp. 356-359, (1993)
198) Ken-ichi Nakamura, Hideki Asada, Toshiyuki Akiyama, Kenji Sera, Hiroshi Tanabe, Fujio Okumura, Ken Ito, Hiroyuki Nakajima, and Hiroshi Saeki, "Fluorescent light source (FLS) with low-temperature poly-Si TFT driver", Proc. SPIE 2171, Color Hard Copy and Graphic Arts III, pp. 66-73, (1994), DOI: https://doi.org/10.1117/12.175290
199) Hiroshi Tanabe, Japanese Patent, 318611, (1993)
200) Hans-Jurgen Kahlert, “Optics for Laser Crystallization Technology,” The Review of Laser Engineering, vo. 31, pp. 40-45, (2003)
201) Shinji Morozumi, Tomio Sonehara, Hiroshi Kamakura, “LCD Full-Color Video Projector,” SID Digest, pp. 375-378, (1986)
202) M. Kunigita, Y. Hirai, Y. Ooi, S. Niiyama, T. Asakawa, K. Masumo, H. Kumai, M. Yuki, T. Gunjima, “A full color projection TV using LC/polymer composite light valves,” SID Digest, pp. 227-230, (1990)
203) K. Yoshinaga, H. Sekine, S. Onda, T. Satoh, K. Hirata, Y. Sato, K. Ishikawa, H. Okumura K. Sera, F. Okumura, “A 0.9” XGA low temperature Poly-Si TFT LCLV with stacked storage capacitor,” SID Digest, pp. 1013-1016, (2002)
204) Y. Tomihari, K. Yoshinaga, H. Sekine, M. Sugimoto, T. Okumura, N. Seko, N. Takada, H. Okumura, K. Shiota, K. Hirata, K. Sera, F. Okumura, “A low temperature Poly-Si TFT liquid crystal light valve (LCLV) with a novel light shielding structure for high performance projection displays,” SID Digest, pp. 972-975, (2004)
205) N. Matsunaga, T. Korenari, K. Hayashi, K. Shiota, H. Tanabe, K. Sera "Ultra-thin-film transistors with reduced photo-leakage currents,” International Workshop on Active-Matrix Liquid-Crystal Displays 2000, Digest of Technical Papers, pp. 181-184, (2004)
206) Shigeru Mori, Isao Shouji, Hiroshi Tanabe, "Semiconductor device, semiconductor device manufacturing method, liquid crystal display device and electronic apparatus," US Patent, No. 8570455

207) NEC & NEC LCD Technologies, “New 2.7-inch LCD Module Boasting an Exceptionally High Pixel Density,” press released on April 14, http://www.nec.co.jp/press/ja/0804/1401.html, https://www.tianma.co.jp/en/news/release_080421.html
208) A. Kohno, T. Sameshima, N. Sano, M. Sekiya and M. Hara, "High performance poly-Si TFTs fabricated using pulsed laser annealing and remote plasma CVD with low temperature processing," IEEE Transactions on Electron Devices, vol. 42, pp. 251-257,(1995), DOI: 10.1109/16.370072.
209) M. Yamamoto, H. Nishitani, M. Sakai, M. Gotoh, Y. Taketomi, H. Tsutsu, and M. Nishitani, Proceedings of International Display Research Conference, pp. 53-56, (1999)
210) M. Sekiya, M. Hara, N. Sano, A. Kohno and T. Sameshima, "High performance poly-crystalline silicon thin film transistors fabricated using remote plasma chemical vapor deposition of SiO_2," IEEE Electron Device Letters, vol. 15, pp. 69-71, (1994), DOI: 10.1109/55.285370.
211) H. Tanabe and K. Sera, “A Clean Poly-Si/Gate Oxide Interface Formation through Consecutive Remote-Plasma Chemical Vapor Deposition of SiO_2 Following Excimer Laser Crystallization of Si Layer,” International Workshop on Active-Matrix Liquid-Crystal Displays 2001, Digest of Technical Papers, pp. 155-158, (2001)
212) Katsuhisa Yuda, Hiroshi Tanabe, Kenji Sera and Fujio Okumura, “Controlling the Amount of Si-OH Bonds for the Formation of High-Quality Low-Temperature Gate Oxides for Poly-Si TFTs,” MRS Proceedings, vol. 508, pp.167-172, (1998), DOI:10.1557/PROC-508-167
213) Ge Xu, Akila Kumagai, Keiji Ishibashi, Hiroshi Nogami, Masahiko Tanaka, Hiroshi Tanabe, Osamu Okada, “Plasma damage-free SiO_2 deposition for low-temperature poly-Si AMLCDs,” Journal of the Society for Information Display, vol. 9, pp. 181-185, (2001), DOI: https://doi.org/10.1889/1.1828786
214) S. Mori, K. Takechi, H. Tanabe and G. Xu, “Thin Gate Oxides Deposited by Remote Plasma-Enhanced Chemical Vapor Deposition for High-Performance Poly-Si TFTs,” International Workshop on Active-Matrix Liquid-Crystal Displays 2001, Digest of Technical Papers, pp. 193-194, (2001)
215) K. Yuda, K. Sera, F. Uesugi, I. Nishiyama and F. Okumura, "Reliability improvement in low-temperature processed poly-Si TFTs for AMLCDs," Proceedings of 1994 IEEE International Electron Devices Meeting, pp. 519-522, (1994), DOI: 10.1109/IEDM.1994.383355.

216) K. Yuda, H. Tanabe and F. Okumura, “Improvement of Structural and Electrical Properties in Low-Temperature Gate Oxides for poly-Si TFTs by Controlling O2/SiH4 Ratios,” International Workshop on Active-Matrix Liquid-Crystal Displays 1997, Digest of Technical Papers, pp. 87-90, (1997)
217) M. Azami, M. Osame, J. Koyama, H. Ohtani, S. Yamazaki, Y. Kubota, S. Naka, M. Hijikigawa, “A 2.6-in. DTV TFT-LCD with Area-Reduced Integrated 8-bit Digital Data Drivers Using 400-Mobility CGS Technology, SID Digest, pp. 6-9, (1999)
218) H. Haga, H. Tsuchi, K. Abe, N. Ikeda, H. Asada, H. Hayama, K. Shiota, N. Takada, “A Parallel Digital-Data-Driver Architecture for Low-Power Poly-Si TFT-LCDs,” SID Digest, pp. 690-693, (2002)
219) H. Kimura, T. Maeda, T. Tsunashima, T. Morita, H. Murata, S. Hirota, H. Sato, “A 2.15 inch QCIF Reflective Color TFT-LCD with Digital Memory on Glass (DMOG),” SID Digest, pp. 268-271, (2001)
220) H. Haga, Y. Nonaka, Y. Kamon, T. Otose, D. Sasaki, Y. Kitagishi, T. Matsuzaki, Y. Sato, Asada, “A 510-kb SOG-DRAM for mobile displays with embedded frame memories,” Journal of the Society for Information Display, vol. 14, pp. 339-344, DOI: https://doi.org/10.1889/1.2196509
221) Hiroshi Tanabe, “High-performance TFT technologies that enable systemization,” LCD/PDP International 2002, October 31, Yokohama, Japan, I-4-4, (2002)
222) Bu-Yeol LeeYasushi KubotaShigeki Imai, “CPU on a Glass Substrate Using CG Silicon TFT,” Sharp Technical Journal, no. 4, (2003), https://cgi.sharp-world.com/corporate/info/rd/tj4/4-2-1.html
223) Robert S. Sposili and James S. Im, “Sequential lateral solidification of thin silicon films on SiO_2,” Applied Physics Letters, vo. 69, pp. 2864-2866, (1996), DOI: https://doi.org/10.1063/1.117344
224) James S. Im, Robert S. Sposili, and M. A. Crowder, “Single-crystal Si films for thin-film transistor devices,” Applied Physics Letters, vol. 70, pp. 3434-3436, (1997), DOI: https://doi.org/10.1063/1.119194
225) M. Matsumura, “Advanced Laser-Crystallization Technologies of Si for High-Performance TFTs,” Proceedings of the 9th International Display Workshop (IDW), pp. 263-266, (2002)
226) R. Dassow, J.R. Köhler, M. Grauvogl, R.B. Bergmann, Jens Werner, “Laser-Crystallized Polycrystalline Silicon on Glass for Photovoltaic Applications,” Solid State Phenomena, vol. 67-68, pp. 193-198, (1999), DOI: https://doi.org/10.4028/www.scientific.net/SSP.67-68.193
227) Y. Helen, R. Dassow, K. Mourgues, O. Bonnaud, T. Mohammed-Brahim, F.

Raoult, J.R. Koehler, J.H. Werner, D. Lemoine, "Reproducible high field effect mobility polysilicon thin film transistors involving pulsed Nd:YVO/sub 4/ laser crystallization," International Electron Devices Meeting 1999. Technical Digest, pp. 297-300, (1999), DOI: 10.1109/IEDM.1999.824155.

228) Ryoichi Ishihara, Artyom Burtsev and Paul F. A. Alkemade, "Location-Control of Large Si Grains by Dual-Beam Excimer-Laser and Thick Oxide Portion," Jpn. J. Appl. Phys., vol. 39, pp. 3872-3878, (2000), DOI: https://doi.org/10.1143/JJAP.39.3872

229) Paul Ch. van der Wilt, B. D. van Dijk, G. J. Bertens, R. Ishihara, and C. I. M. Beenakker, "Formation of location-controlled crystalline islands using substrate-embedded seeds in excimer-laser crystallization of silicon films," Applied Physics Letters, vol. 79, pp. 1819-1821, (2001), DOI: https://doi.org/10.1063/1.1402641

230) Hiromichi Takaoka, Yoshinobu Sato, Takaomi Suzuki, Takuya Sasaki, Hiroshi Tanabe, Hiroshi Hayama, "Excimer-Laser-Induced Lateral Grain Growth of Silicon on Large Glass Substrates and its Application to Thin Film Transistors," Proceedings of the 21st International Display Workshop (IDW), pp. 395-398, (2001)

231) Hiroshi Tanabe, Tomoyuki Akahi, Yoshimi Watabe, US patent, 7312418 (2005)

232) Hiromichi Takaoka, Yoshinobu Sato, Takaomi Suzuki, Takuya Sasaki, Hiroshi Tanabe, Hiroshi Hayama, "Excimer-Laser-Induced Zone-Melting-Recrystallization of Silicon Thin Films on Large Glass Substrates and Its Application to TFTs," IEICE TRANSACTIONS on Electronics, vol. E85-C, pp. 1860-1865, (2002). Partially reused from the above under the permission of the IEICE. Copyright©2002 IEICE.

233) Hiroshi Tanabe, Tomoyuki Akahi, Yoshimi Watabe, US patent, 6861614 (2000)

234) Hiroshi Tanabe, Hiroshi Haga, US Patent, 713830, (2004)

235) Hiroyuki Ohshima, "Past, present and future of mobile displays," Proceedings of International Workshop on Active-Matrix FlatPanel Displays and devices 2013, pp. 13-16, (2013)

236) Youxiang Wu, "Automotive display market outlook," Proceedings of International Workshop on Active-Matrix FlatPanel Displays and devices 2018, SS2-1, (2018)

237) Yoshihiro Nonaka, Jiro Yanase, Masamichi Shimoda, Youichiro Matsueda, Shigeru Mori, Hiroshi Tanabe and Koji Shigemura, "OLED Displays with a Specialized Pixel Circuit for Automotive Applications," SID Digest, vol. 49, pp. 1272-1275, (2018), DOI: https://doi.org/10.1002/sdtp.12148

238) Toshiaki Arai, "Innovative Technologies for OLED Display Manufacturing,"

Proceedings of International Workshop on Active-Matrix FlatPanel Displays and devices 2018, SP2-1, (2018)

239) Jaeseob Lee, Thanh Tien Nguyen, Joonwoo Bae, Gyoochul Jo, Yongsu Lee, Sunghoon Yang, Hyeyong Chu, Jinoh Kwag, “5.8-inch QHD flexible AMOLED display with enhanced bendability of LTPS TFTs,” Society for Information Display 2018, Digest of Technical Papers, pp. 895-898, (2018)

240) Chen-Hao Kuo, Yung-Sheng Tsai, Ching-Chieh Tseng, Chee-Wai Lau, Chun-Yen Liu, Hannibal Wang, Leon Huang, Scott Lin, You-Pang Wei, Po-Tsun Liu, “A Novel Method for LTPS Model Extraction with Hysteresis and Transient Current Analysis,” SID Digest, vol. 46, pp. 1123-1126, (2015), DOI: https://doi.org/10.1002/sdtp.10022

241) Ting-Kuo Chang, Chin-Wei Lin, Shihchang Chang, "LTPO TFT technology for AMOLEDs", Society for Information Display Symposium, Digest of Technical Paper, p. 545, 2019

242) Anis Daami, François Olivier, Ludovic Dupré, Franck Henry, François Templier, “Electro-Optical Size-Dependence Investigation in GaN Micro-LED Devices,” SID Digest, 59-4, p. 790, (2018)

243) Jun Zhu, Tokio Takahashi, Daisuke Ohori, Kazuhiko Endo, Seiji Samukawa, Mitsuaki Shimizu, Xue-Lun Wang, “Near-Complete Elimination of Size-Dependent Efficiency Decrease in GaN Micro-Light-Emitting Diodes,” vol. 216, 1970075, (2019)

244) Chien-Chung Lin, Yen-Hsiang Fang, Ming-Jer Kao, Ping-Kai Huang, Feng-Pin Chang, Li-Chang Yang, Chih-I Wu., “Ultra-Fine Pitch Thin-Film Micro LED Display for Indoor Applications,” SID digest, 59-2, p. 782, (2018)

245) Goshi Biwa, Masato Doi, Atsushi Yasuda, Hisashi Kadota, “Technologies for the Crystal LED Display System,” SID digest, 11-1, p.121, (2019)

246) Hiroshi Ishiwara, Hiroshi Yamamoto, Seijiro Furukawa Masao Tamura and Takashi Tokuyama, “Lateral solid phase epitaxy of amorphous Si films on Si substrates with SiO2 patterns,” Applied Physics Letters, vol. 43, pp. 1028-1030, (1983), DOI: https://doi.org/10.1063/1.94217

247) Hisao Hayashi, Takashi Noguchi and Takefumi Oshima “Polysilicon Super-Thin-Film Transistor (SFT),” Jpn. J. Appl. Phys., vol. 23, pp. L819-821, (1984), https://doi.org/10.1143/JJAP.23.L819

248) Hiroaki Kitahara, “How LCD has grown into a huge industry (in Japanese),” Nikkei Microdevices, April, 2007, pp. 79-86, (2007)

List of publications

Papers relevant to this thesis

1) H. Tanabe, M. Azuma, T. Uematsu, H. Shirai, J. Hanna, and I Shimizu, "Growth of crystalline silicon, microcrystalline and epitaxial at low substrate temperature", Mat. Res. Soc. Symp. Proc., vol. 149, pp. 17-22, (1989)
2) H. Tanabe, K. Sera, K. Nakamura, K. Hirata, K. Yuda, and F. Okumura, "Excimer laser crystallization of amorphous silicon films for poly-Si TFT fabrication", Mat. Res. Soc. Symp. Proc., vol. 321, pp. 677-682, (1994)
3) Hiroshi Tanabe, Claudine M. Chen and Harry A. Atwater, "Grain boundary filtration by selective nucleation and solid phase epitaxy of Ge through planar constructions", Applied Physics Letters, vol. 77, pp. 4325-4327, (2000)

Other papers in this field

1) Hiroshi Tanabe, Kenji Sera, Ken-ichi Nakamura, Kazumi Hirata, Katsuhisa Yuda, and Fujio Okumura, "Excimer laser crystallization of amorphous silicon films", NEC Research and Development, vol. 35, No. 3, pp. 254-260, (1994)
2) Hiroyuki Sekine, Hideki Asada, Ichiro Fujieda, K. Sera, H. Tanabe, and F. Okumura, "High-Speed Linear Image Sensor with a Single-Phase-Clock Poly-Si TFT Driver", NEC Research and Development, vol. 37, No. 2, pp. 226-234, (1996)
3) H. Okumura, H. Tanabe, and F. Okumura, "Effect of the grain growth process on the characteristics for the excimer laser crystallized poly-Si thin film transistors", Mat. Res. Soc. Symp. Proc., vol. 403, pp. 315-320, (1996)
4) K. Yuda, H. Tanabe, K. Sera, and F. Okumura, "Controlling the amount of Si-OH bonds for the formation of high-quality low -temperature gate oxides for poly-Si TFTs", Mat. Res. Soc. Symp. Proc.,vol. 508, pp. 167-172, (1998)
5) Katsuhisa Yuda and Hiroshi Tanabe, "Controlling the amount of Si-OH bonds for the formation of high-quality low-temperature gate oxides for poly-Si TFTs", NEC Research and Development, vol. 40, No. 4, pp. 441-445, (1999)
6) Hiroshi Tanabe, "Effect of cooling late on excimer laser crystallization of silicon thin films", NEC Research and Development, vol. 41, No. 2, pp. 202-206, (2000)
7) R. Puglisi, H. Tanabe, C. Chen, H. A. Atwater, E. Rimini, “Ni-Induced Selective Nucleation and Solid Phase Epitaxy of Large-Grained Poly-Si on Glass,” Mat. Res. Soc. Symp. Proc., vol. 587, O8.1, (1999), DOI: 10.1557/PROC-587-O8.1

8) R. A. Puglisi, H. Tanabe, C. M. Chen, H. A. Atwater, and E. Rimini, "Large-grained polycrystalline Si films obtained by selective nucleation and solid phase epitaxy", Materials Science and Engineering, Vol. B73, pp. 212-217, (2000)
9) Ge Xu, Akila Kumagai, Keiji Ishibashi, Hiroshi Nogami, Masahiko Tanaka, Hiroshi Tanabe, and Osamu Okada, "Plasma damage-free SiO_2 deposition for low-temperature poly-Si AMLCDs", Journal of the Society for Information Display, vol. 9 pp. 181-185, (2001)
10) Hiromichi Takaoka, Yoshinobu Sato, Takaomi Suzuki, Takuya Sasaki, Hiroshi Tanabe, Hiroshi Hayama, "Excimer-Laser-Induced Zone-Melting-Recrystallization of Silicon Thin Films on Large Glass Substrates and Its Application to TFTs," IEICE TRANSACTIONS on Electronics, vol. E85-C, pp. 1860-1865, (2002)

Meeting digests and presentations in this field

1) K. Sera, H. Asada, F. okumura, H. Tanabe, K. Nakamura, A. Tada, S. Kaneko, "Excimer Laser Annealed poly-Si TFTs for CMOS Circuits", Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials, Yokohama, 1991, pp. 590-592. (1991)
2) N. Kodama, H. Tanabe, K. Sera, K. Hamada, S. Saitoh, F. Okumura, and K. Ikeda, "Uniform performance TFT with excimer laser annealing of solid phase crystallized poly-Si", Extended abstracts of the 1993 International Conference on Solid State Devices and Materials, pp. 431-433, (1993)
3) K. Sera, H. Asada, F. Okumura, H. Tanabe, K. Nakamura, H. Sekine, I. Fujieda, S. Tsujimura, and S. Kaneko, "Integrated contact-type linear image sensor with excimer-laser-annealed poly-Si TFT driver", Society for Information Display 93, Digest of Technical Papers, pp. 356-359, (1993)
4) Ken-ichi Nakamura, Hideki Asada, Toshiyuki Akiyama, Kenji Sera, Hiroshi Tanabe, Fujio Okumura, Ken Ito, Hiroyuki Nakajima, and Hiroshi Saeki, "Fluorescent light source (FLS) with low-temperature poly-Si TFT driver", The International Society for Optical Engineering Proceedings, Vol. 2171, pp. 66-69, San Jose, CA, (1994)
5) H. Sekine, H. Asada, I. Fujieda, K. Sera, H. Tanabe, F. Okumura, "A High Speed Linear-Image Sensor with Integrated Poly-Si TFT Driver", Society for Information Display 95, Digest of Technical Papers, pp. 315-318, (1995)
6) F. Okumra, K. Sera, H. Tanabe, K. Yuda, and H. Okumura, "Excimer laser annealed poly-Si TFT technology", Abstracts Materials Research Society 1995 Spring Meeting, (1995)

7) H. Okumura, H. Tanabe and F. Okumura, "TFT Characteristics with Microstructure for Excimer Laser Annealed Poly-Si Films", International Workshop on Active-Matrix Liquid-Crystal Displays 1995, Digest of Technical Papers, pp. 19-22, (1995)
8) H. Asada, K. Hirata, K. Ozawa, K. Nakamura, H. Tanabe, K. Sera, K. Hamada, K. Mochizuki, S. Ohi, S. Saitoh, F. Okumura, and S. Kaneko, "A 2.7 in. 1.3 MPixel driver-integrated poly-Si TFT-LCD for multimedia projectors", Solid-State Circuits Conference, Digest of Technical Papers. 42nd ISSCC., pp. 190-191, (1996)
9) H. Tanabe, H. Okumura, K. Yuda, K. Sera and F. Okumura, "Capping layer effect on uniformity of excimer laser crystallized ply-Si thin film transistors", Abstracts Materials Research Society 1996 Spring Meeting, p.124, (1996)
10) K. Sera, H. Tanabe, H. Okumura, K. Yuda, and F. Okumura, "Uniformity improvement of excimer laser crystallized poly-Si thin film transistors", International Workshop on Active-Matrix Liquid-Crystal Displays '96/ International Display Workshop '96, Digest of Technical Papers, pp. 85-88, (1996)
11) K. Yuda, H. Tanabe, and F. Okumura, "Improvement of structural and electrical properties in low temperature gate oxides for poly-Si TFTs by controlling O2/SiH4 ratios", International Workshop on Active-Matrix Liquid-Crystal Displays 97, Digest of Technical Papers, pp. 87-90, (1997)
12) Hiroshi Tanabe, Claudine M. Chen and Harry A. Atwater, "GRAIN BOUNDARY FILTRATION BY FILM PATTERNING IN SELECTIVE NUCLEATION AND SOLID PHASE EPITAXY OF Si AND Ge ON AMORPHOUS SUBSTRATE," Symposium A-Amorphous and Heterogeneous Silicon Thin Films Fundamentals to Devices, MRS Spring Meeting & Exhibit, April 5-9, 1999, San Francisco, A18.6, (1999)
13) H. Tanabe, "Cooling Rate Simulations and Film Properties in Excimer Laser Crystallization of Silicon Thin Films", International Workshop on Active-Matrix Liquid-Crystal Displays 2000, Digest of Technical Papers, pp. 269-272, (2000)
14) H. A. Atwater, H. Tanabe, C.M. Chen, R. Puglisi, S. Okada and S. McHugo, "Microstructure Control and Tailoring of Si and Ge Thin Films for Device Applications", International Workshop on Active-Matrix Liquid-Crystal Displays 2000, Digest of Technical Papers, pp. 81-84, (2000)
15) H. Tanabe and K. Sera, "A Clean Poly-Si/Gate Oxide Interface Formation through Consecutive Remote-Plasma Chemical Vapor Deposition of SiO_2 Following Excimer Laser Crystallization of Si Layer", International Workshop on Active-Matrix Liquid-Crystal Displays 01, Digest of Technical Papers, pp. 155-158, (2001)
16) S. Mori, K. Takechi, H. Tanabe and G. Xu, "Thin Gate Oxides Deposited by Remote

Plasma-Enhanced Chemical Vapor Deposition for High-Performance Poly-Si TFTs", International Workshop on Active-Matrix Liquid-Crystal Displays 01, Digest of Technical Papers, pp. 193-194, (2001)

17) H. Takaoka, Y. Satou, T. Suzuki, T. Sasaki, H. Tanabe, and H. Hayama, "Excimer-laser-induced lateral grain growth of silicon on large glass substrates and its application to thin film transistors", Asia Display/IDW '01, Digest of Technical Papers, pp. 395-398, (2001)
18) N. Matsunaga, T. Korenari, K. Hayashi, K. Shiota, H. Tanabe and K. Sera, "Ultra-Thin-Film- Transistors with Reduced Photo-Leakage Currents", International Workshop on Active-Matrix Liquid- Crystal Displays 04, Digest of Technical Papers, pp. 181-184, 2004
19) Yoshihiro Nonaka, Jiro Yanase, Masamichi Shimoda, Youichiro Matsueda, Shigeru Mori, Hiroshi Tanabe and Koji Shigemura, “OLED Displays with a Specialized Pixel Circuit for Automotive Applications,” SID Digest, vol. 49, pp. 1272-1275, (2018)
20) Shigeru Mori, Keita Hamada, Hiromu Hanashima, Masamichi Shimoda, Jiro Yanase, Yojiro Matsueda, and Hiroshi Tanabe, “OLED Device Technologies for Automotive Application,” Society for Information Display 2020, Digest of Technical Papers, pp.29-32, (2020)
21) Shigeru Mori, Keita Hamada, Hiromu Hanashima, Masamichi Shimoda, Jiro Yanase, Yojiro Matsueda, and Hiroshi Tanabe, “OLED Device Technologies for High-Luminance, Long-Lifetime and Wide-color gamut displays,” International Display Workshop 2020, Digest of Technical Papers, (to be published)

Patents in this field granted in the United States

1) Soichi Saito, Shinya Niioka, Masayuki Jumonji, Hiroshi Tanabe, Masamichi Shimoda, "Liquid crystal display device and electronic apparatus using the same," US Patent, No. 8941803
2) Shigeru Mori, Takahiro Korenari, Hiroshi Tanabe, "Top gate thin-film transistor, display device, and electronic apparatus," US Patent, No. 8912583
3) Hiroshi Tanabe, "Semiconductor device, manufacturing method for the same, and electronic device," US Patent, No. 8723240
4) Shigeru Mori, Isao Shouji, Hiroshi Tanabe, "Semiconductor device, semiconductor device manufacturing method, liquid crystal display device and electronic apparatus," US Patent, No. 8570455
5) Kenichi Mori, Michiaki Sakamoto, Ken Sumiyoshi, Hiroshi Nagai, Kenichirou Naka,

Masayuki Jumonji, Hiroshi Tanabe, "Liquid crystal display device," US Patent, No. 8488087

6) Soichi Saito, Shinya Niioka, Masayuki Jumonji, Hiroshi Tanabe, Masamichi Shimoda, "Liquid crystal display device and electronic apparatus using the same and manufacturing method thereof," US Patent, No. 8427620
7) Hiroshi Tanabe, "Thin film transistor and manufacturing method of the same," US Patent, No. 8389345
8) Shigeru Mori, Takahiro Korenari, Hiroshi Tanabe, "Top gate thin-film transistor, display device, and electronic apparatus," US Patent, No. 8334553
9) Shigeru Mori, Hiroshi Tanabe, Jun Tanaka, "Silicon oxide film, production method therefor and semiconductor device having gate insulation film using the same," US Patent, No. 8330193
10) Takahiro Korenari, Hiroshi Tanabe, "Thin film transistor substrate and thin film transistor used for the same," US Patent, No. 8242553
11) Shigeru Mori, Takahiro Korenari, Tadahiro Matsuzaki, Hiroshi Tanabe, "Semiconductor device and method for manufacturing same," US Patent, No. 7981811
12) Hiroshi Tanabe, "Thin film transistor and manufacturing method of the same," US Patent, No. 7932137
13) Hiroshi Tanabe, "Semiconductor ferroelectric device, manufacturing method for the same, and electronic device," US Patent, No. 7816716
14) Hiroshi Tanabe, "Semiconductor thin film, thin film transistor, method for manufacturing same, and manufacturing equipment of semiconductor thin film," US Patent, No. 7635894
15) Takahiro Korenari, Hiroshi Tanabe, Nobuya Seko, "Thin-film transistor with semiconductor layer and off-leak current characteristics," US Patent, No. 7633571
16) Kunihiro Shiota, Hiroshi Tanabe, "Pixel circuit substrate, LCD apparatus and projection display apparatus having interlayer insulating film comprising a laminate of inorganic insulating material having a uniformly flat surface over TFT," US Patent, No. 7626648
17) Satou Yoshinobu, Katsuhisa Yuda, Hiroshi Tanabe, "Method for manufacturing a thin-film transistor," US Patent, No. 7585708
18) Shigeru Mori, Takahiro Korenari, Tadahiro Matsuzaki, Hiroshi Tanabe, "Transistor with electrode-protecting insulating film," US Patent, No. 7582933
19) Kunihiro Shiota, Hiroshi Tanabe, "Electro-optical display device and image projection unit," US Patent, No. 7468765

20) Hiroshi Tanabe, Akihiko Taneda, "Thin film processing method and thin processing apparatus," US Patent, No. 7396712
21) Hiroshi Tanabe, Tomoyuki Akashi, Yoshimi Watabe, "Semiconductor thin film forming system," US Patent, No. 7312418
22) Hiroshi Tanabe, Hiroshi Haga, "Thin film transistor having high mobility and high on-current," US Patent, No. 7285809
23) Hiroshi Tanabe, Hiroshi Haga, "Method for manufacturing a thin film transistor having high mobility and high on-current," US Patent, No. 7138303
24) Satou Yoshinobu, Katsuhisa Yuda, Hiroshi Tanabe, "Thin film transistor formed on a transparent substrate," US Patent, No. 7119363
25) Hiroshi Tanabe, Akihiko Taneda, "Thin film processing method and thin film processing apparatus including controlling the cooling rate to control the crystal sizes," US Patent, No. 7063999
26) Hiroshi Tanabe, "Thin-film transistor and method of manufacture thereof," US Patent, No. 7052944
27) Hiroshi Tanabe, "Semiconductor thin film, thin film transistor, method for manufacturing same, and manufacturing equipment of semiconductor thin film," US Patent, No. 7049184
28) Hiroshi Tanabe, "Method for forming semiconductor films at desired positions on a substrate," US Patent, No. 6989300
29) Hiroshi Tanabe, "Apparatus for fabricating thin-film semiconductor device," US Patent, No. 6863733
30) Hiroshi Tanabe, Tomoyuki Akashi, Yoshimi Watabe, "S system for the formation of a silicon thin film and a semiconductor-insulating film interface," US Patent, No. 6861614
31) Katsuhisa Yuda, Hiroshi Tanabe, "Silicon oxide film, method of forming the silicon oxide film, and apparatus for depositing the silicon oxide film," US Patent, No. 6830786
32) Satou Yoshinobu, Katsuhisa Yuda, Hiroshi Tanabe, "Thin film transistor formed on a transparent substrate," US Patent, No. 6822263
33) Hiroshi Tanabe, "System and method for manufacturing semiconductor devices controlled by customer," US Patent, No. 6801826
34) Hiroshi Tanabe, "Thin film transistor and method for fabricating same," US Patent, No. 6797535
35) Hiroshi Tanabe, Katsuhisa Yuda, Hiroshi Okumura, Yoshinobu Sato, "Method of manufacturing thin film transistor," US Patent, No. 6703267

36) Hiroshi Tanabe, "Thin film transistor and method for fabricating same," US Patent, No. 6667188
37) Hiroshi Tanabe, Setsuo Kaneko, "Semiconductor manufacturing apparatus and manufacturing method for thin film semiconductor device," US Patent, No. 6657154
38) Hiroshi Tanabe, "Thin-film semiconductor device and apparatus for fabricating thin-film semiconductor device," US Patent, No. 6642091
39) Hiroshi Tanabe, "Thin film transistor," US Patent, No. 6512246
40) Hiroshi Tanabe, "Apparatus for transforming semiconducting thin layer," US Patent, No. 6486437
41) Hiroshi Tanabe, Katsuhisa Yuda, Hiroshi Okumura, Yoshinobu Sato, "Method of manufacturing thin film transistor," US Patent, No. 6444508
42) Katsuhisa Yuda, Hiroshi Tanabe, "Silicon oxide film, method of forming the silicon oxide film, and apparatus for depositing the silicon oxide film," US Patent, No. 6444327
43) Katsuhisa Yuda, Hiroshi Tanabe, "Silicon oxide film, method of forming the silicon oxide film, and apparatus for depositing the silicon oxide film," US Patent, No. 6383299
44) Hiroshi Okumura, Hiroshi Tanabe, "Method and apparatus for irradiation of a pulse laser beam," US Patent, No. 6372039
45) Hiroshi Tanabe, Katsuhisa Yuda, Hiroshi Okumura, Yoshinobu Sato, "Method of manufacturing thin film transistor," US Patent, No. 6258638
46) Hiroshi Tanabe, Katsuhisa Yuda, Hiroshi Okumura, Yoshinobu Sato, "Thin film transistor," US Patent, No. 5998838
47) Hiroshi Tanabe, "Method for manufacturing a thin film transistor having a forward staggered structure," US Patent, No. 5512494

Papers, meeting presentations and US patents in other technical fields

1) Kazushige Takechi, Shinnosuke Iwamatsu, Toru Yahagi, Yoshiyuki Watanabe, Seiya Kobayashi* and Hiroshi Tanabe, "Top-gate effects in dual-gate amorphous $InGaZnO_4$ thin-film transistors", Electrochemical Society Transactions, 50, (8) 139-149, (2012)
2) Kazushige Takechi, Shinnosuke Iwamatsu, Toru Yahagi, Yoshiyuki Watanabe, Seiya Kobayashi and Hiroshi Tanabe, "Characterization of Top-Gate Effects in Amorphous $InGaZnO_4$ Thin-Film Transistors Using a Dual-Gate Structure", Japanese Journal of Applied Physics, vol. 51, (2012) 104201

3) Shinnosuke Iwamatsu, Kazushige Takechi, Toru Yahagi Yoshiyuki Watanabe, Hiroshi Tanabe, and Seiya Kobayashi, "Depth Profiling Study on Amorphous $InGaZnO_4$ Thin-Film Transistors by X-ray Photoelectron Spectroscopy", Japanese Journal of Applied Physics, vol.52, (2013) 03BB03
4) Kazushige Takechi, Shinnosuke Iwamatsu, Toru Yahagi, Yutaka Abe, Seiya Kobayashi, and Hiroshi Tanabe, “Sensitivity evaluation on amorphous $InGaZnO_4$ thin-film transistor pH sensors having various capacitances of ion-sensitive and bottom-gate insulators”, ECS Journal of Solid State Science and Technology, 3 (2014) Q3076.
5) Kazushige Takechi, Shinnosuke Iwamatsu, Toru Yahagi, Yutaka Abe, Seiya Kobayashi, and Hiroshi Tanabe, “Bottom-gate amorphous $InGaZnO_4$ thin-film transistor pH sensors utilizing top-gate effects”, Japanese Journal of Applied Physics, vol.53 (2014) 076702
6) Jun Tanaka, Yoshihiro Ueoka, Koji Yoshitsugu, Mami Fujii, Yasuaki Ishikawa, Yukiharu Uraoka, Kazushige Takechi, and Hiroshi Tanabe, "Comparison between Effects of PECVD-SiOx and Thermal ALD-AlOx Passivation Layers on Characteristics of Amorphous InGaZnO TFTs", ECS Journal of Solid State Science and Technology, 4, Q3050 (2015)
7) Kazushige Takechi, Shinnosuke Iwamatsu, Shunsuke Konno, Toru Yahagi, Yutaka Abe, Mutsuto Katoh, and Hiroshi Tanabe, "Gate-to-source voltage response in high-sensitivity amorphous $InGaZnO_4$ thin-film transistor pH sensors", Japanese Journal of Applied Physics vol.54, (2015) 078004
8) Kazushige Takechi and Hiroshi Tanabe, " Photoinduced top-gate effect in amorphous $InGaZnO_4$ thin-film transistors", Japanese Journal of Applied Physics 55, 040307 (2016)
9) Kazushige Takechi, Shinnosuke Iwamatsu, Shunsuke Konno, Toru Yahagi, Yutaka Abe, Mutsuto Katoh, and Hiroshi Tanabe, "Demonstration of Detecting Small pH Changes Using High-Sensitivity Amorphous $InGaZnO_4$ Thin-Film Transistor pH Sensor System", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 64, NO. 2, FEBRUARY (2017)
10) Kunihiro Shiota, Mamoru Okamoto and Hiroshi Tanabe, "Viewing-angle-switching device based on array of optical micro-rods incorporated with electrophoretic material systems", Journal of the Society for Information Display, vol. 25, pp. 76-82, (2017)
11) Kazushige Takechi, Shinnosuke Iwamatsu, Yutaka Murakami,Toru Yahagi, Yutaka Abe,Mutsuto Katoh, and Hiroshi Tanabe, "Sensing of Electrostatic Potential by

Using Top-Gate Effect in Amorphous InGaZnO4 Thin-Film Transistors", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 65, NO. 7, JULY (2018)

12) Takanori Takahashi, Ryoko Miyanaga, Mami N. Fujii, Jun Tanaka, Kazushige Takechi, Hiroshi Tanabe, Juan Paolo Bermundo, Yasuaki Ishikawa, and Yukiharu Uraoka, "Hot carrier effects in InGaZnO thin-film transistor", Applied Physics Express 12, 094007 (2019)
13) Yuya Kuwahara, Kazushige Takechi, Jun Tanaka and Hiroshi Tanabe, "Investigation of Hump Effect of Amorphous In-Ga-Zn-O Thin-Film Transistor Using Scanning Capacitance Microscopy", IEEE Electron Device Letters, vol. 40, pp.1273-1276, (2019)
14) Hiroshi Tanabe, Kzushige Takechi and Setsuo Kaneko, "Flexible Displays and TFT Technologies", S9-1-Invited, 2010 International Conference on Flexible and Printed Electronics, Hshinchu, Taiwan, Oct. 29, (2010)
15) Hiroshi Tanabe, Kzushige Takechi and Setsuo Kaneko, "TFT Technologies for Flexible Displays", 2011 International TFT Conference, Cambridge, UK, Mar. 2011
16) Shinnosuke Iwamatsu, Kazushige Takechi, Toru Yahagi Yoshiyuki Watanabe, Hiroshi Tanabe, and Seiya Kobayashi, "Depth Profiling Study on Amorphous $InGaZnO_4$ Thin-Film Transistors by X-ray Photoelectron Spectroscopy", International workshop of AM-FPD, Digest of Technical Papers, pp.139-142, (2012)
17) Kazushige Takechi, Shinnosuke Iwamatsu, Toru Yahagi, Yoshiyuki Watanabe, Seiya Kobayashi and Hiroshi Tanabe, "Top-gate effects in dual-gate amorphous $InGaZnO_4$ thin-film transistors", ECS (Electrochemical Society) meeting 2012@Honolulu, October 8
18) Shinnosuke Iwamatsu, Kazushige Takechi, Toru Yahagi Yoshiyuki Watanabe, Hiroshi Tanabe, and Seiya Kobayashi, "Characterization of Stress-Controlled a-IGZO Thin Films and Their Applications to Thin-Film Transistor and Micro-Electromechanical System Processes", International workshop of AM-FPD, Digest of Technical Papers, pp. 133-136, (2013)
19) Jun Tanaka, Yoshihiro Ueoka, Koji Yoshitsugu, Mami Fujii, Yasuaki Ishikawa, Yukiharu Uraoka, Kazushige Takechi, and Hiroshi Tanabe, "Hydrogen behavior from ALD Al_2O_3 passivation layer for amorphous InGaZnO TFTs", International workshop of AM-FPD, Digest of Technical Papers, pp. 35-36, (2014)
20) Kunihiro Shiota, Mamoru Okamoto and Hiroshi Tanabe, "Viewing-angle-switching device based on array of optical micro-rods incorporated with electrophoretic material systems", Society for Information Display 2017, Digest of Technical Papers, pp.1117-1120, (2017)

21) S. Iwamatsu, K. Takechi, H. Tanabe, and Y. Watanabe, "Demonstration of Extended-Gate Structure for pH Sensors Based on Amorphous Indium-Gallium-Zinc Oxide Thin-Film Transistors", International workshop of AM-FPD, Digest of Technical Papers, 5-2, (2018)
22) Kunihiro Shiota, Mimura Koji, Hiroshi Tanabe, Koji Shigemura, "Image forming apparatus comprising a transparent layer and an optical absorption layer arranged in a pitch of 1/N of a pixel pitch," US Patent, No. 8743317
23) Katsuhiro Echigo, Ichiro Tsuruoka, Manabu Mochizuki, Tsuneo Kurotori, Ariyama Kenzo, Kojima Kenji, Mayumi Miyao, Hiroshi Tanabe, Minoru Iwamoto, "Electrophotographic copier with a developing device using a liquid developer," US Patent, No. 5359398
24) Hiroshi Tanabe, Minoru Iwamoto, Tsuneo Kurotori, Ichiro Tsuruoka, Manabu Mochizuki, Itsuo Ikeda, "Image forming apparatus with ozone detection and deodorizer," US Patent, No. 5164778
25) Tsuneo Kurotori , Manabu Mochizuki, Ichiro Tsuruoka, Katsuhiro Echigo, Itsuo Ikeda, Minoru Iwamoto, Hiroshi Tanabe, Mayumi Miyao, "Apparatus for decomposing ozone by using a solvent mist," US Patent, No. 5155531