Low Temperature Annealing Techniques for Solution Processed Amorphous Oxide Semiconductor Thin-film Transistors

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Abstract

As an emerging material of choice, a-IGZO thin-film transistors (TFTs) have several advantages over other materials such as low-temperature polysilicon (LTPS) or amorphous silicon (a-Si) due to its high electron mobility, wide band gap, and low temperature processability. Despite significant advances in a-IGZO processing, the film itself still possesses many defects such as vacancies, and dangling bonds. Thus, annealing becomes necessary for the device to exhibit the switching characteristics which are necessary in fast response, high resolution displays. In relation to this, there is a concerted effort to transition from vacuum processing to solution processed techniques for device fabrication. Research has shown that using solution processed techniques for device fabrication shortens the process, thus making fabrication much quicker compared to conventional vacuum techniques. This work focuses on using low cost, low temperature techniques which can improve the electrical characteristics of the device compared to conventional annealing. The chapters progress as follows: Identifying low cost low temperature techniques for vacuum processed films, Understanding the effects of each annealing condition through secondary ion mass spectrometry (SIMS) and X-ray photoelectron spectrometry (XPS) analyses in relation to the electrical characteristics of the device, and finally, Applying the previously identified techniques to solution processed films and a reanalysis (SIMS, XPS) of each annealing condition in relation to the device characteristics.

In the 2nd chapter, research has suggested that introducing ultraviolet (UV) light or ozone (O_3) during the annealing process, the channel can be activated at lower temperatures. This chapter shows that a combination of UV & O_3 thermal annealing is the next step for low temperature activation. Deposition of the a-IGZO channel (In_2O_3:Ga_2O_3:ZnO = 1:1:1) unto the substrate at room temperature was done using RF sputtering and was patterned by UV

photolithography followed by wet etching. The source/drain electrodes are composed of Mo (80nm) and Pt (20nm). The annealing process was conducted via a Samco UV-1 organic stripper for 15 minutes. The samples are annealed at the following conditions: UV, O_3, UV and O_3. The annealing temperatures are 290^{o}C, 250^{o}C, 200^{o}C, 150^{o}C, and 100^{o}C. The results show that a combination of UV & O_3 treatment after S/D deposition yields a device with TFT characteristics at annealing temperatures as low as 100^{o}C. UV irradiation combined with ozone breaks down the gas into dioxygen and reactive oxygen; reactive oxygen can react with oxygen vacancies. UV irradiation in conjunction with thermal treatment may also help in the creation of metal oxide (M-O) bonds, resulting in a higher quality film with respectable TFT characteristics. Thus, the combination of low-temperature thermal annealing using UV & O_3 shows great promise for channel layer activation for next generation flexible and transparent devices.

Chapter 3 delves deeper into the effects of each annealing ambient. The previous chapter has shown certain low cost, low temperature annealing methods improve the electrical characteristics of the TFT. With the aid of surface and bulk characterization techniques in comparison to the device characteristics, this work aims to elucidate further on the improvement mechanisms of wet and dry annealing ambients that affect the electrical characteristics of the device. Secondary Ion Mass Spectrometry results show that despite outward diffusion of -H and -OH species, humid annealing ambients counteract outward diffusion of these species, leading to defect sites which can be passivated by the wet ambient. X-ray Photoelectron Spectroscopy results show that for devices annealed for only 30 min in a wet annealing environment, the concentration of metal-oxide bonds increased by as much as 21.8% and defects such as oxygen vacancies were reduced by as much as 18.2% compared to an unannealed device. This work shows that due to the oxidizing power of water vapor, defects are reduced, and overall electrical characteristics are improved as evidenced with the 150^{o}C wet O_2, 30 min annealed sample which exhibited the highest mobility of 5.00 cm^2/Vs, compared to 2.36 cm^2/Vs for a sample that was annealed at 150^{o}C in a dry ambient atmospheric environment for 2h.

In the 4th chapter, we show a facile method of annealing solution processed IZO thin-films in a wet annealing ambient at low temperatures. TG-DTA data indicate that film densification and precursor removal happen at temperatures higher than 244ºC. The electrical characteristics of the 250ºC wet annealed (250WO2) devices compared to the 250ºC atmospherically annealed (250ATM) devices are superior, especially for factors such as field-effect mobility, on/off current, and subthreshold swing. Negative bias stress tests also show that 250WO2 devices have smaller V_{on} shift of -5.1 V versus -12.1 V for the 250ATM devices. SIMS and XPS results show that wet annealing ambients can drastically improve the electrical characteristics of the film versus atmospherically annealed films despite having the same annealing temperature by removing remaining nitrogen precursors and by improving the oxide network of the IZO film. This can be attributed to the nature of wet annealing ambients at low annealing temperatures. Thus, 250WO2 annealed devices were able to reach an S.S. of 0.331 V/dec, $I_{on/off}$ of 10^7, and a maximum field-effect mobility of 2.99 cm^2/Vs which is about 4x higher than 250ATM devices. This annealing method can pave the way for manufacturing solution processed devices that require low thermal budgets.

The final chapter summarizes the work and proposes steps that can be taken to further the research such as possible process optimization procedures or alternative forms of film deposition. These improvements may lead to the fabrication of low temperature, solution processed devices on flexible substrates.

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"You will ride eternal, shiny and chrome."

List of Abbreviations

Abbreviation	Description
AFM	Atomic Force Microscopy
ATM	Atmospheric Conditions
AR-XPS	Angle Resolved X-Ray Photoelectron Spectroscopy
CRT	Cathode Ray Tube
FPD	Flat Panel Display
GI	Gate Insulator
GI-XRD	Grazing Incidence X-Ray Diffraction
IGZO	Indium Gallium Zinc Oxide
IZO	Indium Zinc Oxide
LCD	Liquid Crystal Display
NBS	Negative Bias Stress Test
PMA	Post Metallization Annealing
SIMS	Secondary Ion Mass Spectrometry
STEM	Scanning Transmission Electron Microscopy
S/D	Source & Drain
TFT	Thin-Film Transistor
TG-DTA	Thermogravimetry and Differential Thermal Analysis
TAOS	Transparent Amorphous Oxide Semiconductors
UV	Ultraviolet
WO2	Wet O_2
W/L	Width and Length Dimensions of the channel
XPS	X-Ray Photoelectron Spectroscopy

Table of Contents

Chapter 1 | Introduction

1.1 Brief History of Transistors

Transistors, originally a portmanteau of the word transresistance, have greatly changed society in the past century in terms of creating the connected world that we live in today [1]. One does not need to look far – albeit closely – at the myriad of technologies which use these nano-devices. Some would even argue that transistors are one of the most important inventions mankind has discovered as it ushered in the information/digital age [2] [3] [4]. As such, William B. Shockley, John Bardeen, and Walter H. Brattain were conferred the 1956 Nobel Prize in Physics for their pioneering work on semiconductors and the discovery of the point-contact transistor. On the face of it, transistors primarily have a very basic function: given a certain input signal, an output signal is emitted from the device. What makes a transistor unique is its ability to modulate the input signal, depending on certain device characteristics, to produce a weaker/stronger output signal. The ability to modulate this signal can be attributed to the interactions between p-type and n-type semiconductors, typically upon exposure to a potential difference [5]. Transistors comprise a vast number of modern-day devices which replaced massive, dated technologies such as vacuum tubes which used to occupy sizeable rooms. Initially, these vacuum tubes would serve to function as one of the first electronic processors, albeit with the added inconvenience of size. As manufacturing and processing technologies developed further, devices which used the transistor grew in number as the transistor size decreased further. Processors, which use nanoscale transistors, are labelled according to

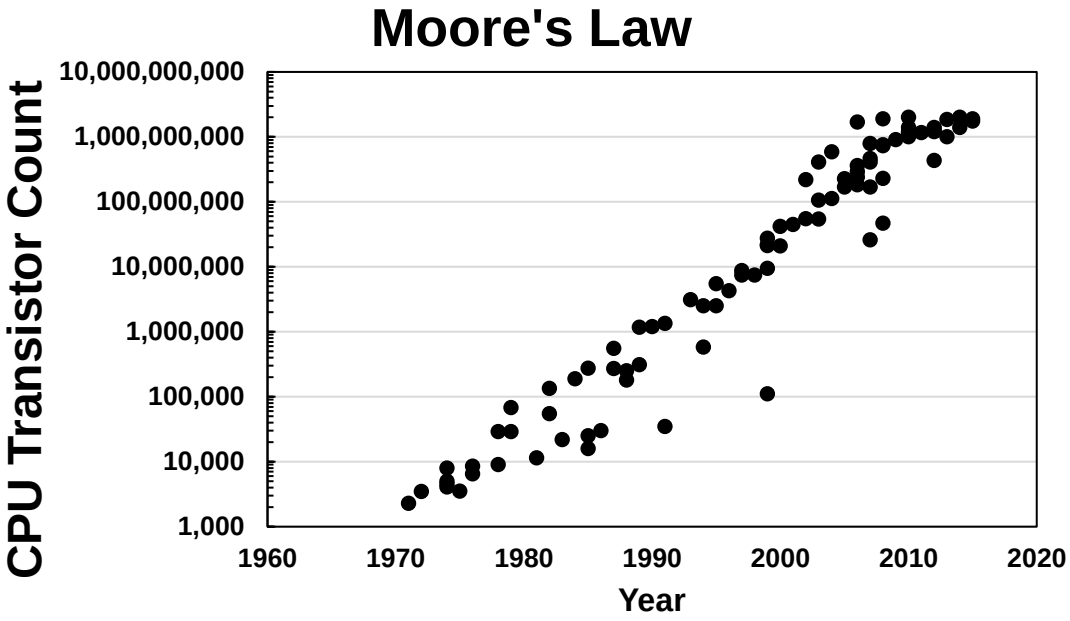

Figure 1.1. Number of transistors per chip since the early 1970s.

their chip size and ranges from 10 μm (1971) up to a projected 5 nm (2020). Gordon Moore, co-founder of Fairchild Semiconductor and chairman emeritus of Intel, famously stated in 1965 that the number of transistors on a dense integrated circuit would double every two years [6]. This trend can clearly be seen in the number of transistors per microprocessor/CPU since the commercialization of transistors into devices [Fig. 1.1]. Intel has continuously rolled out generation after generation of CPUs, thus elevating the processing ability of computers and mobile workstations year on year. Thus, transistors can be found in almost every device being used by a society that lives in the information age: computers, cellphones, cameras, signal processing devices, and display technologies just to name a few. These “microswitches” have made everyday life more convenient, more automated, and more streamlined; facilitating mundane, repetitive tasks by making calculations faster. Clearly, the transistor is central in maintaining and driving today’s connected world.

1.2 Thin-film Transistors

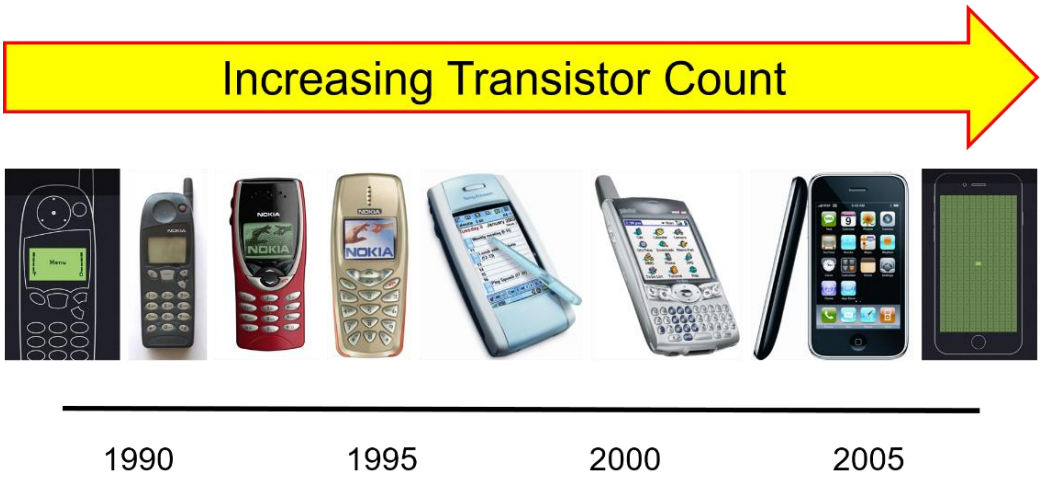

Figure 1.2. The number of transistors found in cellular phone displays over time.

In the digital age, the ability to display information is as important as the speed of processing the data. In this specific facet, transistors also play an important role. Display devices have also benefitted from the scaling down of transistor technology. From massive color cathode-ray tubes (CRT) in the 1950s, vacuum fluorescent displays in the 1960s, twisted nematic field effect liquid crystal displays (LCDs) of the 1970s, to the introduction of thin-film transistors (TFT) LCDs in the 1990s, display technology has evolved at almost the same pace as their processor counterparts [7]. As seen in Fig. 1.2, even cellular phone displays have greatly increased their resolution to match the amount of information displayed on the screen. A cellular phone display in the early 90s only accounts for a fraction of space in the most recent smart phone.

As the name implies, thin-film transistors are devices which operate along the same principles as their "larger" scale counterparts by utilizing p-type and n-type semiconductors to modulate an output signal given a specific input signal. In this specific application, TFTs act as the switching element in the backplane of the LCD by acting as the switch that controls a specific pixel. These TFTs are arranged in a specific grid pattern

so that microcontrollers can easily triangulate which specific pixels need to be turned on/off. The net effect of each of these pixels creates a vivid image, akin to portraits and paintings which adopted pointillism, albeit at a higher resolution. The discoveries of manufacturing methods, processing techniques, and new materials have allowed significant advancement in TFT technology. Manufacturing techniques that utilize ultra clean fabrication conditions ensure that the quality of the devices meets a certain threshold. Advancements in Physics and Chemistry such as sputtering (RF/DC magnetron), plasma enhanced chemical vapor deposition (PECVD), and reactive ion etching (RIE) have also expedited producing high quality devices in vacuum conditions, thus minimizing device contamination and increasing throughput. Thus, the quality of the images/videos produced by displays which use TFTs in their backplane have allowed the creation of different – increasing – display resolutions to what was once a very short list: High Definition (HD), Full High Definition (FHD), Quad High Definiton (QHD), 4K & 8K Ultra High Definition (UHD) to name a few. Similarly, screens have slowly evolved from fixed, rigid substrates to displays which use flexible substrates. As of 2019, different display manufacturers such as LG, Samsung, and even Intel have patented, marketed, and introduced flexible displays which can be rolled and folded into small containers but when unfurled, have massive high resolution form factors [8] [9]. Thus, the consumer display market has been inundated with portable high-resolution displays which can be "unfolded" revealing even larger vivid displays [10]. Glass developers such as Corning have also invented flexible glass substrates and their associated manufacturing methods which enable creating a bendable screen with fantastic opacity [11] [12]. Aside from this, there has also been a shift in the past two decades regarding the materials used in display technologies. The introduction of hydrogenated Silicon to active matrix liquid crystal

displays (AMLCD) for flat panel displays (FPD) was the turning point for the cathode ray tube (CRT) displays. Up until that point, it was widely regarded that manufacturing costs for displays far outweigh the benefits of producing AMLCD FPDs – which use TFTs for the display backplane. By using hydrogenated amorphous Silicon (a-Si:H), the TFTs had very low leakage currents, can be easily deposited over large areas, and can be processed at temperatures which were compatible with glass. 2003 was even regarded as the turning point, in terms of profit, that FPDs will overtake CRT displays as the market leader in display technology [13]. Despite the advantages of a-Si:H, it also has its fair share of drawbacks for next generation, flexible displays: low field effect mobilities in the range of ~1-2.7 cm^2/Vs, and localized tail-state hopping instead of band conduction. As for other variants of Si such as high-temperature annealed polycrystalline silicon (HTPS), these limit the type of substrates that the devices can be deposited on to due to the high annealing temperature.

1.3 Transparent Amorphous Oxide Thin-film Transistors

During 1996, Hideo Hosono proposed an interesting hypothesis: wide band gap oxide semiconducting materials can have Hall mobilities higher that Si:H and amorphous transition metal oxides due to the formation of oxygen vacancies or doping through ion implantation [14]. It was proposed that transparent amorphous oxide semiconductor (TAOS) materials would also be perfect to drive large organic light emitting diodes (OLEDs) because of their high mobilities (>10 cm^2/Vs), low range thermal process window from room temperature (RT) to ≥300°C, and the ability to deposit large area films due to the amorphous nature of the material. The excellent electrical properties of the materials, despite being amorphous films, can be attributed to the spatial overlap between

Table 1.1 Comparison of TAOS devices versus Silicon based devices *[69]*

AMOLED Panel	Poly-Si TFT	a-Si:H TFT	Oxide TFT
Semiconductor	Polycrystalline Si	Amorphous Si	TAOS
Film Uniformity	Poor	Good	Good
Pixel Circuit	Complex	Complex	Simple/Complex
Channel Mobility	~100 cm^2/Vs	1 cm^2/Vs	>10 cm^2/Vs
TFT Type	PMOS (CMOS)	NMOS	NMOS
TFT mask steps	5-11	4-5	5-7
Cost/Yield	High/Medium	Low	Low/Medium
Thermal Budget	250-500	150-350	RT-400
Scalability	<40"	>100"	Potential 100"
Challenges	Uniformity, Cost, scalability	Poor Mobility, stability	Manufacturing process not mature

the metal cations and the vacant s orbitals [3] [14] [15]. 2004 saw the first device which utilized TAOS materials as the semiconducting material used in the channel layer of the TFT device. Kenji Nomura et al. reported on amorphous Indium Gallium Zinc Oxide (a-IGZO) TFTs with saturation mobilities of 6-9 cm^2/Vs, leakage currents well below 1 nA, and a reasonable on/off ratio ($I_{on/off}$) of 10^3 despite bending the substrate multiple times [16]. Back then, these electrical characteristics were unheard of for TFTs that utilized TAOS materials and opened the door for the fabrication of next generation, RT processed TFT devices. It was even reported that several companies started the development of incorporating TAOS materials in fabricating their FPDs [17]. As seen in table 1.1, a quick comparison between TAOS and their silicon counterparts reveal a very promising future for oxide TFTs. Typical TAOS materials used for fabricating TFTs aside from IGZO are: Indium-Zinc-Oxide (IZO) [18] [19], Zinc-Tin-Oxide (ZTO) [20] [21] [22], Gallium-Zinc-Oxide (GZO) [23] [24], and Indium-Tungsten-Zinc-Oxide (IWZO) [25] [26].

Table 1.2 Electrical characteristics of TAOS materials found in TFTs

Characteristics	IGZO	InZnO	ZnSnO	GaZnO	InWZnO	ZnO
Mobility (cm^2/Vs)	~6 – 38	~2 – 32	~10 – 43	1 – 10	~15 – 60	~5 – 25
Subthreshold Swing (V/dec)	0.1 – 0.3	0.2 – 0.7	0.2 – 0.3	0.09 – 0.2	0.1 – 0.5	0.1 – 1
Process Temperature (°C)	~450	~350	~500	~200	~300	~300
Current On/Off Ratio	$10^6 – 10^8$	$10^5 – 10^7$	$10^6 – 10^9$	$10^5 – 10^9$	$10^6 – 10^7$	$10^5 – 10^9$
Structure	Amorphous	Amorphous	Amorphous	Amorphous	Amorphous	Polycrystalline

Researchers try to change the different elemental concentrations for each materials to improve the device characteristics. Table 1.2 summarizes commonly researched TAOS materials and their corresponding electrical properties. As can be observed, most of these materials have respectable electrical characteristics despite being predominantly amorphous. Large area films can be produced without the inconvenience of worrying about the quality of the film due to its amorphous nature. It can also be said that although certain characteristics, such as electron mobility for TAOS materials, are generally lower compared to their Poly-Si counterparts, the scalability of the material allows for higher resolution displays and improved pixel densities due to the relatively smaller transistor sizes. Recent advances in TAOS TFT research have even shown that the electrical properties of the devices are soon approaching – if not achieving better – characteristics such as mobilities in the range of 60 to >300 cm^2/Vs for IGZO based TFTs [27] [28]. Since its inception in 1996, it can also be said that TAOS semiconductors are turning the idea of flexible, transparent displays into reality [29]. In the recent consumer electronics show (CES) 2019, LG Electronics of South Korea – one of the leading companies in the world of display technology and smartphone devices – unveiled a rollable television which features a 4K organic light emitting diode (OLED) display that utilizes TAOS

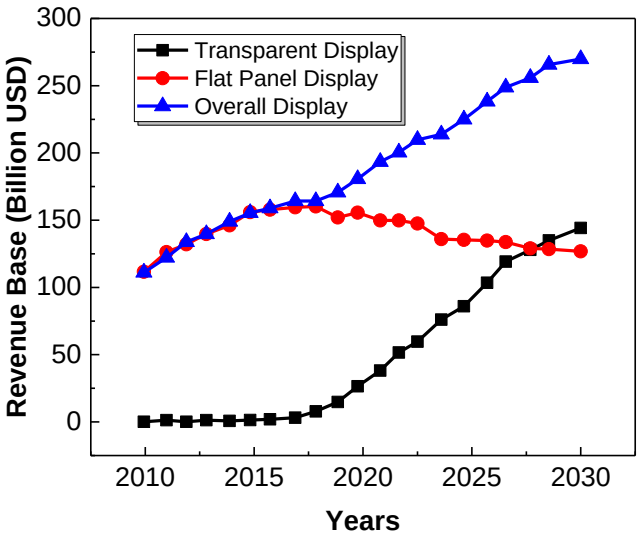

Figure 1.3. Display technology evolution and the corresponding revenue per decade. *[69]*

materials, thus prompting other manufacturers and companies to follow suit [30] [31] [32]. Figure 1.3 shows the projected revenue in the display market with a clear uptick in transparent displays as the technology becomes more mature. All current developments are pointing to the fact that most, if not all future display devices will at least feature an amorphous oxide material as a vital component for relaying visual information.

1.4 Basic Thin-film Transistor Operation

In principle, TFTs can be classified as metal oxide semiconductor field effect transistors (MOSFETs) due to the similarities in their operation. The fundamental physics of device operation for thin-film transistors has long been established [5] [13]. The typical components of a TFT are as follows: substrate, source, drain, gate, semiconducting channel material, and for the sake of device stability, an encapsulation or passivation layer; each component is vital in operating the device. Thus, various architectures for TFTs have been adopted by manufacturers when fabricating their display panels. These architectures utilize different geometries to minimize unwanted effects such as charge

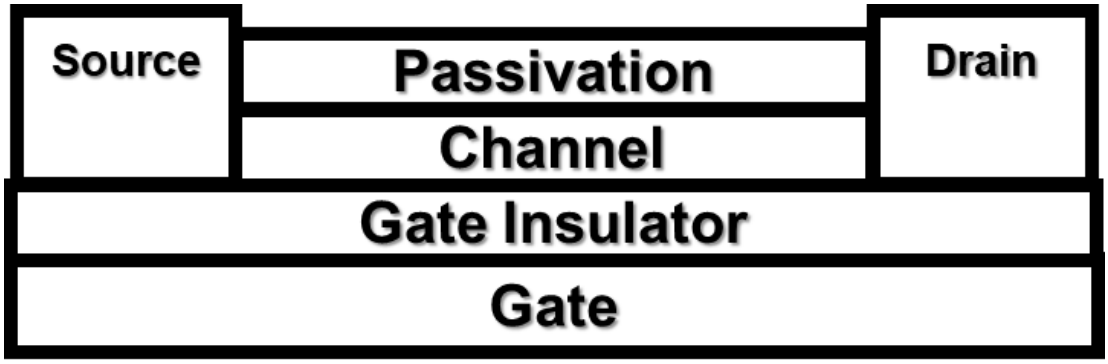

Figure 1.4. Bottom Gate, top contact device structure with passivation.

accumulation, heat accumulation. One common structure for most TFTs is called the inverted-staggered configuration or what is otherwise known as a bottom gate, top contact (BGTC) device as seen in Figure 1.4. To operate the device, a potential difference is placed across the top source and drain electrodes whilst the gate is also subjected to a certain voltage. The voltage required to allow the formation of the conduction channel is usually called the threshold voltage V_{th}. Take for example an n-channel device such as a BGTC In-Ga-Zn oxide TFT which behaves in enhancement mode at 0 V gate voltage V_g. "Turning on" the device necessitates a voltage applied at the gate – typically at a voltage which is higher compared to the source voltage – and a conduction channel is formed between the source and drain. The number of electrons that flow from source to drain is regulated by the gate voltage thus transforming what is called a "normally off" device to a device in the "on state". The region between the channel layer and the gate insulator (GI) upon application of V_g is usually called the inversion layer. As V_g is applied at the gate, band bending happens in the inversion layer as electrons accumulate to form the conduction channel.

1.5 Deposition Processes for Thin-film Transistors

Fabrication techniques have drastically improved since the first iteration of the bipolar junction FET. Modern devices are manufactured in clean room environments to prevent contamination and to increase device yield whilst still producing high quality and high-performance devices. This is due to scientific and engineering breakthroughs in large-are chemistry or physics-based processes, fabrication techniques, the discovery of alternative semiconductor materials (a-Si:H, poly-Si, TAOS, etc.), and developments in substrates to name a few [33]. In between each step in Fig. 1.5, thin-film deposition and patterning techniques are used. In relation to thin-film deposition and device fabrication, processing techniques can be broadly categorized into two methods: vacuum and solution processed deposition techniques. The current consensus for high quality films with high throughput is to utilize vacuum processing techniques to produce excellent devices. Deposition methods include radio frequency (RF) sputtering, pulsed laser deposition (PLD), resistive heating, or atomic layer deposition (ALD) among others [34] [35] [36] [37] [38] [39] [40] [41]. These deposition techniques entail the use of a system of pumps to bring the base pressure to levels which minimize contamination. These systems typically operate in the range of high (HV; 0.1~10^{-4} Pa) to ultra-high vacuum (UHV; ~10^{-4}-10^{-7} Pa). A typical high vacuum system possesses the following components: rotary pump(s), vacuum chambers and lines, vacuum feed throughs, turbo molecular pumps and the corresponding controllers, low and high vacuum gauges. With these components, the estimated cost for

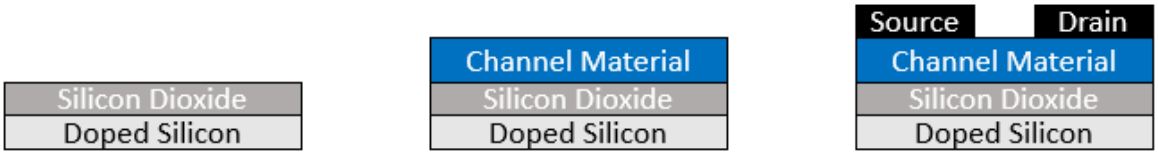

Figure 1.5 Simplified version of the TFT device fabrication process.

Table 1.3 Expected cost for a fabrication plant that manufactures 200 mm wafers per year.

Section	Class	Machines	Area (m^2)	Cost (USD Million)
Fabrication	1	171	~2,900	108.4
Testing	100	14	~230	4.3
Packaging	100	5	~100	1.8
Totals	-	190	~3,230	114.5

the equipment alone already can be staggering for small to medium scale university-based research labs. Table 1.3 briefly summarizes the expected cost for a fabrication plant, wherein most of the expenditure comes from machine procurement [42]. Arthur Rock's law, or as other call Moore's second law, still holds true even with current manufacturing costs. Rock's law dictates that the cost of establishing a semiconductor chip fabrication plant doubles every four years. Projections and studies have shown that despite the massive revenue in semiconductor device sales (and all semiconductor related technologies), the acquisition and maintenance cost for fabrication equipment is increasing at a steady pace; It can also be inferred that much of the cost of fabrication is directly related to the cost of acquiring and maintaining the manufacturing equipment [43]. Therefore, despite the prevailing agreement in manufacturing circles that the quality of vacuum processed devices is better than the non-vacuum counterparts, there has been a clear drive in the past decades to switch to solution processed deposition methods [3] [4] [44] [45]. The intention here is to maximize profit margins by minimizing the acquisition and maintenance costs of high vacuum systems. Thus, the emerging second method of film deposition relies on using solution-based techniques to fabricate high quality films and devices whilst considering minimizing or eliminating vacuum processes. Recent developments in solution processed techniques have enabled the creation of devices which are comparable in performance to vacuum processed devices

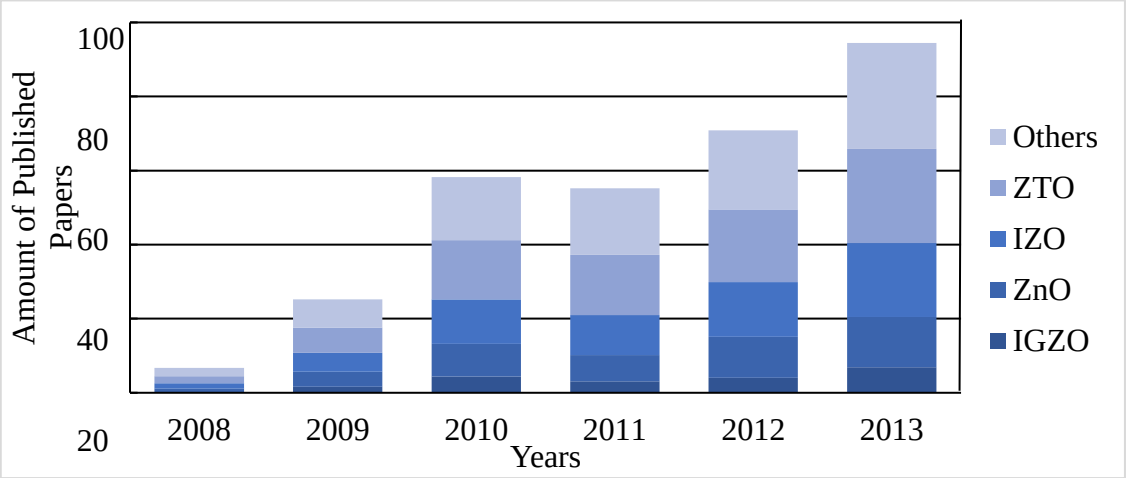

Figure 1.6 Research on solution processed oxide thin-film transistors from 2008-2013 *[4]*.

[46] [51] [52] [53]. Table 1.4 lists only a select few of the current research since 2007 on solution processed devices. As seen in Fig. 1.6, since 2008, there has been a clear interest in the advancement and development of solution processed techniques. One does not need to look far in terms of the research output in the past decade to ascertain that solution processed techniques have certainly improved in terms of quality and repeatability; An issue which initially plagued research which was based on solution processed techniques. Indubitably, challenges still exist regarding solution processed oxide thin-film devices on

Table 1.4 Comparison of vacuum versus solution processed devices

Channel Material	Mobility (cm^2/Vs)	Current On/Off Ratio	Deposition Process	Reference
InO	43.7	$\sim 10^6$	Spin Coating	[46]
ZnO	85.0	$\sim 10^6$	Spray Pyrolysis	[47]
ZTO	4.98	$\sim 10^9$	Ink Jet	[48]
IGZO	7.65	$\sim 10^7$	Spin Coating	[49]
IGZO	20.9	$\sim 10^7$	DC Sputtering	[50]

an industrial scale, but ongoing research has made the dream of replacing vacuum processed techniques closer to a “mass production level” reality. As fabrication and processing techniques evolve for solution processed devices, roll to roll systems can be assembled in clean room environments without the need for costly vacuum equipment whilst still manufacturing devices with good performance.

1.6 Challenges and Strategies for Fabricating Thin-film Transistors on Flexible Substrates

Transparent amorphous oxide semiconductors are driving the push for transparent devices by being incorporated into thin-film transistors. Due to the materials’ controllable conductivity, TAOS can be used in both the electrodes or channel layer of the TFTs. As compared to conventional semiconductor materials, this property can be attributed to overlapping regions in the orbitals related to the conduction band [54]. Despite the promising developments, TAOS materials still face certain challenges when it comes to the market and industry demands for next generation displays. Despite significant advances in processing and fabrication of TAOS materials in TFTs, the semiconductor channel still possesses many defects such as vacancies, and dangling bonds [55]. As mentioned in the earlier section, films are typically manufactured through vacuum processed techniques such as sputtering; Due to this, there can be an increase in the surface morphology roughness of the semiconducting layer which may lead to an increase of contact resistance or the presence of interface traps between the device layers; interface charge traps, grain boundary scattering, increase in contact resistance, can greatly diminish important characteristics such as the threshold voltage (V_{th}), current on/off ($I_{on/off}$) ratio, as well as the saturation mobility (μ_{sat}). Despite the property of TAOS

materials to exhibit high mobilities despite their amorphous composition, during film deposition, Research has shown that performing post deposition annealing on the oxide films greatly improves the reproducibility, yield, and electrical characteristics of the devices [56] [54] [57] [58] [59]. Thus, post deposition annealing is a vital step in ensuring that the manufactured devices have a high yield and reliable performance.

Table 1.5 shows the typical post annealing temperatures for some TAOS materials as well as flexible substrates with their corresponding max temperatures. Depositing on a substrate with good transparency is usually correlated to a very low max process temperature. Given that most TAOS materials need to be post annealed at temperatures greater than 200°C, this means despite having a flexible substrate, concessions need to be made in terms of opacity. Thus, researchers have investigated different techniques to either: lower the overall annealing temperature by introducing additional processing steps [60] [61], change material characteristics (channel and/or dielectric) [62] [63] [64], or localize the annealing temperature [65] [66] [67] [68] [69]. These methods include changing the annealing conditions or annealing ambient, doping the channel and/or dielectric used for the device, or by using annealing techniques such as flash lamp or

Table 1.5 Comparison between annealing/process temperatures between transparent amorphous oxide materials and commonly used flexible substrates *[70]*.

TAOS Channel Material	Annealing Temperature (°C)	Flexible Substrates	Max Process Temperature (°C)	Transparency
InO ZnO	230	Polyethylene terephthalate (PET)	78-160	Very good
InO	350	Polyethylene naphthalate (PEN)	120-200	Very Good
ITO	350	Polycarbonate (PC)	150	Excellent
IGZO	450	Polyether ether ketone (PEEK)	143-260	Very Good
ZTO	500	Polyimide (PI)	350-400	Good

Excimer laser annealing. Thus, by incorporating these techniques in relation to fabricating devices which can be deposited on flexible substrates, next generation rollable and transparent devices can pave the way for further integration of display technology in the Internet of Things (IoT).

1.7 Objectives and Outline of this Thesis

The first chapter talked about the relevance of TFTs in society, TAOS materials used in TFT devices, fabrication methods, and the current challenges in TAOS TFT s. As an emerging material of choice, a-IGZO thin-film transistors (TFTs) have several advantages over other materials such as low-temperature polysilicon (LTPS) or amorphous silicon (a-Si) due to its high electron mobility, wide band gap, and low temperature processability. Despite significant advances in a-IGZO processing, the film itself still possesses many defects such as vacancies, and dangling bonds. Thus, annealing becomes necessary for the device to exhibit the switching characteristics which are necessary in fast response, high resolution displays. In relation to this, there is a concerted effort to transition from vacuum processing to solution processed techniques for device fabrication. Research has shown that using solution processed techniques for device fabrication shortens the process, thus making fabrication much quicker compared to conventional vacuum techniques. The overarching goal of this work focuses on using low cost, low temperature techniques which can improve the electrical characteristics of the device compared to conventional atmospheric annealing. The hypothesis of this work is as follows: first, identify low cost low temperature techniques for vacuum processed TAOS films by analyzing their electrical characteristics. Second, understanding the effects of each annealing condition through secondary ion mass spectrometry (SIMS) and

X-ray photoelectron spectrometry (XPS) analyses in relation to the electrical characteristics of the device. Finally, apply the previously identified techniques to solution processed films and a reanalysis of the effect of each annealing condition in relation to the device characteristics, film quality, and device performance.

The second chapter shows that a combination of UV & O_3 thermal annealing is the next step for low temperature activation. It has been suggested that introducing ultraviolet (UV) light or ozone (O_3) during the annealing process, the channel can be activated at lower temperatures. Deposition of the a-IGZO channel (In_2O_3:Ga_2O_3:ZnO = 1:1:1) unto the substrate at room temperature was done using RF sputtering and was patterned by UV photolithography followed by wet etching. The source/drain electrodes are composed of Mo (80nm)/Pt (20nm). The annealing process was conducted via a Samco UV-1 organic stripper for 15 minutes. The samples are annealed at the following conditions: UV, O_3, UV and O_3. The annealing temperatures are 290℃, 250℃, 200℃, 150℃, and 100℃. The results show that a combination of UV & O_3 treatment after S/D deposition yields a device with TFT characteristics at annealing temperatures as low as 100℃. UV irradiation combined with ozone breaks down the gas into dioxygen and reactive oxygen; reactive oxygen can react with oxygen vacancies. UV irradiation in conjunction with thermal treatment may also help in the creation of metal oxide (MO) bonds, resulting in a higher quality film with respectable TFT characteristics. Thus, the combination of low-temperature thermal annealing using UV & O_3 shows great promise for channel layer activation for next generation flexible and transparent devices.

The previous chapter has shown certain low cost, low temperature annealing methods improve the electrical characteristics of the TFT. With the aid of surface and

bulk characterization techniques in comparison to the device characteristics, this chapter aims to elucidate further on the improvement mechanisms of wet and dry annealing ambients that affect the electrical characteristics of the device. Secondary Ion Mass Spectrometry (SIMS) results show that despite outward diffusion of -H and -OH species, humid annealing ambients counteract outward diffusion of these species, leading to defect sites which can be passivated by the wet ambient. X-ray Photoelectron Spectroscopy (XPS) results show that for devices annealed for only 30 min in a wet annealing environment, the concentration of metal-oxide bonds increased by as much as 21.8% and defects such as oxygen vacancies were reduced by as much as 18.2% compared to an unannealed device. This chapter shows that due to the oxidizing power of water vapor, defects are reduced, and overall electrical characteristics are improved as evidenced with the 150℃ wet O_2, 30 min annealed sample which exhibited the highest mobility of 5.00 cm^2/Vs, compared to 2.36 cm^2/Vs for a sample that was annealed at 150℃ in a dry ambient atmospheric environment for 2h.

In the next chapter, we show a facile method of annealing solution processed IZO thin-films in a wet annealing ambient at low temperatures. TG-DTA data indicate that film densification and precursor removal happen at temperatures higher than 244℃. The electrical characteristics of the 250ºC wet annealed (250WO2) devices compared to the 250ºC atmospherically annealed (250ATM) devices are superior, especially for factors such as field-effect mobility, on/off current, and subthreshold swing. Negative bias stress tests also show that 250WO2 devices have smaller V_{on} shift of -5.1 V versus -12.1 V for the 250ATM devices. SIMS and XPS results show that wet annealing ambients can drastically improve the electrical characteristics of the film versus atmospherically

annealed films despite having the same annealing temperature by removing remaining nitrogen precursors and by improving the oxide network of the IZO film. This can be attributed to the nature of wet annealing ambients at low annealing temperatures. Thus, 250WO2 annealed devices were able to reach an S.S. of 0.331 V/dec, $I_{on/off}$ of ~10^7, and a maximum field-effect mobility of 2.99 cm^2/Vs which is about 4x higher than 250ATM devices. This annealing method can pave the way for manufacturing solution processed devices that require low thermal budgets.

The final chapter summarizes this work by showing that low cost, low temperature techniques can be effective alternatives to other low temperature techniques. The roles of hydrogen related species can greatly affect the quality of the oxide network in the film as evidenced in the different characterization tests that were done. These low cost, low temperature techniques can pave the way for the realization of high-performance solution processed TFTs. This chapter also discusses immediate next steps to further the research.

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Chapter 2 | Low Temperature Annealing Methods for Vacuum Processed Films

2.1 Introduction

The market is currently experiencing a new wave of next generation displays: Transparent Amorphous Oxide Semiconductors, otherwise known as TAOS, are quickly becoming the successor to the old silicon back planes found in Liquid Crystal Displays (LCDs). TAOS materials are used in the back plane of display devices, particularly the switching thin-film transistor (Sw-TFT) which controls the on or off state of the corresponding pixel. As such, TAOS materials have become the perfect choice for the transistor plane due to the following properties: high electron mobility, wide band gap, and low process temperature. These three characteristics push the boundaries of the technology by enabling high resolution displays which consume less energy, the ability to fabricate a completely transparent display, and the choice of having a flexible substrate respectively [1]. TAOS materials such as amorphous In-Ga-Zn-O (a-IGZO) and amorphous In-Zn-O (a-IZO) are ever expanding research fields. Figure 2.1 shows various products that use the aforementioned materials which are already in the market.

Figure 2.1. Devices which use TAOS materials for their display backplane *[50]*.

Table 2.1 Summary of oxide semiconductor TFTs on flexible substrates.

Year	Substrate	TAOS	Bending Cycle	Mobility (cm^2/Vs)	Reference
2012	PI	a-IGZO	1000	14.5	[2]
2012	PET	ZnO	2000	0.49	[3]
2013	PI	IZO	-	51.0	[4]
2014	PEN	IGZO	100,000	11.2	[5]
2014	PI	IGZO	10,000	14.9	[6]
2015	PEN	IGZO	10,000	15.5	[7]
2015	PEN	IGZO	10,000	16.0	[8]
2016	PI	InO_x	10,000	15.0	[9]
2016	PET	IZO	5000	40.1	[10]
2016	PI	In_2O_3	5000	7.12	[11]
2017	PI	IGZO	5000	76.8	[12]

Typically, these materials are used as the active channel layer, serving as the semiconductor material for the transistor. During the fabrication process of the channel, certain defects such as Frenkel defects or vacancies are present in the film [13] [14]. As such, this drastically limits the performance and, in most cases, the overall functionality of the device. Typically, these defects are addressed by annealing the device in temperatures that typically reach temperatures greater than 300℃ [14] [15] [16]. Given these factors, current trends in display technology are directed towards consumers who live a digital lifestyle. Concepts such as the Internet of Things (IOT) integrate various devices and appliances with the internet; from mobile devices and smart appliances, there is an ever-growing need for ubiquitous displays [17] [18]. Companies have addressed this by creating transparent displays that leverage on TAOS materials; the idea is taken a step further by fabricating these devices on flexible substrates. Table 2.1 shows the electrical properties of devices fabricated on flexible substrates. There is a clear interest in developing flexible technology as evidenced by the uptick in research activities over the years in relation to TAOS devices [19]. Current advances in low temperature annealing point to ELA or excimer laser annealing as an effective method of annealing the

channel layer of the device without causing serious thermal damage to the substrate underneath. Unfortunately, ELA systems encounter a significant roadblock when it comes to scaling these devices to factory scale machines. The sheer cost of making a new manufacturing line currently far outweigh the potential profits [20]. Strategies are being developed to improve scaling issues such as laser cooling, beam quality issues due to beam shaping, and beam uniformity to name a few. Nonetheless, these developments are falling short of the demand in the overall scheme of display development [21]. Consumers are demanding a progressive and aggressive rollout for next generation flexible and transparent displays; The number of papers that introduce novel methods in producing high performance bendable devices has rapidly risen since the inception of TAOS materials [22] [23] [24]. Thus, realizing a low temperature annealing process is necessary for next generation, transparent, and flexible displays. This chapter focuses on exploring and observing the effects of using low temperature, low cost annealing techniques on vacuum processed films. Variations in the annealing temperature with respect to the annealing ambient were explored. Finally, annealing ambient candidates which exhibited the most promising results will be explored further with different characterization techniques in the proceeding chapter.

2.2 Low Temperature Annealing Processes for Flexible Device Applications

Currently, a-IGZO research has pushed the boundaries of low temperature annealing. Low temperature annealing methods have been researched and explored in literature such as: excimer laser annealing (ELA), high pressure water vapor annealing (HPWVA), flash lamp or microwave annealing, as well as changes to the post-annealing ambient [25] [26] [27] [28] [29] [30]. On top of the low temperature methods, low cost alternatives have also been proposed which focus on mid-process or post annealing ambients such as ultraviolet (UV,) ozone (O_3),

and wet ambient annealing environments [31] [32] [33]. Of particular interest in this work are the aforementioned low temperature and low-cost annealing methods as integrating these processes in existing industrial settings are economically favorable and relatively easier.

Ultraviolet annealing ambients have been shown to reduce the defects that are found in the channel of the device [33] [34]. Incident UV light may have enough energy to break existing metal-oxide (M-O) bonds. Channel defects and film quality can be improved by combining thermal annealing of the film whilst exposing it to UV light; Thus, lattice relaxation and reordering may happen. As for annealing in an O_3 rich atmosphere, the diffusivity of O_3 may help in passivating the defects and improving the overall quality of the film. It is believed that due to the higher oxidative effects of the O_3, the electrical characteristics of the film are improved by lowering the electron density (N_e) of the channel layer [31]. Wet annealing ambients also leverage on the diffusivity of water and hydroxide related elements in passivating defects whilst promoting thermal reorganization [35]. This may be attributed to the vital role of hydrogen (H) content in the channel layer by acting as effective passivator of subgap states or acts as a regulator of carrier density located in the channel layer of the device [36] [37]. In all of these annealing processes, the annealing ambients or conditions are added in conjunction with thermal annealing to maximize the effect of each condition on the quality of the film/device. It is important to note that in these annealing ambients, there is a delicate balance between passivating/removing defects and the electrical characteristics of the device. For instance, oxygen related defects can be reduced through wet annealing, but the presence of excess H_2O may lead to unwanted hydroxyl bonding [37].

2.3 Experimental Conditions

2.3.1 Device Annealing and Channel Activation

Freshly deposited films possess defects which can significantly limit the device performance and reliability. A myriad of papers have shown that annealing the device/channel layer during the device fabrication process can significantly affect its electrical characteristics [14] [38] [39] [40]. Low temperature techniques also focus on improvements to the channel layer of the TFT or the device as a whole [32] [33] [35] [36]. Thus, these works have coined the term "channel activation" which relates to improvements such as defect reduction in the channel layer which lead to the improvement of the electrical characteristics of the device. These improvements can be in the form of surface roughness reduction of the device through rapid thermal annealing (RTA) [38], or improvement of the oxide network through different annealing ambients [39]. Thus, channel activation can be interpreted as an annealing technique which utilizes a change in the annealing ambient or annealing conditions which promotes defect passivation. For low temperature processed devices, an interesting point that rarely gets raised is the timing of the process. To be more precise, timing refers to a particular step in the fabrication process wherein the low temperature annealing techniques can be introduced as seen in Fig. 2.2. It has been argued that defect passivation and improvement in the electrical characteristics of the device lies in the intermediary step prior to source/drain deposition [41]. In this work, channel activation happens immediately after the channel deposition and

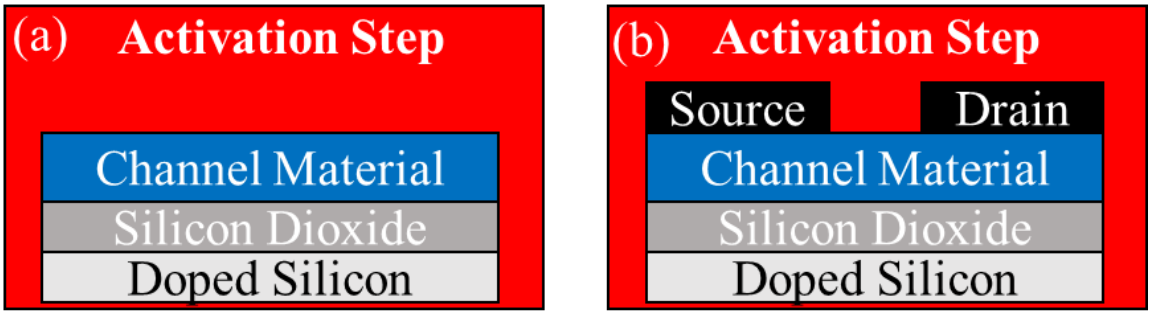

Figure 2.2 Channel activation of the films prior to (a) and after source/drain (b) deposition.

formation step. Further details regarding the channel activation step used in this work will be enumerated in the subsequent sections of this chapter.

2.3.2 Calculating Electrical Characteristics

Thin-film transistor devices are typically evaluated on 3 main criteria: the threshold voltage (V_{th}), the carrier mobility (μ), and subthreshold swing (S) [42]. The units of measurement for these criteria are in volts V, cm^2/Vs, and mV/decade respectively. V_{th} pertains to the 1 nA gate voltage (V_{gs}) measured across the source and drain of the device. Put simply, V_{th} represents the minimum voltage necessary to form a conductive channel at the interface of the dielectric and the semiconductor. The capacitance of the oxide gate insulator is represented by C_{ox} whilst the dimensions of the channel are in terms of its width (W) and length (L). In the saturation region of the device, wherein there is little change in the drain current I_{ds}, the saturation mobility μ_{sat} of the device can be extracted from the following equation:

$$I_{ds}{}^{1/2} = (V_{gs} - V_{th})\sqrt{\frac{W}{2L}\mu_{sat}C_{ox}} \tag{2.1}$$

The linear regime of the transfer characteristics where V_{ds} has a very low, non-zero value, enables the calculation of the linear field effect mobility (μ_{lin}). This value is extracted from an additional parameter called transconductance (g_m) which is the ratio of an infinitesimal change in output current versus a small change in the input voltage. A simple way of interpreting transconductance is that it is a measure of how much current can be produced when a certain V_{gs} is supplied. Thus, μ_{lin} can be obtained from the following equation at a certain drain voltage V_{ds}:

$$\mu_{lin} = g_m \frac{L}{WC_{ox}V_{ds}} \tag{2.2}$$

Finally, the *S* value can be extracted from taking the slope of the subthreshold/linear regime in the transfer characteristics of the device; it measures the inverse of the slope of the $I_{ds} - V_{gs}$. It can be interpreted as the smallest V_{gs} value required to turn on the device. The *S* value can also be used to measure the amount of interface traps between the semiconductor and the gate insulator layer. The absolute minimum *S* value for metal-insulator-semiconductor field effect transistors (MISFET) is 59.5 mV/decade at 300 K [42] [43]. Thus, the *S* measures how efficiently a TFT can change between on/off states and is represented by:

$$S = \left(\frac{d \log I_{ds}}{dV_{gs}}\right)^{-1} \tag{2.3}$$

All in all, these parameters give a robust picture of the performance of oxide TFT devices and are typically evaluated at these characteristics. Figure 2.3 shows an IGZO TFT with good electrical characteristics such as mobilities (μ_{lin}) higher than ~14 cm^2/Vs with a subthreshold swing (*S*) of ~440 mV/decade, and a threshold voltage (V_{th}) of approximately 4.68 V. Another

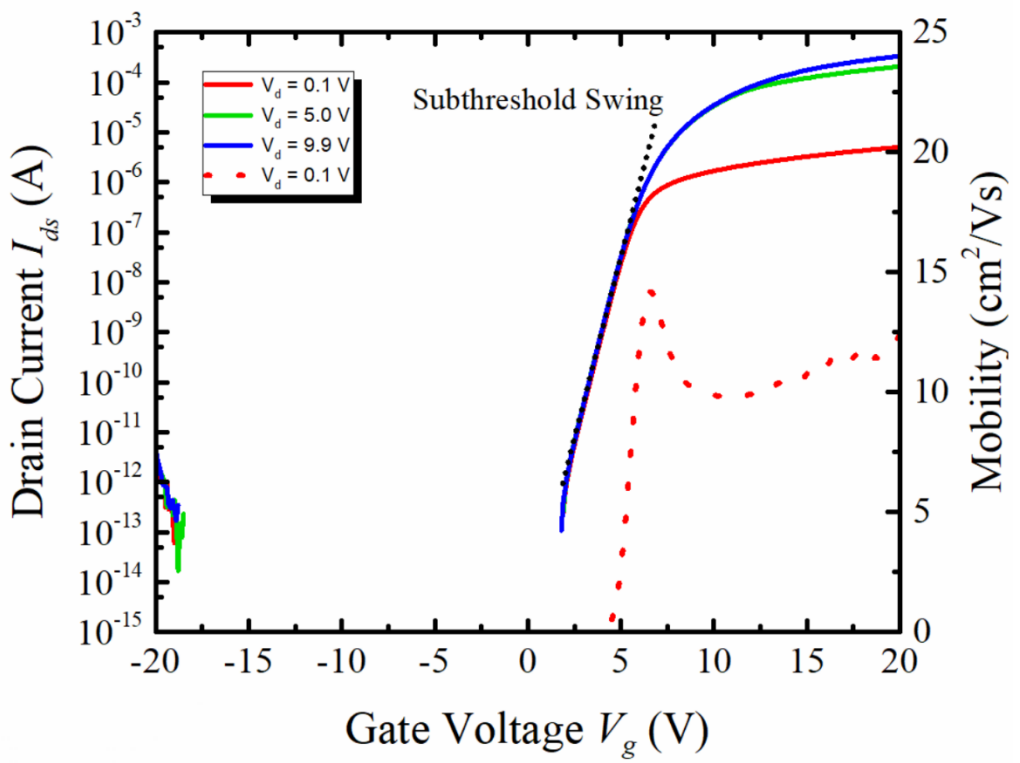

Figure 2.3 Transfer characteristics for a bottom gate, top contact IGZO TFT at different V_d. The dashed line denotes the mobility at V_d=0.1 V. Channel dimensions are W/L=90/10 µm.

parameter of note is the ratio of the on current (I_{on}) and off current (I_{off}), more commonly denoted as on/off current ($I_{on/off}$). More importantly, from a power consumption standpoint, the I_{off} is an indicator of the minimum power that the device will consume. It has been argued that the I_{off} is dictated by the following factors: a strongly localized valence band in oxide semiconductors, the formation of Schottky contacts at the source/drain contact points, and deep subgap density of states which are higher than the minimum value of the valence band [43] [44]. Figure 2.4 illustrates the output characteristics of the device mentioned earlier. Almost similar to the transfer characteristics in the earlier figure, the output characteristics have a small nonlinear section between the linear and saturation regions. Qualitatively, the slope of the linear region can provide vital information regarding certain device characteristics and defects: it can be an indicator of the contact resistance between the electrodes and the channel layer of the device, or the compatibility of the source/drain material with the semiconductor layer. A steeper slope for the linear region generally means a nominal value for the contact resistance, indicating a reduction in the resistivity between the source/drain and the channel layer of the device. Assuming work function compatibility between the source/drain and the channel

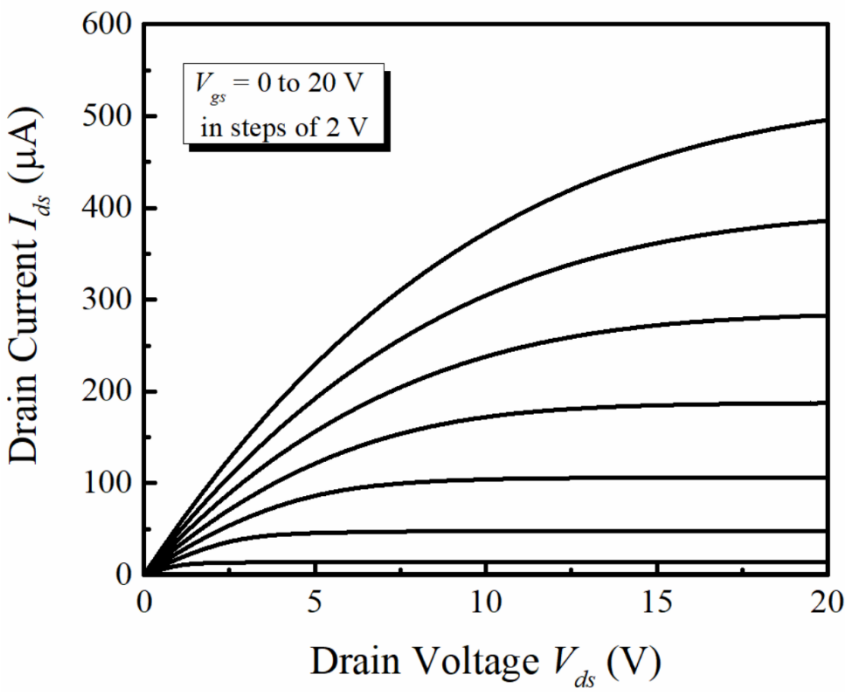

Figure 2.4 Output characteristics for a bottom gate, top contact IGZO TFT device.

material has been optimized, contact resistance can be reduced by performing post-metallization annealing (PMA), thus improving the bonding between the interfaces.

2.3.3 Device Fabrication Process

The device structure used in this experiment is a bottom gate, top contact (BGTC) TFT which is similar to Fig. 1.3. A quick fabrication process is illustrated in Fig. 2.5. A heavily doped n-type Si substrate with thermally oxidized SiO_2 possessing a thickness of 100 nm were used as the substrate and gate insulator respectively. Prior to deposition of the channel layer, the substrate was cleaned with a sulfuric peroxide mix (SPM) in an 80℃ hot bath to strip any remaining organic residue on the substrate. Afterwards, the substrates were washed in high purity water and blow dried with nitrogen gas (Fig. 2.5 (a)). Next, a-IGZO thin films were deposited at a nominal thickness of approximately 70 nm via radio frequency (RF) magnetron sputtering at room temperature. The target used has a target composition of In_2O_3:Ga_2O_3:ZnO = 1:1:1 and films were deposited at a pressure of 0.6 Pa at 100 W (Fig. 2.5 (b)). High purity argon was used as a sputtering gas with an oxygen partial pressure $O_2/(Ar+O_2)$ of 4.5%. To ensure film uniformity, pre-sputtering of the target was performed; the samples were rotated at

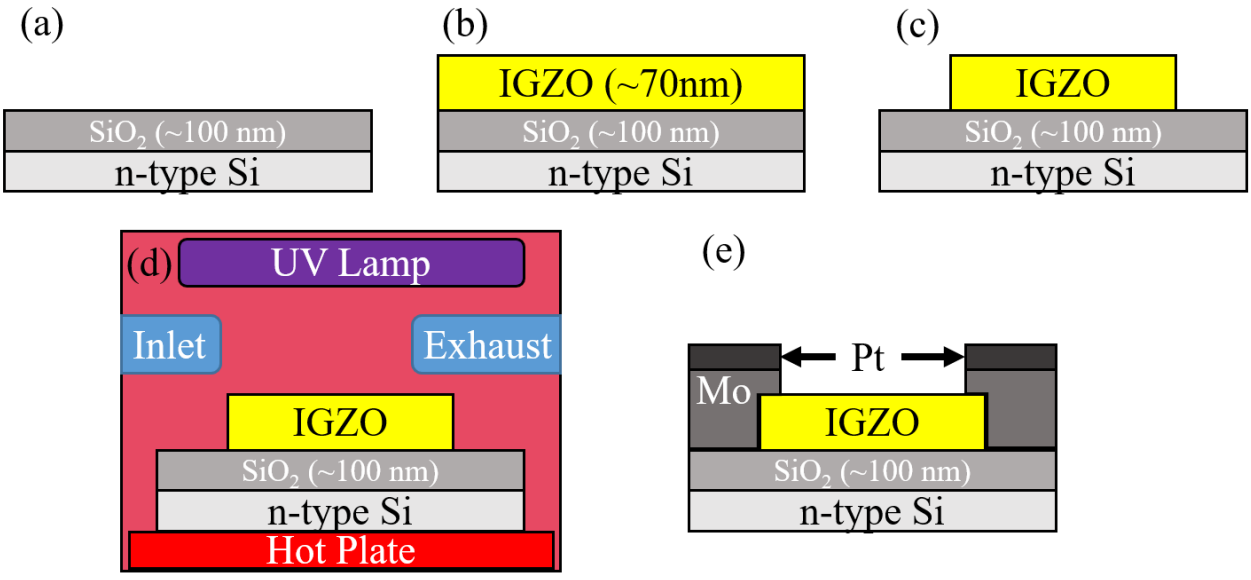

Figure 2.5 Condensed fabrication process for the devices fabricated in this chapter.

a speed of 5 rpm during deposition. Ultraviolet photolithography with the use of positive and negative resists were used to pattern the channel. Wet etching with 0.02 mol/L HCl was used to define the channel as illustrated in Fig. 2.5 (c). Prior to source and drain deposition, channel activation steps were performed in a SAMCO UV-1 UV/Ozone annealer (Fig. 2.5 (d)). Figure 2.6 illustrates a more detailed breakdown of the components of the annealer system which consists of: a silent discharge ozone generator, a built-in UV lamp which emits wavelengths at 185 nm & 254 nm, and a custom-built aerator which allows O_2 gas to pass through water before entering the annealing chamber. The different kinds of channel activation methods performed are classified into two categories: dry annealing ambients (UV, O_3, UV & O_3), and wet annealing ambients (Wet O_2, UV & Wet O_2). These ambients are achieve either by switch control or by introducing wet or humid air, otherwise known as wet O_2 (WO2). WO2 here relates to aerating high purity oxygen in high purity water before entering the annealing chamber at a flowrate of 0.5 L/min. For ozone generation, the aerator is not used to prevent any electrical short which may damage the system. Five annealing temperatures during the channel activation were explored in this experiment: 100℃, 150℃, 200℃, 250℃, and 290℃. The 290℃ maximum temperature is a device limit of the SAMCO UV-1 annealer. Patterned samples were placed inside the annealing chamber under the respective annealing ambients

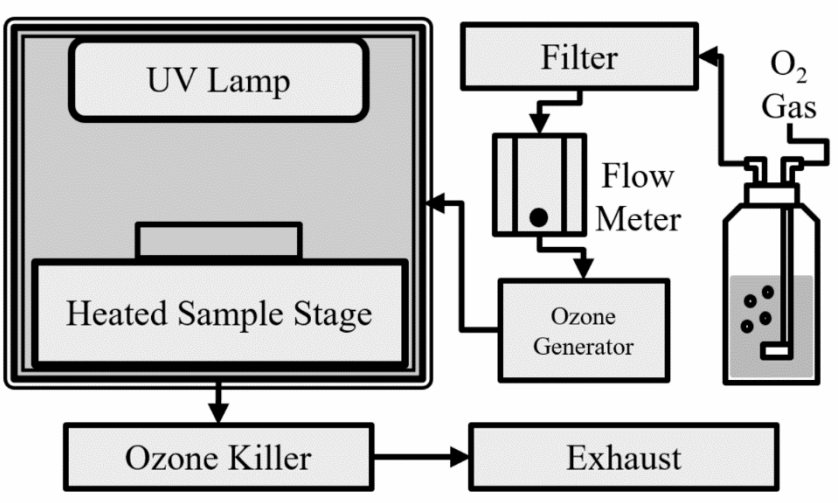

Figure 2.6 Detailed schematic of the annealer system used during channel activation.

and temperature was raised at a rate of 13 ℃/min until the desired temperature is reached. Afterwards, the samples are allowed to cool down to room temperature in the corresponding annealing ambients. Next, Molybdenum/Platinum source/drain electrodes with approximate thicknesses of 80/20 nm respectively were deposited by RF sputtering at a deposition pressure of 0.5 Pa and at an RF power of 100 W. Here, the samples are also rotated to ensure uniform film distribution along the surface of the samples. The source/drain electrodes are then patterned with the liftoff technique by submerging the samples in acetone, methanol, water, and then dried with nitrogen. Figure 2.5 (e) illustrates the finished device. To serve as an overarching baseline and point of comparison for the different annealing ambients, TFTs were fabricated similar to Fig. 2.5 without step d. Typical TFT devices in our group are annealed in atmospheric conditions after S/D deposition at 300℃ for 2 h to remove defects in the channel material, lessen the contact resistance between the channel/electrode interface, and have shown decent electrical characteristics [25] [26]. Electrical characteristics of the devices are measured using an Agilent 4156C Precision Semiconductor Parameter Analyzer. Measurements on the devices performed after 2 days show similar characteristics as long as the devices are stored in a nitrogen backfilled bag and kept in a humidity cabinet at room temperature. Measurements performed after 3 days show partial degradation with regard to the electrical characteristics of the devices. Thus, measurements of the devices are done immediately after device fabrication as the fabricated devices do not possess any passivation layer which can prevent the back channel from long term atmospheric affects during temporal measurements. At least 2 samples were made for each annealing condition and at least 6 devices were measured for each sample to give a qualitative and quantitative view on the effect of each annealing ambient.

2.4 Electrical Characteristics of Low Temperature Annealing Methods

Figure 2.7 shows the transfer characteristics of the dry annealed samples (UV, O_3, UV & O_3) show marked differences, especially in key aspects such as I_{on}, S, and V_{th}. For the dry annealing conditions, it can be observed that a UV annealing environment is insufficient at low temperatures (≤200°C) in producing a film with good characteristics. The same can be said for an O_3 annealing environment wherein high threshold voltages and low mobility are observed. This might be due to sub-gap traps formed by the excess oxygen aside from the suppression of oxygen vacancies which can reduce carrier concentration [31]. Among the dry annealing processes, the one which resulted with the best characteristics at 150°C was the UV & O3

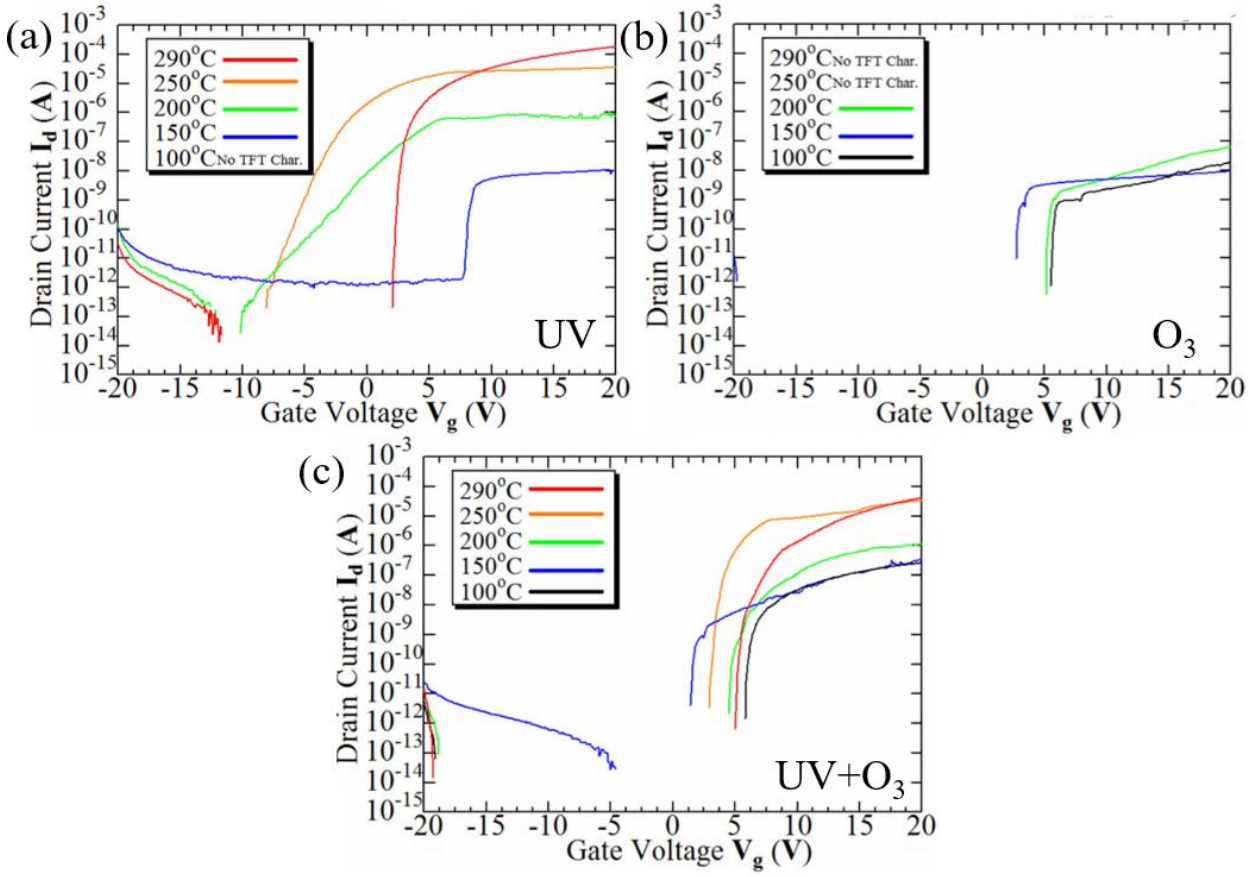

Figure 2.7 Transfer characteristics for the dry annealed devices at different annealing ambients: a) UV, b) O_3, c) UV + O_3 and at different annealing temperatures at V_d = 0.5 V & W/L = 90/10 µm.

annealing condition as seen in Tab. 2.2. 150℃ was chosen as the intention of this work is to eventually deposit TAOS on flexible substrates that have low thermal budgets. The dashed lines indicate that no device on any sample was found working for that particular annealing ambient. It is proposed that UV irradiation combined with ozone breaks down the gas into dioxygen and reactive oxygen; reactive oxygen can lessen oxygen vacancies in the film and may also reduce carbon residues on the surface. Also, the UV energies (185 nm : 6.7 eV | 254 nm : 4.8 eV) during the annealing process is greater than that of the metal-oxide (M-O) bonds in the a-IGZO film [45]. Likewise, UV irradiation in conjunction with thermal treatment may also help in the rearrangement of M-O bonds (InO: 1.7 eV, GaO: 2.0 eV, ZnO: 1.5 eV) [33] [46]. Thus, a combination of UV + O_3 with thermal annealing is necessary to not only simultaneously decompose existing bonds (UV) and reorganize the film (thermal annealing),

Table 2.6 Electrical characteristics of dry annealed samples with corresponding standard deviations. The units for μ, S, and V_{th} are cm^2/Vs, mV/dec, and V respectively.

Temp.	**UV**			**O_3**			**UV & O_3**		
	μ	S	V_{th}	μ	S	V_{th}	μ	S	V_{th}
100℃	-	-	-	0.03 ± 0.01	160 ± 39.1	16.6 ± 4.84	0.04 ± 0.01	160 ± 21.1	7.86 ± 1.41
150℃	0.01 ± 0.03	300 ± 12.2	8.02 ± 2.66	0.03 ± 0.01	160 ± 51.4	16.3 ± 4.23	0.36 ± 0.11	120 ± 13.5	6.24 ± 0.73
200℃	0.78 ± 0.26	360 ± 11.0	0.03 ± 0.01	0.02 ± 0.01	150 ± 50.2	12.0 ± 3.27	0.27 ± 0.09	180 ± 14.5	6.67 ± 1.82
250℃	2.54 ± 0.54	320 ± 11.3	-4.12 ± 1.43	-	-	-	7.28 ± 2.35	130 ± 12.3	3.59 ± 1.61
290℃	11.8 ± 2.75	106 ± 25.1	2.63 ± 0.67	-	-	-	4.91 ± 1.25	160 ± 11.4	6.09 ± 1.02

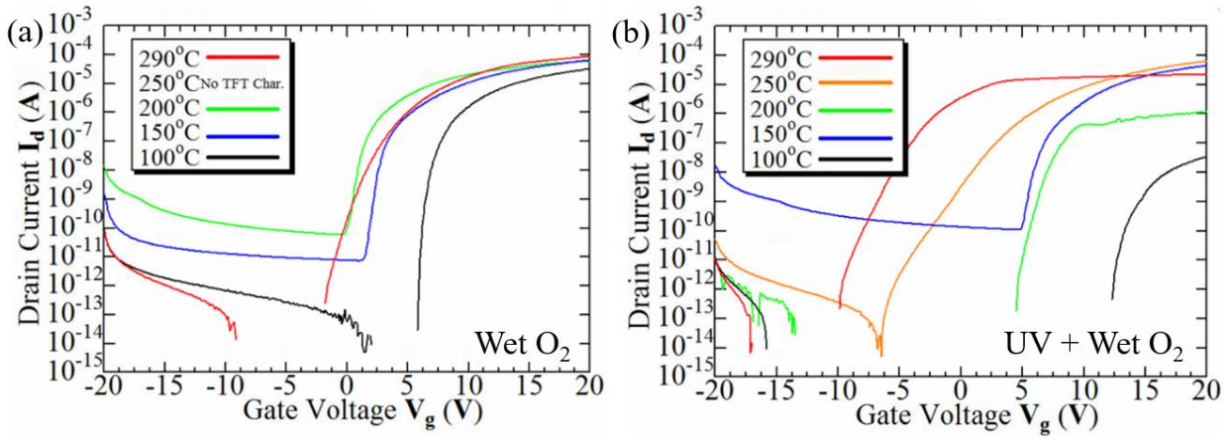

Figure 2.8 Transfer characteristics for the wet annealed devices at different annealing ambients: a) UV, b) O_3, c) UV + O_3 and at different annealing temperatures. Here, V_d = 0.5 V & W/L = 90/10 µm.

but to also help passivate defects such as oxygen vacancies that are present in the film (presence of O_3) aside from carbon contamination removal due to the oxygen radial. Annealing in either ambient alone – solely UV or O_3 – will be insufficient in passivating the defects found in the film [47]. The details of this channel activation mechanism will be discussed further in the next chapter. Figure 2.8 shows the transfer characteristics for the wet annealed devices at different annealing temperatures. For both wet annealing ambients, almost all devices exhibited switching characteristics and better overall $I_{on/off}$ ratios. Improvements the electrical

Table 2.1 Electrical characteristics of wet annealed samples with corresponding standard deviations. The units for μ, S, and V_{th} are cm^2/Vs, mV/dec, and V. *Annealed at 300°C.

Temp.	Wet O_2			UV + Wet O_2			Atmospheric Anneal		
	μ	S	V_{th}	μ	S	V_{th}	μ	S	V_{th}
100°C	2.92 ± 0.83	100 ± 28.8	7.84 ± 0.81	0.01 ± 0.01	200 ± 67.0	-5.62 ± 1.47	-	-	-
150°C	5.00 ± 0.44	390 ± 41.8	5.86 ± 0.61	3.22 ± 0.39	320 ± 74.1	2.55 ± 0.55	2.36 ± 0.13	130 ± 13.1	4.05 ± 0.91
200°C	2.91 ± 0.67	350 ± 78.6	0.85 ± 0.24	4.70 ± 1.22	110 ± 31.5	6.93 ± 1.23	-	-	-
250°C	-	-	-	4.72	390	4.58	-	-	-

characteristics of the devices may be attributed to the ability of water vapor to have higher reported diffusivity and oxidizing values versus O_2 gas [32] [42] [48] [49]. Thus, it is expected that wet annealing ambients play a role in improving the electrical characteristics of the device and the effect of this is more pronounced at lower annealing temperatures. Again, based on Tab. 2.3 and by looking at 150°C annealing temperature, the wet annealed devices have respectable electrical characteristics especially when compared to devices annealed in an atmospheric ambient at the same temperature. The disparity in the electrical performance is even more glaring when comparing between dry and wet annealing ambient results at an annealing temperature of 150°C. From these results, it can be gleaned that wet annealing ambients are more effective in passivating the inherent defects in the TAOS film versus the dry annealing ambients. As such, it becomes quintessential to perform film characterization in relation to the annealing ambients and the electrical characteristics of the device.

2.5 Conclusions

There is an active drive in display technology research groups to push for depositing TFT devices on flexible substrates. Due to preexisting defects in the channel layer of these devices, annealing is performed to improve the reliability and performance of the devices. These bendable substrates have lower thermal budgets compared to their glass or silicon counterparts. Therefore, low temperature and low-cost alternatives can greatly usher in these next generation transparent displays. Alternatives to low temperature processing used in this work can be broadly classified between dry and wet annealing ambients as a means of improving the channel material in the TFTs.

Research on low temperature channel activation methods have shown that the timing of the method in relation to the device fabrication process has an impact on the performance of the device. Devices in this work were subjected to channel activation prior to source/drain

deposition to maximize the effect of each annealing condition. The annealing ambients used in this work are all done in conjunction with thermal annealing at different temperatures to find the lowest annealing temperature that would give respectable electrical characteristics. These patterned films are exposed to: ultraviolet light (UV), ozone via a silent discharge (O_3), a combination of UV + O_3, wet O_2 annealing, and a combination of UV + wet O_2.

The results show that for different annealing conditions, devices generally exhibit switching behavior. For the purpose of depositing on flexible substrates with low thermal budgets, at a temperature of 150℃, wet annealing ambients have better electrical characteristics than dry annealing ambients. The results show that among all the annealing conditions, wet O2 might be the best candidate as a low temperature, low cost annealing process with a mobility of 5.00 cm^2/Vs and an S of 390 mV/dec. Despite this, further characterization tests should be performed to isolate and understand the effect of the annealing ambients. Thus, in the next chapter, film characterization techniques such as depth profile X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectrometry (SIMS) are done in conjunction with the associated electrical characteristics to understand the improvement mechanism. The top 3 annealing ambients (UV + O_3, Wet O_2, UV + Wet O_2) will be analyzed in the next chapter under these parameters.

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Chapter 3 | A Comparative Study Between Dry and Wet Ambient Annealing Environments

3.1 Introduction

Research has shown that differences in the annealing environment can affect the performance of TFTs. The ambient annealing environment can affect the device characteristics by densifying films, improving surface morphology, passivating defects, or acting as donors that can help in providing free charge carriers during device operation [1] [2] [3]. In the previous chapter, two annealing ambients were explored: wet, and dry ambient environments. Wet annealing ambients refer to high purity oxygen which is aerated through high purity water and is then fed through the annealing chamber before exiting through the exhaust [4]. The patterned films are placed in the chamber and are annealed in respective annealing ambients before source/drain deposition. The results from electrical measurements in the previous chapter indicate that specific annealing ambients – whether wet or dry ambient – may activate the channel layer of the IGZO TFT devices leading to switching behavior. Unfortunately, only specific annealing ambients result in devices with decent electrical characteristics especially at 150℃. Thus, this chapter is dedicated to understanding the improvement mechanism of three annealing ambients for vacuum processed IGZO films: UV & O_3, Wet O_2, UV & Wet O_2. With the use of film characterization techniques such as X-ray photoelectron spectroscopy (XPS), and secondary ion mass spectrometry (SIMS) in relation to the electrical characteristics of the devices annealed at 150℃, a clearer picture can be established regarding the mechanisms that govern the improvement or deterioration of the films under each annealing ambient.

3.2 Low Temperature (150°C) Annealing Ambients

Table 3.1 Summary of electrical characteristics for different annealing ambients.

Ambient Condition	**Annealing Condition**	**Temperature (°C)**	**μ (cm2/Vs)**	**S (mV/dec)**	**V_{th} (V)**
Dry Ambient	*AT300	300	13.4 ± 0.83	110 ± 64.2	3.76 ± 0.54
	*AT150	150	2.36 ± 0.13	130 ± 13.1	4.05 ± 0.91
	UV & O3	150	0.36 ± 0.11	120 ± 13.5	6.24 ± 0.73
Wet Ambient	Wet O2	150	5.00 ± 0.44	390 ± 41.8	5.86 ± 0.61
	UV & Wet O2	150	3.22 ± 0.39	320 ± 74.1	2.55 ± 0.55

Table 3.1 summarizes the electrical characteristics of devices that were annealed in dry and wet ambient conditions. The raw electrical characteristics were recorded by measuring numerous devices on at least 2 samples per annealing condition to account for the yield coupled with the corresponding standard deviation of the data. The measurements with asterisks (*) are devices that were subjected to post metallization annealing (PMA) in atmospheric conditions for 2 hours. The AT300 samples were annealed at a temperature of 300°C by following the optimized high temperature fabrication process for IGZO TFTs [5] [6]. The AT150 sample serve as a point of comparison for devices manufactured using the standard high temperature process. These measurements were included in this table to serve as a baseline for devices annealed at elevated temperatures and devices that follow the high temperature process. The rest of the devices are annealed for a total of 30 minutes in their respective annealing

conditions. The saturation mobility μ is calculated from I_{ds} located in the saturated regime at V_{ds} = 5 V [7] [8] [9].

The AT300 sample exhibits good characteristics with a mobility, subthreshold swing, and threshold voltage of 13.4 cm^2/Vs, ~110 mV/dec, and 3.76 V respectively. These characteristics fall well within the reported characteristics of IGZO devices annealed in atmospheric conditions [6] [10] [11]. As for the AT150 devices, it can be observed that there is a clear deterioration in the electrical characteristics of the device. Aside from the electrical characteristics, despite exhibiting switching behavior, the curves for the dry annealed devices exhibit hump like characteristics which may be accredited to the low annealing temperature thus resulting in an incompletely formed oxide network or long range ion migration [12] [13]. Figure 3.1 illustrates the transfer curves for the different annealing ambients. It can also be observed that there is also a different with regard to the I_{on} for the wet annealed devices. The

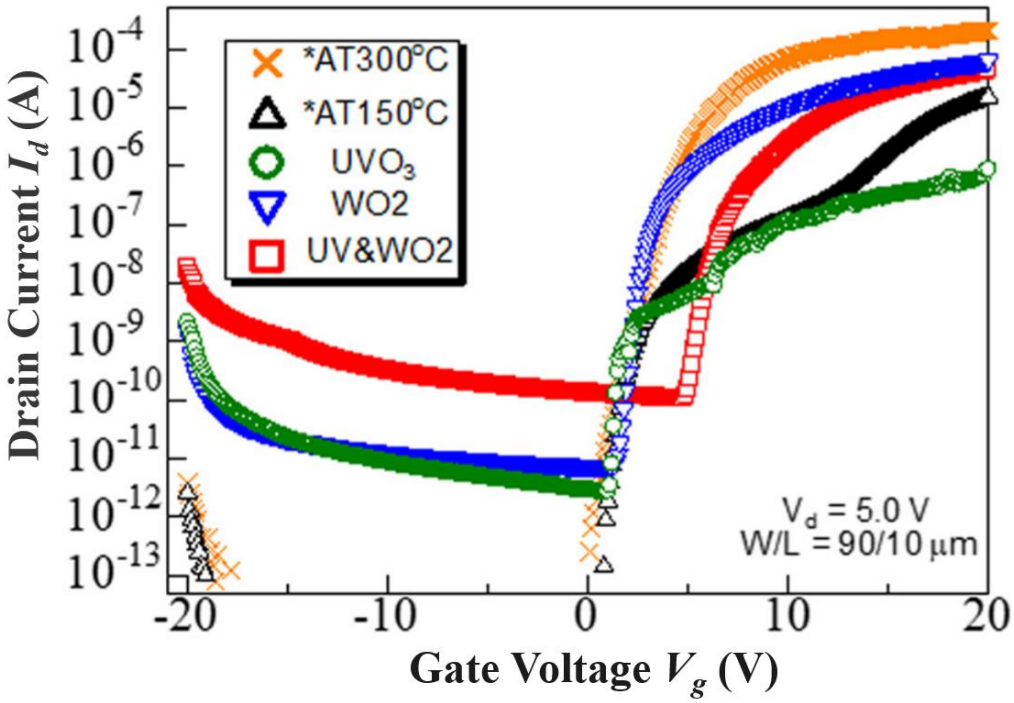

Figure 3.7 Transfer characteristics for 5 different annealing conditions.

improvement of the electrical characteristics for the wet annealed devices may be attributed to defect passivation and a better oxide network owing to the diffusivity of H_2O into the channel

layer of the film [14] [15] [16] [17]. As for the I_{off} being slightly higher for the wet annealed devices, this may be due to the excess incorporation of hydrogen, oxygen, or hydroxide related species. Research has shown that an excess amount of hydroxide-related species that diffuses into the film may deteriorate electrical characteristics such as I_{off} by behaving as deep level, acceptor like traps which hinder charge conduction [8] [15] [18]. As for the UV & O_3 devices, the calculated mobilities are lower as there still might be defects present in the channel layer as evidenced by the transfer characteristics exhibiting hump like defects. The annealing time during channel activation may also play a part in this marked decrease in the performance as an annealing time of 30 minutes might be insufficient in passivating these defects. Research has shown that prolonging the annealing times, even at low annealing temperatures, can significantly decrease the defects as well as improve the overall quality of the film (roughness, density, etc.) leading to a good device [19] [20] [21]. For the wet annealed devices, the higher *S* value may be related to the higher concentration of hydroxyl traps which act as bulk trap density sites due to the nature of wet annealing ambients [18] [22]. As for the variations in the threshold voltage of the devices, this may be attributed to the humid annealing environment which may affect the semiconductor/gate dielectric interface, an increase in deep charged defects in the film, or insufficient anneal times [18] [23] [24].

3.3 Film Characterization Techniques

To further understand the effects of the annealing ambients on the electrical characteristics of the devices, characterization techniques were performed to check for any difference in the elemental composition in the film as well as the state of the oxide network when compared to a film fabricated without channel layer activation. Secondary ion mass spectrometry (SIMS) is a powerful analytical technique which provides high sensitivity and decent depth resolution by using a beam of high energy primary ions which sputter the sample surface. This, in turn,

produces ionized secondary particles which can be detected by a mass spectrometer [25] [26]. As such, it can be a powerful tool which can provide elemental information for films, and even liquid samples [27]. In line with this, it is also important to look at the effects of the annealing ambients on the oxide network of the devices. Small variations (~5-10%) in the oxide network can have drastic effects on the electrical characteristics of the device [8] [19] [28] [29]. X-ray photoelectron spectroscopy (XPS) allows the measurement and analysis of the chemical elements and the oxygen bonding behavior on the surface of the film [30]. Angle resolved XPS (AR-XPS) gives a more detailed view of the shallow surface (top layer to ~ 5 nm) of the film whilst depth profile XPS (DP-XPS) takes the idea further by sputtering a certain thickness of the film away, revealing a deeper layer which can be measured and analyzed. In effect, a quantitative way of gathering information on the bulk of the film in relation to its oxide network can be obtained and analyzed. IGZO thin films were sputtered on to Si/SiO_2 substrates which were cleaned in the same manner as section 2.3.3. These films were then subject to channel activation (UV & O_3, Wet O_2, UV & Wet O_2) and were then loaded into the corresponding analytical equipment (SIMS/XPS) on the same day of fabrication to avoid contamination and unwanted external effects. To serve as a point of comparison to the other channel activation methods, an as-deposited IGZO sample was made. The average thickness of these films is 70.7 ± 1.30 nm and were measured by a Horiba Jobin Yvon UVISEL spectroscopic ellipsometer after SIMS/XPS measurements. For the XPS measurements, AR-XPS was first done as this is a nondestructive analytical method compared to DP-XPS which involves sputtering the film layer by layer.

3.3.1 Secondary Ion Mass Spectrometry Analysis

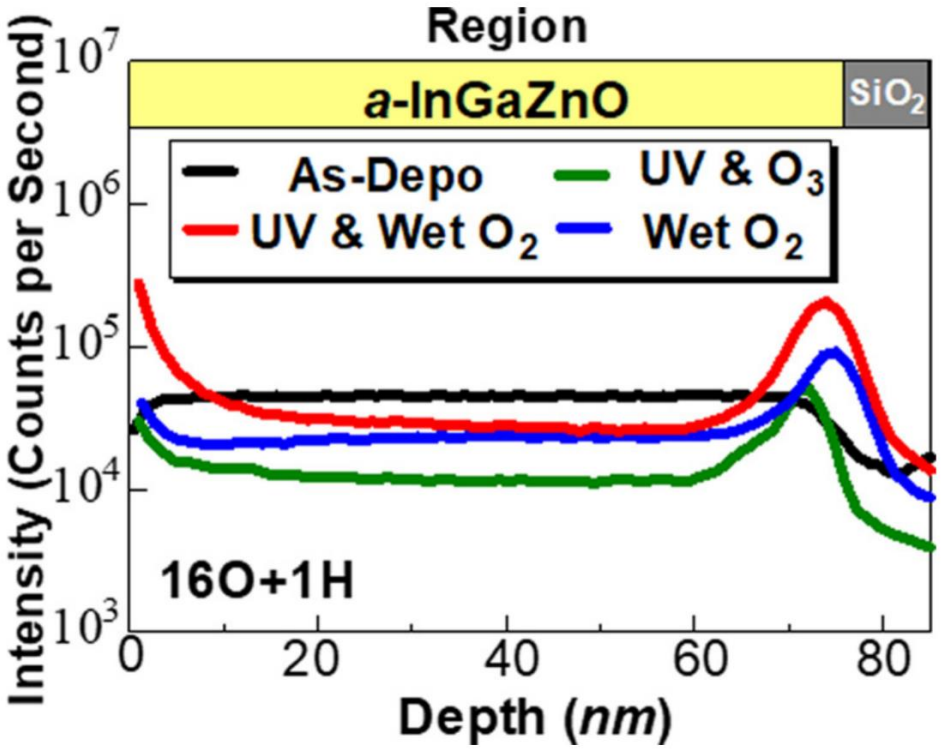

Figure 3.2 Secondary ion mass spectrometry (SIMS) data for hydroxide species (16O + 1H) for As-Depo, UV & O3, Wet O2, UV & Wet O2 samples.

Data gathered from the SIMS measurement was obtained by sputtering up to until the semiconductor/gate insulator interface of the films. A ULVAC-PHI ADEPT-1010 Dynamic SIMS machine was used with the following parameters: a cesium gun was used with an aperture of 50 mm and an irradation current of 50 nA. From the electrical measurements of each annealing condition, the one that showed the best characteristics were the Wet O_2 samples. The other annealing ambients either hand poor electrical characteristics (UV & O3) or did not have the best values for mobility (UV & Wet O_2). The results from the SIMS measurements indicate that there is an optimum concentration of hydroxide and hydrogen related species that should be present in the film [18] [31]. Wet ambient, low temperature annealing atmospheres have been shown to inhibit the outward diffusion and passivation of oxygen related defects as seen in Fig. 3.2 [14] [18] [32]. Thus, for the films annealed in wet ambient environments, despite the diffusion like behavior of the hydroxide related species out of the film, the bulk of the films themselves exhibit higher – OH content compared to the UV & O_3 film.

Figure 3.3 shows that the UV & Wet O_2 film has hydrogen content comparable to the As-deposited film. The UV & Wet O_2 sample also has the highest –OH content amongst all the other samples despite having decent relative electrical properties. This can be due to the findings that UV light has the ability to reorganize the M-O bonds in the channel layer coupled with the high diffusivity and surface reactivity of H_2O [18] [31]. It has been shown that excess absorption of hydroxide related groups and H_2O may lead to the formation of hydroxyl traps. These traps can hinder mobility as well as induce higher I_{off} as seen in the electrical characteristics of the UV & Wet O_2 devices. It can even be argued that ion migration may have influenced the amount of hydrogen at the semiconductor/gate insulator interface due to the combined effect of UV and diffusivity of H_2O for the UV & Wet O_2 sample [33]. Again, similar with the 16O + 1H data, there seems to be an optimum amount of hydrogen content in the films as the samples lowest amount of hydrogen exhibited better electrical characteristics than the dry ambient samples annealed at the similar temperature of 150°C. Thus, these results

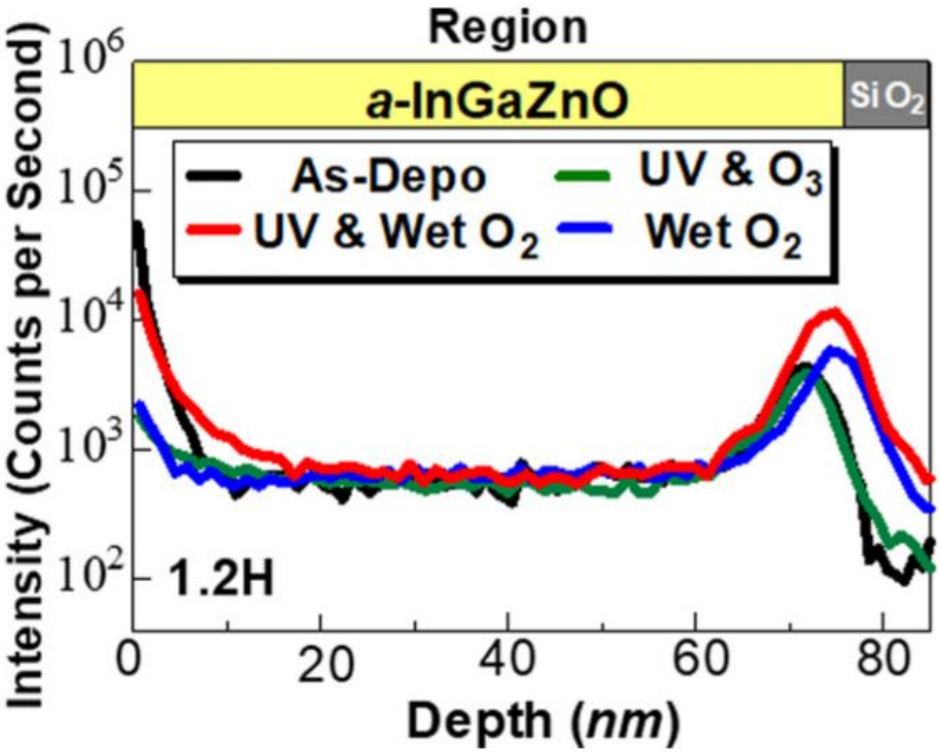

Figure 3.3 Secondary ion mass spectrometry (SIMS) data for hydrogen species (1.2H) for As-Depo, UV & O3, Wet O2, UV & Wet O2 samples.

tie in to the results from the electrical characteristics of the devices. Nonetheless, XPS analyses should be performed to confirm any changes in the oxide network of the devices in relation to their corresponding annealing ambients.

3.3.2 Angle Resolved and Depth Profile X-Ray Photoelectron Spectroscopy Analysis

To analyze the effects of the annealing ambients on the oxide network at the surface and the bulk of the channel, angle resolved (AR-XPS) and depth profile XPS (DP-XPS) were performed. A ULVAC-PHI PHI 5000 Versa Probe II XPS system was used to take measurements of the films using angle resolved and depth profile modes. Narrow and wide scan measurements were performed for both measurement modes. The carbon (C1s) components for all the curves were calibrated at a binding energy of 284.8 eV and deconvolutions of the curves were performed with Casa XPS software. To gain a better picture as to the effects of each annealing ambient on the oxide network, the oxygen (O1s) components were decomposed into three Gaussian-Lorentzian fitting curves at a full width at half maximum (FWHM) of 1.4. The three deconvoluted curves for all the measurements correspond to the oxygen species in metal-oxygen (M-O; 530. ± 0.1 eV), oxygen deficient bonding sites otherwise called oxygen vacancies (M-V_o; 531.2 ± 0.1 eV, and the oxygen species related with the hydroxide or carbon content in the film (M-OH/C; 532.0 ± 0.1 eV). The FWHM and binding energy constraints enable a consistent and quantitative analysis of the oxide network in the film in relation to the effects of the chosen annealing ambients.

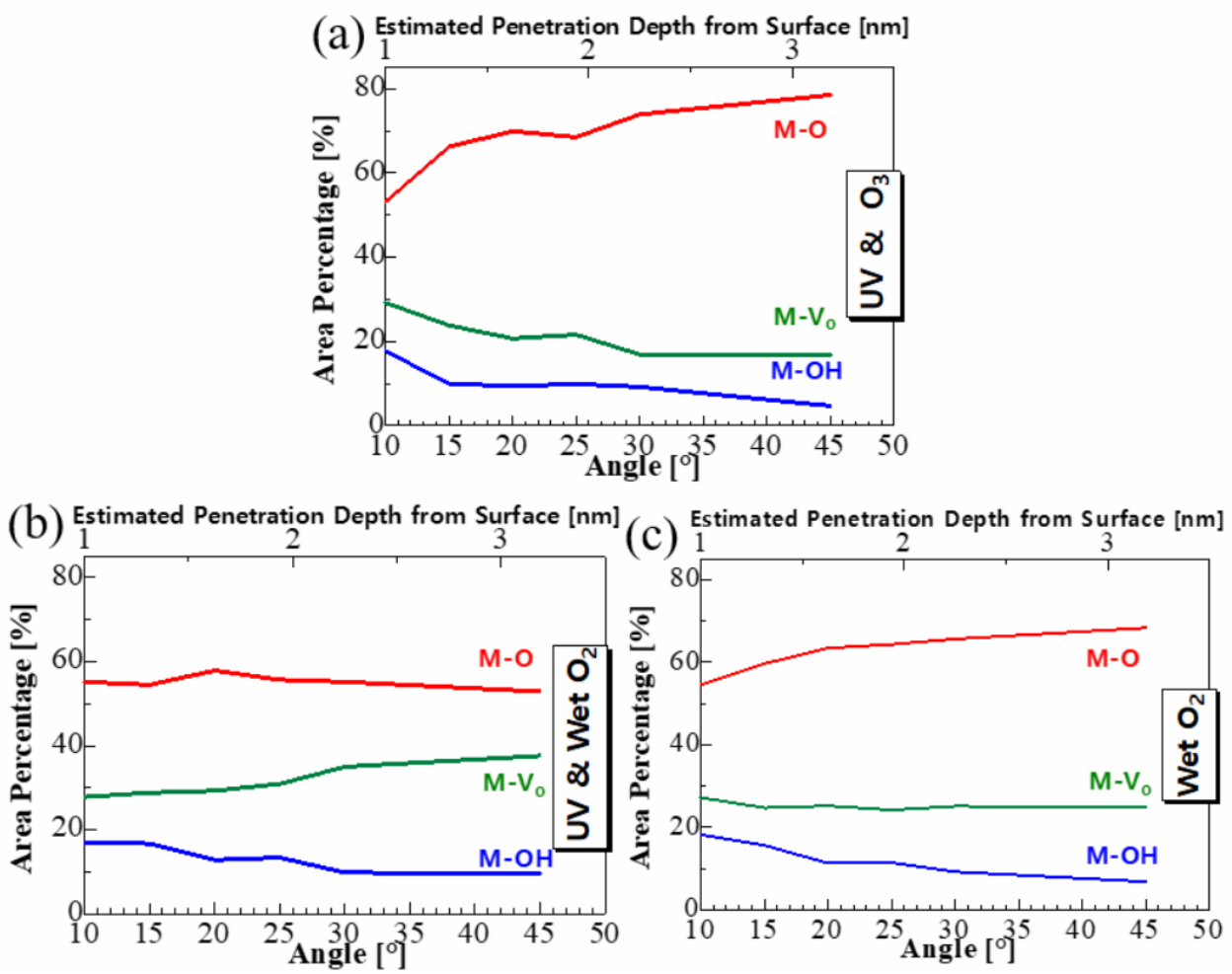

Figure 3.4 O1s angle resolved XPS measurements for samples annealed in dry (UV & O_3) and wet (UV & Wet O_2, Wet O_2,) annealing ambients.

The AR-XPS measurements can measure up until a depth of 3 nm from the surface of the film. A lower angle closer to 0^o means the detector is at an angle which is perpendicular to the surface of the film being analyzed. As seen in Fig. 3.4, the AR-XPS data shows that just underneath the surface of the film, there is generally a higher M-OH concentration for the wet annealing ambients which persist to just beneath the surface of the film. As for the dry annealing condition (UV & O_3), higher M-O bonds are found with lower oxygen vacancies up until approximately 3 nm into the film, which exhibit a marked difference when compared to its wet annealing counterpart. This may be explained by the ability of UV light to break existing M-O bonds and in conjunction with the thermal annealing and the presence of oxygen radicals, defects are passivated and the quality of the film is improved [19] [34] [35] [36]. Thus, close

to the surface of the film, the dry annealing ambient is effective in increasing the M-O oxide network, which can lessen contact resistance and decrease the number of defects found in the back channel of the device. The DP-XPS results, however, tell a different story and gives a more holistic view of the effects of each annealing ambient on the bulk of the film itself. Figure 3.5 shows that from the surface up until an approximate depth of 24 nm from the back channel, the wet ambient annealed films exhibit higher M-O, and lower M-V_o concentrations compared to the AD and UV & O_3 samples. It can be observed from the data that the wet ambient annealed films had a noticeable impact on the oxide network and the bonding states versus the dry ambient annealing. Table 3.2 summarizes the percentages of each of the annealing ambients located in the bulk of the film. Compared to the as-deposited (AD) film, the wet annealing

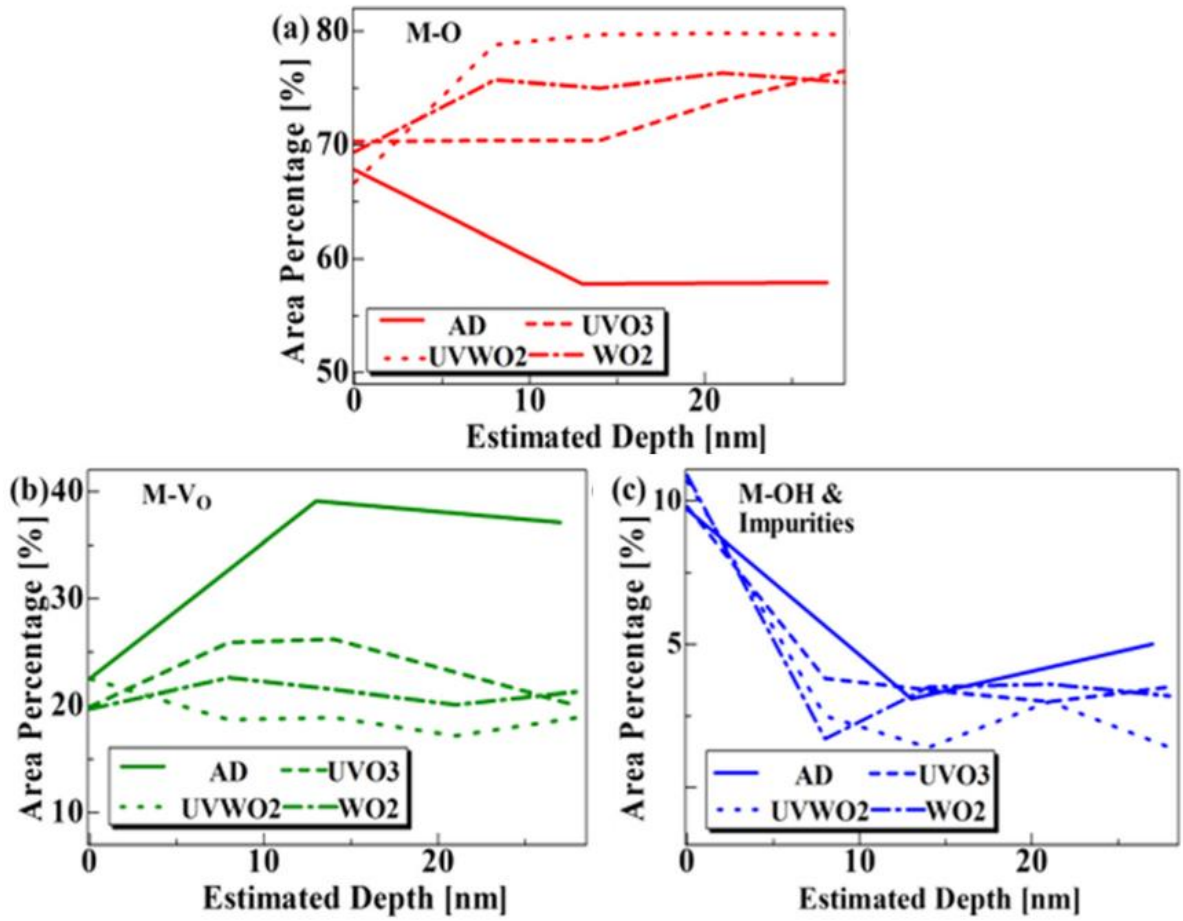

Figure 3.5 Depth profile XPS O1s contribution ratios from the integrated intensities related to a) M-O, b) M-V_o, and c) M-OH/C. AD refers to an as-deposited IGZO sample.

ambients have significantly higher M-O percentages even when compared to the UV & O_3 film. These variations in the M-O concentration, even small changes in the percentage of the bonding states, can greatly influence the electrical characteristics of the film and the device [32] [37] [38] [39] [40]. For the UV & WO_2 films, despite having the lowest oxygen vacancies and the highest metal-oxide concentrations, as observed in the SIMS data, the increase in hydroxyl bonding due to the presence of water, UV light, and thermal annealing can hamper the mobilities of the devices and also increase the I_{off} [15] [41] [42] [43]. With the more substantial results from the DP-XPS data, it can be concluded that wet ambient annealing environments are more effective in reducing oxygen vacancies aside from improving the M-O oxide network of the film. This net improvement in the oxide network improve the electrical characteristics of the device by providing a better percolation path and reducing the electron trap sites in the channel layer of the device [32] [44] [45] [46]. The combined results of the electrical characteristics, SIMS, and XPS show that for wet ambient annealed devices, there is a net positive effect on the devices, provided that the amount of hydroxide related elements diffusing into the film is regulated.

Table 3.2 Contribution ratio of the integrated intensities for the O1s peak related to M-O, $M\text{-}V_o$, M-OH/C located in the bulk (~20-30 nm) of the film.

Annealing Ambient	**M-O (%)**	**$M\text{-}V_o$ (%)**	**M-OH/C (%)**
UV & Wet O2	79.7	18.9	1.4
Wet O2	75.5	21.3	3.2
UV & O3	68.9	28.6	2.8
As-Deposited	57.9	37.1	5.0

3.4 Improvement Mechanism for Dry and Wet Annealing Ambients

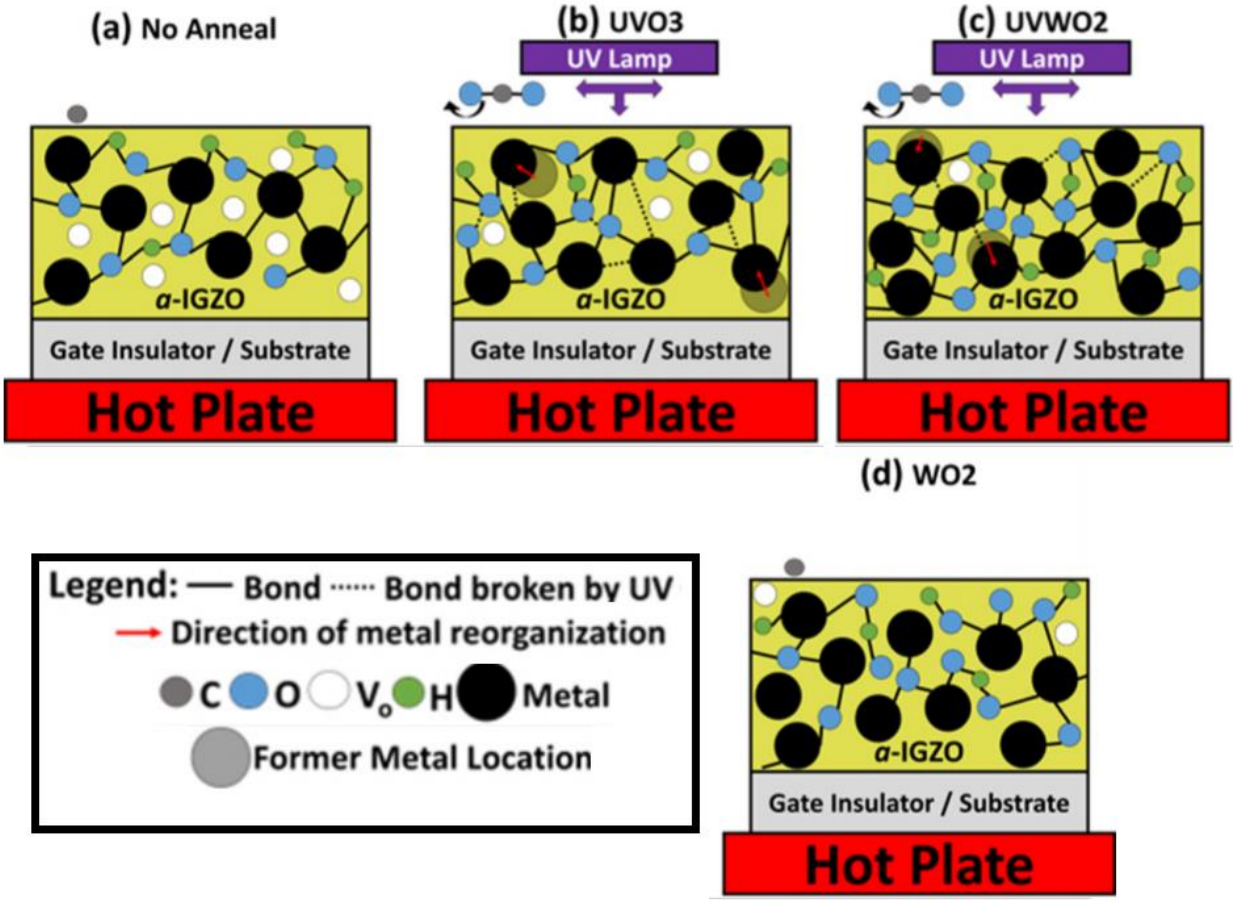

Figure 3.6 The different mechanisms that affect the channel layer for (a) a sample that was not annealed, (b) a UV & O_3, (c) UV & Wet O_2, and (d) Wet O_2 annealed sample.

As discussed earlier in this work, sputtered films have intrinsic defects such as interstitial cations, vacancies, and stresses in the channel layer of the device [11] [47] [48] [49]. Similarly, the surface of the films may also have carbon residues which may adversely affect the performance of the film. Figure 3.6(a) illustrates the condition of the unannealed film. Thus, thermal annealing should be done to improve the quality of the film. Based on the results from the SIMS and XPS data that was gathered, for the UV & O_3 dry ambient annealing condition, the thermal annealing, in combination with the UV light and the O_3, oxygen vacancies are passivated, carbon residues are removed, and reorganization occurs due to bond breakage and thermal reordering as seen in Fig. 3.6(b) [32]. Also, in the presence of the UV light, the O_3

undergoes the following reaction due to photodissociation (Eq. 3.1-3.3) which enhances the passivation of oxygen related defects and the removal of carbon impurities on the surface of the film:

$$O_3 + h\upsilon\ (254\ nm) \rightarrow O_2 + O^* \tag{3.1}$$

$$O_2 + h\upsilon\ (185\ nm) \rightarrow O + O \tag{3.2}$$

$$O_2 + O \rightarrow O_3 \tag{3.3}$$

$$O^* + H_2O \rightarrow 2OH \cdot \tag{3.4}$$

For the wet annealing ambients, specifically the UV & Wet O_2 annealing ambient, the mechanism is almost similar, but oxygen vacancies are then occupied by either oxygen, hydrogen, or hydroxide species as seen in the SIMS data (Eq. 3.4). Due to the UV light, the content of hydroxide related elements are higher. The effect of this can be seen in the electrical characteristics of the device as the H_2O may have had an effect in the formation of hydroxyl trap sites [46]. Thus, with the XPS data on top of the SIMS data, the UV light and the wet ambient annealing condition passivated M-V_o sites and increased the M-O percentage. As was mentioned earlier, research has shown that the amount of hydroxyl content in oxide films may result in the worsening of the mobility and higher I_{off} which accounts for the electrical characteristics of the UV & Wet O_2 devices. [50] [51] [52] [53]. As for the last annealing ambient, as seen in the XPS data, the Wet O_2 condition aids in suppressing the outward diffusion of oxygen related species in the film. Also, because of the high diffusivity and mobility of water vapor in oxide materials such as IGZO and ZnO, wet ambients have higher M-O networks than dry ambient annealing conditions [31] [54]. Without the presence of UV light, there is an overall reduction in electron traps present in the film as the Wet O_2 annealed devices have the best mobility when compared to other low temperature annealing processes.

3.5 Conclusions

This chapter focused on analyzing the effects of dry and wet annealing ambients on devices which were annealed at a temperature of 150°C. Compared to a device which was annealed in atmospheric conditions, the wet ambient annealed devices exhibited better transfer characteristics. Thus, further analysis was necessary to understand the effect of each annealing condition. Secondary ion mass spectrometry measurements show that wet annealing ambients help in suppressing the removal of hydroxide and oxygen related elements in the channel layer of the device. X-ray photoelectron spectroscopy results show that wet annealing ambients enhance the oxide network in the films by passivating oxygen related defects and improving the overall metal-oxide composition in the films. In this regard, wet annealing ambients improve the percolation path for charge carriers by improving the quality of the oxide network.

With these results, the next chapter will focus on applying low temperature wet annealing ambient conditions to solution processed films. Analytical techniques will also be performed to verify if any changes to the improvement mechanism proposed in this chapter will change due to the transition from vacuum to solution processed films.

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Chapter 4 | Low Temperature Wet Annealed Ambients for Solution Processed Oxide TFTs

4.1 Introduction

The previous two chapters investigated low temperature annealing methods and the results narrowed down the annealing conditions to one: wet annealing ambients. For vacuum processed IGZO films, wet annealing ambients were shown to reduce defects found in the film, to improve the oxide network, and remove impurities found on the film due to the oxidizing power of water vapor [1] [2]. For the Wet O_2 annealed devices, the electric characteristics for a 30-minute, 150°C annealed sample exhibited the highest mobility of 5.00 cm^2/Vs. Comparing this to atmospherically annealed devices for 2 hours with a mobility of 2.36 cm^2/Vs, clearly at low temperatures, a wet annealing ambient which uses only a Wet O_2 ambient while annealing is preferred versus the dry annealed devices that were investigated in previous chapters.

As mentioned in the first chapter of this work, studies have steadily risen with regard to display technology research, to transition from vacuum processed to solution processed manufacturing techniques [3] [4] [5]. Thus, by verifying and analyzing the effects of the annealing ambient on vacuum processed IGZO films, these annealing methods can then be extended to solution processed films such as IZO solutions. The IZO solutions used in this work are sourced from the industry collaborators – Nissan Chemical Corporation – that the researchers are working with. Also, the allure of using solutions is the ability to easily dope the solution with additional elements other than Gallium which can enhance the electrical properties of the device. Therefore, in this chapter, the Wet O_2 annealing ambient was used as a channel activation process. Despite the change in deposition method, it is expected that the Wet O_2 annealing will be able to improve the film, and consequently the electrical

characteristics of the device [2]. The films are made through spin coating a solution of TAOS material on the substrate. Due to the nature of solution processing and the film formation process, it is first important to determine the absolute lowest temperature that the film can be formed with minimal amount of precursor left in the solution. Afterwards, different analytical techniques will be used to characterize the quality of the films in relation the electrical characteristics of the devices. Further details regarding this endeavor will be discussed in the subsequent sections.

Table 4.1 Electrical characteristics for solution processed TAOS TFTs. [6]

*Vacuum processed device mentioned earlier in this work.

Material	**Temperature (°C)**	μ **(cm^2/Vs)**	V_{th} **(V)**	S **(mV/dec)**
IZO	220	2.43	1.51	560
	280	4.85	1.17	770
IGZO	220	1.81	4.86	630
	250	3.13	4.74	690
ZTO	220	0.85	12.3	720
	250	2.88	5.18	840
IGZO*	300	13.4	3.76	110

4.2 Current Status of Solution Processed Thin-film Transistors

Solution processed techniques in relation to TFT devices have been gaining traction due to the promise of eliminating the use of high vacuum equipment. Transparent amorphous oxide semiconductors are expected to be better than their low temperature poly-silicon (LTPS) counterparts due to their ability to exhibit semiconducting properties despite their amorphous nature [7] [8]. Thus, using TAOS materials with solution processed techniques are expected to be the next generation in manufacturing TFT devices. Unfortunately, just like any technology

in its early stages of development, the current challenges in solution processed TFTs prevent them from being fully launched into the market [6]. These challenges, however, come hand in hand as the technology of solution processed TFTs is relatively still in its infancy compared to its vacuum processed counterparts. There have been great strides in improving the performance of solution processed devices, with a particular emphasis on the mobility of the device [9]. Table 4.1 lists electrical characteristics for different solution processed TAOS materials. Early forays into solution processed organic TFTs presented mobilities in the range of ~0.1 – 0.2 cm^2/Vs [10]. It can be observed that vacuum processed devices still possess excellent mobilities and subthreshold swing values when compared to solution processed devices but despite this, the characteristics for solution processed have greatly improved over the past two decades. The solutions used for fabricating TFT devices are typically composed of salt or metal precursors that are dissolved in solvents and that typically contain stabilizers. Research has shown that introducing dopants, changes in the gate insulator, or improvements in the deposition process can greatly improve the electrical characteristics of the solution processed devices [11] [12] [13]. Typically, during the film deposition process, the solution is deposited on a substrate then soft baking/pre-annealing is performed to remove most of the solvent. Afterwards, the substrate is post-annealed at a typically higher temperature to promote oxide formation and to further improve the quality of the film. Figure 4.1 illustrates the aforementioned film deposition process through spray coating. There are also different deposition methods in fabricating the films: spin coating, ultrasonic spray deposition, inkjet printing, and electrospray coating to name a few [14, 15, 16, 17, 18]. Stabilizers help keep the morphology of the film smooth during

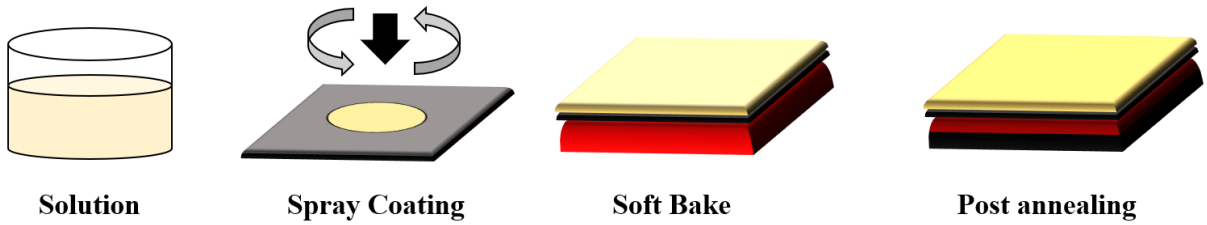

Figure 4.1 Typical film deposition process for solution-based films.

the deposition and annealing processes. Without the presence of stabilizers, rough film morphologies can affect important parameters such as contact resistance, $I_{on/off}$ ratios, and the overall electric characteristics of the device [19] [20].

4.3 Experimental Conditions

The NX-7001 solution used in this experiment is provided for by Nissan Chemical Corporation and are derived from Zinc and Indium metal salts with a formadide stabilizer [21]. Simultaneous thermogravimetric analysis and differential scanning calorimetry was performed with a Hitachi Hitachi DSC7000X/STA7200. Multiple measurements, aside from measurements made by Nissan Chemical Corporation were performed. For film fabrication, substrates were cleaned in a manner similar to the cleaning process mentioned in chapter 2: substrates are cleaned in a sulfuric peroxide mix to remove organic layers that may be present on the surface. The hydrophilicity of these substrates was further improved by exposing them to UV/O_3 by using a SAMCO UV-1 tabletop cleaner. The NX-7001 solution was then spin coated on the substrates at a relative humidity of 60-70%; each layer undergoes a 2-step baking procedure [21]. Keeping the humidity at this range ensures that the films have a small variation in terms of thickness as research has shown that different levels of humidity can affect the film thickness [22] [23]. As mentioned in the previous section, this 2-step baking process is important in removing the solvent and to form the oxide film. Each layer ranges from approximately 12-16 nm. After depositing 5 layers, the film is annealed for 1 hour as a calcination step. For the device fabrication process, UV photolithography and wet etching were done to pattern the film. Channel layer activation for 1 hour was performed and grouped into two categories: samples annealed in 250℃ atmosphere (250ATM), and samples annealed in 250℃ Wet O_2 ambient (250WO2). Afterwards, molybdenum/platinum source/drain electrodes with corresponding thicknesses of 80 nm/20 nm were deposited via RF sputtering. Further

patterning was done with the lift-off technique. A reference sample (300ATM) was made without channel activation. Finally, all the devices are subjected to post metallization annealing (PMA) and divided into 2 groups: 250ATM and 250WO2 devices were annealed for 2 hours at a maximum process temperature of 250℃ whilst 300ATM was annealed for the same duration but at a higher temperature of 300℃. PMA is done in atmospheric conditions at a N_2:O_2 ratio of 4:1. For the devices, the substrates are heavily doped silicon substrates with thermally oxidized SiO2 with an approximate thickness of 100 nm. Films for the characterization measurements are deposited on silicon substrates. The subsequent sections will discuss film characterization measurements according to each annealing condition.

4.4 Evaluation of Solution Processed Films

Analytical techniques are used to determine the effect of the annealing ambient on the film. To determine the lowest temperature possible to anneal the film with channel activation techniques, TG-DTA experiments were redone and coordinated with Nissan Chemical Corporation to ascertain the lowest temperature possible with little to no solvent. Afterwards, the effects of the annealing ambients on the surface of the film, as well as information on the bulk of the film were obtained by performing atomic force microscopy (AFM), grazing incidence X-ray diffraction (GI-XRD), and scanning transmission electron microscopy (STEM). The STEM samples were prepared through ion milling by using focused ion beam (FIB) preparation methods. To check for any changes in the elemental composition and the oxide network of the films subjected to Wet O_2 annealing ambients, secondary ion mass spectrometry (SIMS), and X-ray photoelectron spectroscopy (XPS) measurements were done. Finally, electrical characteristics and negative bias stress (NBS) tests of the devices were done with a Agilent 4156C semiconductor parameter analyzer to tie in all the information in relation to Wet O_2 annealing versus atmospheric annealing. NBS stress tests were performed to see the

effect of Wet O_2 annealing on the reliability of the device when subjected to a constant load over a period of time.

4.4.1 TG-DTA

Thermogravimetry-differential thermal analysis (TG-DTA) is used to evaluate parameters such as pyrolysis, dehydration, and solvent evaporation of certain materials. Figure 4.2 shows the TG-DTA data for the NX-7001 IZO solution used in this experiment which is similar to the data obtained by Nissan [21]. It can be observed that much of the solution happens at temperatures below 100°C, indicating an endothermic reaction as the temperature is increased. At temperatures >100°C, alloying, precursor decomposition, and possible dihydroxylation happens especially in the region of 233 to 244°C. It can be argued, as the data shows, for an IZO film to form with little to no solvent, precursor, or other impurities, the annealing temperatures must exceed at least 244°C. As evidenced in the TG-DTA data, temperatures lower than 244°C, let alone lower than 100°C will result in films that contain the water-based solvent, the nitrates which are derived from the precursor, aside from a film with a partially

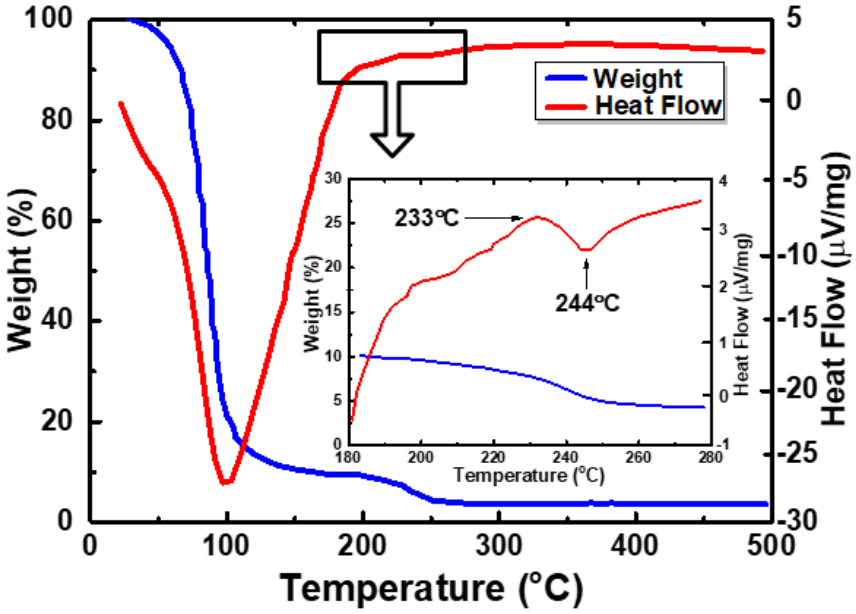

Figure 4.2 TG-DTA data for the IZO solution showing weight loss and heat flow as a function of temperature. The inset shows the region between 180°C and 280°C.

formed oxide network. Various papers have shown that solvent residuals or improper annealing temperatures can lead to significant deterioration to the electrical characteristics of the device [6] [24]. Thus, the lowest annealing temperature chosen for this experiment is 250℃.

4.4.2 Atomic Force Microscopy, X-Ray Diffraction, and Scanning transmission Electron Microscopy Analysis

Research has shown that smoother surfaces have an appreciable effect on the film quality and device performance [25] [26] [27]. Figure 4.3 shows the AFM images scanned from a 10 x 10 µm2 area of the 250ATM, 250WO2, and 300ATM films. These films were deposited on silicon substrates and subjected to their respective annealing conditions. The root mean square roughness (R_q) values are 0.28 nm, 0.23 nm, and 0.41 nm respectively. These values fall within reported measurements for solution processed IZO films annealed at 300℃ It can be observed

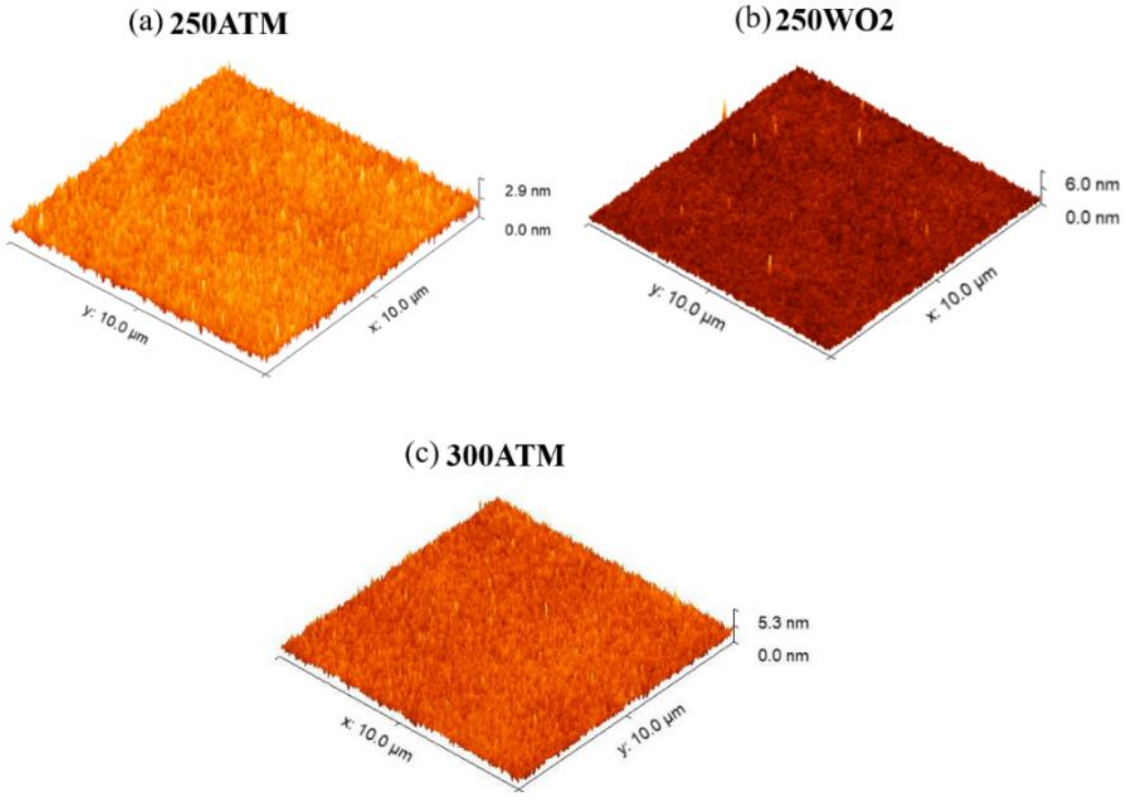

Figure 4.3 AFM images of the surface of IZO thin films annealed in 250ATM, 250WO2, & 300ATM conditions. R_q values are calculated from the arithmetical mean deviation of a measure group of data.

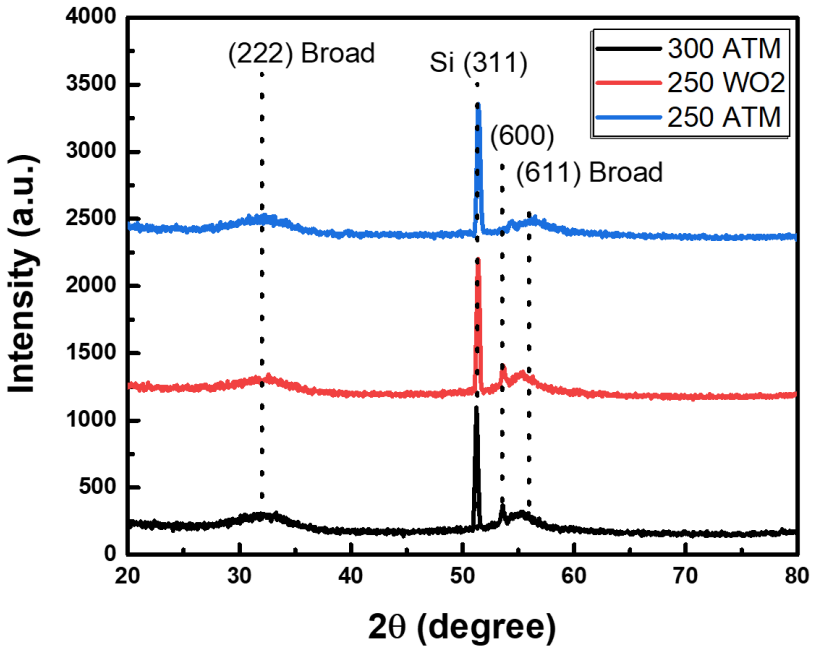

Figure 4.4 Grazing incidence X-ray diffraction data for the different annealing ambients with Indium peaks at different crystal orientations. Grazing angle is ω = 0.5°.

that the R_q values for the 250°C annealed samples are smoother compared to the 300ATM film. This may be due to the relatively higher annealing temperature which leads to the formation of large clusters due to agglomeration of the grains in the film [28] [29] [30]. On the other hand, it is interesting to note that the surface of the 250WO2 has regions that exhibit features that appear to be nanorods despite the relatively low value for R_q whereas the 250ATM film surface exhibits a more uniform surface. This surface feature may play an important role related to the electrical characteristics of the TFT. Figure 4.4 shows the grazing incidence x-ray diffraction data with respect to the three annealing conditions for indium peaks taken from the JCPDS card 76-0152; a sharp peak at 51° is the intensity contribution from the substrate [31]. The data shows that for all films, most of the film is amorphous in nature as indicated by the broad peaks centered at approximately 32° and 55°. For the 250ATM sample it can be observed that the indium peaks for the 600 and 611 orientation have shifted at higher 2θ angles. This may be due to a number of factors due to remaining solvents which may act as Frenkel defects in the film or, an imperfectly formed oxide network which causes tensile stress in the film, thus shifting

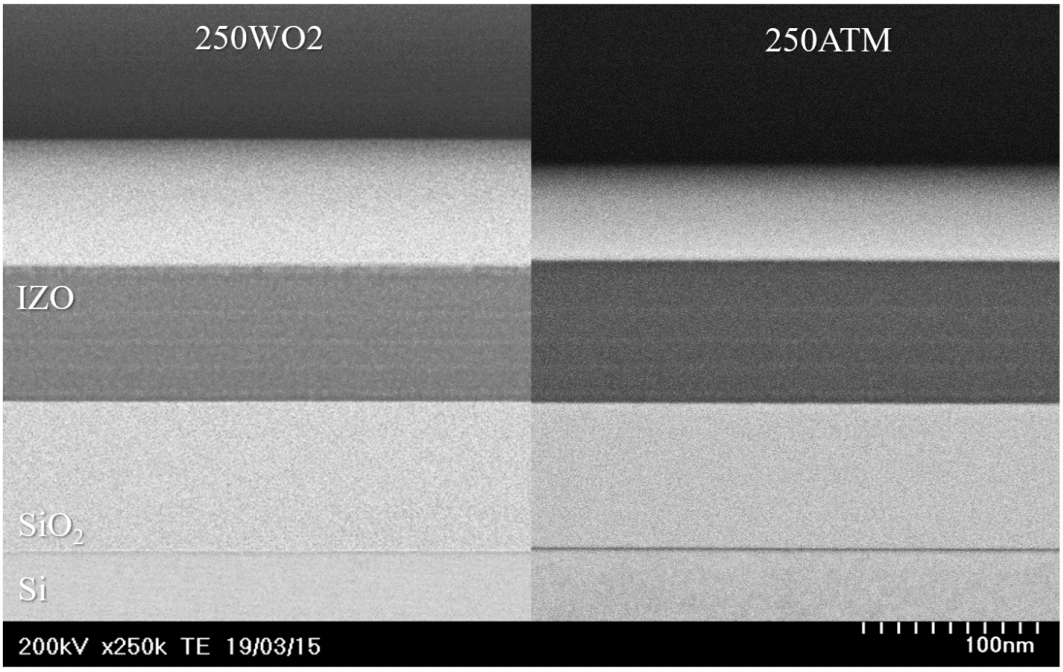

Figure 4.5 STEM images of 250WO2 and 250ATM samples deposited on a Si/SiO_2 substrate.

the peaks at a higher angle [32]. It can also be observed that for the 250WO2 and 300ATM sample, a small peak indicating partial crystallization happens at 53^o at the 600 orientation whilst a slight discernible blip can be seen for the 250ATM sample. This implies that the nanorods observed earlier for the 250WO2 sample may be possible locations where grain agglomeration happens or where crystallites form, thus possibly partially increasing the crystallinity of the film. Research has shown that improvements in the crystallinity of the film can improve the electrical characteristics of the TFT device by [33] [34] [35]. Thus, a partial increase in the crystallinity of the film on top of the relative smoothness of the 250WO2 annealed film may improve the electrical characteristics of the Wet O_2 annealed devices. To check this further, some samples were investigated with the use of a Hitachi HD-2700 scanning transmission electron microscope (STEM). A five-layer film was deposited on a Si/SiO_2 substrate according to the same fabrication process mentioned earlier. To observe cross sectional areas of the films, the sample must be prepared via ion milling with a Hitachi focused ion beam (FIB) FB2200 machine which mills and shapes the sample with a Ga ion source. Figure 4.5 shows the STEM micrographs for the 250WO2 and 250ATM sample. It can be

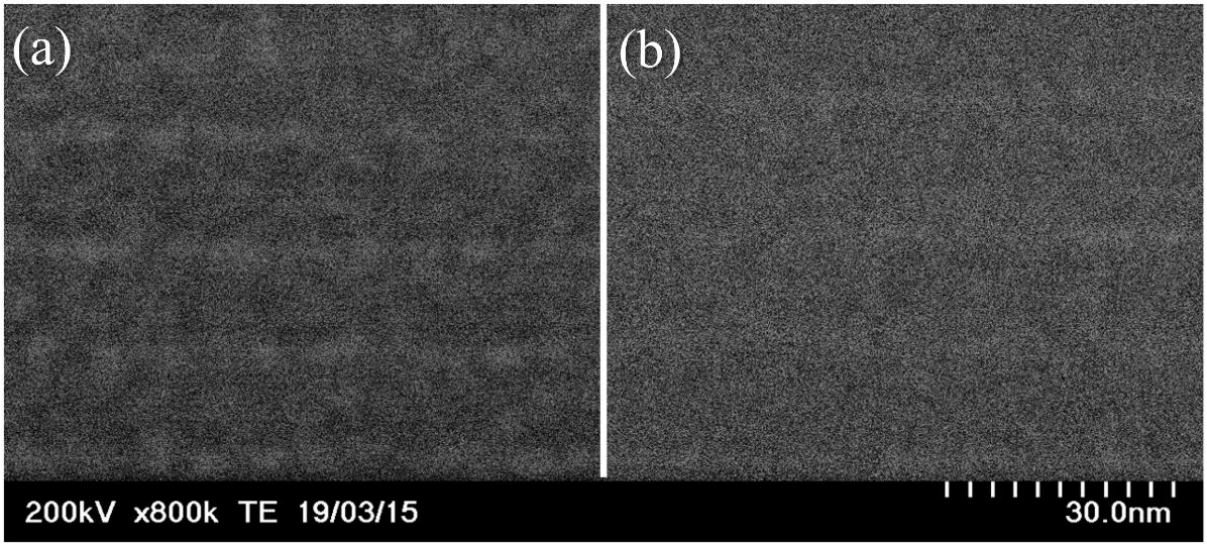

Figure 4.6 Enhanced contrast STEM images of a) 250WO2 and b) 250ATM films.

observed that the 250WO2 sample exhibits bright spots/locations that is atypical of a 100% amorphous film. By adjusting the contrast of localized areas in the IZO films, these features become more prominent (Fig. 4.6). This implies that the 250WO2 wet ambient annealing method can help promote grain agglomeration in the film by reducing intergrain transport, a factor that inhibits mobility in the devices due to the grain boundaries/amorphous nature of the film which has been shown in previous experimental and theoretical research [36] [37]. Thus, it is expected that the electrical characteristics of the 250WO2 devices will be better than the 250ATM devices.

4.4.3 SIMS and XPS Analysis

To further understand the effects of the annealing ambients (Wet O_2, and atmospheric) on the devices, secondary ion mass spectrometry (SIMS) and X-ray photoelectron spectroscopy (XPS) were performed to analyze the elemental composition and oxide network of the films. The nitrogen species were obtained as the precursor of the NX-7001 solution is nitrate based. The data shows that for the 250WO2 films, the –OH content is almost similar to that of the 300ATM samples. As stated in the earlier chapter, for shorter anneal times, wet annealing

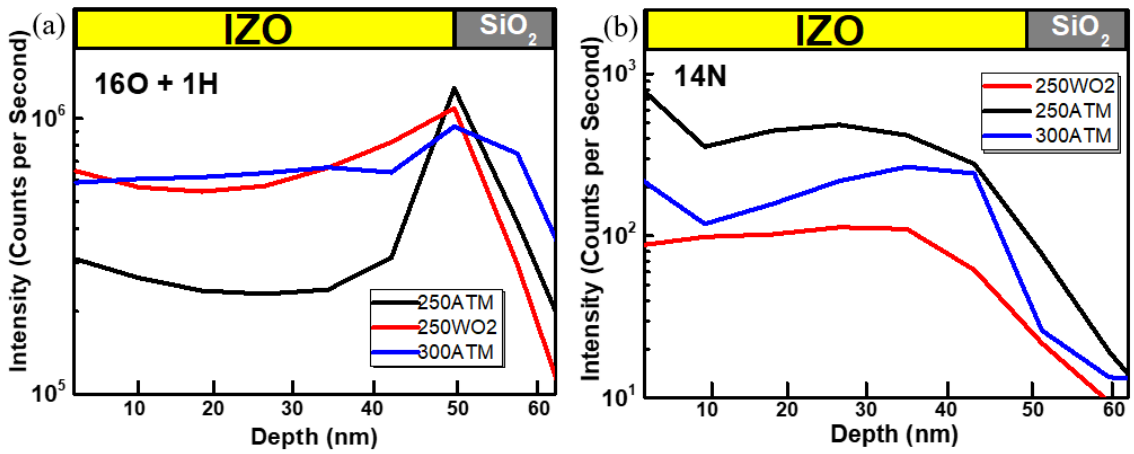

Figure 4.7 SIMS data for 16O + 1H and 14N species for the different samples.

ambients can mitigate the desorption of oxygen and hydrogen related species aside from passivate defects that are found in the film. For the 250ATM sample, although small, there is a noticeable decrease in the –OH content due to the outward diffusion during annealing. Figure 4.7 shows the SIMS data for the 16O + 1H and 14N species in the film. The nitrogen content in the 250WO2 films also exhibit the lowest amount and may be attributed to the surface reactivity and diffusion of water vapor into the film which may remove any residual nitrogen that came from the precursor due to the low annealing temperature. These factors are also expected to affect the electrical characteristics of the devices, which will be presented in the next section. The XPS measurements in figure 8 for the solution processed IZO films also show

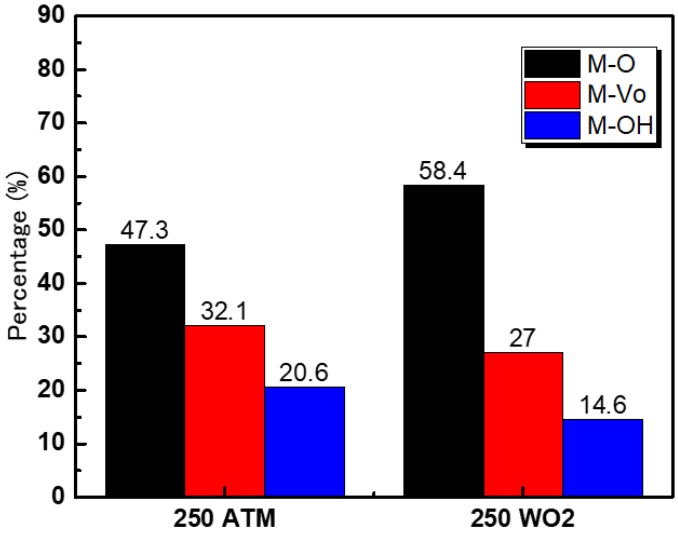

Figure 4.8 XPS contribution ratios from the integrated intensities related to M-O, M-V_o, and M-OH/C.

similar trends that were observed for the vacuum processed IGZO films for the Wet O_2 annealing condition. The M-O (530.0 ± 0.1 eV), M-V_o (531.2 ± 0.1 eV), and M-OH/C (532.0 ± 0.1 eV) analyzed and fitted with the same parameters in the previous chapter. The data shows that there is a clear difference in terms of the quality of the oxide network for the 250ATM sample versus the 250WO2 sample. These results are consistent and in agreement with our previous work as to the effects of dry versus wet ambient annealing conditions [2]. The overall improvement in the oxide network of the 250WO2 films can again be attributed to the characteristic of wet annealing ambients to passivate oxygen vacancies in the film, reduce trap sites, and an increase in the M-O network thus promoting a better percolation path for electrons.

4.5 Electrical Characteristics of the Devices

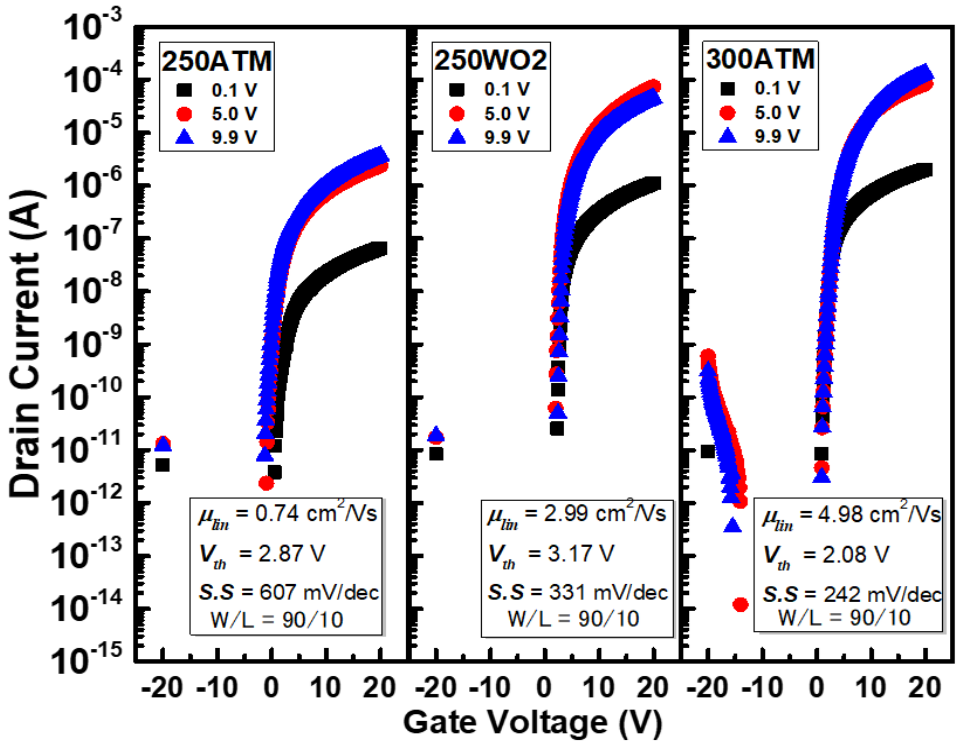

Figure 4.9 Transfer curves for devices with channel layer activation under a) atmospheric, b) Wet O2, and c) no channel activation.

Figure 4.9 illustrates the electrical characteristics of the devices annealed at a maximum process temperature of 250℃. A standard sample annealed at 300℃ is also presented as a point

of reference. Although the 250WO2 devices have lower mobilities compared to the 300ATM devices, the electrical characteristics of the 250WO2 devices are very different and significantly better than the 250ATM devices. An important observation here is that the maximum field effect mobility for the 250WO2 annealed devices is roughly 4 times higher than the 250ATM devices as well as a higher $I_{on/off}$ ratio compared to the 300ATM device. Thus, the results from the analytical measurements performed on the films which indicate that the 250WO2 annealed film has a better quality than the 250ATM films are very apparent. Table 4.2 details the electrical characteristics for the Wet O_2 versus atmospheric annealing conditions for the 2 annealing temperatures. The fabrication process for annealing at 300℃ has already been optimized for the 300ATM devices, which explains the overall better characteristics of the devices. Nonetheless, by comparing the devices annealed at 250℃, annealing in Wet O_2 conditions has a considerable effect on the electrical characteristics of the devices when compared to the 250ATM annealing condition.

Table 4.2 Summary of electrical characteristics for the WO2 and ATM annealing condition. *Here the drain voltage V_d = 0.1 V.

Sample	μ **(cm^2/Vs)**	V_{th} **(V)**	***S.S. (mV/dec)***
250ATM	0.47 ± 0.29	4.52 ± 1.81	510 ± 172
250WO2	1.98 ± 0.37	3.28 ± 0.23	330 ± 120
300ATM	4.79 ± 0.44	2.98 ± 1.77	161 ± 51

To also check the effect of the wet annealing ambient on the stability of the device, negative bias stress (NBS) tests were performed. The NBS stress tests were performed by applying a constant voltage at the gate of the device at a fixed drain voltage. For these devices, the gate voltage V_g = - 20 V for a total stress time of 10,000 seconds. The drain voltage applied for the

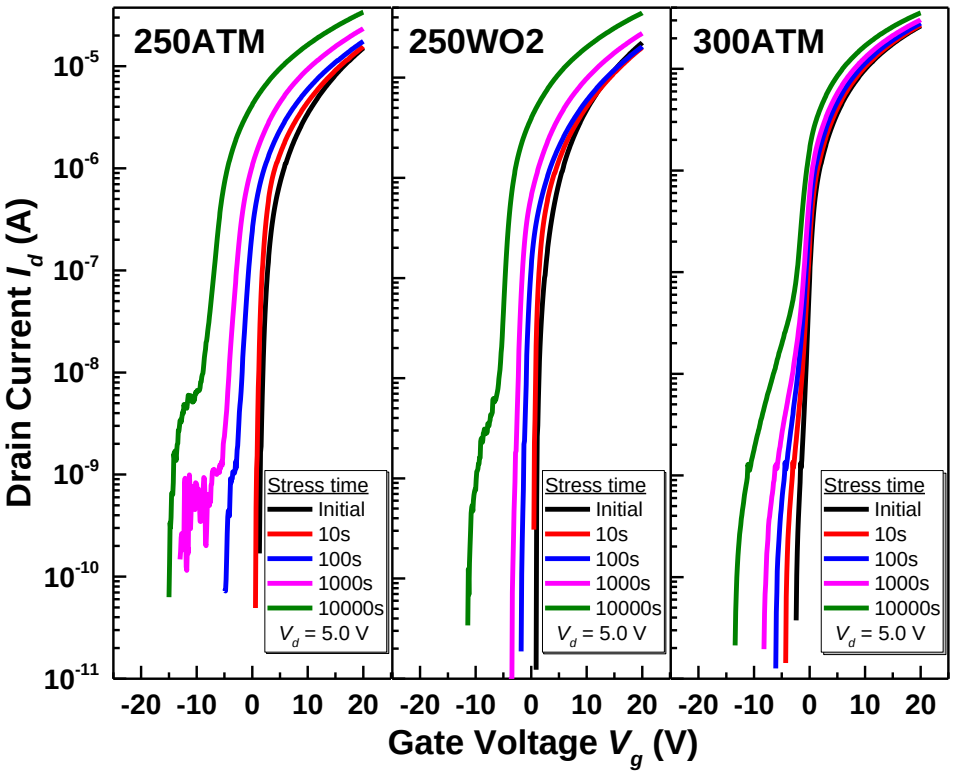

Figure 4.10 Temporal measurements of the transfer characteristics for the different annealing conditions as a function of applied stress (V_{gs} = - 20 V) under NBS and W/L = 90/10 µm.

devices was set at V_d = 5 V. NBS stress tests can give a picture of the defect states and quality of the semiconductor and gate insulator interface; changes in the shape of the subthreshold swing or shifts in the threshold voltage may indicate defects related to oxygen vacancies or traps located in the film. Figure 4.10 plots the different NBS curves obtained during the measurement. The data shows that the transfer curves have shifted negatively for all the annealing conditions due to the nature of NBS tests. This indicates the presence of traps and oxygen vacancies in the film which results in hole trapping which happens in the channel layer of the devices [38] [39]. It can also be observed that the hump/kink effect is more pronounced for all devices. For the 250ATM sample, at longer stress times, the channel may still possess defects and nitrogen impurities as shown in the previous sections due to the relatively low annealing temperature. As for the 250WO2 sample, at a stress time of 10,000 s, the hump can be observed with little change in the subthreshold swing of the device. This result supports the findings in the previous analytical sections of this work that suggest that the quality of the

250WO2 annealed films are far superior to those of films annealed in atmospheric conditions at 250°C. This implies that annealing at relatively low temperatures in wet ambient conditions have the ability to passivate defects in the film, improve the oxide network, and improve the quality of the film versus its atmospheric counterpart. The shifts in the on voltage (ΔV_{on}) give evidence to this as the values are -12.1 V, -5.1 V, and -4.1 V for the 250ATM, 250WO2, and 300ATM devices respectively. The ΔV_{on} values are extracted from the value of the threshold voltage V_{th} at a drain current I_{ds} value of 1 nA. The 250WO2 sample is far superior in terms of mobility and subthreshold swing value despite not having the lowest shift due to the improvements attributed to annealing in wet ambient conditions.

4.6 Improvement Mechanism for Solution Processed Films

Figure 4.11 illustrates the proposed improvement mechanism for the solution processed IZO films. As deposited IZO films have defects such as oxygen vacancies and residual precursors located in the bulk of the film. For films annealed in atmospheric environments, the oxygen vacancies are passivated by the surrounding oxygen with the aid of thermal annealing. As for the wet ambient annealing condition, due to the higher diffusivity of water vapor, it

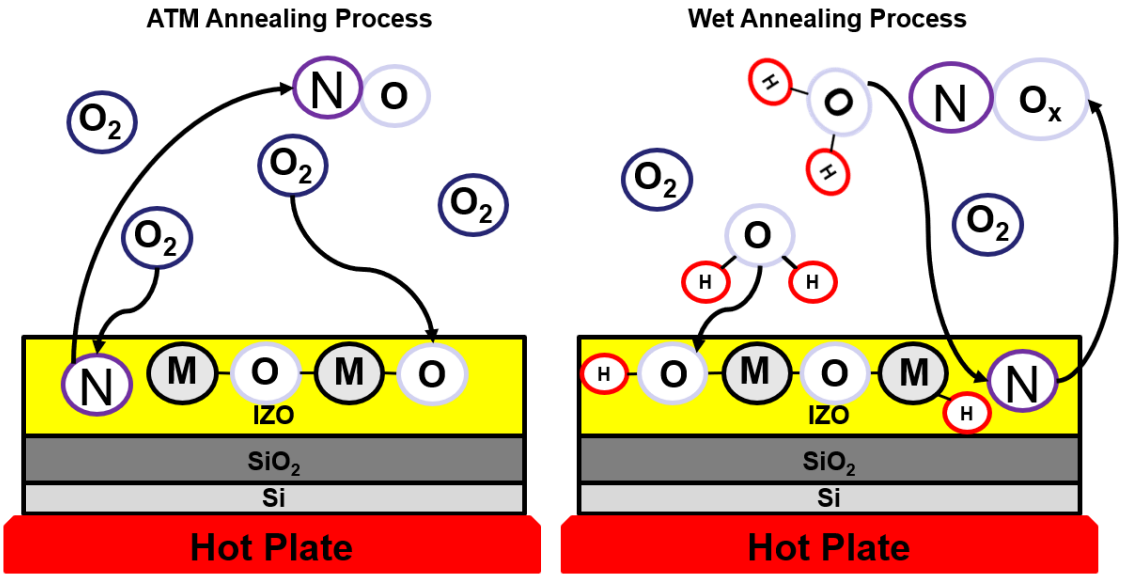

Figure 4.11 Mechanism of 250°C atmospheric annealing and Wet O_2 annealing for the IZO films during the channel activation procedure.

helps passivate oxygen vacancies better and help remove residual precursors located in the film as evidenced by the SIMS and XPS data. Thus, any residual nitrogen precursor in the IZO film can be removed by the wet annealing ambient. It also promotes the agglomeration of grains in the film as evidenced by the GI-XRD and STEM data. Thus, in conjunction with thermal annealing, the 250WO2 films and subsequently the 250WO2 devices exhibited better characteristics that their atmospheric counterparts annealed at the same temperature.

4.7 Conclusions

This chapter shows that the wet O_2 annealing method can also improve the quality of solution processed oxide films. The TG-DTA data showed that the lowest temperature possible to avoid excess precursor remaining in the film aside from film formation and densification is at temperatures higher than 244°C. The AFM, GI-XRD, and XPS results show that wet annealing ambients can improve the surface roughness of the film, promote grain agglomeration which may result in small semi crystalline pockets located in the bulk of the films, and a better oxide network all due to the diffusivity of water vapor during the channel annealing step. The Wet O_2 annealed devices exhibited decent stability under NBS tests with a small V_{on} shift of -5.1 V versus a shift of -12.1 V for the 250ATM devices. Finally, the 250WO2 annealed devices showed a maximum field effect mobility of 2.99 cm^2/Vs, an $I_{on/off}$ ratio of 10^7, and a decent subthreshold swing S of 330 mV/dec. The mobility of the 250WO2 devices exhibit a 4-fold increase when compared to the 250ATM devices. Thus, this low temperature, low cost annealing method can pave the way for fabricating good performance, solution processed devices that have low thermal budgets.

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Chapter 5 | Summary

5.1 Conclusions

Studies on transparent amorphous oxide semiconductor (TAOS) materials have seen a dramatic rise in activity ever since its introduction in 2004. Diverse materials such as IGZO, IWZO, and IZO have been explored by acting as the switching element in active matrix displays. Normally, the devices need to be annealed at temperature >300℃ to remove any existing defects during the fabrication process such as defects found in the channel aside from improving source/drain contacts through post metallization annealing. Lowering the annealing temperature facilitates the ability to deposit on flexible substrates which have a low thermal budget. The first chapter of this work discussed the developments on oxide semiconductors for use in thin-film transistor applications and the current direction of display technology research to shift from vacuum processed techniques to solution processed ones. The challenges in this endeavor are centered on lowering annealing temperatures to enable the deposition of devices with good electrical characteristics on flexible substrates with low thermal budgets. Thus, the work focused on low temperature, lost cost methods of improving the electrical characteristics of the devices with the intention of proposing a means of improving the electrical characteristics of devices that will be deposited on flexible substrates.

The second chapter of this work focused on finding low temperature, low cost methods of processing vacuum processed IGZO films at different annealing ambients and different annealing temperatures. The results show that not all devices exhibit switching characteristics as this was dependent not only on the temperature, but also the annealing ambient during channel activation. For the purpose of depositing films on substrates that have a low process temperature, a trio of annealing ambients were chosen with wet annealing ambients showing

the most promising results in terms of mobility and subthreshold swing values: dry annealing ambients (UV & O_3) and wet annealing ambients (Wet O_2, and UV & Wet O_2).

The third chapter of this work focused on understanding the mechanisms involved in each of the chosen annealing ambients: UV and O_3, Wet O_2, UV & Wet O_2. With the use of analytical techniques such as secondary ion mass spectrometry (SIMS) and X-ray photoelectron spectroscopy (XPS), the prevailing improvement mechanism points to wet annealing ambients as an effective means of passivating oxygen related defects aside from the overall improvement of the oxide network in the film which led to decent electrical characteristics for wet annealed devices. Electrical characteristics such as the mobility and I_{on} are better compared to the devices annealed in dry annealing ambients.

The fourth chapter of this work extended the wet annealing ambient process to solution processed films. Due to the nature of the deposition process, TG-DTA measurements were first performed and confirmed with the supplier to verify the absolute lowest temperature of processing the solution with little to no solvent or precursor remaining in the film. The films were then subjected to Wet O_2 annealing and were compared to atmospherically annealed films. Through different analytical techniques such as AFM, GI-XRD, STEM images, SIMS, and XPS measurements, the quality of the films were evaluated with respect to how the Wet O2 annealing condition may improve the electrical characteristics of the device. After device fabrication, the results of the electrical characteristics support the results from the different analytical measurements leading to the conclusion that wet annealing ambients can improve the roughness, oxide network, and stability of the devices.

All in all, this work was able to show that a low temperature, low cost annealing method can produce devices with good electrical characteristics and can pave the way for next generation fabrication of oxide TFTs on flexible substrates.

5.2 Recommendations and Possible Future Work

This work has shown the ability to use a low temperature annealing method that results in devices with good performance. The next logical step is to fabricate an all solution device deposited on a flexible substrate which utilizes the method proposed in this work. Of course, this introduces a new set of challenges as the research transitions to an all solution process. These involve the issue of film uniformity, film roughness, and contamination which hinder the device performance. Thus, other possible avenues of improvement involve the use of other methods of film deposition such as spray coating, ink jet printing, or spray pyrolysis to improve the surface roughness of the film. It would also be worthwhile to possible change the precursor used in the experiment from a water based solvent to alcohol based solvents, thus opening the path for lower thermal budgets. Also, doping the solution with elements such as Tin, Gallium, or Tungsten may make it easier to engineer the device to perform to certain standards. Also, solution processed passivation layers as well as solution processed high κ dielectrics can be used to not only improve device stability but as well as improve the device performance.

List of publications

1. Michael Paul A. Jallorina, Juan Paolo S. Bermundo, Mami N. Fujii, Yasuaki Ishikawa, Yukiharu Uraoka, “Significant mobility improvement of amorphous In-Ga-Zn-O thin-film transistors annealed in a low temperature wet ambient environment”, Appl. Phys. Lett. 112, 193501 (2018).

2. Michael Paul A. Jallorina, Juan Paolo S. Bermundo, Mami N. Fujii, Yasuaki Ishikawa, Yukiharu Uraoka, “Low temperature good performance solution processed IZO thin-film transistors”,
   Appl. Phys. Lett. (in preparation)

3. Michael Paul A. Jallorina, Giorgos Antoniou, Juan Paolo S. Bermundo, Yukiharu Uraoka, George Adamopoulos, “Spray coated Gallium Oxide/Magnesium Oxide Channel/Gate Insulator Thin-film Transistor”,
   Appl. Phys. Lett. (in preparation)

Presented Works and Awards

A. Presentations at international conferences

1. Michael Paul A. Jallorina, Juan Paolo S. Bermundo, Mami N. Fujii, Yasuaki Ishikawa, Yukiharu Uraoka, The 6th International Symposium on Organic and Inorganic Electronic Materials and Related Technologies (EM-NANO17), University of Fukui, Fukui Prefectural Hall, Fukui, Japan, 2017

2. Michael Paul A. Jallorina, Juan Paolo S. Bermundo, Mami N. Fujii, Yasuaki Ishikawa, Yukiharu Uraoka, The 24th International Workshop on Active-Matrix and Flatpanel Displays and Devices (AM-FPD 2017), Ryukoku University, Avanti Kyoto Hall, Kyoto, Japan, 2017

3. Michael Paul A. Jallorina, Juan Paolo S. Bermundo, Mami N. Fujii, Yasuaki Ishikawa, Yukiharu Uraoka, The 17th International Meeting on Information Display (IMID 2017), BEXCO, Busan, Korea, 2017

4. Michael Paul A. Jallorina, Giorgos Antoniou, Yukiharu Uraoka, George Adamopoulos, 7th International Symposium on Transparent Conductive Materials and 4th EMRS & MRS-J Bilateral Symposium on Advanced Oxides and Wide Bandgap Semiconductors, Crete, Greece, October 2018

5. Michael Paul A. Jallorina, Juan Paolo S. Bermundo, Mami N. Fujii, Yasuaki Ishikawa, Yukiharu Uraoka, Society of Information Display (SID), Display Week 2019. McEnery Convention Center, San Jose, California, United States of America. May 9, 2019

6. Michael Paul A. Jallorina, Juan Paolo S. Bermundo, Mami N. Fujii, Yasuaki Ishikawa, Yukiharu Uraoka, 28th International Conference on Amorphous and Nanocrystalline Semiconductors, Ecole Polytechnique, Palaiseau, France, August 2019

B. Presentations at domestic conferences

1. Michael Paul A. Jallorina, Juan Paolo S. Bermundo, Mami N. Fujii, Yasuaki Ishikawa, Yukiharu Uraoka, The 79th Japanese Society of Applied Physics Autumn Meeting 2018, Nagoya, Japan, September 2018

C. Awards

1. Ministry of Education, Culture, Sports, Science and Technology (MEXT),
   Top Global University Project Scholarship Recipient
   (October 2016 – September 2017).

2. Nara Institute of Science and Technology, Graduate School of Materials Science,
   2017 Grant-in-Aid for Ph.D. Students

3. Nara Institute of Science and Technology, Graduate School of Materials Science
   GSMS Scholarship (October 2017 – March 2019).

4. Ministry of Education, Culture, Sports, Science and Technology (MEXT),
   Top Global University Project Scholarship Recipient
   (April 2019 – September 2019).

5. International Meeting on Information Display (IMID),
   IMID 2017 Student Travel Grant
   (August 2017)

6. NAIST Mid-Term Student Research Evaluation Symposium 2018,
   The Best Presentation Award
   (November 2018).

7. Society of Information Display, Display Week 2019,
   Student Travel Grant
   (May 2019).